PEREGRINE SEMICONDUCTOR

PRODUCT SPECIFICATION

# PE3336

## 3.0 GHz Integer-N PLL for Low Phase Noise Applications

### Features

- 3.0 GHz operation
- ÷10/11 dual modulus prescaler
- Internal phase detector
- Serial, parallel or hardwired programmable
- Pin compatible with PE3236
- Available in 44-lead PLCC and miniature 48-lead MLP package
- Ultra-low phase noise

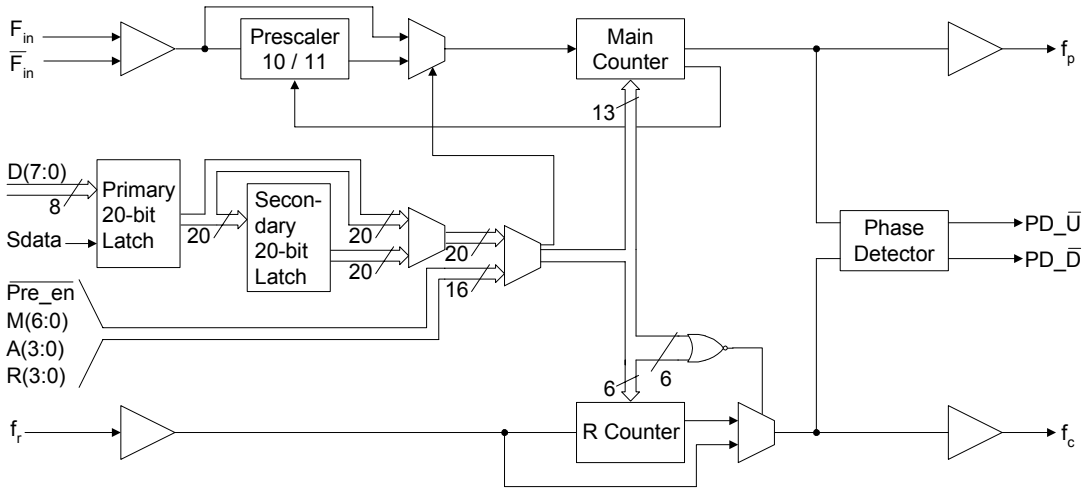
## Product Description

*Peregrine's PE3336 is a high performance integer-N PLL capable of frequency synthesis up to 3.0 GHz. The superior phase noise performance of the PE3336 makes it ideal for applications such as LMDS / MMDS / WLL basestations and demanding terrestrial systems.*

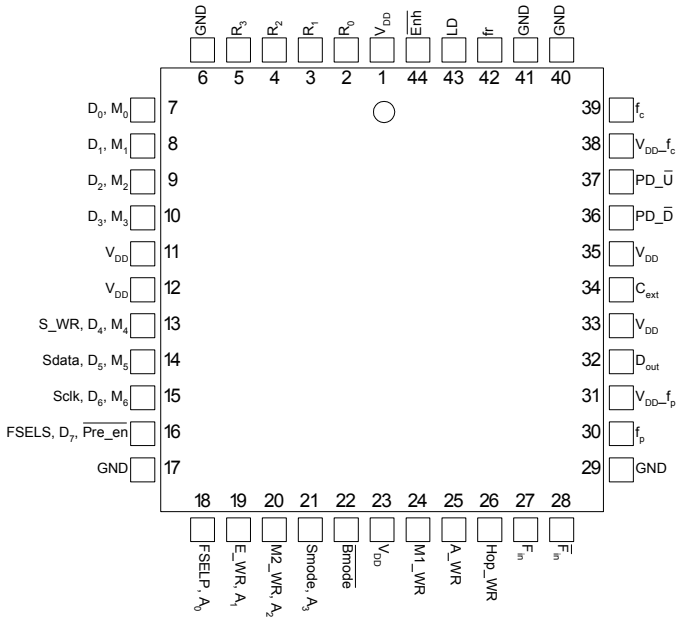
*The PE3336 features a 10/11 dual modulus prescaler, counters and a phase comparator as shown in Figure 1. Counter values are programmable through either a serial or parallel interface and can also be directly hard wired.*

*The PE3336 is optimized for terrestrial applications. Fabricated in Peregrine's patented UTSi® (Ultra Thin Silicon) CMOS technology, the PE3336 offers excellent RF performance with the economy and integration of conventional CMOS.*

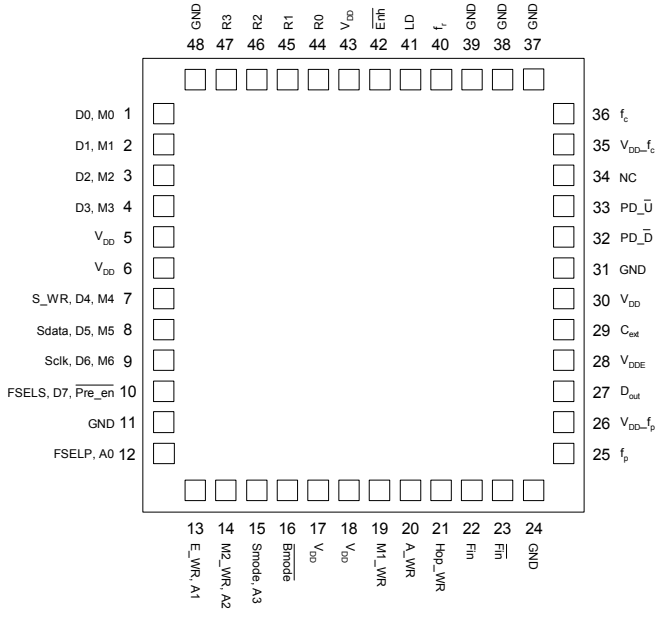
**Figure 1. Block Diagram**



## Figure 2. Pin Configuration




**44-lead PLCC**




**48-lead MLPQ**

## Table 1. Pin Descriptions

| Pin No. (44-lead PLCC) | Pin No. (48-lead MLPQ) | Pin Name | Interface Mode | Type | Description |
|---|---|---|---|---|---|
| 1 | 43 | $V_{DD}$ | ALL | (Note 1) | Power supply input. Input may range from 2.85 V to 3.15 V. Bypassing recommended. |
| 2 | 44 | $R_0$ | Direct | Input | R Counter bit0 (LSB). |
| 3 | 45 | $R_1$ | Direct | Input | R Counter bit1. |
| 4 | 46 | $R_2$ | Direct | Input | R Counter bit2. |
| 5 | 47 | $R_3$ | Direct | Input | R Counter bit3. |
| 6 | 48 | GND | ALL | (Note 1) | Ground. |
| 7 | 1 | $D_0$ | Parallel | Input | Parallel data bus bit0 (LSB). |
| | | $M_0$ | Direct | Input | M Counter bit0 (LSB). |
| 8 | 2 | $D_1$ | Parallel | Input | Parallel data bus bit1. |
| | | $M_1$ | Direct | Input | M Counter bit1. |
| 9 | 3 | $D_2$ | Parallel | Input | Parallel data bus bit2. |
| | | $M_2$ | Direct | Input | M Counter bit2. |
| 10 | 4 | $D_3$ | Parallel | Input | Parallel data bus bit3. |
| | | $M_3$ | Direct | Input | M Counter bit3. |
| 11 | 5 | $V_{DD}$ | ALL | (Note 1) | Same as pin 1. |
| 12 | 6 | $V_{DD}$ | ALL | (Note 1) | Same as pin 1. |

| Pin No. (44-lead PLCC) | Pin No. (48-lead MLPQ) | Pin Name | Interface Mode | Type | Description |
|---|---|---|---|---|---|
| 13 | 7 | S_WR | Serial | Input | Serial load enable input. While S_WR is "low", Sdata can be serially clocked. Primary register data are transferred to the secondary register on S_WR or Hop_WR rising edge. |
| | | $D_4$ | Parallel | Input | Parallel data bus bit4 |
| | | $M_4$ | Direct | Input | M Counter bit4 |
| 14 | 8 | Sdata | Serial | Input | Binary serial data input. Input data entered MSB first. |
| | | $D_5$ | Parallel | Input | Parallel data bus bit5. |
| | | $M_5$ | Direct | Input | M Counter bit5. |
| 15 | 9 | Sclk | Serial | Input | Serial clock input. Sdata is clocked serially into the 20-bit primary register (E_WR "low") or the 8-bit enhancement register (E_WR "high") on the rising edge of Sclk. |
| | | $D_6$ | Parallel | Input | Parallel data bus bit6. |
| | | $M_6$ | Direct | Input | M Counter bit6. |
| 16 | 10 | FSELS | Serial | Input | Selects contents of primary register (FSELS=1) or secondary register (FSELS=0) for programming of internal counters while in Serial Interface Mode. |
| | | $D_7$ | Parallel | Input | Parallel data bus bit7 (MSB). |
| | | $\overline{\text{Pre\_en}}$ | Direct | Input | Prescaler enable, active "low". When "high", $F_{in}$ bypasses the prescaler. |
| 17 | 11 | GND | ALL | | Ground. |
| 18 | 12 | FSELP | Parallel | Input | Selects contents of primary register (FSELP=1) or secondary register (FSELP=0) for programming of internal counters while in Parallel Interface Mode. |
| | | $A_0$ | Direct | Input | A Counter bit0 (LSB). |
| 19 | 13 | E_WR | Serial | Input | Enhancement register write enable. While E_WR is "high", Sdata can be serially clocked into the enhancement register on the rising edge of Sclk. |
| | | | Parallel | Input | Enhancement register write. D[7:0] are latched into the enhancement register on the rising edge of E_WR. |
| | | $A_1$ | Direct | Input | A Counter bit1. |
| 20 | 14 | M2_WR | Parallel | Input | M2 write. D[3:0] are latched into the primary register (R[5:4], M[8:7]) on the rising edge of M2_WR. |
| | | $A_2$ | Direct | Input | A Counter bit2. |
| 21 | 15 | Smode | Serial, Parallel | Input | Selects serial bus interface mode ($\overline{\text{Bmode}}$=0, Smode=1) or Parallel Interface Mode ($\overline{\text{Bmode}}$=0, Smode=0). |
| | | $A_3$ | Direct | Input | A Counter bit3 (MSB). |
| 22 | 16 | $\overline{\text{Bmode}}$ | ALL | Input | Selects direct interface mode ($\overline{\text{Bmode}}$=1). |
| 23 | 17,18 | $V_{DD}$ | ALL | (Note 1) | Same as pin 1. |
| 24 | 19 | M1_WR | Parallel | Input | M1 write. D[7:0] are latched into the primary register ($\overline{\text{Pre\_en}}$, M[6:0]) on the rising edge of M1_WR. |
| 25 | 20 | A_WR | Parallel | Input | A write. D[7:0] are latched into the primary register (R[3:0], A[3:0]) on the rising edge of A_WR. |
| 26 | 21 | Hop_WR | Serial, Parallel | Input | Hop write. The contents of the primary register are latched into the secondary register on the rising edge of Hop_WR. |
| 27 | 22 | $F_{in}$ | ALL | Input | Prescaler input from the VCO. 3.0 GHz max frequency. |

| Pin No. (44-lead PLCC) | Pin No. (48-lead MLPQ) | Pin Name | Interface Mode | Type | Description |
|---|---|---|---|---|---|
| 28 | 23 | $\overline{F}_{in}$ | ALL | Input | Prescaler complementary input. A bypass capacitor should be placed as close as possible to this pin and be connected in series with a 50 Ω resistor directly to the ground plane. |
| 29 | 24 | GND | ALL | | Ground. |
| 30 | 25 | $f_p$ | ALL | Output | Monitor pin for main divider output. Switching activity can be disabled through enhancement register programming or by floating or grounding $V_{DD}$ pin 31. |
| 31 | 26 | $V_{DD}$-$f_p$ | ALL | (Note 1) | $V_{DD}$ for $f_p$. Can be left floating or connected to GND to disable the $f_p$ output. |
| 32 | 27 | Dout | Serial, Parallel | Output | Data Out. The MSEL signal and the raw prescaler output are available on Dout through enhancement register programming. |
| 33 | 28 | $V_{DD}$ | ALL | (Note 1) | Same as pin 1. |
| 34 | 29 | Cext | ALL | Output | Logical "NAND" of PD_$\overline{U}$ and PD_$\overline{D}$ terminated through an on chip, 2 kΩ series resistor. Connecting Cext to an external capacitor will low pass filter the input to the inverting amplifier used for driving LD. |
| 35 | 30 | $V_{DD}$ | ALL | (Note 1) | Same as pin 1. |
| 36 | 32 | PD_$\overline{D}$ | ALL | Output | PD_$\overline{D}$ is pulse down when $f_p$ leads $f_c$. |
| 37 | 33 | PD_$\overline{U}$ | ALL | | PD_$\overline{U}$ is pulse down when $f_c$ leads $f_p$. |
| 38 | 35 | $V_{DD}$-$f_c$ | ALL | (Note 1) | $V_{DD}$ for $f_c$ can be left floating or connected to GND to disable the $f_c$ output. |
| 39 | 36 | $f_c$ | ALL | Output | Monitor pin for reference divider output. Switching activity can be disabled through enhancement register programming or by floating or grounding $V_{DD}$ pin 38. |
| 40 | 31,37 | GND | ALL | | Ground. |
| 41 | 38,39 | GND | ALL | | Ground. |
| 42 | 40 | $f_r$ | ALL | Input | Reference frequency input. |
| 43 | 41 | LD | ALL | Output | Lock detect and open drain logical inversion of CEXT. When the loop is in lock, LD is high impedance, otherwise LD is a logic low ("0"). |
| 44 | 42 | $\overline{Enh}$ | Serial, Parallel | Input | Enhancement mode. When asserted low ("0"), enhancement register bits are functional. |
| N/A | 34 | NC | ALL | | No connection. |

**Note 1:** All $V_{DD}$ pins are connected by diodes and must be supplied with the same positive voltage level.
$V_{DD}$-$f_p$ and $V_{DD}$-$f_p$ are used to power the $f_p$ and $f_c$ outputs and can alternatively be left floating or connected to GND to disable the $f_p$ and $f_c$ outputs.

**Note 2:** All digital input pins have 70 kΩ pull-down resistors to ground.

## Table 2. Absolute Maximum Ratings

| Symbol | Parameter/Conditions | Min | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | -0.3 | 4.0 | V |
| $V_I$ | Voltage on any input | -0.3 | $V_{DD}$ + 0.3 | V |
| $I_I$ | DC into any input | -10 | +10 | mA |
| $I_O$ | DC into any output | -10 | +10 | mA |
| $T_{stg}$ | Storage temperature range | -65 | 150 | °C |

## Table 3. Operating Ratings

| Symbol | Parameter/Conditions | Min | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 2.85 | 3.15 | V |
| $T_A$ | Operating ambient temperature range | -40 | 85 | °C |

## Table 4. ESD Ratings

| Symbol | Parameter/Conditions | Level | Units |
|---|---|---|---|
| $V_{ESD}$ | ESD voltage (Human Body Model) | 1000 | V |

**Note 1:** Periodically sampled, not 100% tested. Tested per MIL-STD-883, M3015 C2

## Electrostatic Discharge (ESD) Precautions

When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 4.

## Latch-Up Avoidance

Unlike conventional CMOS devices, UTSi CMOS devices are immune to latch-up.

## Table 5. DC Characteristics

$V_{DD}$ = 3.0 V, -40° C < $T_A$ < 85° C, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Operational supply current;<br>Prescaler disabled<br>Prescaler enabled | $V_{DD}$ = 2.85 to 3.15 V | | <br>10<br>19 | <br><br>26 | <br>mA<br>mA |
| Digital Inputs: All except $f_r$, $R_0$, $F_{in}$, $\overline{F}_{in}$ | | | | | | |
| $V_{IH}$ | High level input voltage | $V_{DD}$ = 2.85 to 3.15 V | 0.7 x $V_{DD}$ | | | V |
| $V_{IL}$ | Low level input voltage | $V_{DD}$ = 2.85 to 3.15 V | | | 0.3 x $V_{DD}$ | V |
| $I_{IH}$ | High level input current | $V_{IH}$ = $V_{DD}$ = 3.15 V | | | +70 | µA |
| $I_{IL}$ | Low level input current | $V_{IL}$ = 0, $V_{DD}$ = 3.15 V | -1 | | | µA |
| Reference Divider input: $f_r$ | | | | | | |
| $I_{IHR}$ | High level input current | $V_{IH}$ = $V_{DD}$ = 3.15 V | | | +100 | µA |
| $I_{ILR}$ | Low level input current | $V_{IL}$ = 0, $V_{DD}$ = 3.15 V | -100 | | | µA |
| R0 Input (Pull-up Resistor): $R_0$ | | | | | | |
| $I_{IHRO}$ | High level input current | $V_{IH}$ = $V_{DD}$ = 3.15 V | | | +5 | µA |
| $I_{ILRO}$ | Low level input current | $V_{IL}$ = 0, $V_{DD}$ = 3.15 V | -5 | | | µA |
| Counter and phase detector outputs: $f_c$, $f_p$, PD_$\overline{D}$, PD_$\overline{U}$ | | | | | | |
| $V_{OLD}$ | Output voltage LOW | $I_{out}$ = 6 mA | | | 0.4 | V |
| $V_{OHD}$ | Output voltage HIGH | $I_{out}$ = -3 mA | $V_{DD}$ - 0.4 | | | V |
| Lock detect outputs: Cext, LD | | | | | | |
| $V_{OLC}$ | Output voltage LOW, Cext | $I_{out}$ = 100 mA | | | 0.4 | V |
| $V_{OHC}$ | Output voltage HIGH, Cext | $I_{out}$ = -100 mA | $V_{DD}$ - 0.4 | | | V |
| $V_{OLLD}$ | Output voltage LOW, LD | $I_{out}$ = 6 mA | | | 0.4 | V |

## Table 6. AC Characteristics

$V_{DD}$ = 3.0 V, -40° C < $T_A$ < 85° C, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| Control Interface and Latches (see Figures 3, 4, 5) | | | | | |
| $f_{Clk}$ | Serial data clock frequency | | | 10 | MHz |
| $t_{ClkH}$ | Serial clock HIGH time | | 30 | | ns |
| $t_{ClkL}$ | Serial clock LOW time | | 30 | | ns |
| $t_{DSU}$ | Sdata set-up time after Sclk rising edge, D[7:0] set-up time to M1_WR, M2_WR, A_WR, E_WR rising edge | | 10 | | ns |
| $t_{DHLD}$ | Sdata hold time after Sclk rising edge, D[7:0] hold time to M1_WR, M2_WR, A_WR, E_WR rising edge | | 10 | | ns |
| $t_{PW}$ | S_WR, M1_WR, M2_WR, A_WR, E_WR pulse width | | 30 | | ns |
| $t_{CWR}$ | Sclk rising edge to S_WR rising edge. S_WR, M1_WR, M2_WR, A_WR falling edge to Hop_WR rising edge | | 30 | | ns |
| $t_{CE}$ | Sclk falling edge to E_WR transition | | 30 | | ns |
| $t_{WRC}$ | S_WR falling edge to Sclk rising edge. Hop_WR falling edge to S_WR, M1_WR, M2_WR, A_WR rising edge | | 30 | | ns |
| $t_{EC}$ | E_WR transition to Sclk rising edge | | 30 | | ns |
| $t_{MDO}$ | MSEL data out delay after Fin rising edge | $C_L$ = 12 pf | | 8 | ns |
| Main Divider (Including Prescaler) | | | | | |
| $F_{in}$ | Operating frequency | | 500 | 3000 | MHz |
| $P_{Fin}$ | Input level range | External AC coupling | -5 | 5 | dBm |
| Main Divider (Prescaler Bypassed) | | | | | |
| $F_{in}$ | Operating frequency | | 50 | 300 | MHz |
| $P_{Fin}$ | Input level range | External AC coupling | -5 | 5 | dBm |
| Reference Divider | | | | | |
| $f_r$ | Operating frequency | (Note 1) | (Note 2) | 100 | MHz |
| $P_{fr}$ | Reference input power | Single ended input | -2 | 10 | dBm |
| $V_{fr}$ | Input sensitivity | External AC coupling (Note 3) | 0.5 | | $V_{P-P}$ |
| Phase Detector | | | | | |
| $f_c$ | Comparison frequency | (Note 1) | | 20 | MHz |

**Note 1:** Parameter is guaranteed through characterization only and is not tested.

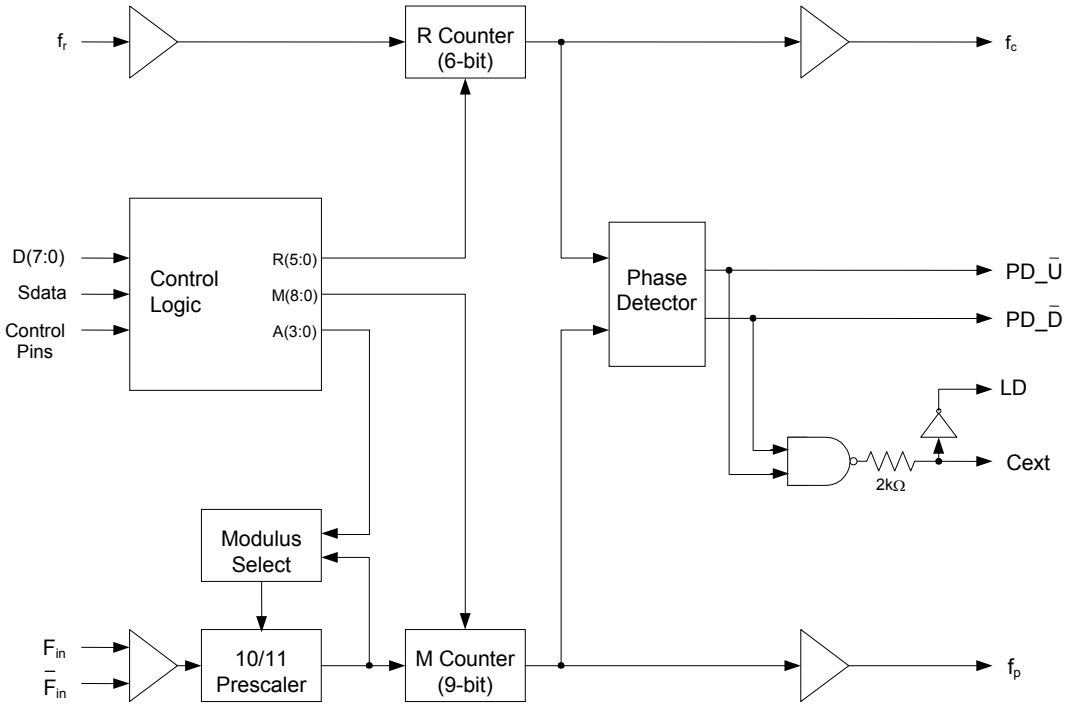
**Note 2:** Running at low frequencies (< 10 MHz sinewave), the device will still be functional but may cause phase noise degradation. Inserting a low-noise amplifier to square up the edges is recommended at lower input frequencies.

**Note 3:** CMOS logic levels may be used if DC coupled. For optimum phase noise performance, the reference input falling edge rate should be faster than 80mV/ns.

## Functional Description

The PE3336 consists of a prescaler, counters, a phase detector and control logic. The dual modulus prescaler divides the VCO frequency by either 10 or 11, depending on the value of the modulus select. Counters “R” and “M” divide the reference and prescaler output, respectively, by integer values stored in a 20-bit register. An additional counter (“A”) is used in the modulus select logic. The phase-frequency detector generates up and down frequency control signals. The control logic includes a selectable chip interface. Data can be written via serial bus, parallel bus, or hardwired direct to the pins. There are also various operational and test modes and lock detect.

**Figure 3. Functional Block Diagram**



## Main Counter Chain

The main counter chain divides the RF input frequency, $F_{in}$, by an integer derived from the user defined values in the "M" and "A" counters. It is composed of the 10/11 dual modulus prescaler, modulus select logic, and 9-bit M counter. Setting Pre_en "low" enables the 10/11 prescaler. Setting Pre_en "high" allows $F_{in}$ to bypass the prescaler and powers down the prescaler.

The output from the main counter chain, $f_p$, is related to the VCO frequency, $F_{in}$, by the following equation:

$$f_p = F_{in} / [10 \times (M + 1) + A] \quad (1)$$
$$\text{where } A \leq M + 1,\ 1 \leq M \leq 511$$

When the loop is locked, $F_{in}$ is related to the reference frequency, $f_r$, by the following equation:

$$F_{in} = [10 \times (M + 1) + A] \times (f_r / (R+1)) \quad (2)$$
$$\text{where } A \leq M + 1,\ 1 \leq M \leq 511$$

A consequence of the upper limit on A is that $F_{in}$ must be greater than or equal to 90 x ($f_r$ / (R+1)) to obtain contiguous channels. Programming the M Counter with the minimum value of "1" will result in a minimum M Counter divide ratio of "2".

When the prescaler is bypassed, the equation becomes:

$$F_{in} = (M + 1) \times (f_r / (R+1)) \quad (3)$$
$$\text{where } 1 \leq M \leq 511$$

In Direct Interface Mode, main counter inputs $M_7$ and $M_8$ are internally forced low.

## Reference Counter

The reference counter chain divides the reference frequency, $f_r$, down to the phase detector comparison frequency, $f_c$.

The output frequency of the 6-bit R Counter is related to the reference frequency by the following equation:

$$f_c = f_r / (R + 1) \quad (4)$$
$$\text{where } 0 \leq R \leq 63$$

Note that programming R equal to "0" will pass the reference frequency, $f_r$, directly to the phase detector.

In Direct Interface Mode, R Counter inputs $R_4$ and $R_5$ are internally forced low ("0").

## Register Programming

*Parallel Interface Mode*

Parallel Interface Mode is selected by setting the Bmode input "low" and the Smode input "low".

Parallel input data, D[7:0], are latched in a parallel fashion into one of three, 8-bit primary register sections on the rising edge of M1_WR, M2_WR, or A_WR per the mapping shown in Table 7 on page 10. The contents of the primary register are transferred into a secondary register on the rising edge of Hop_WR according to the timing diagram shown in Figure 4. Data are transferred to the counters as shown in Table 7 on page 10.

The secondary register acts as a buffer to allow rapid changes to the VCO frequency. This double buffering for "ping-pong" counter control is programmed via the FSELP input. When FSELP is "high", the primary register contents set the counter inputs. When FSELP is "low", the secondary register contents are utilized.

Parallel input data, D[7:0], are latched into the enhancement register on the rising edge of E_WR according to the timing diagram shown in Figure 4. This data provides control bits as shown in Table 8 on page 10 with bit functionality enabled by asserting the Enh input "low".

*Serial Interface Mode*

Serial Interface Mode is selected by setting the Bmode input "low" and the Smode input "high".

While the E_WR input is "low" and the S_WR input is "low", serial input data (Sdata input), $B_0$ to $B_{19}$, are clocked serially into the primary register on the rising edge of Sclk, MSB ($B_0$) first. The contents from the primary register are transferred into the secondary register on the rising edge of either S_WR or Hop_WR according to the timing diagram shown in Figures 4-5. Data are transferred to the counters as shown in Table 7 on page 10.

The double buffering provided by the primary and secondary registers allows for "ping-pong" counter control using the FSELS input. When FSELS is "high", the primary register contents set the counter inputs. When FSELS is "low", the secondary register contents are utilized.

While the E_WR input is "high" and the S_WR input is "low", serial input data (Sdata input), $B_0$ to $B_7$, are clocked serially into the enhancement register on the rising edge of Sclk, MSB ($B_0$) first. The enhancement register is double buffered to prevent

inadvertent control changes during serial loading, with buffer capture of the serially entered data performed on the falling edge of E_WR according to the timing diagram shown in Figure 5. After the falling edge of E_WR, the data provide control bits as shown in Table 8 with bit functionality enabled by asserting the $\overline{Enh}$ input "low".

*Direct Interface Mode*

Direct Interface Mode is selected by setting the $\overline{Bmode}$ input "high".

Counter control bits are set directly at the pins as shown in Table 7. In Direct Interface Mode, main counter inputs $M_7$ and $M_8$, and R Counter inputs $R_4$ and $R_5$ are internally forced low ("0").

## Table 7. Primary Register Programming

| Interface Mode | $\overline{Enh}$ | $\overline{Bmode}$ | Smode | $R_5$ | $R_4$ | $M_8$ | $M_7$ | $\overline{Pre\_en}$ | $M_6$ | $M_5$ | $M_4$ | $M_3$ | $M_2$ | $M_1$ | $M_0$ | $R_3$ | $R_2$ | $R_1$ | $R_0$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Parallel | 1 | 0 | 0 | M2_WR rising edge load | | | | M1_WR rising edge load | | | | | | | | A_WR rising edge load | | | | | | | |
| | | | | $D_3$ | $D_2$ | $D_1$ | $D_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| Serial* | 1 | 0 | 1 | $B_0$ | $B_1$ | $B_2$ | $B_3$ | $B_4$ | $B_5$ | $B_6$ | $B_7$ | $B_8$ | $B_9$ | $B_{10}$ | $B_{11}$ | $B_{12}$ | $B_{13}$ | $B_{14}$ | $B_{15}$ | $B_{16}$ | $B_{17}$ | $B_{18}$ | $B_{19}$ |
| Direct | 1 | 1 | X | 0 | 0 | 0 | 0 | Pre_en | $M_6$ | $M_5$ | $M_4$ | $M_3$ | $M_2$ | $M_1$ | $M_0$ | $R_3$ | $R_2$ | $R_1$ | $R_0$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ |

*Serial data clocked serially on Sclk rising edge while E_WR "low" and captured in secondary register on S_WR rising edge.

MSB (first in) ↑ ... ↑ (last in) LSB

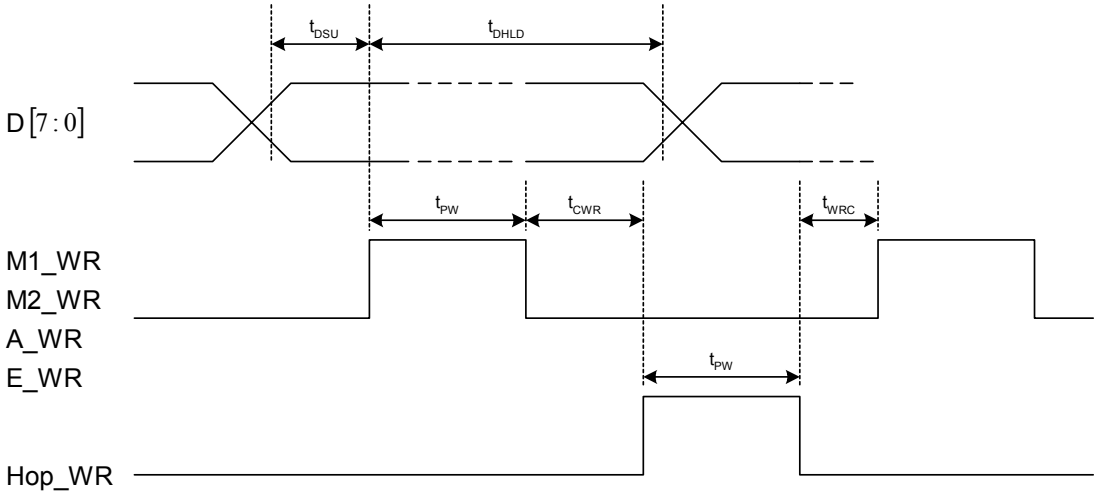
## Table 8. Enhancement Register Programming

| Interface Mode | $\overline{Enh}$ | $\overline{Bmode}$ | Smode | Reserved | Reserved | Reserved | Power down | Counter load | MSEL output | Prescaler output | $f_c$, $f_p$ $\overline{OE}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Parallel | 0 | X | 0 | E_WR rising edge load | | | | | | | |
| | | | | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| Serial* | 0 | X | 1 | $B_0$ | $B_1$ | $B_2$ | $B_3$ | $B_4$ | $B_5$ | $B_6$ | $B_7$ |

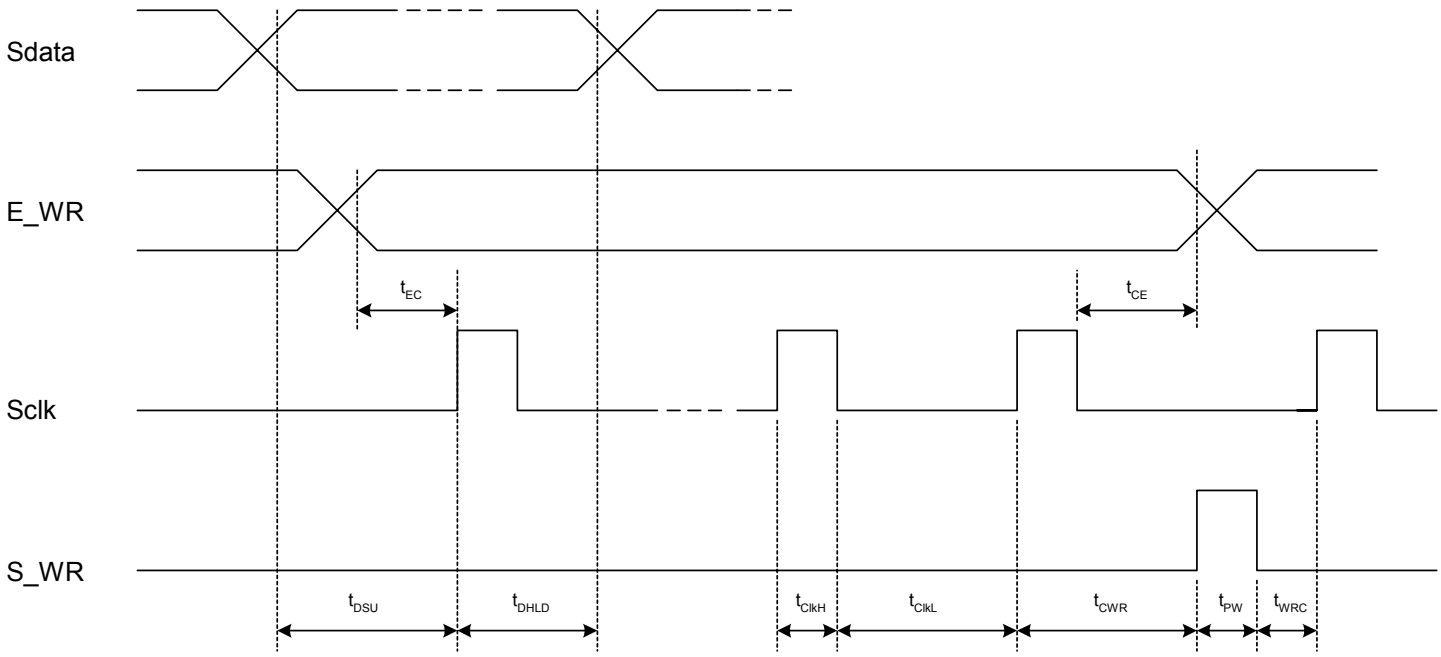
*Serial data clocked serially on Sclk rising edge while E_WR "high" and captured in the double buffer on E_WR falling edge.

MSB (first in) ↑ ... ↑ (last in) LSB

## Figure 4. Parallel Interface Mode Timing Diagram




## Figure 5. Serial Interface Mode Timing Diagram



### Enhancement Register

The functions of the enhancement register bits are shown below with all bits active “high”.

### Table 9. Enhancement Register Bit Functionality

| Bit Function | | Description |
|---|---|---|
| Bit 0 | Reserved** | |
| Bit 1 | Reserved** | |
| Bit 2 | Reserved** | |
| Bit 3 | Power down | Power down of all functions except programming interface. |
| Bit 4 | Counter load | Immediate and continuous load of counter programming as directed by the $\overline{\text{Bmode}}$ and Smode inputs. |
| Bit 5 | MSEL output | Drives the internal dual modulus prescaler modulus select (MSEL) onto the Dout output. |
| Bit 6 | Prescaler output | Drives the raw internal prescaler output onto the Dout output. |
| Bit 7 | $f_p$, $f_c$ $\overline{\text{OE}}$ | $f_p$, $f_c$ outputs disabled. |

** Program to 0

### Phase Detector

The phase detector is triggered by rising edges from the main Counter ($f_p$) and the reference counter ($f_c$). It has two outputs, PD_$\overline{\text{U}}$, and PD_$\overline{\text{D}}$. If the divided VCO leads the divided reference in phase or frequency ($f_p$ leads $f_c$), PD_$\overline{\text{D}}$ pulses “low”. If the divided reference leads the divided VCO in phase or frequency ($f_c$ leads $f_p$), PD_$\overline{\text{U}}$ pulses “low”. The width of either pulse is directly proportional to phase offset between the two input signals, $f_p$ and $f_c$.

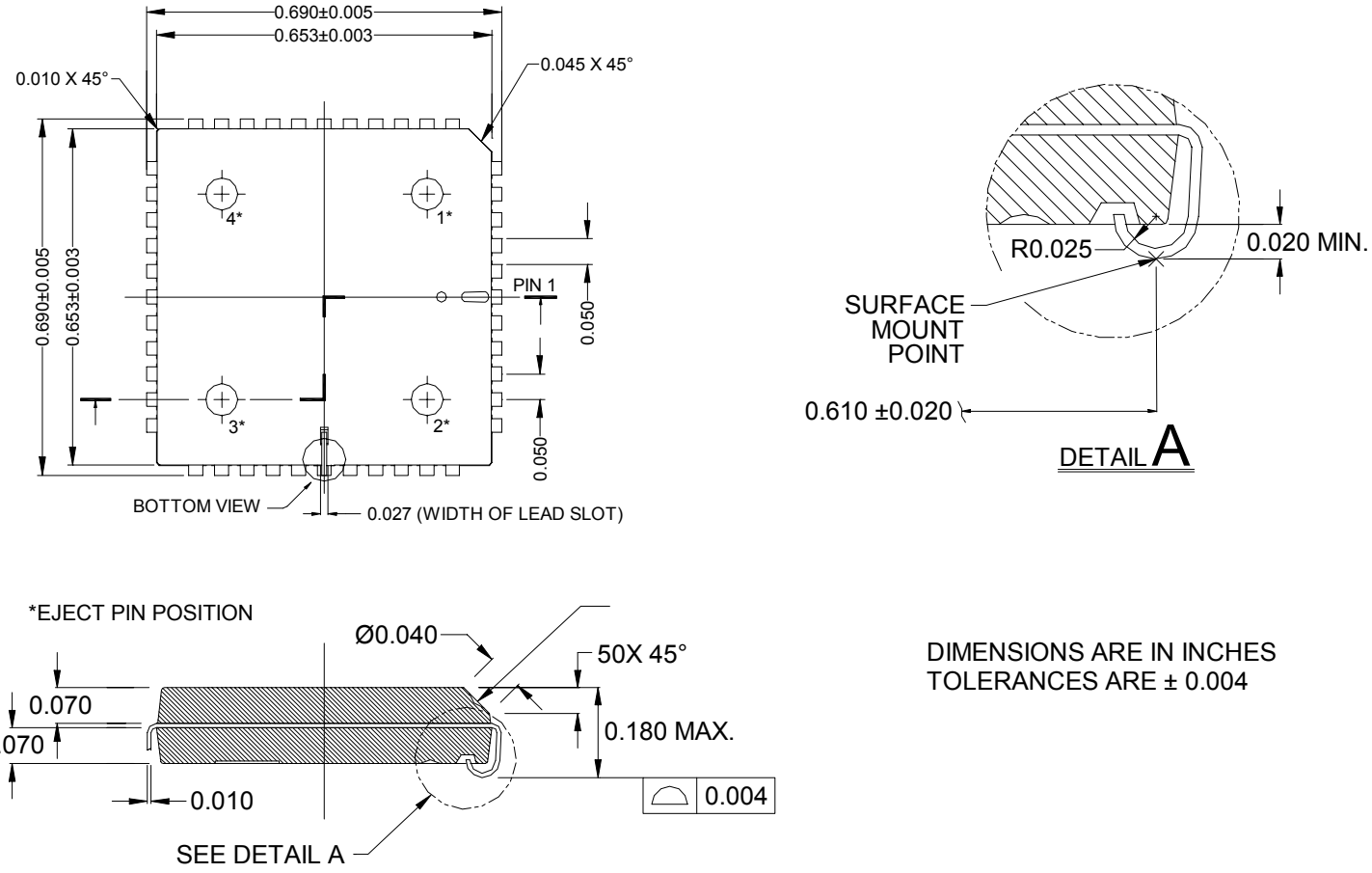
The phase detector gain is equal to 2.7 V / 2 π, which numerically yields 0.43 V / radian.

PD_$\overline{\text{U}}$ and PD_$\overline{\text{D}}$ drive an active loop filter which controls the VCO tune voltage. PD_$\overline{\text{U}}$ pulses result in an increase in VCO frequency; PD_$\overline{\text{D}}$ pulses result in a decrease in VCO frequency (for a positive Kv VCO).

A lock detect output, LD is also provided, via the pin Cext. Cext is the logical “NAND” of PD_$\overline{\text{U}}$ and PD_$\overline{\text{D}}$ waveforms, which is driven through a series 2 kohm resistor. Connecting Cext to an external shunt capacitor provides low pass filtering of this signal. Cext also drives the input of an internal inverting comparator with an open drain output. Thus LD is an “AND” function of PD_$\overline{\text{U}}$ and PD_$\overline{\text{D}}$.

## Figure 6. Package Drawing

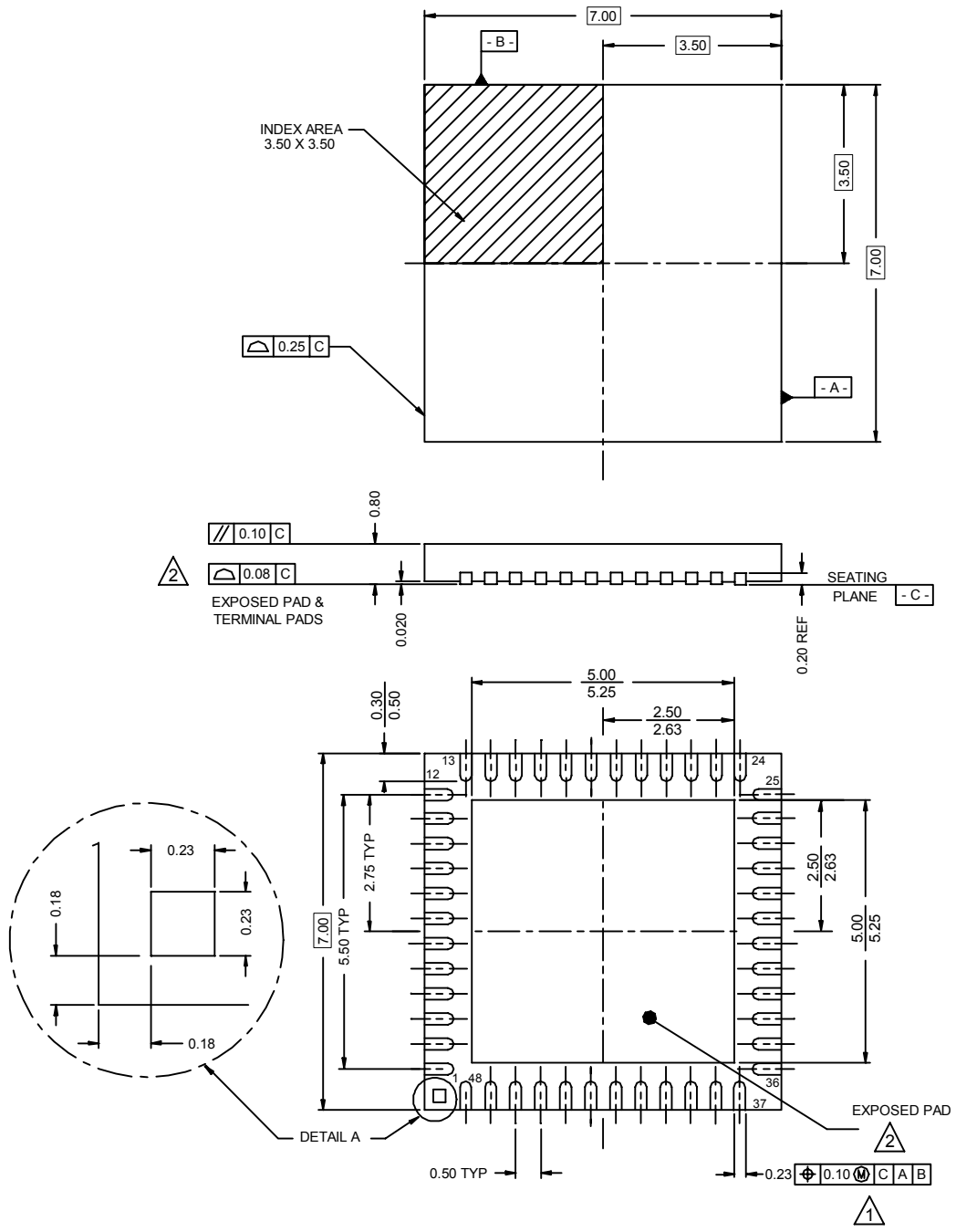
44-lead PLCC




DIMENSIONS ARE IN INCHES
TOLERANCES ARE ± 0.004

## Figure 7. Package Drawing

48-lead MLPQ




1. DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 FROM TERMINAL TIP.

2. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

## Table 10. Ordering Information

| Order Code | Part Marking | Description | Package | Shipping Method | Product Status |
|---|---|---|---|---|---|
| 3336-21 | PE3336 | | 44-lead PLCC | 26 units / Tube | Production |
| 3336-22 | PE3336 | | 44-lead PLCC | 500 units / T&R | Production |
| 3336-23 | PE3336 | | 48-lead MLPQ | 52 units / Tube | Evaluation Samples |
| 3336-24 | PE3336 | | 48-lead MLPQ | 4000 units / T&R | Evaluation Samples |
| 3336-00 | PE3336EK | PLCC Evaluation Board with Software | 44-lead PLCC | 1 / Box | Available |
| 3336-01 | PE3336EK | MLPQ Evaluation Board with Software | 48-lead MLPQ | 1 / Box | Available |

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For a list of representatives in your area, please refer to our Web site at: ***http://www.peregrine-semi.com***

# Data Sheet Identification

### *Advance Information*

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

### *Preliminary Specification*

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

### *Product Specification*

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a PCN (Product Change Notice).

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