PRELIMINARY DATA SHEET

gmZAN3

XGA Analog Interface LCD Monitor Controller

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Genesis Microchip Inc.
165 Commerce Valley Dr. West • Thornhill • ON • Canada • L3T 7V8 • Tel: (905) 889-5400 • Fax: (905) 889-5422
2150 Gold Street • PO Box 2150 • Alviso • CA • USA • 95002 • Tel: (408) 262-6599 • Fax: (408) 262-6365
4F, No. 24, Ln 123, Sec 6, Min-Chung E. Rd. • Taipei • Taiwan • Tel: (2) 2791-0118 • Fax: (2) 2791-0196
143-37 Hyundai Tower • Unit 902 • Samsung-dong • Kangnam-gu • Seoul • Korea • 135-090 • Tel: (82-2) 553-5693 • Fax: (82-2) 552-4942
www.genesis-microchip.com / info@genesis-microchip.com.com

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Revision History

Document	Description	Date
C0523-DAT-01A	• Initial Release	Feb. 2003
C0523-DAT-01B	• Changed the LVDS pin names to allow simple board layout. See Figure 3 and Table 5.	Feb. 2003
C0523-DAT-01C	• Fixed typo in Table 19 $V_{VDD\_1.85}$ >> $V_{VDD\_1.8}$. • Updated Table 20 with correct 1.8V voltage min and max • Updated the minimum and maximum operating conditions in Section 5.2 Preliminary AC Characteristics.	Mar. 2003
C0523-DAT-01D	• Removed Dual- edge clocking from section 4.11 • Updated Table 19 with Theta Jc and Theta Ja values • Updated Table 20 with measured Power consumption for gmZAN3L • Added Table 21 with gmZAN3T DC characteristics with measured Power Consumption	Apr. 2003

C0523-DAT-01E	• Added information on the integrated Reset Circuit
	  • Figure 10 gmZAN3 Re-setting external MCU
	  • Figure 11 External MCU re-setting gmZAN3
	  • Figure 12 Reset Signal Timing
	  • Table 13 Temperature & Voltage Variation on the Reset Circuit
	• Added Section 4.3.5 on the Schimtt Trigger
	  • Figure 15 Schmitt Trigger Timing
	  • Table 16 Temperature & Voltage Variation on the Schimtt Trigger
	• Changed Figure 14 drawing with more clarification
		May 2003

C0523-DAT-01F	• Pin corrections (documentation error):
	  • gmZAN3L – corrected pins: 40, 43, 52,53, 60, 63 (GPIO[8:13] to GPO[8:13])
	  • gmZAN3T – corrected pins: 40, 43, 52, 53, 60, 63
	• Part Number change: removed hyphen from chip name throughout document
	• Updated frequency in TCLK specification table.
	• Corrected storage temperature in Preliminary DC Characteristics
		May 2003

C0523-DAT-01G	• Updated Table 16 Temperature and Voltage variation of the Schmitt trigger	July 2003

1 Overview

The gmZAN3 is a graphics processing IC for Liquid Crystal Display (LCD) monitors at XGA resolution. It provides all key IC functions required for the highest quality LCD monitors. On-chip functions include a high-speed triple-ADC and PLL, a high quality zoom and shrink scaling engine, an on-screen display (OSD) controller and digital color controls.

The gmZAN3 is provided with two versions;

- gmZAN3T with 48-bit TTL output and
- gmZAN3L with industry standard single four channel LVDS transmitter for direct connect to LCD panels with LVDS interface.

With this level of integration, the gmZAN3 devices simplify and reduce the cost of LCD monitors while maintaining a high-degree of flexibility and quality.

1.1 gmZAN3 System Design Examples

Figure 1 below shows a typical analog interface LCD monitor system based on the gmZAN3. The gmZAN3 reduces system cost, simplifies hardware and firmware design and increased reliability because only a minimal number of components are required in the system.

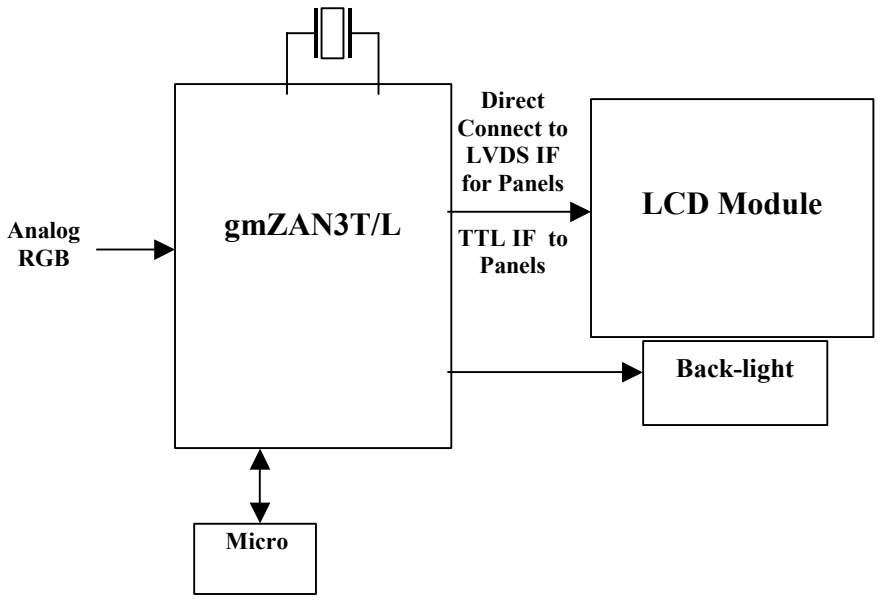


Figure 1. gmZAN3 System Design Examples

1.2 gmZAN3 Features

FEATURE OVERVIEW

- Zoom (from VGA) and shrink (from SXGA) scaling
- Integrated 8-bit triple-channel ADC / PLL
- Csync and SOG support
- On-chip versatile OSD engine
- All system clocks synthesized from a single external crystal
- On-chip reset circuit
- Programmable gamma correction (CLUT)
- PWM back light intensity control
- 5-Volt tolerant inputs – up to 13 GPIO pins
- Low EMI and power saving features

High-Quality Advanced Scaling

- Fully programmable zoom ratios
- Shrink capability from SXGA resolution
- Real Recovery™ function provides full color recovery image for refresh rates higher than those supported by the LCD panel

Analog RGB Input Port

- Supports up to SXGA input
- On-chip high-performance PLLs (only a single reference crystal required)

Auto-Configuration / Auto-Detection

- Automatic input format detection
- Robust phase and image positioning

On-Chip OSD Controller

- On-chip RAM for downloadable menus
- 1 and 2-bit per pixel character cells
- Horizontal and vertical stretch of OSD menus
- Blinking and transparency
- Proportional font support
- 90 degree rotation of fonts for Portrait Display support

Built in Test Pattern Generator

- Simplifies manufacturing and testing

Highly Integrated Solution to Provide Low System Cost

- Two layer PCB support
- On-chip reset feature to eliminate external reset component
- Output slew rate control
- Integrated Schmitt trigger for Vsync and Hsync

OUTPUT INTERFACE

gmZAN3T

- Support for 8 or 6-bit panels (with high-quality dithering)
- Swap red and green channels
- Ability to reverse bit order of each R, G, B output
- Single or double pixel clock
- Support up to XGA 85Hz

Built in Flexible LVDS Transmitter for gmZAN3L

- Four channel 6/8-bit LVDS transmitter (with high-quality dithering)
- Programmable channel swapping and polarity
- Support up to XGA 85Hz output

PACKAGE

- 128-pin PQFP

2 gmZAN3 Pinout

These devices are available in a 128-pin Plastic Quad Flat Pack (PQFP) package. Figure 2 provides the pin locations for all signals.

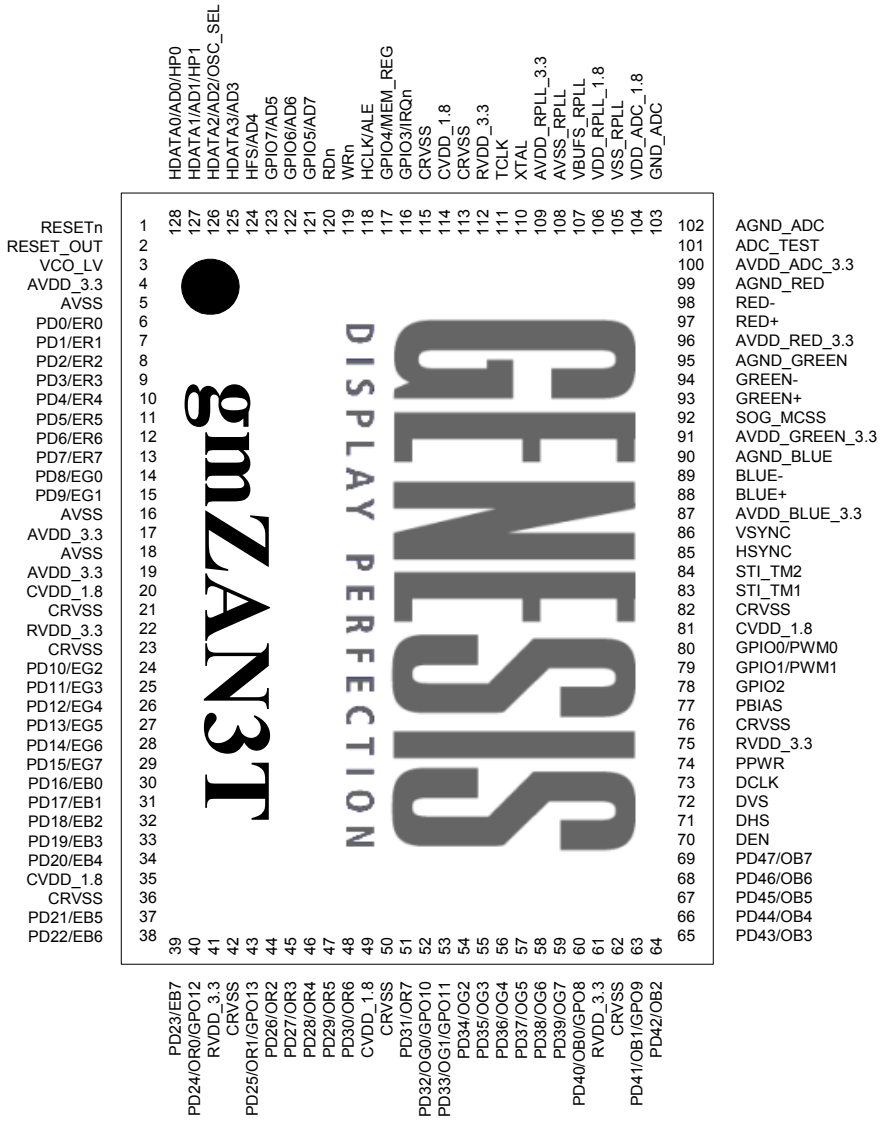


Figure 2. gmZAN3T Pin Out Diagram

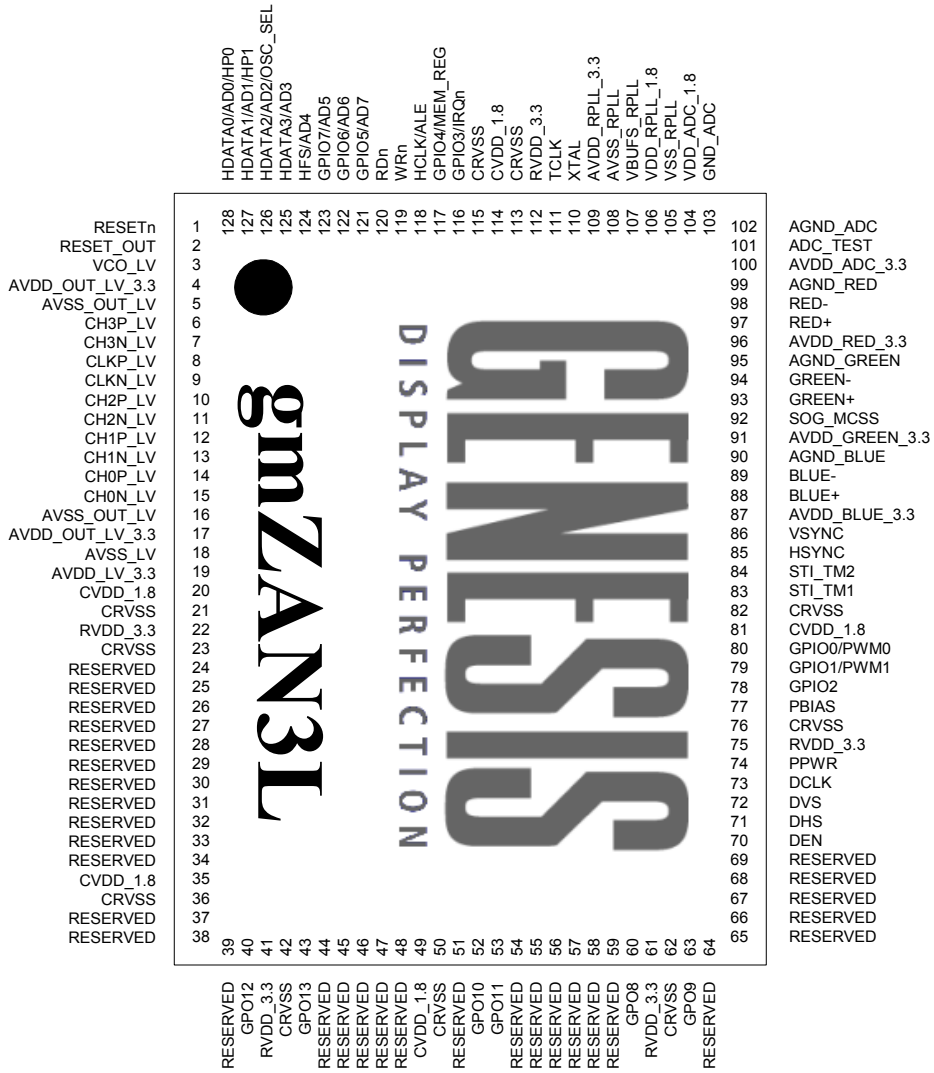


Figure 3. gmZAN3L Pin out Diagram

3 gmZAN3 Pin List

I/O Legend: A = Analog, **I** = Input, **O** = Output, **P** = Power, **G** = Ground, **I-PU** = Input with pull-up, **I-PD** = Input with pull down, **IO-PD** = Bidirectional with pull down

Table 1. Analog Input Port (Common to gmZAN3T and gmZAN3L)

Pin Name	No.	I/O	Description
AVDD_RED_3.3	96	AP	Analog power (3.3V) for the red channel. Must be bypassed with decoupling capacitor (0.1µF) to AGND_RED pin on system board (as close as possible to the pin).
RED+	97	AI	Positive analog input for Red channel.
RED-	98	AI	Negative analog input for Red channel.
AGND_RED	99	AG	Analog ground for the red channel. Must be directly connected to the system ground plane.
AVDD_GREEN_3.3	91	AP	Analog power (3.3V) for the green channel. Must be bypassed with decoupling capacitor (0.1µF) to AGND_GREEN pin on system board (as close as possible to the pin).
SOG_MCSS	92	AI	Dedicated Sync-on-Green pin
GREEN+	93	AI	Positive analog input for Green channel.
GREEN-	94	AI	Negative analog input for Green channel.
AGND_GREEN	95	AG	Analog ground for the green channel. Must be directly connected to the system ground plane.
AVDD_BLUE_3.3	87	AP	Analog power (3.3V) for the blue channel. Must be bypassed with decoupling capacitor (0.1µF) to AGND_BLUE pin on system board (as close as possible to the pin).
BLUE+	88	AI	Positive analog input for Blue channel.
BLUE-	89	AI	Negative analog input for Blue channel.
AGND_BLUE	90	AG	Analog ground for the blue channel. Must be directly connected to the system ground plane.
AVDD_ADC_3.3	100	AP	Analog power (3.3V) for ADC analog blocks that are shared by all three channels. Includes band gap reference, master biasing and full-scale adjust. Must be bypassed with decoupling capacitor (0.1µF) to AGND_ADC pin on system board (as close as possible to the pin).
ADC_TEST	101	AO	Analog test output for ADC. Do not connect.
AGND_ADC	102	AG	Analog ground for ADC analog blocks that are shared by all three channels. Includes band gap reference, master biasing and full-scale adjust. Must be directly connected to system ground plane.
GND_ADC	103	AG	Digital ground for ADC clocking circuit. Must be directly connected to the system ground plane.
VDD_ADC_1.8	104	P	Digital power (1.8V) for ADC encoding logic. Must be bypassed with decoupling capacitor (0.1µF) to GND_ADC pin on system board (as close as possible to the pin).
HSYNC	85	I	ADC input horizontal sync input. The input hysteresis can be set to 0.5V or 1.5V [Input, Schmitt trigger, 5V-tolerant]
VSYNC	86	I	ADC input vertical sync input. The input hysteresis can be set to 0.5V or 1.5V [Input, Schmitt triggered, 5V-tolerant]

Table 2. Clock Pins (Common to gmZAN3T and gmZAN3L)

Pin Name	No	I/O	Description
TCLK	111	AI	Reference clock (TCLK) from the 14.3MHz crystal oscillator (see Figure 5), or from single-ended CMOS/TTL clock oscillator (see Figure 8). This is a 5V-tolerant input. See Table 14.
XTAL	110	AO	Crystal oscillator output.
VBUFS_RPLL	107	AO	Reserved. For test purposes only. Do not connect
AVSS_RPLL	108	G	Analog ground for the reference DDS PLL. Must be directly connected to the system ground plane.
VSS_RPLL	105	G	Digital ground for the RCLK and clock generator. Must be directly connected to the system ground plane.
VDD_RPLL_1.8	106	P	Digital power for the RCLK and clock generators. Connect to 1.8V supply. Must be bypassed with a 0.1µFcapacitor to pin AVSS_RPLL
AVDD_RPLL_3.3	109	P	Analog power for the reference DDS PLL. Connect to 3.3V supply. Must be bypassed with a 0.1µFcapacitor to pin VSS_RPLL

Table 3. System Interface and GPIO Signals (gmZAN3T)

Pin Name	No	I/O	Description
RESETn	1	IO	Active-low hardware reset signal. The reset signal is held low for at least 150ms on the chip power up. It has an internal 60KΩl pull-up resistor which can be used for re-setting other system devices. See section 4.2 [Bi-directional (open drain), 5V-tolerant]
RESET_OUT	2	O	Active-high hardware reset signal. The reset signal is held high for at least 150ms on the chip power up. It can be used for re-setting other system devices[Output, open-drain 5V-tolerant]
GPIO0/PWM0	80	IO	General-purpose input/output signal or PWM0. Open drain option via register setting. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO1/PWM1	79	IO	General-purpose input/output signal or PWM1. Open drain option via register setting. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO2	78	IO	General-purpose input/output signal. Open drain option via register setting. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO3/IRQn	116	IO	General-purpose input/output signal. This is also active-low interrupt input external micro-controller. [Bi-directional, Active low open drain, 5V-tolerant]
GPIO4/MEM_REG	117	IO-PD	General-purpose input/output signal. Open drain option via register setting. For 8-bit A/D host interface, this selects between OSD memory (high) and register access (low). [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant, internal 60KΩ pull-down]
GPIO5/AD7	121	IO	General-purpose input/output signal or Adddress/data[7] for 8-bit A/D host interface. Open drain option via register setting. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO6/AD6	122	IO	General-purpose input/output signal or Adddress/data[6] for 8-bit A/D host interface. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO7/AD5	123	IO	General-purpose input/output signal or Adddress/data[5] for 8-bit A/D host interface. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPO8/PD40/OB0	60	O	General-purpose output signal. GPO or TTL 48-bit panel data/Odd Blue0.
GPO9/PD41/OB1	63	O	General-purpose output signal. GPO or TTL 48-bit panel data/Odd Blue1.
GPO10/PD32/OG0	52	O	General-purpose output signal. GPO or TTL 48-bit panel data/Odd Green0.
GPO11/PD33/OG1	53	O	General-purpose output signal. GPO or TTL 48-bit panel data/Odd Green1.
GPO12/PD24/OR0	40	O	General-purpose output signal. GPO or TTL 48-bit panel data/Odd Red0.
GPO13/PD25/OR1	43	O	General-purpose output signal. GPO or TTL 48-bit panel data/Odd Red1.
HDATA0/ADO/HP0 HDATA1/AD1/HP1	128 127	IO-PD	Host data for 6-wire serial protocol. For 8-bit A/D host interface determines A/D0 and A/D1 bit. Note: See Table 19, Boostrap Signals [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant, internal 60KΩ pull-down]
HDATA2/AD2/OSC_SEL	126	IO-PD	If using 6-wire protocol the HDATA[2] determines bit 2 of the host data. For 8-bit A/D host interface determines A/D2 bit. Note: See Table 19, Boostrap Signals [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant, internal 60KΩ pull-down]
HDATA3/AD3	125	IO-PD	If using 6-wire protocol the HDATA[3] determines the upper A/D3 bits of the host data. For 8-bit A/D host interface determines address/data bit. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant, internal 60KΩ pull-down]
HFS/AD4	124	IO	Host Frame Sync. Frames the packet on the serial channel 6-wire interface. For 8-bit A/D host interface determines A/D4 bit. [Bi-directional, Schmitt trigger (400mV typical hysteresis), slew rate limited, 5V-tolerant]
HCLK/ALE	118	I	Clock signal input for the 6-wire interface and 2-wire modes. For 8-bit A/D host interface it becomes the Address Latch Enable. [Input, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
WRn	119	I-PU	For 8-bit A/D host interface write strobe input. Internal 60KΩ pull-up.
RDn	120	I-PU	For 8-bit A/D host interface read strobe input. Internal 60KΩ pull-up

Table 4. System Interface and GPIO Signals (gmZAN3L)

Pin Name	No	I/O	Description
RESETn	1	IO	Active-low hardware reset signal. The reset signal is held low for at least 150ms on the chip power up. It has an internal 60KΩl pull-up resistor which can be used for re-setting other system devices. See section 4.2 [Bi-directional (open drain), 5V-tolerant]
RESET_OUT	2	O	Active-high hardware reset signal. The reset signal is held high for at least 150ms on the chip power up. It can be used for re-setting other system devices[Output, 5V-tolerant]
GPIO0/PWM0	80	IO	General-purpose input/output signal or PWM0. Open drain option via register setting. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO1/PWM1	79	IO	General-purpose input/output signal or PWM1. Open drain option via register setting. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO2	78	IO	General-purpose input/output signal. Open drain option via register setting. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO3/IRQn	116	IO	General-purpose input/output signal. This is also active-low interrupt input external micro-controller. [Bi-directional, Active low open drain, 5V-tolerant]
GPIO4/MEM_REG	117	IO-PD	General-purpose input/output signal. Open drain option via register setting. For 8-bit A/D host interface, this selects between OSD memory (high) and register access (low). [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant, internal 60KΩ pull-down]
GPIO5/AD7	121	IO	General-purpose input/output signal or Adddress/data[7] for 8-bit A/D host interface. Open drain option via register setting. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO6/AD6	122	IO	General-purpose input/output signal or Adddress/data[6] for 8-bit A/D host interface. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO7/AD5	123	IO	General-purpose input/output signal or Adddress/data[5] for 8-bit A/D host interface. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPO8	60	O	General-purpose output signal.
GPO9	63	O	General-purpose output signal.
GPO10	52	O	General-purpose output.
GPO11	53	O	General-purpose output signal.
GPO12	40	O	General-purpose output signal.
GPO13	43	O	General-purpose output signal.
HDATA0/ADO/HP0 HDATA1/AD1/HP1	128 127	IO-PD	Host data for 6-wire serial protocol. For 8-bit A/D host interface determines AD0 and AD1 bit. Note: See Table 19, Boostrap Signals [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant, internal 60KΩ pull-down]
HDATA2/AD2/OSC_SEL	126	IO-PD	If using 6-wire protocol the HDATA[2] determines bit 2 of the host data. For 8-bit A/D host interface determines AD2 bit. Note: See Table 19, Boostrap Signals [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant, internal 60KΩ pull-down]
HDATA3/AD3	125	IO-PD	If using 6-wire protocol the HDATA[3] determines the upper AD3 bits of the host data. For 8-bit A/D host interface determines address/data bit. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant, internal 60KΩ pull-down]
HFS/AD4	124	IO	Host Frame Sync. Frames the packet on the serial channel 6-wire interface. For 8-bit A/D host interface determines AD4 bit. [Bi-directional, Schmitt trigger (400mV typical hysteresis), slew rate limited, 5V-tolerant]
HCLK/ALE	118	I	Clock signal input for the 6-wire interface and 2-wire modes. For 8-bit A/D host interface it becomes the Address Latch Enable. [Input, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
WRn	119	I-PU	For 8-bit A/D host interface write strobe input. Internal 60KΩ pull-up.
RDn	120	I-PU	For 8-bit A/D host interface read strobe input. Internal 60KΩ pull-up.

Table 5. Display Output Port for (gmZAN3L)

Pin Name	No	I/O	Description
DCLK	73	O	Not required. Panel output clock. Can be used for test purposes [Tri-state output, Programmable Drive]
DVS	72	O	Not required. Panel Vertical Sync. Can be used for test purposes [Tri-state output, Programmable Drive]
DHS	71	O	Not required. Panel Horizontal Sync. Can be used for test purposes [Tri-state output, Programmable Drive]
DEN	70	O	Not required. Panel Display Enable, which frames the output background. Can be used for test purposes [Tri-state output, Programmable Drive]
PBIAS	77	O	Panel Bias Control (back light enable)
PPWR	74	O	Panel Power Control
CH3P_LV	6	O	LVDS Channel 3 positive[1]
CH3N_LV	7	O	LVDS Channel 3 negative[1]
CLKP_LV	8	O	LVDS Clock positive[1]
CLKN_LV	9	O	LVDS Clock negative[1]
CH2P_LV	10	O	LVDS Channel 2 positive[1]
CH2N_LV	11	O	LVDS Channel 2 negative[1]
CH1P_LV	12	O	LVDS Channel 1 positive[1]
CH1N_LV	13	O	LVDS Channel 1 negative[1]
CH0P_LV	14	O	LVDS Channel 0 positive[1]
CH0N_LV	15	O	LVDS Channel 0 negative[1]

Note: [1]These pin names are based on having swapping enabled on the initial positive and negative LVDS signals.

Table 6. Display Output Port for (gmZAN3T)

Pin Name	No	I/O	Description
DCLK	73	O	Panel output clock. [Tri-state output, Programmable Drive]
DVS	72	O	Panel Vertical Sync. [Tri-state output, Programmable Drive]
DHS	71	O	Panel Horizontal Sync. [Tri-state output, Programmable Drive]
DEN	70	O	Panel Display Enable, which frames the output background. [Tri-state output, Programmable Drive]
PBIAS	77	O	Panel Bias Control (back light enable)
PPWR	74	O	Panel Power Control
PD47/OB7	69	O	Panel output data or Odd Blue 7 data bit. [Tri-state output, Programmable Drive]
PD46/OB6	68	O	Panel output data or Odd Blue 6 data bit. [Tri-state output, Programmable Drive]
PD45/OB5	67	O	Panel output data or Odd Blue 5 data bit. [Tri-state output, Programmable Drive]
PD44/OB4	66	O	Panel output data or Odd Blue 4 data bit. [Tri-state output, Programmable Drive]
PD43/OB3	65	O	Panel output data or Odd Blue 3 data bit. [Tri-state output, Programmable Drive]
PD42/OB2	64	O	Panel output data or Odd Blue 2 data bit. [Tri-state output, Programmable Drive]
PD41/OB1/GPO9	63	O	Panel output data or Odd Blue 1 data bit. [Tri-state output, Programmable Drive] When used with 6-bit panels can be used as GPO.
PD40/OB0/GPO8	60	O	Panel output data or Odd Blue 0 data bit. [Tri-state output, Programmable Drive] When used with 6-bit panels can be used as GPO.
PD39/OG7	59	O	Panel output data or Odd Green 7 data bit. [Tri-state output, Programmable Drive]
PD38/OG6	58	O	Panel output data or Odd Green 6 data bit. [Tri-state output, Programmable Drive]
PD37/OG5	57	O	Panel output data or Odd Green 5 data bit. [Tri-state output, Programmable Drive]
PD36/OG4	56	O	Panel output data or Odd Green 4 data bit. [Tri-state output, Programmable Drive]
PD35/OG3	55	O	Panel output data or Odd Green 3 data bit. [Tri-state output, Programmable Drive]
PD34/OG2	54	O	Panel output data or Odd Green 2 data bit. [Tri-state output, Programmable Drive]
PD33/OG1/GPO11	53	O	Panel output data or Odd Green 1 data bit. [Tri-state output, Programmable Drive] When used with 6-bit panels can be used as GPO.
PD32/OG0/GPO10	52	O	Panel output data or Odd Green 0 data bit. [Tri-state output, Programmable Drive] When used with 6-bit panels can be used as GPO.
PD31/OR7	51	O	Panel output data or Odd Red 7 data bit. [Tri-state output, Programmable Drive]
PD30/OR6	48	O	Panel output data or Odd Red 6 data bit. [Tri-state output, Programmable Drive]
PD29/OR5	47	O	Panel output data or Odd Red 5 data bit. [Tri-state output, Programmable Drive]
PD28/OR4	46	O	Panel output data or Odd Red 4 data bit. [Tri-state output, Programmable Drive]
PD27/OR3	45	O	Panel output data or Odd Red 3 data bit. [Tri-state output, Programmable Drive]
PD26/OR2	44	O	Panel output data or Odd Red 2 data bit. [Tri-state output, Programmable Drive]
PD25/OR1/GPO13	43	O	Panel output data or Odd Red 1 data bit. [Tri-state output, Programmable Drive] When used with 6-bit panels can be used as GPO.
PD24/OR0/GPO12	40	O	Panel output data or Odd Red 0 data bit. [Tri-state output, Programmable Drive] When used with 6-bit panels can be used as GPO.
PD23/EB7	39	O	Panel output data or Even Blue 7 data bit. [Tri-state output, Programmable Drive]
PD22/EB6	38	O	Panel output data or Even Blue 6 data bit. [Tri-state output, Programmable Drive]
PD21/EB5	37	O	Panel output data or Even Blue 5 data bit. [Tri-state output, Programmable Drive]
PD20/EB4	34	O	Panel output data or Even Blue 4 data bit. [Tri-state output, Programmable Drive]
PD19/EB3	33	O	Panel output data or Even Blue 3 data bit. [Tri-state output, Programmable Drive]
PD18/EB2	32	O	Panel output data or Even Blue 2 data bit. [Tri-state output, Programmable Drive]
PD17/EB1	31	O	Panel output data or Even Blue 1 data bit. [Tri-state output, Programmable Drive]
PD16/EB0	30	O	Panel output data or Even Blue 0 data bit. [Tri-state output, Programmable Drive]
PD15/EG7	29	O	Panel output data or Even Green 7 data bit. [Tri-state output, Programmable Drive]
PD14/EG6	28	O	Panel output data or Even Green 6 data bit. [Tri-state output, Programmable Drive]
PD13/EG5	27	O	Panel output data or Even Green 5 data bit. [Tri-state output, Programmable Drive]
PD12/EG4	26	O	Panel output data or Even Green 4 data bit. [Tri-state output, Programmable Drive]
PD11/EG3	25	O	Panel output data or Even Green 3 data bit. [Tri-state output, Programmable Drive]
PD10/EG2	24	O	Panel output data or Even Green 2 data bit. [Tri-state output, Programmable Drive]
PD9/EG1	15	O	Panel output data or Even Green 1 data bit. [Tri-state output, Programmable Drive]
PD8/EG0	14	O	Panel output data or Even Green 0 data bit. [Tri-state output, Programmable Drive]
PD7/ER7	13	O	Panel output data or Even Red 7 data bit. [Tri-state output, Programmable Drive]
PD6/ER6	12	O	Panel output data or Even Red 6 data bit. [Tri-state output, Programmable Drive]
PD5/ER5	11	O	Panel output data or Even Red 5 data bit. [Tri-state output, Programmable Drive]
PD4/ER4	10	O	Panel output data or Even Red 4 data bit. [Tri-state output, Programmable Drive]
PD3/ER3	9	O	Panel output data or Even Red 3 data bit. [Tri-state output, Programmable Drive]
PD2/ER2	8	O	Panel output data or Even Red 2 data bit. [Tri-state output, Programmable Drive]

Pin Name	No	I/O	Description
PD1/ER1	7	O	Panel output data or Even Red 1 data bit. [Tri-state output, Programmable Drive]
PD0/ER0	6	O	Panel output data or Even Red 0 data bit. [Tri-state output, Programmable Drive]

Table 7. Reserved Pins for gmZAN3L

Pin Name	No	I/O	Description
Reserved	69	O	Do not connect
Reserved	68	O	Do not connect.
Reserved	67	O	Do not connect.
Reserved	66	O	Do not connect.
Reserved	65	O	Do not connect.
Reserved	64	O	Do not connect.
Reserved	59	O	Do not connect.
Reserved	58	O	Do not connect.
Reserved	57	O	Do not connect.
Reserved	56	O	Do not connect.
Reserved	55	O	Do not connect.
Reserved	54	O	Do not connect.
Reserved	51	O	Do not connect.
Reserved	48	O	Do not connect.
Reserved	47	O	Do not connect.
Reserved	46	O	Do not connect.
Reserved	45	O	Do not connect.
Reserved	44	O	Do not connect.
Reserved	39	O	Do not connect.
Reserved	38	O	Do not connect.
Reserved	37	O	Do not connect.
Reserved	34	O	Do not connect.
Reserved	33	O	Do not connect.
Reserved	32	O	Do not connect.
Reserved	31	O	Do not connect.
Reserved	30	O	Do not connect.
Reserved	29	O	Do not connect.
Reserved	28	O	Do not connect.
Reserved	27	O	Do not connect.
Reserved	26	O	Do not connect.
Reserved	25	O	Do not connect.
Reserved	24	O	Do not connect.
VC0_LV	3	O	For test purposes only. Do not connect
STI_TM1	83	I	For test purposes only. Has internal 60KΩ pull-down register. Must be connected to GND
STI_TM2	84	I	For test purposes only. Has internal 60KΩ pull-down register. Must be connected to GND

Table 8. Reserve Pins for gmZAN3T

Pin Name	No	I/O	Description
VCO_LV	3	O	For test purposes only. Do not connect
STI_TM1	83	I-PD	For test purposes only. Has internal 60KΩ pull-down resistor.
STI_TM2	84	I-PD	For test purposes only. Has internal 60KΩ pull-down resistor.

Table 9. I/O Power and Ground Pins for gmZAN3L

Pin Name	No	I/O	Description
RVDD_3.3	22 41 61 75 112	P P P P P	Connect to 3.3V digital supply. Must be bypassed with a 0.1µF capacitor to CRVSS (as close to the pin as possible).
CRVSS	21 23 36	G G G	Connect to digital ground.

	42 50 62 76 82 113 115	G G G G G G G	
CVDD_1.8	20 35 49 81 114	P P P P P	Connect to 1.8V digital supply. Must be bypassed with a 0.1µF capacitor to CRVSS (as close to the pin as possible).

Table 10. Power and Ground Pins for LVDS Transmitter for gmZAN3L

Pin Name	No	I/O	Description
AVDD_OUT_LV_3.3	4 17	AP	Analog power for on-chip LVDS output buffer. Connect to 3.3V supply. Must be bypassed with a 0.1µFcapacitor to pin AVSS_OUT_LV
AVDD_LV_3.3	19	AP	Analog power for on-chip LVDS PLL. Connect to 3.3V supply. Must be bypassed with a 0.1µFcapacitor to pin AVSS_LV
AVSS_OUT_LV	5 16	G	Analog ground for on-chip LVDS output buffer. Must be directly connected to the system ground plane
AVSS_LV	18	G	Analog ground for on-chip LVDS PLL. Must be directly connected to the system ground plane

Table 11. I/O Power and Ground pins for gmZAN3T

Pin Name	No	I/O	Description
RVDD_3.3	22 41 61 75 112	P P P P P	Connect to 3.3V digital supply. Must be bypassed with a 0.1µF capacitor to CRVSS (as close to the pin as possible).
CRVSS	21 23 36 42 50 62 76 82 113 115	G G G G G G G G G G	Connect to digital ground.
CVDD_1.8	20 35 49 81 114	P P P P P	Connect to 1.8V digital supply. Must be bypassed with a 0.1µF capacitor to CRVSS (as close to the pin as possible).
AVSS	5 16 18	G G G	Connect to digital ground
AVDD_3.3	4 17 19	P	Connect to 3.3V supply Must be bypassed with a 0.1µF capacitor to ACVSS (as close to the pin as possible).

4 Functional Description

A functional block diagram is illustrated below. Each of the functional units shown is described in the following sections.

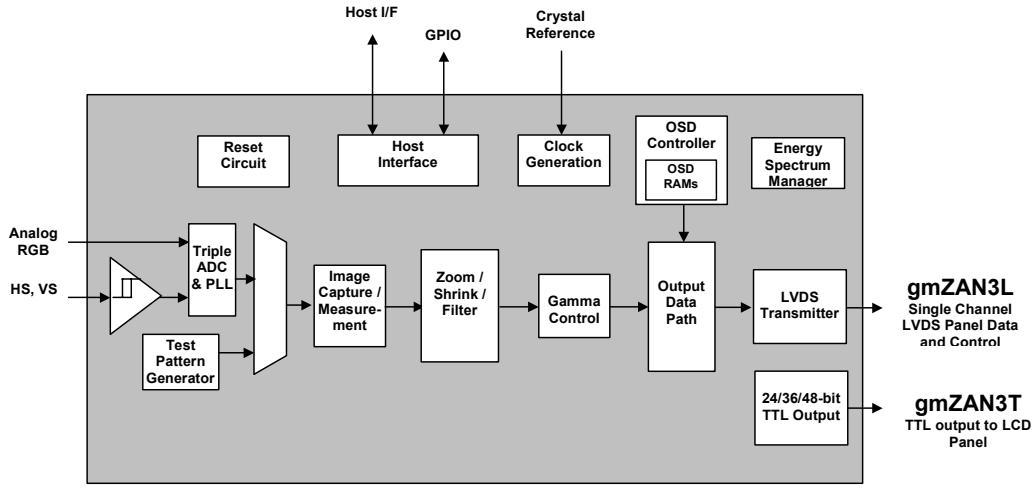


Figure 4. gmZAN3 Functional Block Diagram

4.1 Clock Generation

The gmZAN3 features two clock inputs. All additional clocks are internal clocks derived from one or more of these:

1. Crystal Input Clock (TCLK and XTAL). This is the input pair to an internal crystal oscillator and corresponding logic. A 14.318 MHz crystal is recommended. Other crystal frequencies may be used, but require custom programming. This is illustrated in Figure 5 below. This option is selected by connecting a 10KΩ pull-up to HDATA2/AD2/OSC_SEL. Alternatively a single-ended TTL/CMOS clock oscillator can be driven into the TCLK pin (leave XTAL and HDATA2/AD2/OSC_SEL as N/C in this case). This is illustrated in Figure 8 below. See also Table 14.
2. Host Interface Transfer Clock (HCLK). For 2 or 6-wire Host Interface Port only. Not for muxed A/D.

The gmZAN3 TCLK oscillator circuitry is a custom designed circuit to support the use of an external oscillator or a crystal resonator to generate a reference frequency source for the gmZAN3 device.

4.1.1 Using the Internal Oscillator with External Crystal

The first option for providing a clock reference is to use the internal oscillator with an external crystal. The oscillator circuit is designed to provide a very low jitter and very low harmonic clock to the internal circuitry of the gmZAN3. An Automatic Gain Control (AGC) is used to insure startup and operation over

a wide range of conditions. The oscillator circuit also minimizes the overdrive of the crystal, which reduces the aging of the crystal.

When the gmZAN3 is in reset, the state of the HDATA2/AD2/OSC_SEL pin is sampled. If the pin is pulled high by connecting to VDD through a pull-up resistor (10KΩ recommended, 15KΩ maximum) then internal oscillator is enabled. In this mode a crystal resonator is connected between TCLK and the XTAL with the appropriately sized loading capacitors C_{L1} and C_{L2}. The size of C_{L1} and C_{L2} are determined from the crystal manufacturer's specification and by compensating for the parasitic capacitance of the gmZAN3 device and the printed circuit board traces. The loading capacitors are terminated to the analog VDD power supply. This connection increases the power supply rejection ratio when compared to terminating the loading capacitors to ground.

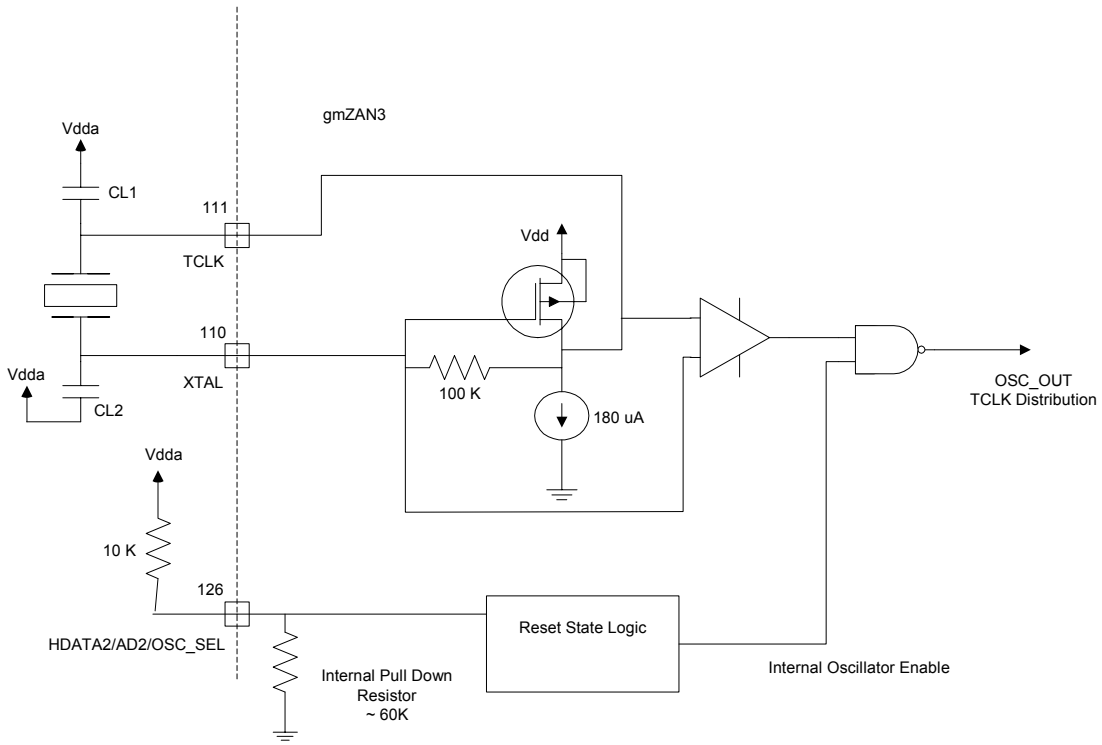


Figure 5. Using the Internal Oscillator with External Crystal

The TCLK oscillator uses a Pierce Oscillator circuit. The output of the oscillator circuit, measured at the TCLK pin, is an approximate sine wave with a bias of about 2 volts above ground (see Figure 6). The peak-to-peak voltage of the output can range from 250 mV to 1000 mV depending on the specific characteristics of the crystal and variation in the oscillator characteristics. The output of the oscillator is connected to a comparator that converts the sine wave to a square wave. The comparator requires a

minimum signal level of about 50-mV peak to peak to function correctly. The output of the comparator is buffered and then distributed to the gmZAN3 circuits.

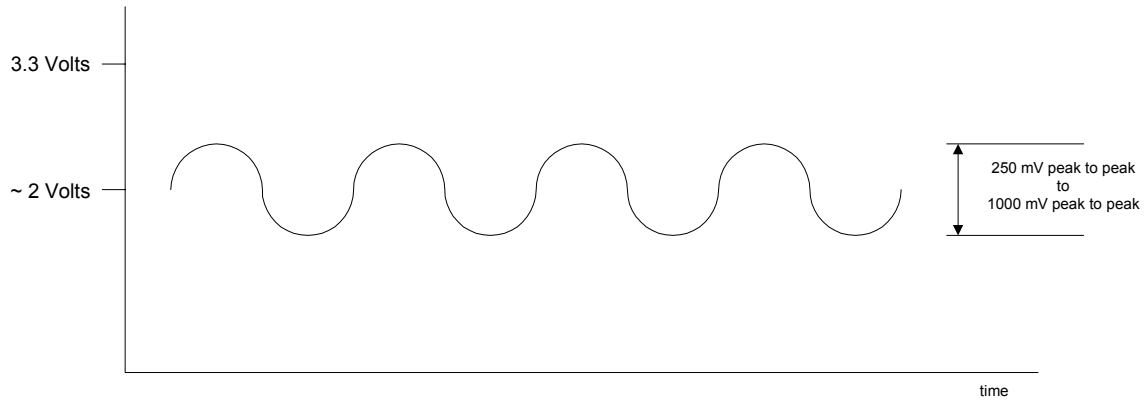


Figure 6. Internal Oscillator Output

One of the design parameters that must be given some consideration is the value of the loading capacitors used with the crystal as shown in Figure 7. The loading capacitance (C_{load}) on the crystal is the combination of C_{L1} and C_{L2} and is calculated by $C_{load} = ((C_{L1} * C_{L2}) / (C_{L1} + C_{L2})) + C_{shunt}$. The shunt capacitance C_{shunt} is the effective capacitance between the XTAL and TCLK pins. For the gmZAN3 this is approximately 9 pF. C_{L1} and C_{L2} are a parallel combination of the external loading capacitors (C_{ex}), the PCB board capacitance (C_{pcb}), the pin capacitance (C_{pin}), the pad capacitance (C_{pad}), and the ESD protection capacitance (C_{esd}). The capacitances are symmetrical so that $C_{L1} = C_{L2} = C_{ex} + C_{PCB} + C_{pin} + C_{pad} + C_{ESD}$. The correct value of C_{ex} must be calculated based on the values of the load capacitances. Approximate values are provided in Figure 7.

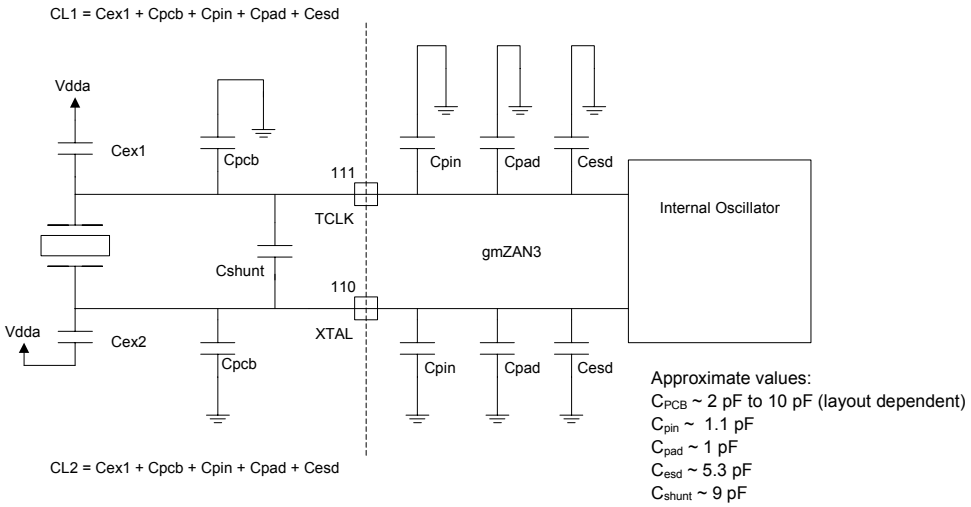


Figure 7. Sources of Parasitic Capacitance

Some attention must be given to the details of the oscillator circuit when used with a crystal resonator. The PCB traces should be as short as possible. The value of C_{load} that is specified by the manufacturer should not be exceeded because of potential start up problems with the oscillator. Additionally, the crystal should be a parallel resonate-cut and the value of the equivalent series resistance must be less then 90 Ohms.

4.1.2 Using an External Clock Oscillator

Another option for providing the reference clock is to use a single-ended external clock oscillator. When the gmZAN3 is in reset, the state of the HDATA2/AD2/OSC_SEL is sampled. If the pin is left unconnected (internal pull-down) then external oscillator mode is enabled. In this mode the internal oscillator circuit is disabled and the external oscillator signal that is connected to the TCLK pin is routed to an internal clock buffer. This is illustrated in Figure 8.

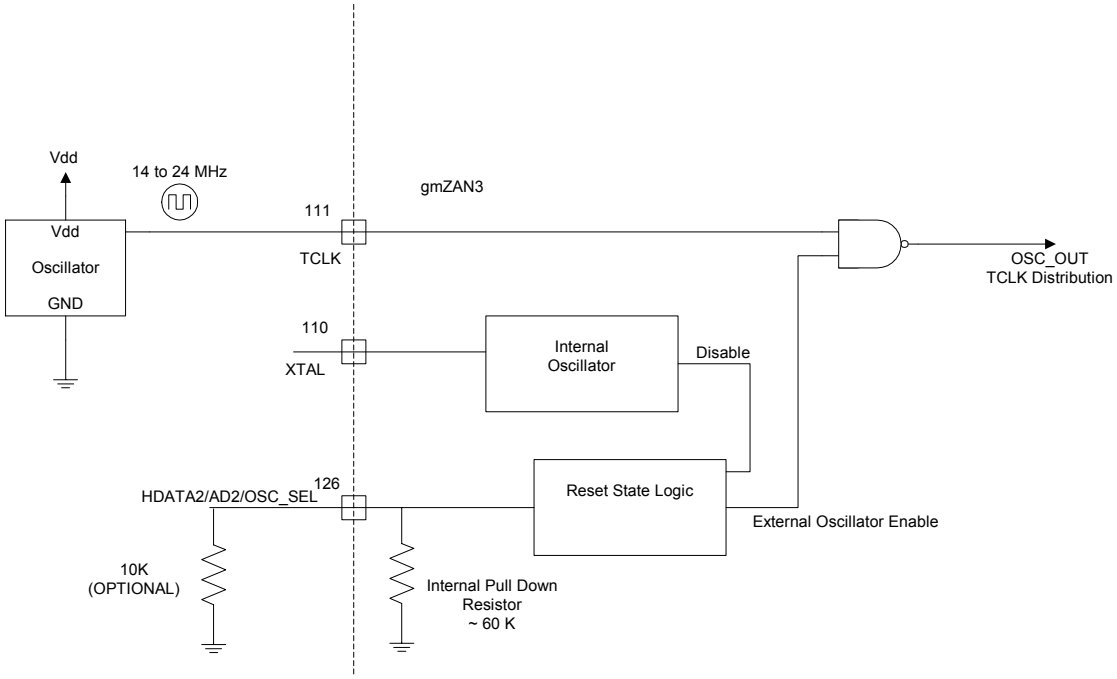


Figure 8. Using an External Single-ended Clock Oscillator

Table 12. TCLK Specification

Frequency	12 to 24 MHz
Jitter Tolerance	250 ps
Rise Time (10% to 90%)	5 ns

Maximum Duty Cycle	40-60

4.1.3 Clock Synthesis

The gmZAN3 synthesizes all additional clocks internally as illustrated in Figure 9 below. The synthesized clocks are as follows:

1. Main Timing Clock (TCLK) is the output of the chip internal crystal oscillator. TCLK is derived from the TCLK/XTAL pad input.
2. Reference Clock (RCLK) synthesized by RCLK PLL (RPLL) using TCLK as the reference.
3. Input Source Clock (SCLK) synthesized by Source DDS (SDDS) PLL using input HSYNC as the reference. The SDDS internal digital logic is driven by RCLK.
4. ADC Output Clock (ACLK) is a delay-adjusted ADC sampling clock, ACLK. ACLK is derived from SCLK.
5. Host Port Clock for OSD SRAM and muxed A/D port. TCLK at power up, and selectable as RCLK/2 or RCLK/4.

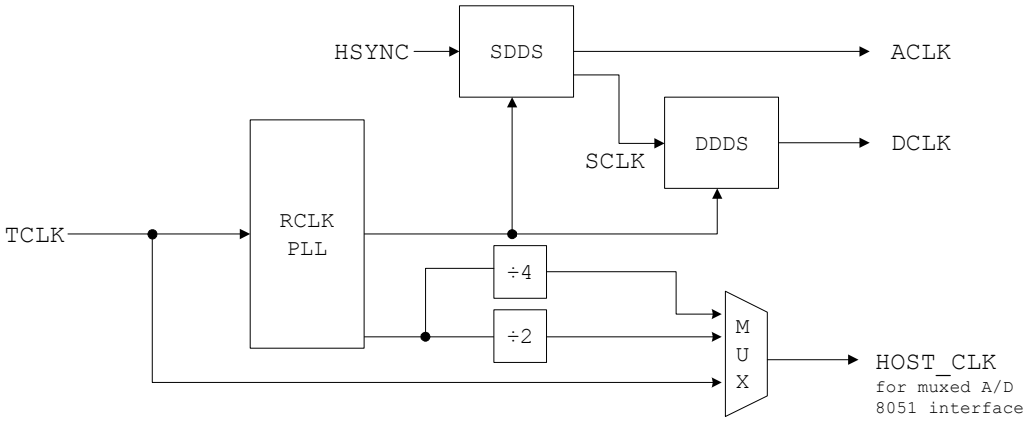


Figure 9. Internally Synthesized Clocks

The on-chip clock domains are selected from the synthesized clocks. These include:

1. ADC Domain Clock (ACLK) which is also the input clock. Max = 100MHz
2. Host Interface (HOST_CLK). Max = 120MHz
3. Scaler and Display Pixel Clock (DP_CLK). Max = 100MHz
4. Source Timing Measurement Domain Clock (IFM_CLK). Max = 50MHz

4.2 Hardware Reset

Hardware Reset is performed during power-up by the internal power-on reset circuit. The power-on reset (POR) circuit generates two signals:

- RESETn: an active-low pulse of around 120ms
- RESET_OUT: an active-high pulse with identical timing as RESETn; this is basically an inverted version of RESETn. Must use 10KΩ pull-up resistor because this is an open-drain output.

The reset signals are generated whenever the supply 3.3V voltage reaches a voltage level of +2.5V, or if the RESETn pin is pulled low for a minimum of 160 us. A TCLK input (see Clock Requirements below) must be applied before, during, and after the reset. While RESETn is active low, pins PD[47:10] DEN, DHS, DVS, and DCLK are all HI-Z; HDATA [3:0], GPIO[7:0] and HFS are inputs; PBIAS and PPWR are active outputs (0 after reset is complete). When the reset period is complete and RESETn is de-asserted, the IC power up sequence is:

1. Reset all registers to their default state (this is 00h unless otherwise specified in the gmZAN3 Register Listing).
2. Force each clock domain to reset. Internal reset will remain asserted for 64 local clock domain cycles following the de-assertion of RESETn.

The following figures illustrate different system configuration options of the gmZAN3 POR circuit:

1. In figure 10, the gmZAN3 RESET_OUT signal resets the external MCU during power-up. An optional push button allows the user to reset the entire system.
2. In figure 11, an external MCU generates the reset, applied to RESETn input of gmZAN3.

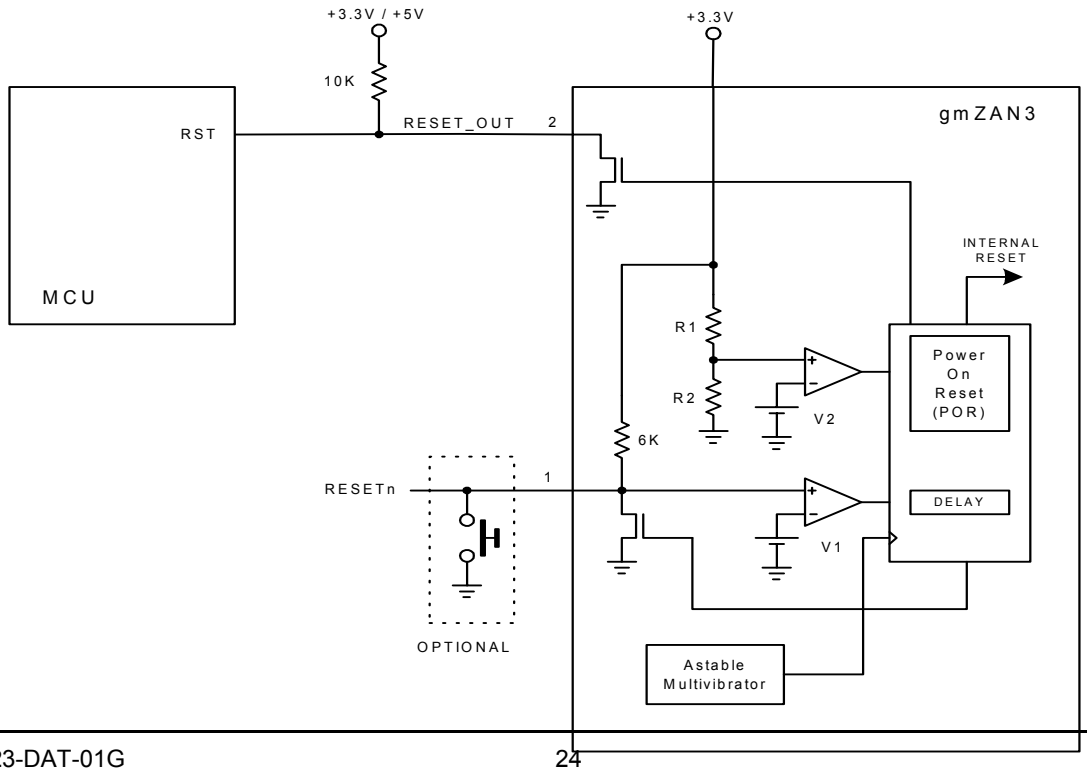


Figure 10. gmZAN3 Re-setting External MCU

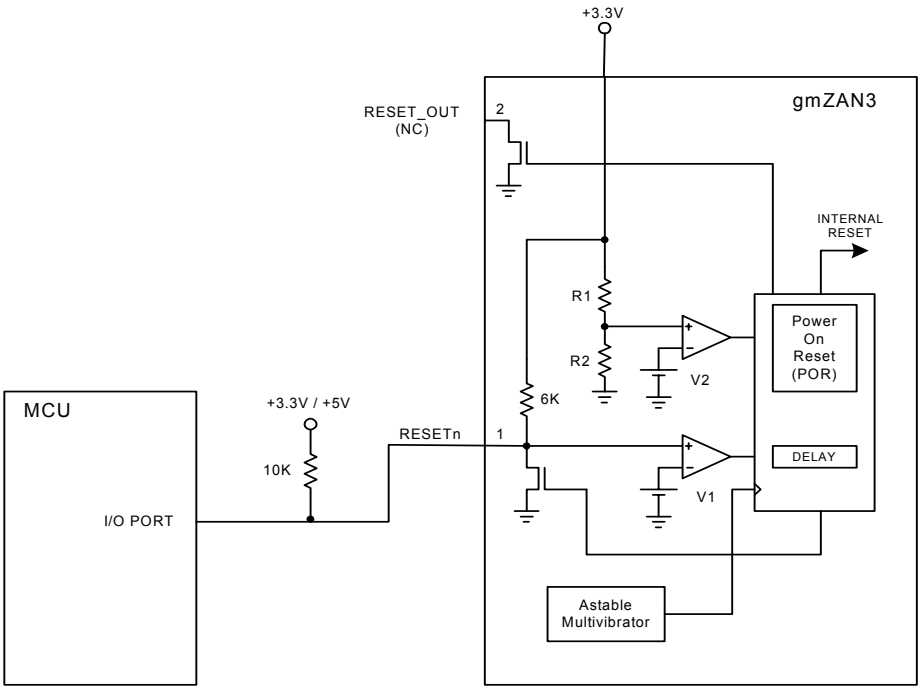


Figure 11. External MCU Re-setting gmZAN3

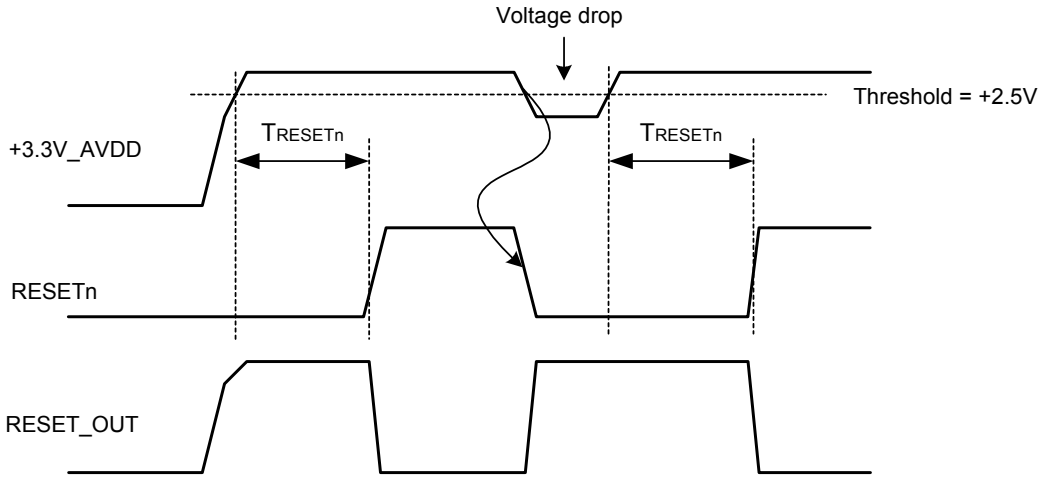


Figure 12. Reset Signal Timing (T_{RESETn})

Note:

- The RESETn pin may also be connected to an external momentary contact switch to ground, for a Reset Button feature.
- When analog 3.3V reaches the reset threshold (2.5V) an active LOW reset signal is generated (RESETn). The duration of the reset pulse is about 120ms.
- The RESET_OUT is active HIGH output pulse held high while RESETn is LOW
- When +3.3V_AVDD drops below 2.5V a reset signal is generated. The reset signal gets de-asserted about 120ms after the input voltage rises above the 2.5V threshold (see figure 12).
- The following table shows the temperature/voltage variation effects on the RESETn timing (T_{RESETn}).

Table 13. Temperature and Voltage variations for T_{RESETn}

Voltage	0°C	Room Temperature	100°C
3.0V	107 ms	105 ms	110 ms
3.3V	119 ms	118 ms	119 ms
3.6V	123 ms	123 ms	126 ms

4.3 Analog to Digital Converter

The gmZAN3chip has three ADC's (analog-to-digital converters), one for each color (red, green, and blue).

4.3.1 ADC Pin Connection

The analog RGB signals are connected to the gmZAN3 as described below:

Table 14. Pin Connection for RGB Input with HSYNC/VSYNC

Pin Name	ADC Signal Name
Red+	Red
Red-	Terminate as illustrated in Figure 13
SOG_MCSS	Dedicated Sync-on-Green pin (for sync-tip clamping)
Green+	Green
Green-	Terminate as illustrated in Figure 13
Blue+	Blue
Blue-	Terminate as illustrated in Figure 13
HSYNC	Horizontal Sync (Terminate as illustrated in Figure 13)
VSYNC	Vertical Sync (Terminate as with HSYNC illustrated in Figure 13)

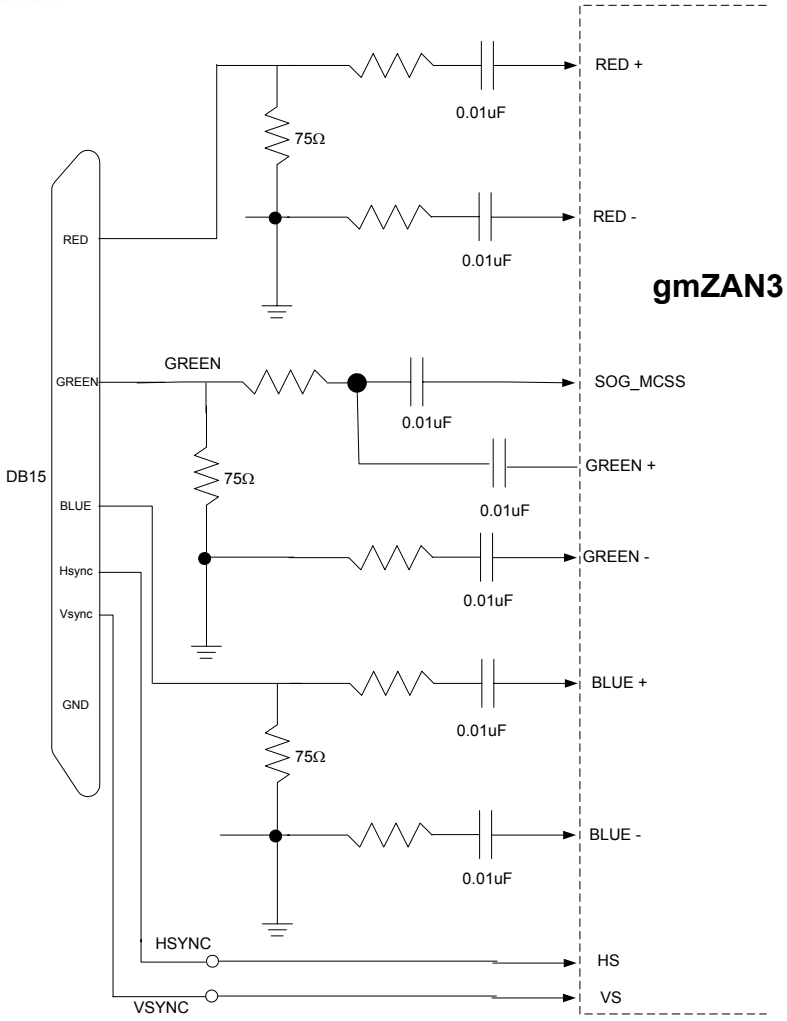


Figure 13. Example ADC Signal Terminations

NOTE: It is very important to follow the recommended layout guidelines for the circuit shown in Figure 13. Follow the recommendations in the *gmZAN3 Layout Guidelines*. For specific component values refer to the *gmZAN3 RD1 Reference Design Schematics*.

4.3.2 ADC Characteristics

The table below summarizes the characteristics of the ADC:

Table 15. ADC Characteristics

	MIN	TYP	MAX	NOTE
Track & Hold Amp Bandwidth			290 MHz	Guaranteed. Note that the Track & Hold Amp Bandwidth is programmable. 290 MHz is the maximum setting.
Full Scale Adjust Range at RGB Inputs	0.55 V		0.90 V	
Full Scale Adjust Sensitivity		+/- 1 LSB		Measured at ADC Output. Independent of full scale RGB input.
Zero Scale Adjust Sensitivity		+/- 1 LSB		Measured at ADC Output.
Sampling Frequency (Fs)	10 MHz		100 MHz	
Differential Non-Linearity (DNL)		+/-0.5 LSB	+/-0.9 LSB	Fs = 100 MHz
No Missing Codes				Guaranteed by test.
Integral Non-Linearity (INL)		+/- 1.5 LSB		Fs =100 MHz
Channel to Channel Matching		+/- 0.5 LSB		

Note that input formats with resolutions or refresh rates higher than that supported by the LCD panel are supported as recovery modes only. This is called RealRecovery™. For example, it may be necessary to shrink the image. This may introduce image artifacts. However, the image is clear enough to allow the user to change the display properties.

The gmZAN3 ADC has a built in clamp circuit for AC-coupled inputs. By inserting series capacitors (about 10 nF), the DC offset of an external video source can be removed. The clamp pulse position and width are programmable.

4.3.3 Clock Recovery Circuit

The SDDS (Source Direct Digital Synthesis) clock recovery circuit generates the clock used to sample analog RGB data (ACLK). This circuit is locked to HSYNC of the incoming video signal.

Patented digital clock synthesis technology makes the gmZAN3 clock circuits resistant to temperature/voltage drift. Using DDS (Direct Digital Synthesis) technology, the clock recovery circuit can generate any ACLK clock frequency within the range of 10 MHz to 100 MHz.

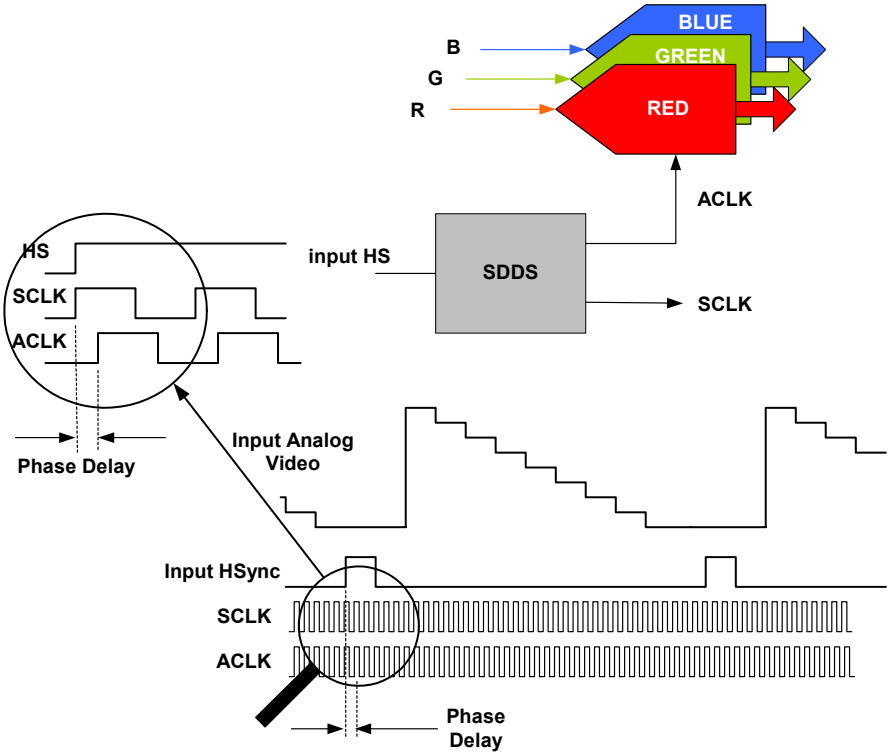


Figure 14. gmZAN3 Clock Recovery

4.3.4 Sampling Phase Adjustment

The programmable ADC sampling phase is adjusted by delaying the (input HSYNC aligned) SCLK to produce the ADC clock (ACLK) inside the SDDS. The phase delay is programmable in 64 steps as a fraction of the ACLK period. The accuracy of the sampling phase is checked and the result read from a register. This feature enables accurate auto-adjustment of the ADC sampling phase.

4.3.5 Integrated Schmitt Trigger for Horizontal and Vertical Sync input

The gmZAN3 has integrated Schmitt triggers for Horizontal and Vertical Sync inputs, pin 85 and pin 86. This allows for less number of components on the system board. It enables easier PCB layout, more reliability and results in reducing the overall BOM cost.

The programmable hysteresis value is either 0.5V or 1.5V

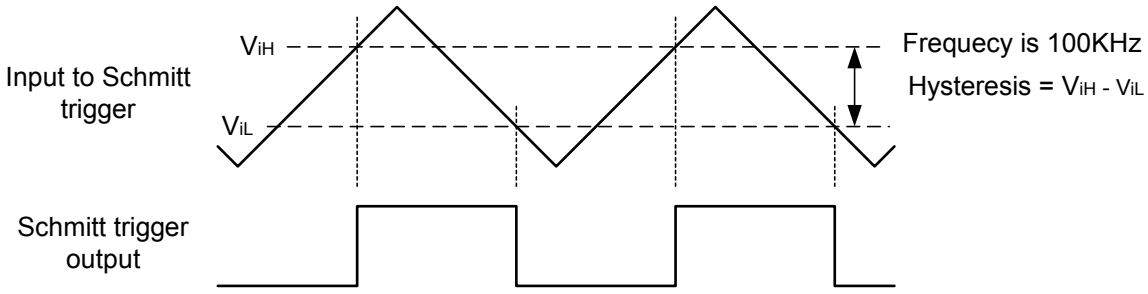


Figure 15. Schmitt Trigger Timing Diagram

Table 16. Temperature and Voltage Variation for Schmitt Trigger

	High hysteresis (0x1E7[7]=0) Default		
	High Threshold ViH(V)	Low Threshold ViL(V)	Hysteresis ViH-ViL(V)
Room Temp @ 3.3V	2.3	1.0	1.3
100°C @ 3.0V	2.15	0.9	1.25
0°C @ 3.6V	2.6	1.1	1.5

NOTE: The power on default value of the hysteresis is set to high

	Low hysteresis (0x1E7[7]=1)		
	High Threshold ViH(V)	Low Threshold ViL(V)	Hysteresis ViH-ViL(V)
Room Temp @ 3.3V	1.6	0.9	0.7
100°C @ 3.0V	1.5	0.8	0.7
0°C @ 3.6V	1.7	1	0.7

4.3.6 SOG and CSYNC support

The gmZAN3 has the capability to support the following types of SOG and CSYNC inputs without having to use external components. The signals below show the Negative types of SOG and CSYNC signals. The gmZAN3 can also support the Positive types.

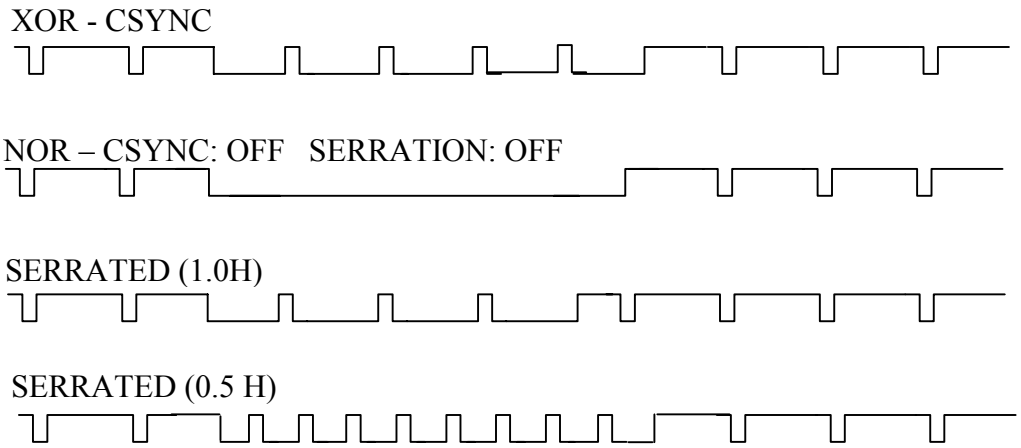


Figure 16. Supported SOG and CSYNC signals

4.3.7 ADC Capture Window

Figure 17 below illustrates the capture window used for the ADC input. In the horizontal direction the capture window is defined in ACLKs (equivalent to a pixel count). In the vertical direction it is defined in lines.

All the parameters beginning with "Source" are programmed gmZAN3 registers values. Note that the input vertical total is solely determined by the input and is not a programmable parameter.

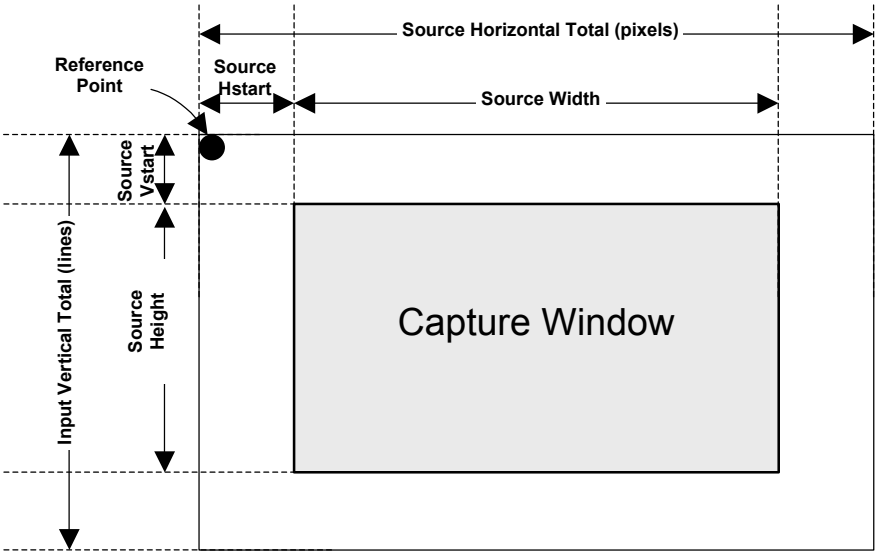


Figure 17. ADC Capture Window

The Reference Point marks the leading edge of the first internal HSYNC following the leading edge of an internal VSYNC. Both the internal HSYNC and the internal VSYNC are derived from external HSYNC and VSYNC inputs.

Horizontal parameters are defined in terms of single pixel increments relative to the internal horizontal sync. Vertical parameters are defined in terms of single line increments relative to the internal vertical sync.

For ADC interlaced inputs, the gmZAN3 may be programmed to automatically determine the field type (even or odd) from the VSYNC/HSYNC relative timing. See Input Format Measurement, Section 4.4.

4.4 Test Pattern Generator (TPG)

The gmZAN3 contains hundreds of test patterns, some of which are shown in Figure 18. Once programmed, the gmZAN3 test pattern generator can replace a video source (e.g. a PC) during factory calibration and test. This simplifies the test procedure and eliminates the possibility of image noise being injected into the system from the source. The foreground and background colors are programmable. In addition, the gmZAN3 OSD controller can be used to produce other patterns.

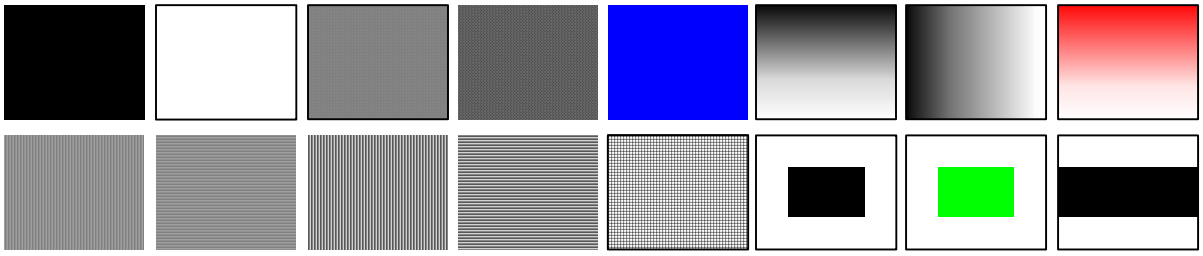


Figure 18. Some of gmZAN3 built-in test patterns

The DDC port can be used for factory testing. The factory test station connects to the gmZAN3 through the Direct Data Channel (DDC) of the DSUB15 connector. Then, the PC can make gmZAN3 display test patterns (see section 4.4). A camera can be used to automate the calibration of the LCD panel.

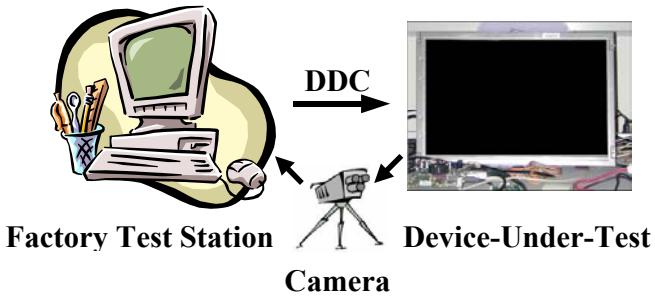


Figure 19. Factory Calibration and Test Environment

4.5 Input Format Measurement

The gmZAN3 has an Input Format Measurement block (the IFM) providing the capability of measuring the horizontal and vertical timing parameters of the input video source. This information may be used to determine the video format and to detect a change in the input format. It is also capable of detecting the field type of interlaced formats.

The IFM features a programmable reset, separate from the regular gmZAN3 soft reset. This reset disables the IFM, reducing power consumption. The IFM is capable of operating while gmZAN3is running in power down mode.

Horizontal measurements are measured in terms of the selected IFM_CLK (either TCLK or RCLK/4), while vertical measurements are measured in terms of HSYNC pulses.

For an overview of the internally synthesized clocks, see section 4.1.

4.5.1 Horizontal and Vertical Measurement

The IFM is able to measure the horizontal period and active high pulse width of the HSYNC signal, in terms of the selected clock period (either TCLK or RCLK/4.). Horizontal measurements are performed on only a single line per frame (or field). The line used is programmable. It is able to measure the vertical period and VSYNC pulse width in terms of rising edges of HSYNC.

Once enabled, measurement begins on the rising VSYNC and is completed on the following rising VSYNC. Measurements are made on every field / frame until disabled.

4.5.2 Format Change Detection

The IFM is able to detect changes in the input format relative to the last measurement and then alert the system microcontroller. The microcontroller sets a measurement difference threshold separately for horizontal and vertical timing. If the current timing is different from the previously captured measurement by an amount exceeding this threshold, a status bit is set. An interrupt can also be programmed to occur.

4.5.3 Watchdog

The watchdog monitors input VSYNC / HSYNC. When any HSYNC period exceeds the programmed timing threshold (in terms of the selected IFM_CLK), a register bit is set. When any VSYNC period exceeds the programmed timing threshold (in terms of HSYNC pulses), a second register bit is set. An interrupt can also be programmed to occur.

4.5.4 Internal Odd/Even Field Detection (For Interlaced Inputs to ADC Only)

The IFM has the ability to perform field decoding of interlaced inputs to the ADC. The user specifies start and end values to outline a "window" relative to HSYNC. If the VSYNC leading edge occurs within this window, the IFM signals the start of an ODD field. If the VSYNC leading edge occurs outside this window, an EVEN field is indicated (the interpretation of odd and even can be reversed). The window start and end points are selected from a predefined set of values.

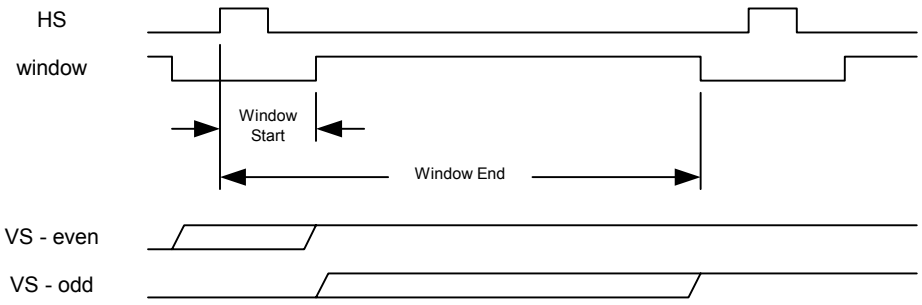


Figure 20. ODD/EVEN Field Detection

4.5.5 Input Pixel Measurement

The gmZAN3 provides a number of pixel measurement functions intended to assist in configuring system parameters such as ACLK frequency (sample clocks per line) and phase setting, centering the image, or adjusting the contrast and brightness.

4.5.6 Image Phase Measurement

This function measures the sampling phase quality over a selected active window region. This feature may be used when programming the source DDS to select the proper phase setting.

4.5.7 Image Boundary Detection

The gmZAN3 performs measurements to determine the image boundary. This information is used when programming the Active Window and centering the image.

4.5.8 Image Auto Balance

The gmZAN3 performs measurements on the input data that is used to adjust brightness and contrast.

4.6 High-Quality Scaling

The gmZAN3 zoom scaler uses an adaptive scaling technique proprietary to Genesis Microchip Inc., and provides high quality scaling of real time video and graphics images. An input field/frame is scalable in both the vertical and horizontal dimensions.

Interlaced fields may be spatially de-interlaced by vertically scaling and repositioning the input fields to align with the output display's pixel map.

4.6.1 Variable Zoom Scaling

The gmZAN3 scaling filter incorporates programmable scaling coefficients. This is useful for improving the sharpness and definition of graphics when scaling at high zoom factors (such as VGA to XGA).

4.6.2 Horizontal & Vertical Shrink

The gmZAN3 provides an arbitrary vertical shrink down to (50% + 1 pixel/line) of the original image size. The integrated ADC performs the horizontal shrink. This allows the gmZAN3 to capture and display images one VESA standard format larger than the native display resolution. For example, SXGA may be captured and displayed on an XGA panel.

4.7 Gamma LUT

The gmZAN3 provides an 8 to 10-bit look-up table (LUT) for each input color channel intended for Gamma correction and to compensate for a non-linear response of the LCD panel. A 10-bit output results in an improved color depth control. The 10-bit output is then dithered down to 8 bits (or 6 bits) per channel at the display (see section 4.8.3 below). The LUT is user programmable to provide an arbitrary transfer function. Gamma correction occurs after the zoom / shrink scaling block.

The LUT has bypass enable. If bypassed, the LUT does not require programming.

4.8 Display Output Interface

The Display Output Port provides data and control signals that permit the gmZAN3 to connect to a variety of flat panel devices. The output interface is configurable for 18 or 24-bit RGB pixels, either single or double (TTL only) pixel wide. All display data and timing signals are synchronous with the DCLK output clock.

4.8.1 Display Synchronization

Refer to section 4.1 for information regarding internal clock synthesis.

The gmZAN3 support the following display synchronization modes:

- **Frame Sync Mode:** The display frame rate is synchronized to the input frame or field rate. This mode is used for standard operation.

- **Free Run Mode:** No synchronization. This mode is used when there is no valid input timing (i.e. to display OSD messages or a splash screen) or for testing purposes. In free-run mode, the display timing is determined only by the values programmed into the display window and timing registers.

4.8.2 Programming the Display Timing

Display timing signals provide timing information so the Display Port can be connected to an external display device. Based on values programmed in registers, the Display Output Port produces the horizontal sync (DHS), vertical sync (DVS), and data enable (DEN) control signals, which are then encoded into the LVDS data stream by the on-chip LVDS transmitter. The figure below provides the registers that define the output display timing.

Horizontal values are programmed in single pixel increments relative to the leading edge of the horizontal sync signal. Vertical values are programmed in line increments relative to the leading edge of the vertical sync signal.

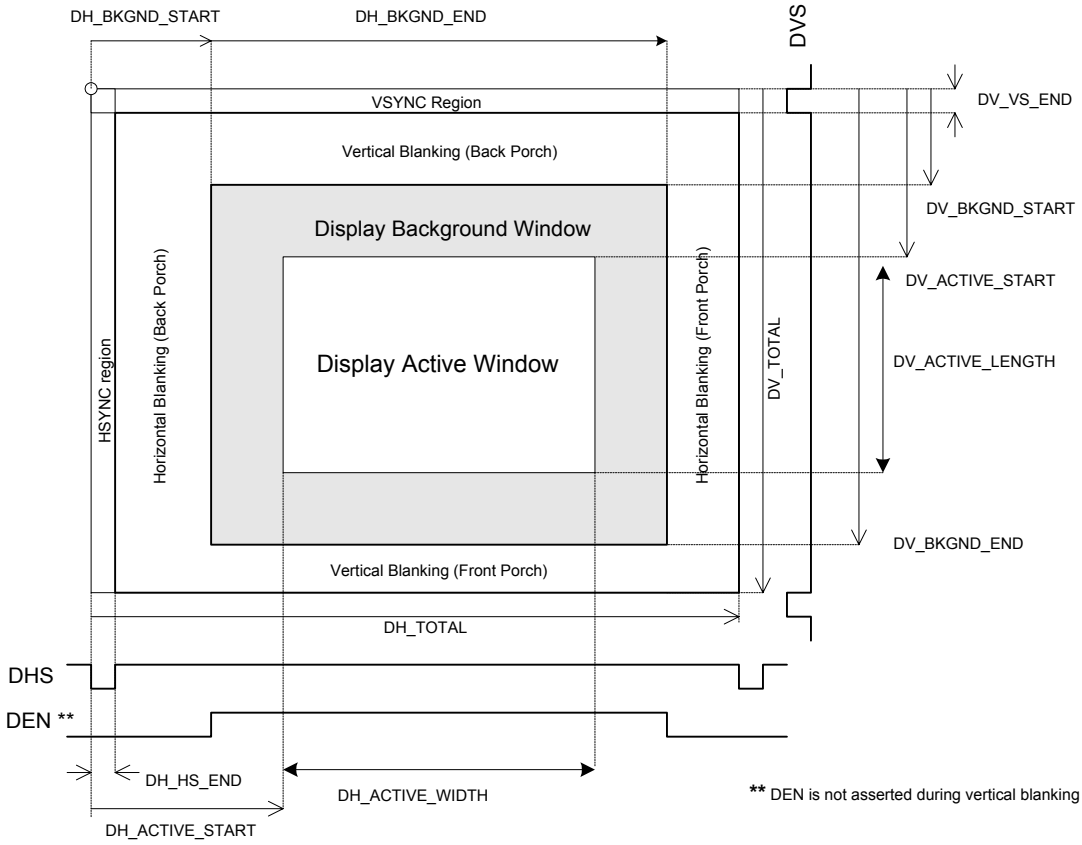


Figure 21. Display Windows and Timing

The double-wide (TTL only) output only supports an even number of horizontal pixels.

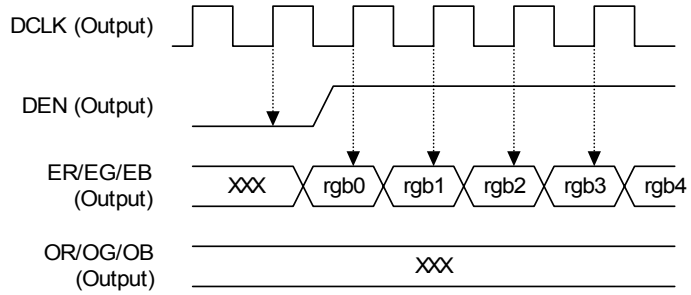


Figure 22. Single Pixel Width Display Data

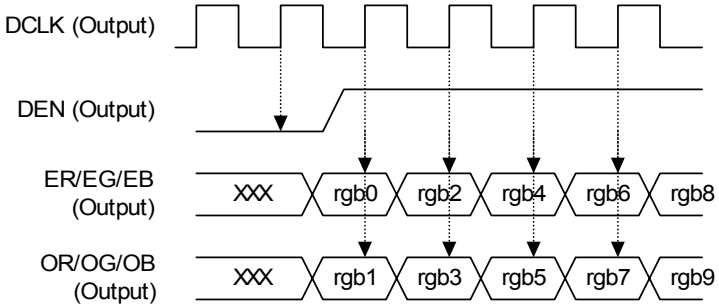


Figure 23. Double Pixel Wide Display Data

4.8.3 Panel Power Sequencing (PPWR, PBIAS)

gmZAN3 has two dedicated outputs PPWR and PBIAS to control LCD power sequencing once data and control signals are stable. The timing of these signals is fully programmable.

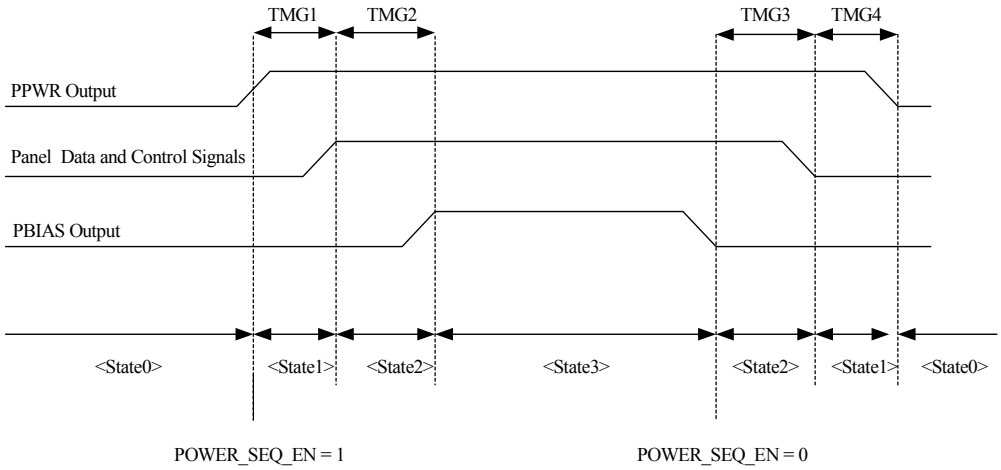


Figure 24. Panel Power Sequencing

4.8.4 Output Dithering

The Gamma LUT outputs a 10-bit value for each color channel. This value is dithered down to either 8-bits for 24-bit per pixel panels, or 6-bits for 18-bit per pixel panels.

The benefit of dithering is that the eye tends to average neighboring pixels and a smooth image free of contours is perceived. Dithering works by spreading the quantization error over neighboring pixels both spatially and temporally. Two dithering algorithms are available: random or ordered dithering. Ordered dithering is recommended when driving a 6-bit panel.

All gray scales are available on the panel output whether using 8-bit panel (dithering from 10 to 8 bits per pixel) or using 6-bit panel (dithering from 10 down to 6 bits per pixel).

4.9 Four Channel LVDS Transmitter (for gmZAN3L Only)

The gmZAN3L implements the industry standard flexible four channel LVDS transmitter. The LVDS transmitter can support the following:

- Single pixel mode
- 24-bit panel mapping to the LVDS channels (see Table 14)
- 18-bit panel mapping to the LVDS channels (see Table 15)
- Programmable channel swapping (the clocks are fixed)
- Programmable channel polarity swapping

Table 17. Supported LVDS 24-bit Panel Data Mappings

Channel 0	R0, R1, R2, R3, R4, R5, G0
Channel 1	G1, G2, G3, G4, G5, B0, B1
Channel 2	B2, B3, B4, B5, PHS, PVS, PDE
Channel 3	R6, R7, G6, G7, B6, B7, RES

Channel 0	R2, R3, R4, R5, R6, R7, G2
Channel 1	G3, G4, G5, G6, G7, B2, B3
Channel 2	B4, B5, B6, B7, PHS, PVS, PDE
Channel 3	R0, R1, G0, G1, B0, B1, RES

Table 18. Supported LVDS 18-bit Panel Data Mapping

Channel 0	R0, R1, R2, R3, R4, R5, G0
Channel 1	G1, G2, G3, G4, G5, B0, B1
Channel 2	B2, B3, B4, B5, PHS, PVS, PDE
Channel 3	Disabled for this mode

4.10 Flexible TTL Outputs (gmZAN3T Only)

The gmZAN3T builds in flexibility with the ability to:

- swap red and green channels,
- swap R, G, B most-significant-bit and least-significant-bit (reverse the bit-order of each R, G, B color output).
- output single or double pixel width data in 24 or 48 bits.

This flexibility enables the building of cost effective (2-layer) PCBs.

4.11 Energy Spectrum Management (ESM)

High spikes in the EMI power spectrum may cause LCD monitor products to violate emissions standards. The gmZAN3 has many features that can be used to reduce electromagnetic interference (EMI). These include drive strength control and clock spectrum modulation. These features help to eliminate the costs associated with EMI reducing components and shielding.

4.12 OSD

The gmZAN3 has a fully programmable, high-quality OSD controller. The OSD controller supports two independent rectangles with graphics divided into “cells” that are programmable in size (from 8 x 8 to 18 x 18 pixels). The cells are stored in an on-chip static RAM and can be stored as 1-bit per pixel data or 2-bit per pixel data. This permits a good compression ratio while allowing more than 16 colors in the image.

Some general features of the gmZAN3OSD controller include:

OSD Position – The OSD menu can be positioned anywhere on the display region. The reference point is Horizontal and Vertical Display Background Start (DH_BKGND_START and DV_BKGND_START in Figure 21).

OSD Stretch – The OSD image can be stretched horizontally and/or vertically by a factor of two. Pixel and line replication is used to stretch the image.

4.12.1 On-Chip OSD SRAM

The on-chip static RAM (10K bytes) stores the cell map and the cell definitions.

In memory, the cell map is organized as an array of words, each defining the attributes of one visible character on the screen starting from upper left of the visible character array. These attributes specify which character to display, whether it is stored as 1 or 2-bits per pixel, the foreground and background colors, blinking, etc.

Registers CELLMAP_XSZ and CELLMAP_YSZ are used to define the visible area of the OSD image. For example, Figure 25 shows a cell map for which CELLMAP_XSZ =25 and CELLMAP_YSZ =10.

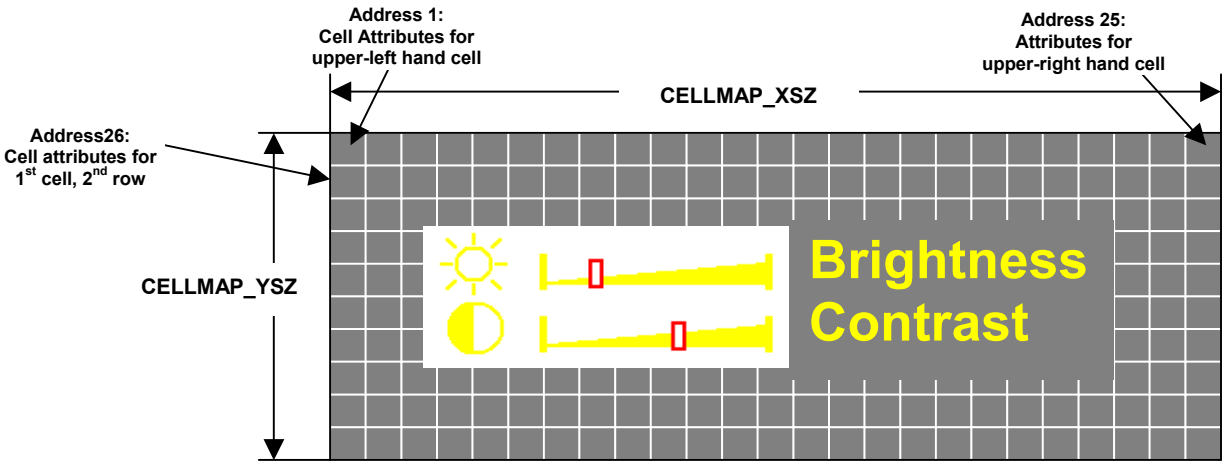


Figure 25. OSD Cell Map

Cell font definitions are stored as bit map data. On-chip registers point to the start of 1-bit per pixel definitions and 2-bit per pixel definitions respectively. 1 and 2-bit per pixel cell definitions require 1 or 2 words of the OSD RAM per character height line.

Note that the cell map and the cell font definitions share the same on-chip RAM. Thus, the size of the cell map can be traded off against the number of different cell definitions. In particular, the size of the OSD image and the number of cell definitions must fit in OSD SRAM. That is, the following inequality must be satisfied.

CELLMAP_XSZ * CELLMAP_YSZ +
CELL_HEIGHT * (Number of 1-bit per pixel fonts) +
CELL_HEIGHT * (Number of 2-bit per pixel fonts) * 2 $\leq$ 5120

For example, an OSD menu 360 pixels wide by 360 pixels high is 30 cells in width and 20 cells in height (if each cell is defined as 12 pixels wide and 18 lines high). Many of these cells would be the same (e.g. empty). In this case, the menu could contain 51 1-bit per pixel cells and 100 2-bit per pixel cells. Of course, different numbers of each type can also be used.

4.12.2 Color Look-up Table (LUT)

The Color Look-up Table (LUT) is stored in an on-chip RAM that is separate from the OSD RAM. The LUT is 64 colors by 16-bit in a RGB 5:5:5 format (bit 0 selectively enables blending with scaler data.

4.13 General Purpose Inputs and Outputs (GPIO's)

The gmZAN3 has up to 11 general-purpose input/output (GPIO) pins for the gmZAN3L and five GPIO for the gmZAN3T.

4.14 Bootstrap Configuration Pins

The gmZAN3 has three bootstrap pins

Table 19. Bootstrap Signals

Signal Name	Pin Name	Description
2_WIRE_ADDR_SEL	HDATA[3]	If using 2-wire protocol, this selects one of the two slave addresses 0 = 0x70 & 0x71 1 = 0x94 & 0x95
HP[1:0]	HDATA/AD/HP[1:0]	To select Host Interface Configuration 00 Muxed Address/Data (AD) 8051 8-bit parallel interface 01 Reserved 10 2-wire interface 11 6-wire Genesis interface
OSC_SEL	HDATA2/AD2/OSC_SEL	TCLK Selection 0 External oscillator (input on TCLK pin) 1 Xtal and internal oscillator (In this mode, it is always recommended to use a 10KΩ pull-up resistor)

4.15 Host Interface

gmZAN3 contains many internal registers that control its operation. These are described in the gmZAN3 Register Listing (C0523-DSL-01).

Option 1: A direct 8051 muxed 8-bit address/data port supports high-speed access.

Option2: A serial host interface is provided to allow an external device to peek and poke registers in the gmZAN3. This is done using a 2-wire serial protocol. Note that 2-wire host interface requires bootstrap settings as described in Table 19.

4.15.1 Host Interface Command Format – for 2 or 6-wire

Transactions on the 2-wire host protocol occurs in integer multiples of bytes (i.e. 8 bits or two nibbles respectively). These form an instruction byte, a device register address and/or one or more data bytes. This is described in Table 20.

The first byte of each transfer indicates the type of operation to be performed by the gmZAN3. The table below lists the instruction codes and the type of transfer operation. The content of bytes that follow the instruction byte will vary depending on the instruction chosen. By utilizing these modes effectively, registers can be quickly configured.

The two LSBs of the instruction code, denoted 'A9' and 'A8' in Table 20 below, are bits 9 and 8 of the internal register address respectively. Thus, they should be set to ‘00’ to select a starting register address of less than 256, ‘01’ to select an address in the range 256 to 511, and '10' to select an address in the range 512 to 767. These bits of the address increment in Address Increment transfers. The unused bits in the instruction byte, denoted by 'x', should be set to ‘1’.

Table 20. Instruction Byte Map

Bit 7 6 5 4 3 2 1 0	Operation Mode	Description
0 0 0 1 x x A9 A8	Write Address Increment	Allows the user to write a single or multiple bytes to a specified starting address location. A Macro operation will cause the internal address pointer to increment after each byte transmission. Termination of the transfer will cause the address pointer to increment to the next address location.
0 0 1 0 x x A9 A8	Write Address No Increment (for table loading)	
1 0 0 1 x x A9 A8	Read Address Increment	Allows the user to read multiple bytes from a specified starting address location. A Macro operation will cause the internal address pointer to increment after each read byte. Termination of the transfer will cause the address pointer to increment to the next address location.
1 0 1 0 x x A9 A8	Read Address No Increment (for table reading)	
0 0 1 1 x x A9 A8 0 1 0 0 x x A9 A8 1 0 0 0 x x A9 A8 1 0 1 1 x x A9 A8 1 1 0 0 x x A9 A8	Reserved	
0 0 0 0 x x A9 A8 0 1 0 1 x x A9 A8 0 1 1 0 x x A9 A8 0 1 1 1 x x A9 A8 1 1 0 1 x x A9 A8 1 1 1 0 x x A9 A8 1 1 1 1 x x A9 A8	Spare	No operation will be performed

4.15.2 2-wire Serial Protocol

The 2-wire protocol consists of a serial clock HCLK and bi-directional serial data line HFS. The bus master drives HCLK and either the master or slave can drive the HFS line (open drain) depending on whether a read or write operation is being performed. The gmZAN3 operates as a slave on the interface.

The 2-wire protocol requires each device be addressable by a 7-bit slave address. The gmZAN3 is initialized on power-up to 2-wire mode by asserting bootstrap pins HP[1:0] to “10” and the slave address select bootstrap option HDATA3 on the rising edge of RESETn. By pulling HDATA3 high or low it is possible to select one of the two slave addresses: 0x94 & 0x95 (for HDATA=1) or 0x70 & 0x71 (for HDATA=0). This provides flexibility to configure the system consisting of multiple devices with the same slave address.

A 2-wire data transfer consists of a stream of serially transmitted bytes formatted as shown in the figure below. A transfer is initiated (START) by a high-to-low transition on HFS while HCLK is held high. A transfer is terminated by a STOP (a low-to-high transition on HFS while HCLK is held high) or by a START (to begin another transfer). The HFS signal must be stable when HCLK is high, it may only change when HCLK is low (to avoid being misinterpreted as START or STOP).

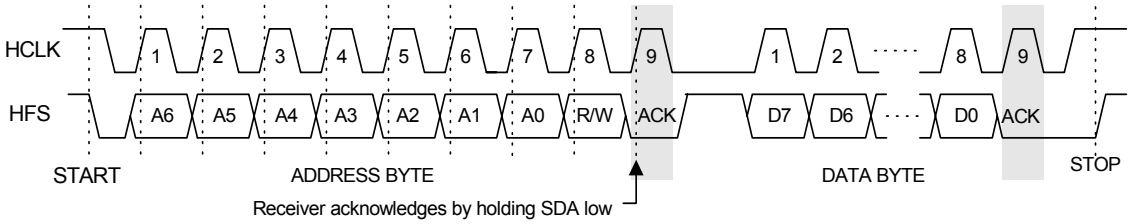


Figure 26. 2-Wire Protocol Data Transfer

Each transaction on the HFS is in integer multiples of 8 bits (i.e. bytes). The number of bytes that can be transmitted per transfer is unrestricted. Each byte is transmitted with the most significant bit (MSB) first. After the eight data bits, the master releases the HFS line and the receiver asserts the HFS line low to acknowledge receipt of the data. The master device generates the HCLK pulse during the acknowledge cycle. The addressed receiver is obliged to acknowledge each byte that has been received.

The Write Address Increment and the Write Address No Increment operations allow one or multiple registers to be programmed with only sending one start address. In Write Address Increment, the address pointer is automatically incremented after each byte has been sent and written. The transmission data stream for this mode is illustrated in Figure 27 below. The highlighted sections of the waveform represent moments when the transmitting device must release the HFS line and wait for an acknowledgement from the gmZAN3 (the slave receiver).

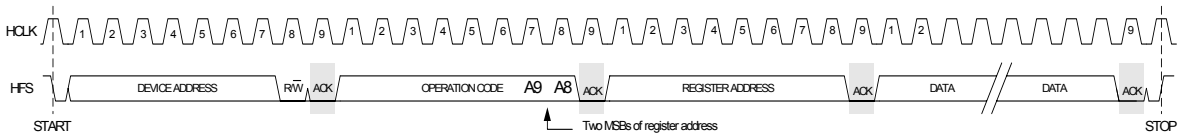


Figure 27. 2-Wire Write Operations (0x1x and 0x2x)

The Read Address Increment (0x90) and Read Address No Increment (0xA0) operations are illustrated in Figure 28. The highlighted sections of the waveform represent moments when the transmitting device must release the HFS line and waits for an acknowledgement from the master receiver.

Note that on the last byte read, no acknowledgement is issued to terminate the transfer.

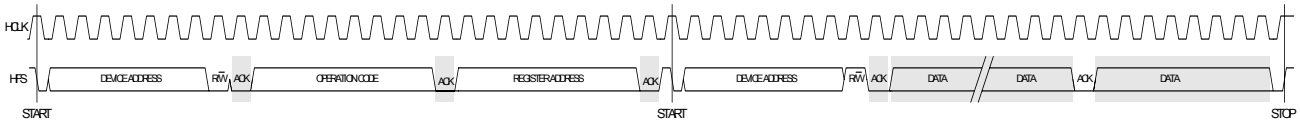


Figure 28. 2-Wire Read Operation (0x9x and 0xAx)

Please note that in all the above operations the operation code includes two address bits, as described in Table 20.

4.15.3 8-bit Parallel Interface

The 8-bit parallel interface connects to the external 8051 microcontroller's external memory interface utilizing the following signals: AD[7..0], ALE, WR#, RD#. An additional input signal (REG_MEM) is used to distinguish between the register set and the OSD SRAM. When REG_MEM is held low the gmZAN3 register set is selected and when it is held high the OSD SRAM will be active. The bus timing requirements are given in Table 27 and Table 28. The OSD SRAM is R/W accessed in "pages" of 256 bytes.

The ALE signal is used to latch the 8-bits of address on the microprocessor's multiplexed Address/Data bus.

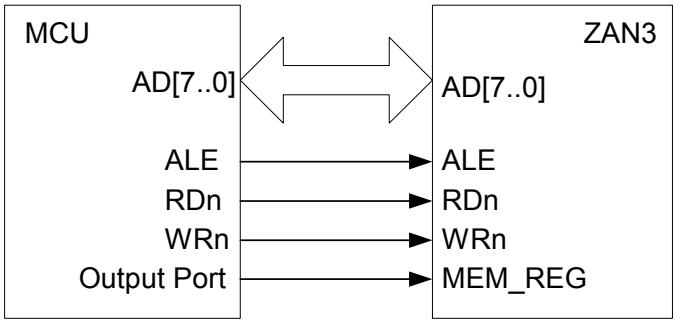


Figure 29. 8-bit Parallel Interface

4.16 Miscellaneous Functions

4.16.1 Low Power State

The gmZAN3 provides a low power state in which the clocks to selected parts of the chip may be disabled (see Table 22) and the ADC powered-off.

4.16.2 Pulse Width Modulation (PWM) Back Light Control

Many of today's LCD back light inverters require both a PWM input and variable DC voltage to minimize flickering (due to the interference between panel timing and inverter's AC timing), and adjust brightness. Most LCD monitor manufactures currently use a microcontroller to provide these control signals. To minimize the burden on the external microcontroller, the gmZAN3 generates these signals directly.

There are two pins available for controlling the LCD back light, PWM0/GPIO0 and PWM1/GPIO1. The duty cycle of these signals is programmable. They may be connected to an external RC integrator to generate a variable DC voltage for a LCD back light inverter or other applications. Panel HSYNC or TCLK may be used as the clock for the counter generating this output signal.

5 Electrical Specifications

The following targeted specifications have been derived by simulation.

5.1 Preliminary DC Characteristics

Table 21. Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
3.3V Supply Voltages (1,2)	$V_{VDD\_3.3}$	-0.3		3.6	V
1.8V Supply Voltages (1.2)	$V_{VDD\_1.8}$	-0.3		1.98	V
Input Voltage (5V tolerant inputs) (1,2)	$V_{IN5Vtol}$	-0.3		5.5	V
Input Voltage (non 5V tolerant inputs) (1,2)	V_{IN}	-0.3		3.6	V
Electrostatic Discharge	V_{ESD}			±2.0	kV
Latch-up	I_{LA}			±100	mA
Ambient Operating Temperature	T_A	0		70	°C
Storage Temperature	T_{STG}	-40		150	°C
Operating Junction Temp.	T_J	0		125	°C
Thermal Resistance (Junction to Air) Natural Convection (3) gmZAN3	θ_{JA_ZAN3}			37.6	°C/W
Thermal Resistance (Junction to Case) Convection (4) gmZAN3	θ_{JC_ZAN3}			16.0	°C/W
Soldering Temperature (30 sec.)	T_{SOL}			220	°C
Vapor Phase Soldering (30 sec.)	T_{VAP}			220	°C

NOTES:

(1) All voltages are measured with respect to GND.

(2) Absolute maximum voltage ranges are for transient voltage excursions.

(3) Package thermal resistance is based on a two-layer PCB. Package θ_{JA} is improved on a PCB with four or more layers.

(4) Based on the figures for the Operating Junction Temperature, θ_{JC} and Power Consumption in Table 22, the typical case temperature is calculated as $T_C = T_J - P \times \theta_{JC}$.

Table 22. gmZAN3L DC Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
POWER					
Power Consumption @ 95 MHz ACLK (4)	P_{XGA}			0.824	W
Power Consumption @ Low Power Mode (1)	P_{LP}			0.025	W
3.3V Supply Voltages (AVDD and RVDD)	$V_{VDD\_3.3}$	3.15	3.3	3.45	V
1.8V Supply Voltages (VDD and CVDD)	$V_{VDD\_1.8}$	1.71	1.8	1.89	V
Supply Current @ Low Power Mode (1)	I_{LP}			9	mA
Supply Current @ 95 MHz ACLK	I_{ZAN3_XGA}				
• 1.8V supply (2)	I_{ZAN3_XGA}			187	mA
• 3.3V supply (3)	I_{ZAN3_XGA}			138	mA
INPUTS					
High Voltage	V_{IH}	2.0		V_{DD}	V
Low Voltage	V_{IL}	GND		0.8	V
Clock High Voltage	V_{IHC}	2.4		V_{DD}	V
Clock Low Voltage	V_{ILC}	GND		0.4	V
High Current (V_{IN} = 5.0 V)	I_{IH}	-25		25	µA
Low Current (V_{IN} = 0.8 V)	I_{IL}	-25		25	µA
Capacitance (V_{IN} = 2.4 V)	C_{IN}			8	pF
OUTPUTS					
High Voltage (I_{OH} = 7 mA)	V_{OH}	2.4		V_{DD}	V
Low Voltage (I_{OL} = -7 mA)	V_{OL}	GND		0.4	V
Tri-State Leakage Current	I_{OZ}	-25		25	µA

NOTES:

(1) **Low power mode or Suspend mode figures measured by shutting down all the blocks including the ADC. The CYSNC/SOG is the only block turned on to detect Sync signals.**

(2) **Includes pins CVDD_1.8, VDD_ADC_1.8 and VDD_RPLL_1.8.**

(3) **Includes pins RVDD_3.3, AVDD_RED_3.3, AVDD_GREEN_3.3, AVDD_BLUE_3.3, AVDD_ADC_3.3, AVDD_3.3, AVDD_RPLL_3.3, AVDD_OUT_LV_3.3 and AVDD_LV_3.3.**

(4) **XGA input at 85Hz with on/off pattern to XGA output operating at room temperature**

Table 23. gmZAN3T DC Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
POWER					
Power Consumption @ 95 MHz ACLK (4)	P_{XGA}			0.812	W
Power Consumption @ Low Power Mode (1)	P_{LP}			0.025	W
3.3V Supply Voltages (AVDD and RVDD)	$V_{VDD\_3.3}$	3.15	3.3	3.45	V
1.8V Supply Voltages (VDD and CVDD)	$V_{VDD\_1.8}$	1.71	1.8	1.89	V
Supply Current @ Low Power Mode (1)	I_{LP}			9	mA
Supply Current @ 95 MHz ACLK	I_{ZAN3_XGA}				
• 1.8V supply (2)	I_{ZAN3_XGA}			178	mA
• 3.3V supply (3)	I_{ZAN3_XGA}			149	mA
INPUTS					
High Voltage	V_{IH}	2.0		V_{DD}	V
Low Voltage	V_{IL}	GND		0.8	V
Clock High Voltage	V_{IHC}	2.4		V_{DD}	V
Clock Low Voltage	V_{ILC}	GND		0.4	V
High Current (V_{IN} = 5.0 V)	I_{IH}	-25		25	µA
Low Current (V_{IN} = 0.8 V)	I_{IL}	-25		25	µA
Capacitance (V_{IN} = 2.4 V)	C_{IN}			8	pF
OUTPUTS					
High Voltage (I_{OH} = 7 mA)	V_{OH}	2.4		V_{DD}	V
Low Voltage (I_{OL} = -7 mA)	V_{OL}	GND		0.4	V
Tri-State Leakage Current	I_{OZ}	-25		25	µA

NOTES:

(4) **Low power mode or Suspend mode figures measured by shutting down all the blocks including the ADC. The CYSNC/SOG is the only block turned on to detect Sync signals.**

(5) **Includes pins CVDD_1.8, VDD_ADC_1.8 and VDD_RPLL_1.8.**

(6) **Includes pins RVDD_3.3, AVDD_RED_3.3, AVDD_GREEN_3.3, AVDD_BLUE_3.3, AVDD_ADC_3.3, AVDD_3.3, AVDD_RPLL_3.3, AVDD_OUT_LV_3.3 and AVDD_LV_3.3.**

(4) **XGA input at 85Hz with on/off pattern to XGA output operating at room temperature**

5.2 Preliminary AC Characteristics

The following targeted specifications have been derived by simulation.

All timing is measured to a 1.5V logic-switching threshold. The minimum and maximum operating conditions used were: T_{DIE} = 0 to 125 °C, Vdd = 1.71 to 1.89V, Process = best to worst, C_L = 16pF for all outputs.

Table 24. Maximum Speed of Operation

Clock Domain	Max Speed of Operation
Main Input Clock (TCLK)	24MHz (14.3MHz recommended)
ADC Clock (ACLK)	100MHz
HCLK Host Interface Clock (6-wire protocol)	5MHz
Reference Clock (RCLK)	240MHz (220MHz recommended)
Display Clock (DCLK)	90MHz

Table 25. Display Timing and DCLK Adjustments

DP_TIMING ->	Tap 0 (default)		Tap 1		Tap 2		Tap 3	
	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Propagation delay from DCLK to DA*/DB*	1.0	4.5	0.5	3.5	-0.5	2.5	-1.5	1.5
Propagation delay from DCLK to DHS	1.0	4.5	0.5	3.5	-0.5	2.5	-1.5	1.5
Propagation delay from DCLK to DVS	0.5	4.5	0.0	3.5	-1.0	2.5	-2.0	1.5
Propagation delay from DCLK to DEN	1.0	4.5	0.5	3.5	-0.5	2.5	-1.5	1.5

Note: **DCLK Clock Adjustments are the amount of additional delay that can be inserted in the DCLK path, in order to reduce the propagation delay between DCLK and its related signals.**

Table 26. 2-Wire Host Interface Port Timing

Parameter	Symbol	MIN	TYP	MAX	Units
SCL HIGH time	T_{SHI}	1.25			us
SCL LOW time	T_{SLO}	1.25			us
SDA to SCL Setup	T_{SDIS}	30			ns
SDA from SCL Hold	T_{SDIH}	20			ns
Propagation delay from SCL to SDA	T_{SDO3}	10		150	ns

Note**: The above table assumes OCM_CLK = R_CLK / 2 = 100 MHz (default) (ie 10ns / clock)**

Table 27. Microcontroller Interface Timing (Muxed Address/Data) for Register Read/Write

Parameter	Symbol	MIN	TYP	MAX	Units
AD valid to ALE trailing edge setup time	T_{asu}	10			ns
Trailing edge of ALE to AD hold time	T_{ah}	5			ns
WR# leading edge to AD valid delay	T_{dw}	5			ns
Trailing edge of WR# to AD hold time	T_{dh}	5			ns
ALE pulse width	T_{ap}	10			ns
WR# pulse width	T_{wp}	4			T_{ref}
RD# pulse width	T_{rp}	30			ns
RD#/WR# trailing edge to ALE leading edge	T_{ra}	10			ns
Leading edge of RD# to AD data delay	T_{rdly}	15			ns
Trailing edge of RD# to AD hold time	T_{rh}	2	5		ns
Trailing edge of ALE to WR# or RD# (command) leading edge	T_{acl}	30			ns

Note: T_{ref} = HOST_CLK = TCLK or (RCLK/4)

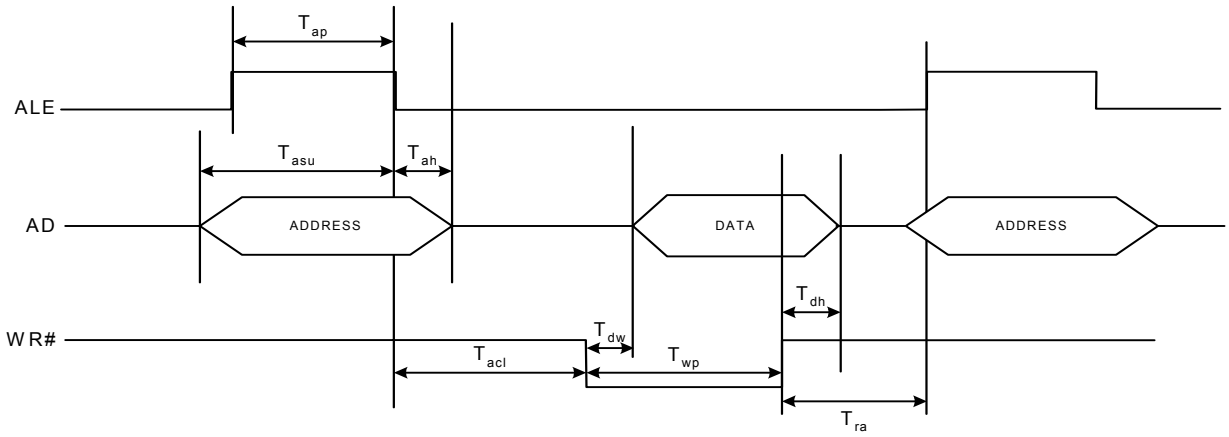


Figure 30. Microcontroller Register Write Cycle

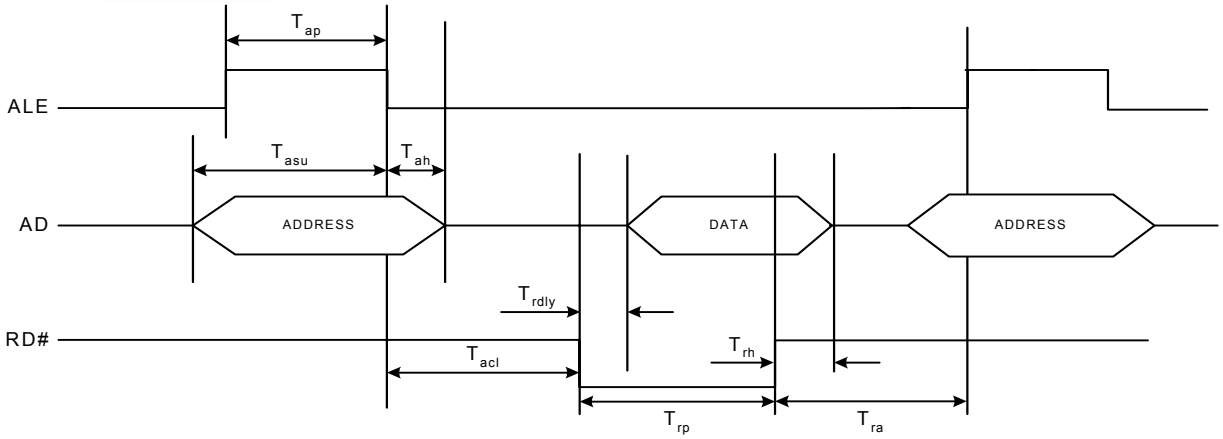


Figure 31. Microcontroller Register Read Cycle

Table 28. Microcontroller Interface Timing (Muxed Address/Data) for OSD Memory Read/Write

Parameter	Symbol	MIN	TYP	MAX	Units
AD valid to ALE trailing edge setup time	T_{asu}	10			ns
Trailing edge of ALE to AD hold time	T_{ah}	5			ns
WR# leading edge to AD valid delay	T_{dw}	5			ns
Trailing edge of WR# to AD hold time	T_{dh}	5			ns
ALE pulse width	T_{ap}	10			ns
WR# pulse width	T_{wp}	4			T_{ref}
RD# pulse width	T_{rp}	30			ns
WR# trailing edge to ALE leading edge	T_{ra}	4			T_{ref}
Trailing edge of ALE to AD data valid delay	T_{rdly}	10			T_{ref}
Trailing edge of RD# to AD hold time	T_{rh}	2	5		ns
Trailing edge of ALE to WR# or RD# (command) leading edge	T_{acl}	30			ns

Note: T_{ref} = HOST_CLK = (RCLK/4)

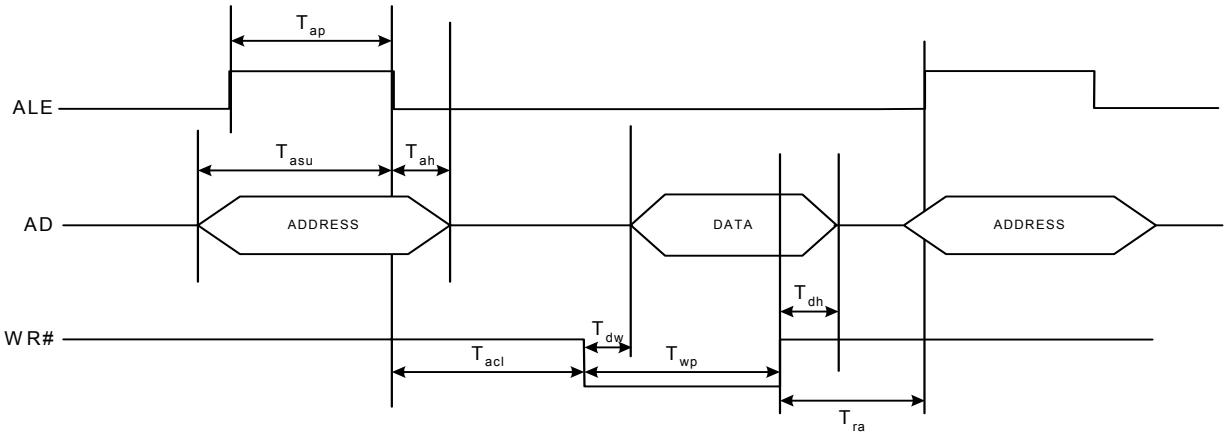


Figure 32. Microcontroller OSD CCF Write Cycle

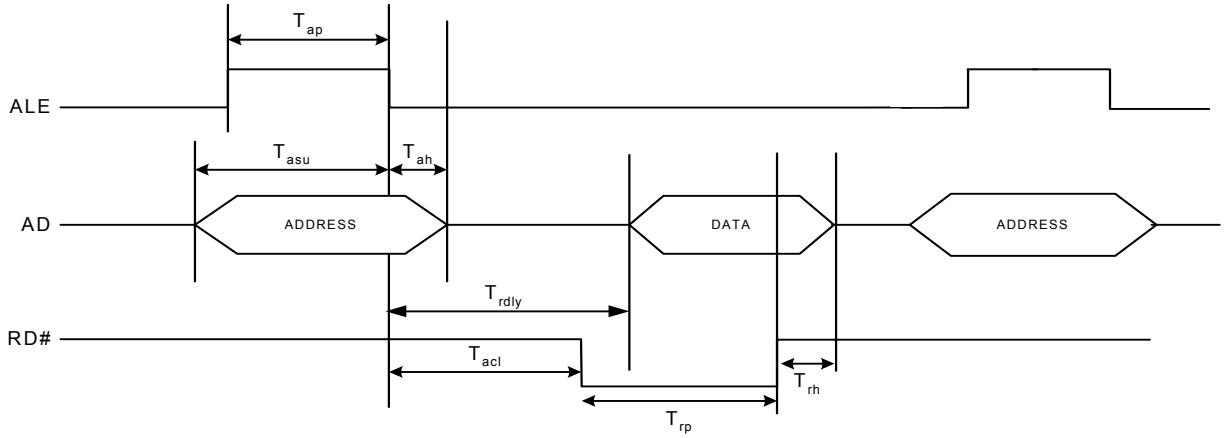
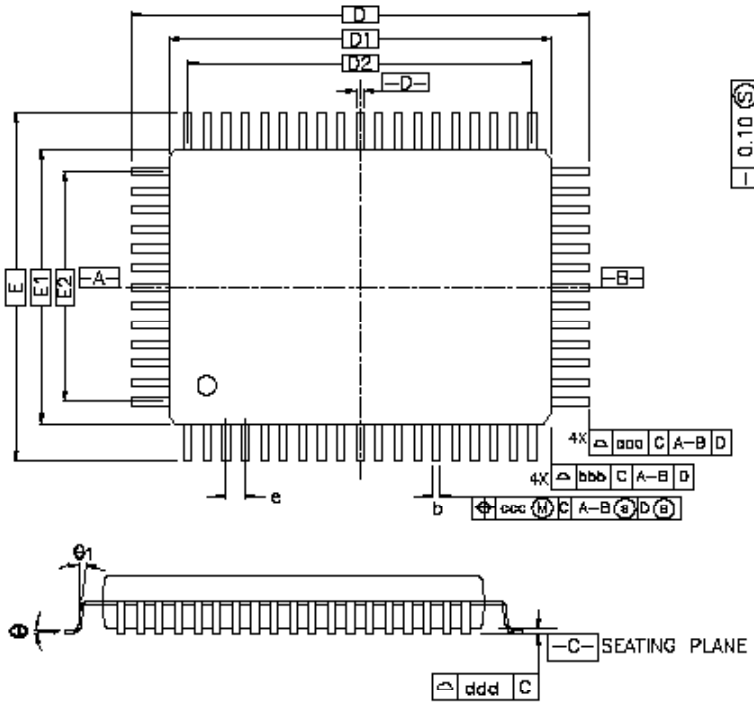


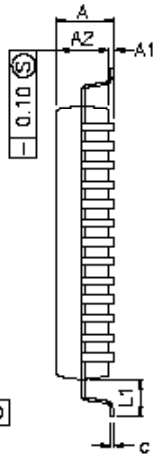
Figure 33. Microcontroller OSD CCF Read Cycle

6 Ordering Information

Order Code	Application	Package	Temperature Range
gmZAN3T	XGA with TTL Panel interface	128-pin PQFP	0-70°C
gmZAN3L	XGA with single LVDS transmitter Panel interface	128-pin PQFP	0-70°C

7 Mechanical Specifications

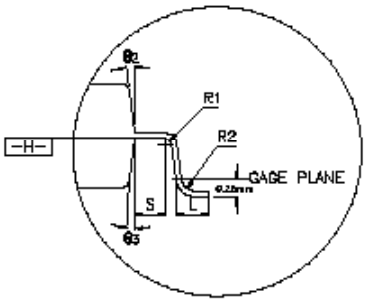




COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A1	0.25	—	—	0.010	—	—
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E	17.20 BASIC			0.677 BASIC		
E1	14.00 BASIC			0.551 BASIC		
R2	0.13	—	0.30	0.005	—	0.012
R1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ1	0°	—	—	0°	—	—
ALLOY 42 L/F θ2 , θ3	7° REF			7° REF		
COPPER L/F θ2 , θ3	15° REF			15° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.170	0.200	0.270	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	18.50			0.728		
E2	12.50			0.492		
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		



NOTES:

1. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 do include mold mismatch and are determined at datum plane -H- .

2. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion can be 0.08mm total in excess of dimension b at maximum material condition. Dambar cannot be located on the lower radius or the lead foot.

Figure 34. gmZAN3 128-pin PQFP Mechanical Drawing