UT61L1024

128K X 8 BIT HIGH SPEED CMOS SRAM

FEATURES

- Fast access time : 12/15 ns (max.)
- Low operating power consumption :
  60 mA (typical)
- Power Supply range 3.1V to 3.6V
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Package : 32-pin 300 mil skinny PDIP
  32-pin 300 mil SOJ
  32-pin 450mil SOP
  32-pin 8mm x 20mm TSOP-1
  32-pin 8mm x 13.4mm STSOP

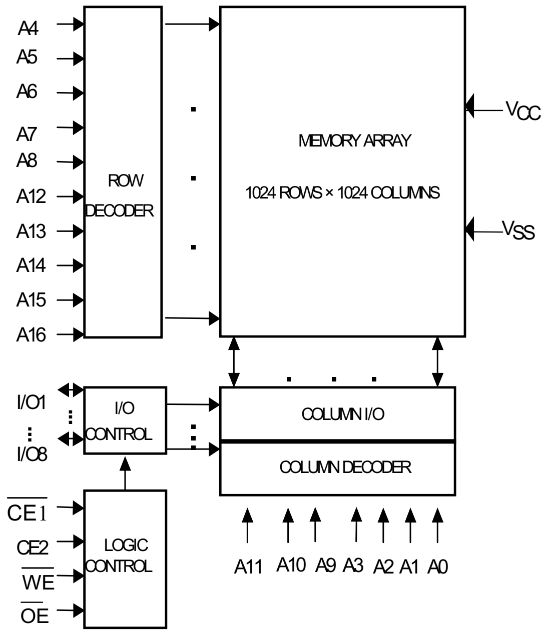
GENERAL DESCRIPTION

The UT61L1024 is a 1,048,576-bit high-speed CMOS static random access memory organized as 131,072 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

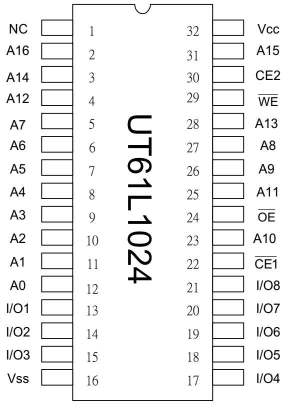
The UT61L1024 is designed for high-speed system applications. It is particularly suited for use in high-density high-speed system applications.

The UT61L1024 operates from a single 3.3V power supply and all inputs and outputs are fully TTL compatible.

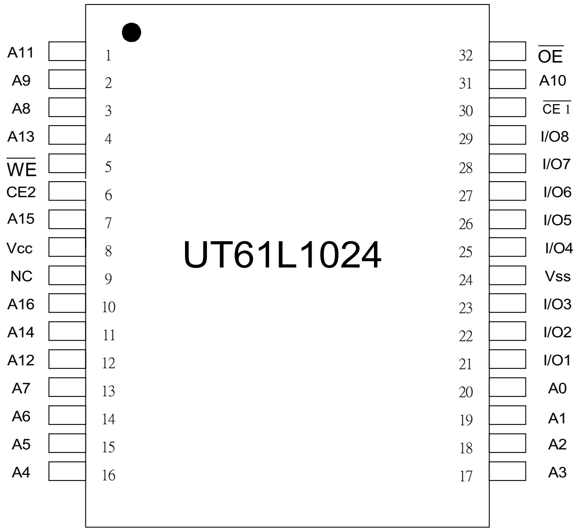
FUNCTIONAL BLOCK DIAGRAM


A4
A5
A6
A7
A8
A12
A13
A14
A15
A16
ROW DECODER
MEMORY ARRAY
1024 ROWS × 1024 COLUMNS
VCC
VSS
I/O1
I/O8
I/O CONTROL
COLUMN I/O
COLUMN DECODER
CE1
CE2
WE
OE
LOGIC CONTROL
A11 A10 A9 A3 A2 A1 A0

PIN CONFIGURATION


UT61L1024
NC 1
A16 2
A14 3
A12 4
A7 5
A6 6
A5 7
A4 8
A3 9
A2 10
A1 11
A0 12
I/O1 13
I/O2 14
I/O3 15
Vss 16
I/O4 17
I/O5 18
I/O6 19
I/O7 20
I/O8 21
CE1 22
A10 23
OE 24
A11 25
A9 26
A8 27
A13 28
WE 29
CE2 30
A15 31
Vcc 32

PDIP / SOJ/SOP


UT61L1024
A11 1
A9 2
A8 3
A13 4
WE 5
CE2 6
A15 7
Vcc 8
NC 9
A16 10
A14 11
A12 12
A7 13
A6 14
A5 15
A4 16
A3 17
A2 18
A1 19
A0 20
I/O1 21
I/O2 22
I/O3 23
Vss 24
I/O4 25
I/O5 26
I/O6 27
I/O7 28
I/O8 29
CE1 30
A10 31
OE 32

TSOP-I/STSOP

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
$\overline{\text{CE1}}$,CE2	Chip enable 1,2 Inputs
$\overline{\text{WE}}$	Write Enable Input
$\overline{\text{OE}}$	Output Enable Input
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to Vss	V_{TERM}	-0.5 to +4.6	V
Operating Temperature	T_A	0 to +70	℃
Storage Temperature	T_{STG}	-65 to +150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA
Soldering Temperature (under 10 sec)	Tsolder	260	℃

*Stress greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High - Z	I_{SB},I_{SB1}
Standby	X	L	X	X	High -Z	I_{SB},I_{SB1}
Output Disable	L	H	H	H	High - Z	I_{CC}
Read	L	H	L	H	D_{OUT}	I_{CC}
Write	L	H	X	L	D_{IN}	I_{CC}

Note: H = V_{IH}, L=V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.1V～3.6V, T_A = 0℃ to 70℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT
Input High Voltage	V_{IH}			2.0	V_{CC}+0.5	V
Input Low Voltage	V_{IL}			- 0.5	0.6	V
Input Leakage Current	I_{LI}	$V_{SS} \leqq V_{IN} \leqq V_{CC}$		- 1	1	μA
Output Leakage Current	I_{LO}	$V_{SS} \leqq V_{I/O} \leqq V_{CC}$ $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		- 1	1	μA
Output High Voltage	V_{OH}	I_{OH} = - 4mA		2.2	-	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA		-	0.4	V
Operating Power Supply Current	I_{CC}	Cycle time=Min,$I_{I/O}$ = 0mA, $\overline{CE1}$ = V_{IL} , CE2 = V_{IH}	- 12	-	100	mA
			- 15	-	90	mA
Standby Power Supply Current	I_{SB}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}		-	20	mA
	I_{SB1}	$\overline{CE1} \geqq V_{CC}$-0.2V ;or CE2$\leqq$0.2V		-	3	mA

CAPACITANCE (T_A=25℃, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L=30pF, I_{OH}/I_{OL}=-4mA/8mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.1V～3.6V , T_A = 0℃ to 70℃)

(1) READ CYCLE

PARAMETER	SYMBOL	UT61L1024-12		UT61L1024-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	12	-	15	-	ns
Address Access Time	t_{AA}	-	12	-	15	ns
Chip Enable Access Time	t_{ACE1}, t_{ACE1}	-	12	-	15	ns
Output Enable Access Time	t_{OE}	-	6	-	7	ns
Chip Enable to Output in Low Z	t_{CLZ1*}, t_{CLZ2*}	3	-	4	-	ns
Output Enable to Output in Low Z	t_{OLZ*}	0	-	0	-	ns
Chip Disable to Output in High Z	t_{CHZ1*}, t_{CHZ2*}	-	6	-	7	ns
Output Disable to Output in High Z	t_{OHZ*}	-	6	-	7	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	ns

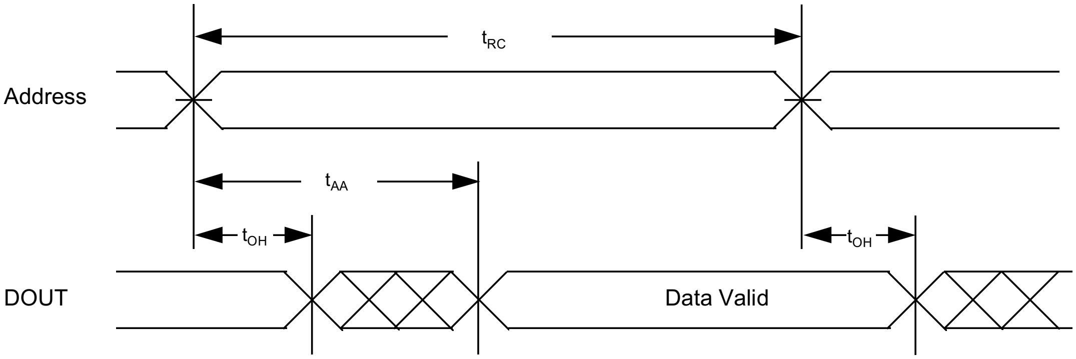
(2) WRITE CYCLE

PARAMETER	SYMBOL	UT61L1024-12		UT61L1024-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	12	-	15	-	ns
Address Valid to End of Write	t_{AW}	10	-	12	-	ns
Chip Enable to End of Write	t_{CW1}, t_{CW2}	10	-	12	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	ns
Write Pulse Width	t_{WP}	9	-	10	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	7	-	8	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	ns
Output Active from End of Write	t_{OW*}	3	-	4	-	ns
Write to Output in High Z	t_{WHZ*}	-	7	-	8	ns

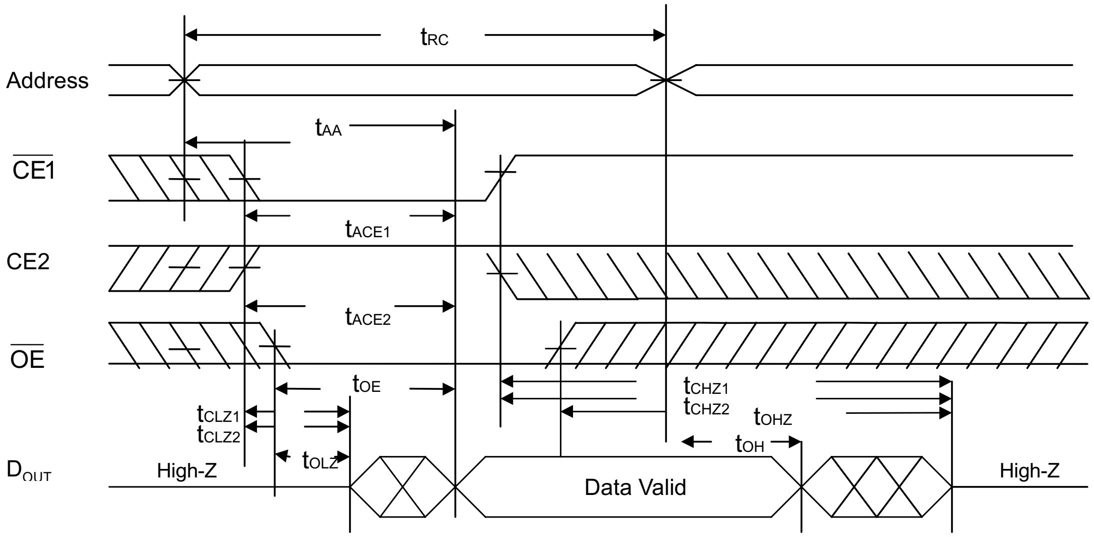
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)


t_{RC}
Address
t_{AA}
t_{OH}
t_{OH}
DOUT
Data Valid

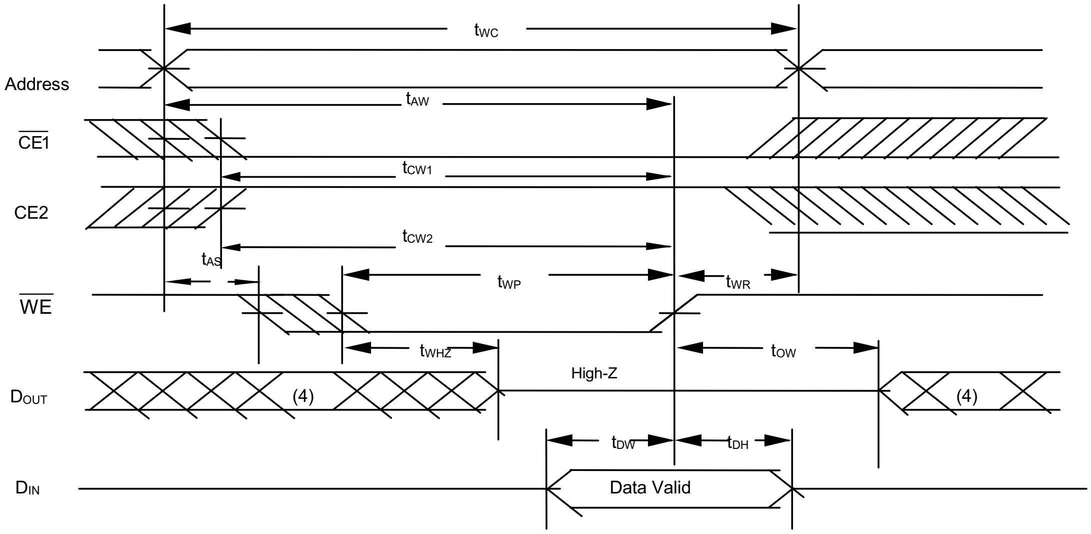
READ CYCLE 2 ($\overline{CE1}$, CE2 and $\overline{OE}$ Controlled) (1,3,5,6)


t_{RC}
Address
t_{AA}
$\overline{CE1}$
t_{ACE1}
CE2
t_{ACE2}
$\overline{OE}$
t_{OE}
t_{CHZ1}
t_{CHZ2}
t_{OHZ}
t_{CLZ1}
t_{CLZ2}
t_{OH}
t_{OLZ}
D_{OUT}
High-Z
Data Valid
High-Z

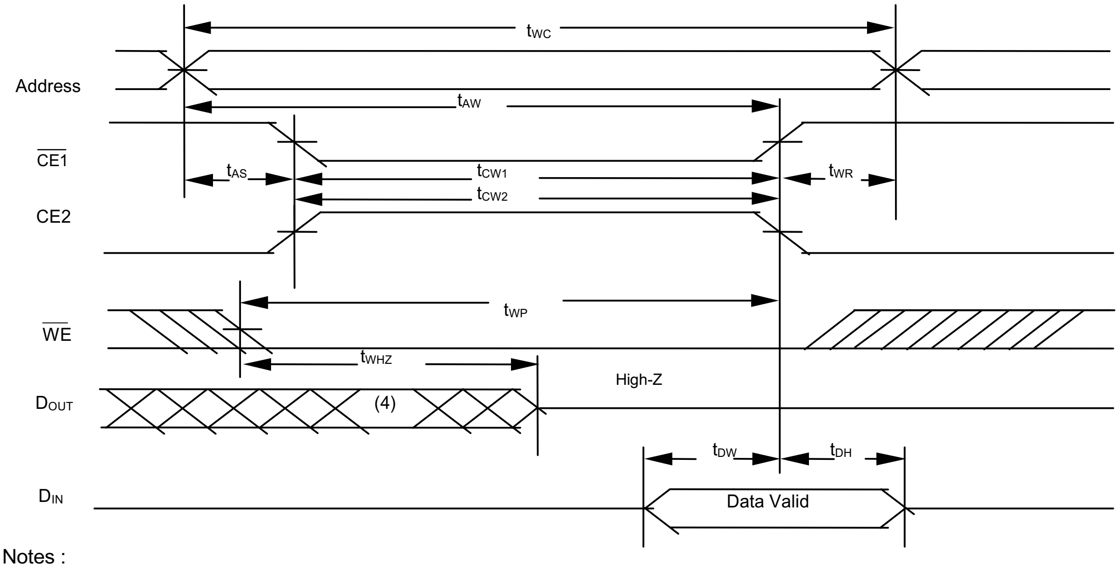
Notes :

1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected $\overline{CE1}$ $=V_{IL}$ and CE2=V_{IH}.
3. Address must be valid prior to or coincident with $\overline{CE1}$ and CE2 transition; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is low.
5. t_{CLZ1}, t_{CLZ2}, t_{OLZ}, t_{CHZ1}, t_{CHZ2} and t_{OHZ} are specified with C_L=5pF. Transition is measured ± 500mV from steady state.
6. At any given temperature and voltage condition, t_{CHZ1} is less than t_{CLZ1}, t_{CHZ2} is less than t_{CLZ2}, t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 ($\overline{WE}$ Controlled) (1,2,3,5)


t_{WC}
Address
t_{AW}
$\overline{CE1}$
t_{CW1}
CE2
t_{CW2}
t_{AS}
t_{WP}
t_{WR}
$\overline{WE}$
t_{WHZ}
t_{OW}
High-Z
D_{OUT}
(4)
(4)
t_{DW}
t_{DH}
D_{IN}
Data Valid

WRITE CYCLE 2 ($\overline{CE1}$ and CE2 Controlled) (1,2,5)

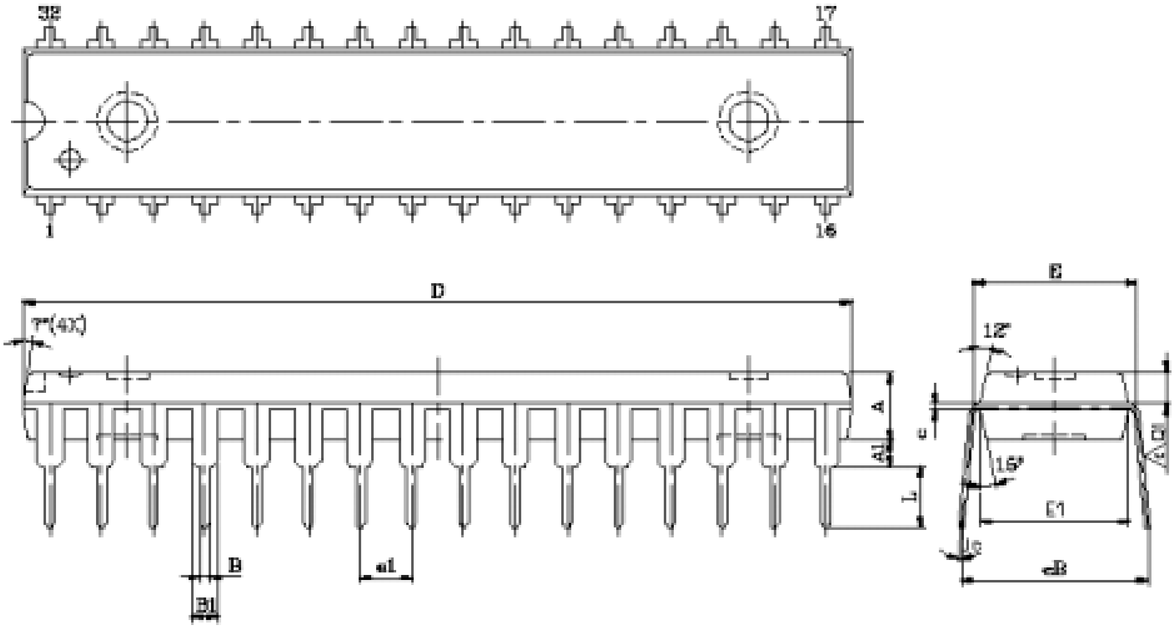

t_{WC}
Address
t_{AW}
$\overline{CE1}$
t_{AS}
t_{CW1}
t_{CW2}
t_{WR}
CE2
t_{WP}
$\overline{WE}$
t_{WHZ}
High-Z
D_{OUT}
(4)
t_{DW}
t_{DH}
D_{IN}
Data Valid

Notes :

1. $\overline{WE}$ or $\overline{CE1}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE1}$ and a low $\overline{WE}$.
3. During a $\overline{WE}$ controlled with write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than $t_{WHZ}+t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input singals must not be applied.
5. If the $\overline{CE1}$ LOW transition occurs simultaneously with or after $\overline{WE}$ LOW transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ± 500mV from steady state.

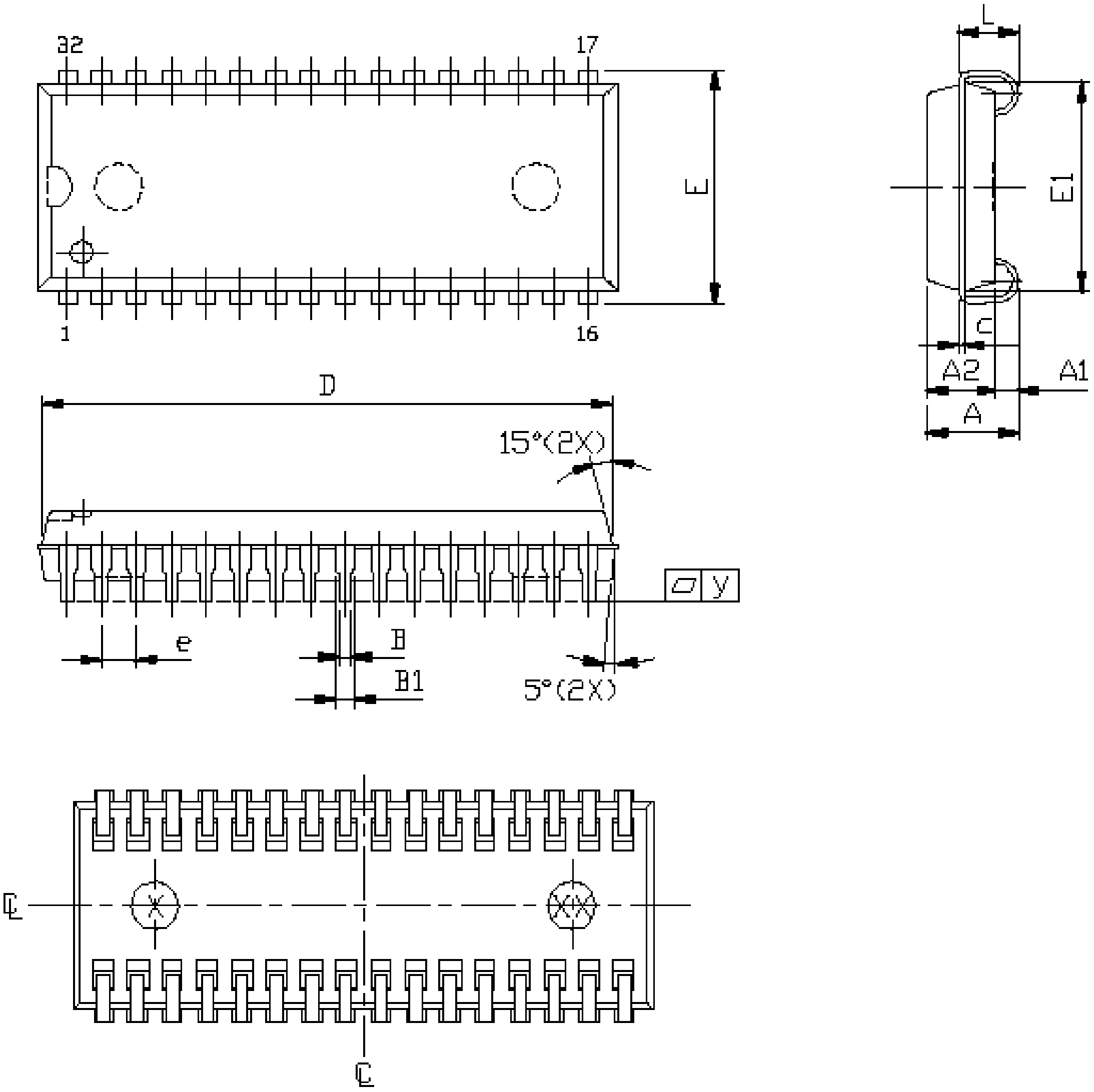
PACKAGE OUTLINE DIMENSION

32 pin PDIP 300mil Package Outline Dimension



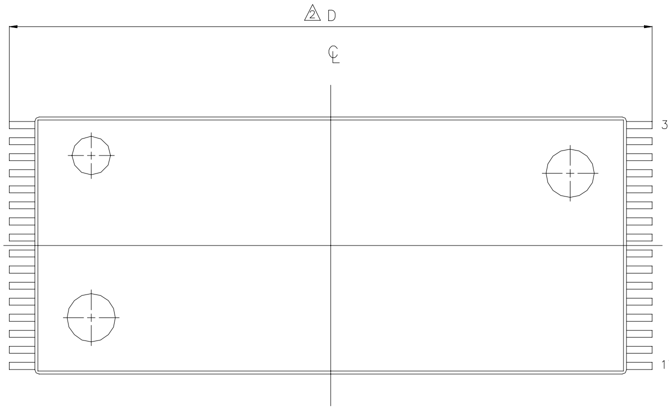
UNIT / SYMBOL	INCH(BASE)	MM(REF)
A	0.130 ± 0.005	3.302 ± 0.127
A1	0.015(MIN)	0.381 (MIN)
B	0.018 ± 0.004	0.457 ± 0.102
B1	0.050 ± 0.008	1.270 ± 0.203
c	0.010 ± 0.004	0.254 ± 0.102
D	1.600 ± 0.005	40.640 ± 0.127
E	0.315 ± 0.010	8.001 ± 0.254
E1	0.288 ± 0.004	7.315 ± 0.102
e1	0.100 TYP	2.540 TYP
eB	0.350 ± 0.020	8.890 ± 0.508
L	0.125 (MIN)	3.175 (MIN)
Q1	0.060 ± 0.005	1.524 ± 0.127
Jc	0°～10°	0°～10°

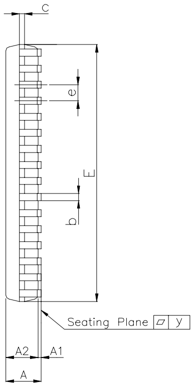
32 pin SOJ Package Outline Dimension

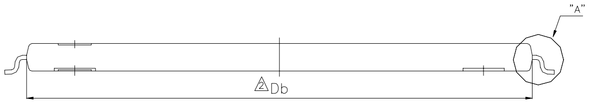


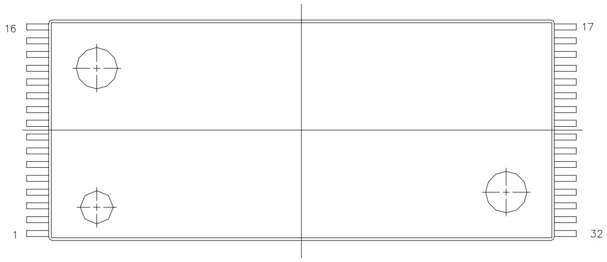
UNIT / SYMBOL	INCH(BASE)	MM(REF)
A	0.148 (MAX)	3.759 (MAX)
A1	0.026 (MIN)	0.660 (MIN)
A2	0.100 ± 0.005	2.540 ± 0.127
B	0.018 (TYP)	0.457(TYP)
B1	0.028 (TYP)	0.711 (TYP)
C	0.010 (TYP)	0.254 (TYP)
D	0.830 (MAX)	21.082 (MAX)
E	0.335 (TYP)	8.509 (TYP)
E1	0.300 ± 0.005	7.620 ± 0.127
e	0.050 (TYP)	1.270 (TYP)
L	0.086 ± 0.010	2.184 ± 0.254
y	0.003 (MAX)	0.076 (MAX)

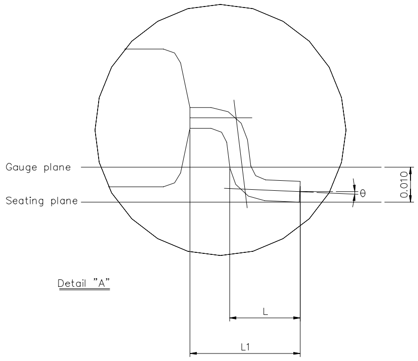
32 pin 8mm × 20mm TSOP-I Package Outline Dimension


D
CL
1
32
16
17


c
e
E
b
Seating Plane
y
A2
A1
A

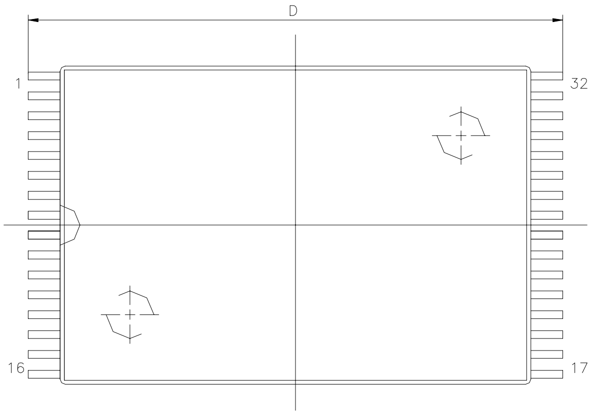


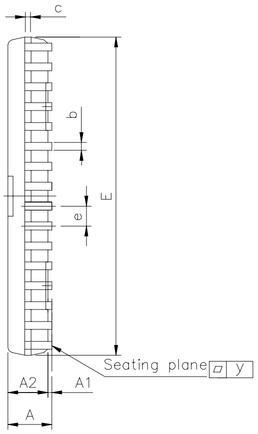


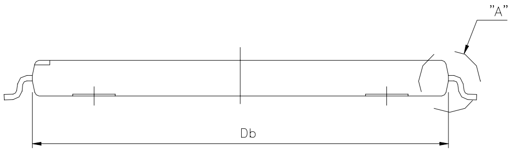

Gauge plane
Seating plane
θ
0.010
Detail "A"
L
L1

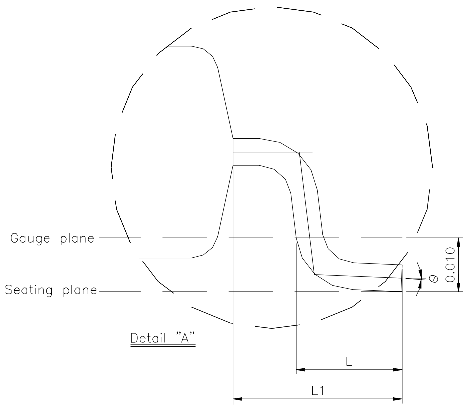
	UNIT / SYMBOL	INCH(BASE)	MM(REF)
	A	0.047 (MAX)	1.20 (MAX)
	A1	0.004 ± 0.002	0.10 ± 0.05
	A2	0.039 ± 0.002	1.00 ± 0.05
	b	0.008 + 0.002	0.20 + 0.05
	c	0.005 (TYP)	0.127 (TYP)
C	D	0.724 ± 0.004	18.40 ± 0.10
	E	0.315 ± 0.004	8.00 ± 0.10
E C	e	0.020 (TYP)	0.50 (TYP)
	HD	0.787 ± 0.008	20.00 ± 0.20
	L	0.0197 ± 0.004	0.50 ± 0.10
B	L1	0.0315 ± 0.004	0.08 ± 0.10
	y	0.003 (MAX)	0.076 (MAX)
	Θ	0°～5°	0°～5°

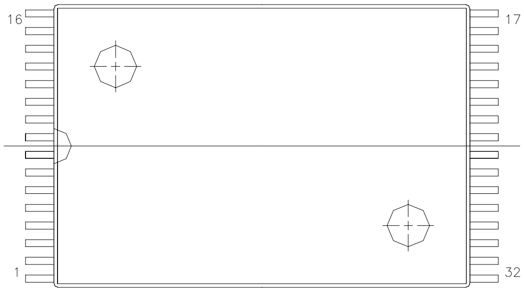
32 pin 8mm x 13.4mm STSOP Package Outline Dimension




c
b
e
E
Seating plane
y
A2
A1
A




Gauge plane
Seating plane
0.010
θ
Detail "A"
L
L1



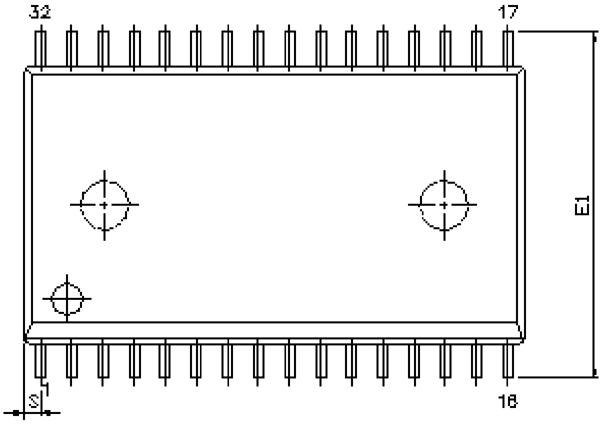
Note：

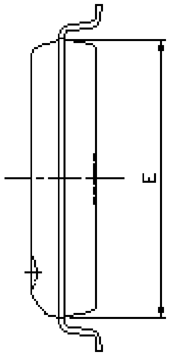
1.E dimension is not including end flash.

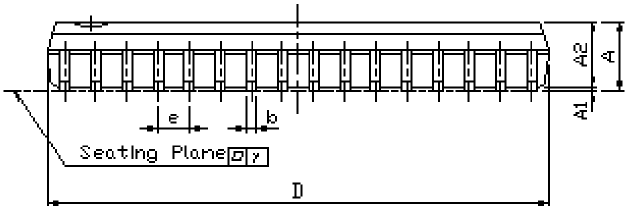
2.The total of both sides' end flash Is not above 0.3mm.

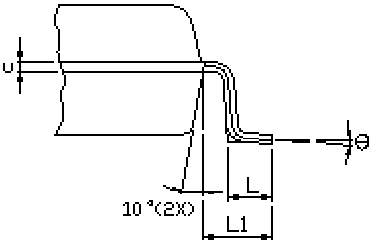
UNIT SYMBOL	MM(REF)	INCH(BASE)
A	1.20(Max.)	0.047(Max).
A1	0.1060.05	0.00460.002
A2	1.0060.05	0.03960.002
b	020(typ.)	0.006(typ.)
c	0.15(typ.)	0.006(typ.)
D	13.4060.20	0.52660.006
Db	11.8060.10	0.46560.004
E	8.00060.10	0.31560.004
e	0.50(typ.)	0.020(typ.)
L	0.5060.10	0.02060.004
L1	0.8060.10	0.031560.004
y	0.08(Max.)	0.003(Max.)
e	08~58	08~58

32 pin 445mil SOP Package Outline Dimension









UNIT SYMBOL	INCH(BASE)	MM(REF)
A	0.118(MAX.)	0.047(MAX).
A1	0.004(MIN)	0.00460.002
A2	0.111(MAX)	0.03960.002
b	0.016(TYP.)	0.006(TYP.)
c	0.008(TYP.)	0.006(TYP.)
D	0.817(MAX)	0.52660.006
E	0.44560.005	0.31560.004
e	0.050(TYP.)	0.020(TYP.)
L	00.034760.008	0.02060.004
L1	0.05560.008	0.031560.004
S	0.026(MAX)	0.914(MAX)
y	0.004(MAX.)	0.101(MAX.)
Θ	08~108	08~108

ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	PACKAGE
UT61L1024KC-12	12	32PIN SKINNY PDIP
UT61L1024KC-15	15	32PIN SKINNY PDIP
UT61L1024JC-12	12	32PIN SOJ
UT61L1024JC-15	15	32PIN SOJ
UT61L1024SC-12	12	32PIN SOP
UT61L1024LC-12	12	32PIN TSOP-1
UT61L1024LC-15	15	32PIN TSOP-1
UT61L1024LS-12	12	32PIN STSOP
UT61L1024LS-15	15	32PIN STSOP

REVISION HISTORY

REVISION	DESCRIPTION	DATE
Rev. 1.0	Original.	Apr. 05 2000
Rev. 1.1	Add TSOP-I Package	Aug. 29.2000
Rev. 1.2	Modify the format of power consumption	Sep. 01.2000
Rev. 1.3	1. V_{OH} : 2.4 -> 2.2 2. Input Rise & Fall times : 5->3ns 3. The symbols CE1# ,OE# & WE# are revised as $\overline{CE1}$, $\overline{OE}$ & $\overline{WE}$	Jun. 18,2001
Rev.1.4	Add SOP Package.	Jul. 6,2001