



GLT440L16

256K X 16 CMOS DYNAMIC RAM WITH EXTENDED DATA OUTPUT

Nov. 2004 (Rev.2.6)

Features :

- * 262,144 words by 16 bits organization.
- * Fast access time and cycle time.
- * Dual $\overline{\text{CAS}}$ Input.
- * Low power dissipation.
- * Read-Modify-Write, $\overline{\text{RAS}}$ -Only Refresh, $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh, Hidden Refresh and Test Mode Capability.
- * 512 refresh cycles per 8ms.
- * Available in 40-Pin 400 mil SOJ and 40/44 Pin TSOP(II)
- * Single +3.3V \pm 10% Power Supply.
- * All inputs and Outputs are TTL compatible.
- * Extended Data-Out(EDO) Page Mode operation.
- * Self – refresh capability. (S-Version).

Description :

The GLT440L16 is a 262,144 x 16 bit high-performance CMOS dynamic random access memory. The GLT440L16 offers Fast Page mode with Extended Data Output, and has both BYTE WRITE and WORD WRITE access cycles via two $\overline{\text{CAS}}$ pins. The GLT440L16 has symmetric address and accepts 512-cycle refresh in 8ms interval.

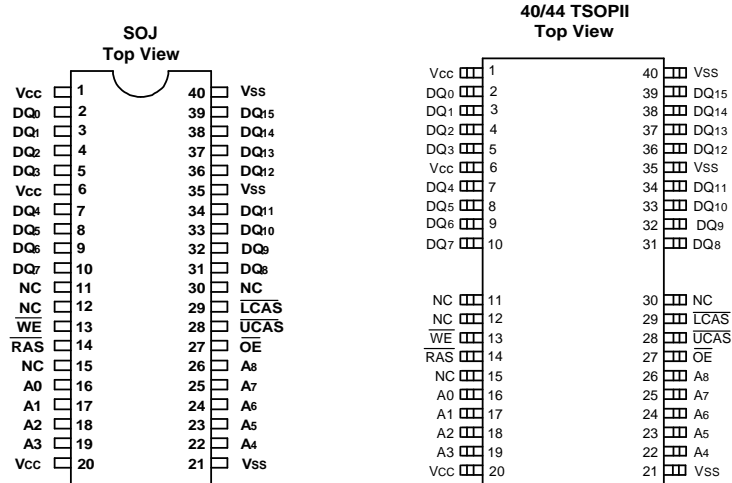
All inputs are TTL compatible. EDO Page Mode operation allows random access up to 512 x 16 bits within a page, with cycle time as short as 14ns.

The GLT440L16 is best suited for graphics, and DSP applications requiring high performance memories.

| HIGH PERFORMANCE | 35 | 40 | 50 | 60 |
|--|-------|-------|-------|--------|
| Max. $\overline{\text{RAS}}$ Access Time, (t_{RAC}) | 35 ns | 40 ns | 50 ns | 60 ns |
| Max. Column Address Access Time, (t_{CAA}) | 18 ns | 20 ns | 25 ns | 30 ns |
| Min. Extended Data Out Page Mode Cycle Time, (t_{PC}) | 14 ns | 15 ns | 19 ns | 25 ns |
| Min. Read/Write Cycle Time, (t_{RC}) | 45 ns | 75 ns | 90 ns | 104 ns |
| Max. $\overline{\text{CAS}}$ Access Time, (t_{CAC}) | 11 ns | 12 ns | 13 ns | 15 ns |

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Pin Configuration :

Pin Descriptions:

| Name | Function |
|------------------------------------|--|
| A ₀ - A ₈ | Address Inputs |
| $\overline{\text{RAS}}$ | Row Address Strobe |
| $\overline{\text{UCAS}}$ | Column Address Strobe/Upper Byte Control |
| $\overline{\text{LCAS}}$ | Column Address Strobe/Lower Byte Control |
| $\overline{\text{WE}}$ | Write Enable |
| $\overline{\text{OE}}$ | Output Enable |
| DQ ₀ - DQ ₁₅ | Data Inputs / Outputs |
| V _{CC} | +3.3V Power Supply |
| V _{SS} | 0V Supply |
| NC | No Connection |

Absolute Maximum Ratings*

Operating Temperature, T_A (ambient)
-10°C to +70°C
 Storage Temperature(plastic).....-55°C to +150°C
 Voltage Relative to V_{SS}-1.0V to + 4.6V
 Short Circuit Output Current.....50mA
 Power Dissipation.....1.0W

Capacitance*

$T_A=25^\circ\text{C}$, $V_{CC}=3.3\text{V}\pm 10\%$, $V_{SS}=0\text{V}$

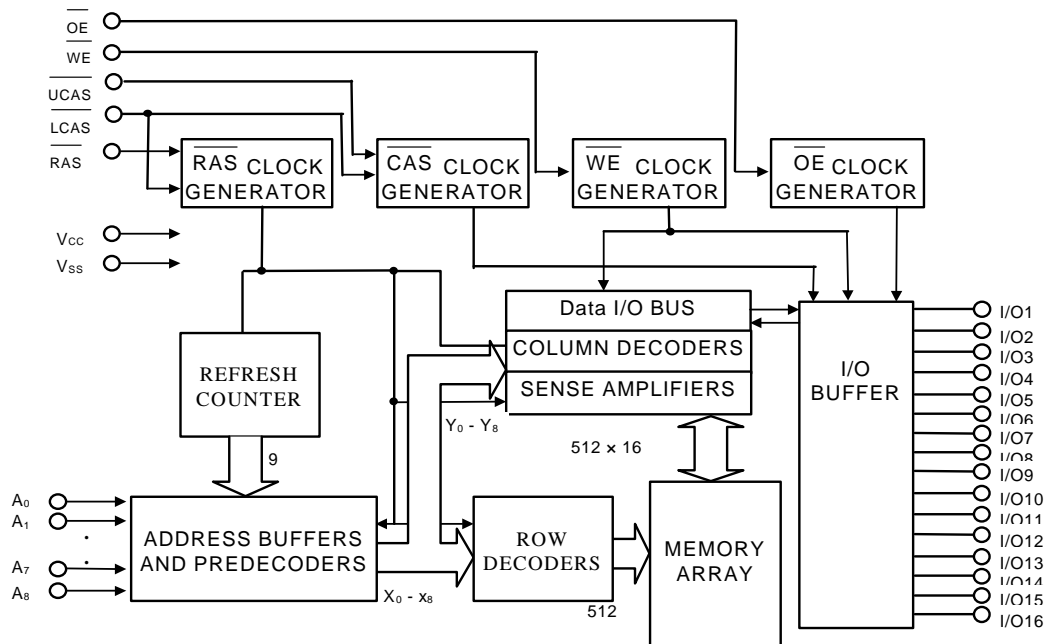
| Symbol | Parameter | Typ | Max. | Unit |
|-----------|---|-----|------|------|
| C_{IN1} | Address Input | 3 | 4 | pF |
| C_{IN2} | $\overline{\text{RAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ | 4 | 5 | pF |
| C_{OUT} | Data Input/Output | 5 | 7 | pF |

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

*Note: Capacitance is sampled and not 100% tested

Electrical Specifications

- CAS means $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
- All voltages are referenced to GND.
- After power up, wait more than 100 μs and then, execute eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ -only refresh cycles as dummy cycles to initialize internal circuit.

Block Diagram :


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- 3 -



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Truth Table: GLT440L16

| Function | RAS | CASL | CASH | WE | OE | ADDRESS | DQs | Notes | |
|----------------------------------|-----------|-------|------|-----|-----|---------|--|------------------|-----|
| Standby | H | H | H | X | X | | High-Z | | |
| Read: Word | L | L | L | H | L | ROW/COL | Data Out | | |
| Read: Lower Byte | L | L | H | H | L | ROW/COL | Lower Byte,Data-Out Upper Byte,High-Z | | |
| Read: Upper Byte | L | H | L | H | L | ROW/COL | Lower Byte,High-Z Upper Byte,Data-Out | | |
| Write: Word(Early Write) | L | L | L | L | X | ROW/COL | Data-In | | |
| Write: Lower Byte (Early) | L | L | H | L | X | ROW/COL | Lower Byte,Data-In Upper Byte,High-Z | | |
| Write: Upper Byte (Early) | L | H | L | L | X | ROW/COL | Lower Byte,High-Z Upper Byte,Data-In | | |
| Read Write | L | L | L | H→L | L→H | ROW/COL | Data-Out,Data-In | 1,2 | |
| EDO-Page- Mode Read | 1st Cycle | L | H→L | H→L | H | L | ROW/COL | Data-Out | 2 |
| | 2nd Cycle | L | H→L | H→L | H | L | COL | Data-Out | 2 |
| EDO-Page- Mode Write | 1st Cycle | L | H→L | H→L | L | X | ROW/COL | Data-In | 2 |
| | 2nd Cycle | L | H→L | H→L | L | X | COL | Data-In | 2 |
| EDO-Page- Mode Read- Write | 1st Cycle | L | H→L | H→L | H→L | L→H | ROW/COL | Data-Out,Data-In | 1,2 |
| | 2nd Cycle | L | H→L | H→L | H→L | L→H | COL | Data-Out,Data-In | 1,2 |
| Hidden Refresh | Read | L→H→L | L | L | H | L | ROW/COL | Data-Out | 2 |
| | Write | L→H→L | L | L | H | L | ROW/COL | Data-In | 2 |
| RAS-Only Refresh | L | H | H | X | X | ROW | High-Z | | |
| CBR Refresh | H→L | L | L | X | X | | High-Z | 3 | |

Notes:

1. These READ cycles may also be BYTE READ cycles (either \overline{UCAS} or \overline{LCAS} active).
2. These WRITE cycles may also be BYTE WRITE cycles (either \overline{UCAS} or \overline{LCAS} active).
3. EARLY WRITE only.
4. At least one of the two CAS signals must be active (\overline{UCAS} or \overline{LCAS}).

DC and Operating Characteristics (1-2)
 $T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{CC}=3.3\text{V}\pm 10\%$, $V_{SS}=0\text{V}$, unless otherwise specified.

| Sym. | Parameter | Test Conditions | Access Time | Min. | Typ | Max. | Unit | Notes |
|-----------|---|---|--|------|-----|--------------------------|---------------|-------|
| I_{LI} | Input Leakage Current (any input pin) | $0\text{V} \leq V_{IN} \leq 5.5\text{V}$ (All other pins not under test=0V) | | -10 | | +10 | μA | |
| I_{LO} | Output Leakage Current (for High-Z State) | $0\text{V} \leq V_{out} \leq 5.5\text{V}$ Output is disabled (Hiz) | | -10 | | +10 | μA | |
| I_{CC1} | Operating Current, Random READ/WRITE | $t_{RC} = t_{RC} (\text{min.})$ | $t_{RAC} = 35\text{ns}$ $t_{RAC} = 40\text{ns}$ $t_{RAC} = 50\text{ns}$ $t_{RAC} = 60\text{ns}$ | | | 160 145 125 110 | mA | 1,2 |
| I_{CC2} | Standby Current,(TTL) | $\overline{\text{RAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$ at V_{IH} other inputs $\geq V_{SS}$ | | | | 4 | mA | |
| I_{CC3} | Refresh Current, RAS-Only | $\overline{\text{RAS}}$ cycling, $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$ at V_{IH} $t_{RC} = t_{RC} (\text{min.})$ | $t_{RAC} = 35\text{ns}$ $t_{RAC} = 40\text{ns}$ $t_{RAC} = 50\text{ns}$ $t_{RAC} = 60\text{ns}$ | | | 160 145 125 110 | mA | 2 |
| I_{CC4} | Operating Current, EDO Page Mode | $\overline{\text{RAS}}$ at V_{IL} , $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$ address cycling: $t_{PC}=t_{PC}(\text{min.})$ | $t_{RAC} = 35\text{ns}$ $t_{RAC} = 40\text{ns}$ $t_{RAC} = 50\text{ns}$ $t_{RAC} = 60\text{ns}$ | | | 160 145 125 110 | mA | 1,2 |
| I_{CC5} | Refresh Current, CAS Before RAS | $\overline{\text{RAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$ address cycling: $t_{RC}=t_{RC} (\text{min.})$ | $t_{RAC} = 35\text{ns}$ $t_{RAC} = 40\text{ns}$ $t_{RAC} = 50\text{ns}$ $t_{RAC} = 60\text{ns}$ | | | 160 145 125 110 | mA | 1 |
| I_{CC6} | Standby Current, (CMOS) | $\overline{\text{RAS}} \geq V_{CC}-0.2\text{V}$, $\overline{\text{UCAS}} \geq V_{CC}-0.2\text{V}$, $\overline{\text{LCAS}} \geq V_{CC}-0.2\text{V}$, All other inputs V_{SS} | | | | 1 | mA | |
| I_{CC7} | Self refresh Current | $\overline{\text{RAS}} = \overline{\text{CAS}} = 0.2\text{V}$, $\overline{\text{WE}} = \overline{\text{OE}} = A_0 \sim A_{10} = V_{CC}-0.2\text{V}$ or 0.2V $\overline{\text{DQ}_0} \sim \overline{\text{DQ}_3} = V_{CC}-0.2\text{V}$ or Open | | | | 300 | μA | 1,5 |
| V_{CC} | Supply Voltage | | | 3.0 | | 3.6 | V | |
| V_{IL} | Input Low Voltage | | | -0.3 | | 0.8 | V | 3 |
| V_{IH} | Input High Voltage | | | 2.0V | | $V_{CC}+0.3$ | V | 3 |
| V_{OL} | Output Low Voltage | $I_{OL} = 2\text{mA}$ | | | | 0.4 | V | |
| V_{OH} | Output High Voltage | $I_{OH} = -2\text{mA}$ | | 2.4 | | | V | |

Notes:

- I_{CC} is dependent on output loading when the device output is selected. Specified $I_{CC}(\text{max.})$ is measured with the output open.
- I_{CC} is dependent upon the number of address transitions specified $I_{CC}(\text{max.})$ is measured with a maximum of one transition per address cycle in random Read/Write and EDO Fast Page Mode.
- Specified $V_{IL}(\text{min.})$ is steady state operation. During transitions $V_{IL}(\text{min.})$ may undershoot to -0.3V for a period not to exceed 20ns. All AC parameters are measured with $V_{IL}(\text{min.}) \geq V_{SS}$ and $V_{IH}(\text{max.}) \leq V_{CC}$.
- S-Version.

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AC Characteristics

 $T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{CC} = 3.3\text{ V} \pm 10\%$ $V_{IH}/V_{IL} = 2.0/0.8\text{V}$, $V_{OH}/V_{OL} = 2.0/0.8\text{V}$

 An initial pause of 100 μs and 8 CAS-before-RAS or RAS-only refresh cycles are required after power-up.

| Parameter | Symbol | 35 | | 40 | | 50 | | 60 | | Unit | Notes |
|--|-----------|------|------|------|------|------|------|------|------|------|--------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Read or Write Cycle Time | t_{RC} | 70 | | 75 | | 90 | | 104 | | ns | |
| Read Modify write Cycle Time | t_{RWC} | 90 | | 93 | | 109 | | 140 | | ns | |
| RAS Precharge Time | t_{RP} | 25 | | 25 | | 30 | | 40 | | ns | |
| RAS Pulse Width | t_{RAS} | 35 | 75k | 40 | 100k | 50 | 100k | 60 | 10k | ns | |
| Access Time from $\overline{\text{RAS}}$ | t_{RAC} | | 35 | | 40 | | 50 | | 60 | ns | 1,2,3 |
| Access Time from $\overline{\text{CAS}}$ | t_{CAC} | | 11 | | 12 | | 13 | | 15 | ns | 1,5,10 |
| Access Time from Column Address | t_{AA} | | 18 | | 20 | | 25 | | 30 | ns | 1,5,6 |
| CAS to Output Low-Z | t_{CLZ} | 0 | | 0 | | 0 | | 3 | | ns | |
| CAS to Output High-Z | t_{CEZ} | 3 | 8 | 3 | 8 | 3 | 8 | 3 | 15 | ns | |
| RAS Hold Time | t_{RSH} | 10 | | 12 | | 14 | | 15 | | ns | |
| RAS Hold Time Referenced to OE | t_{ROH} | 7 | | 8 | | 9 | | 10 | | ns | |
| CAS Hold Time | t_{CSH} | 34 | | 34 | | 45 | | 45 | | ns | |
| CAS Pulse width | t_{CAS} | 6 | | 6 | | 8 | | 10 | 10k | ns | |
| RAS to CAS Delay Time | t_{RCD} | 13 | 24 | 18 | 28 | 19 | 37 | 20 | 45 | ns | |
| RAS to Column Address Delay Time | t_{RAD} | 10 | 17 | 13 | 20 | 14 | 25 | 15 | 30 | ns | 7 |
| CAS to RAS Precharge Time | t_{CRP} | 5 | | 5 | | 5 | | 5 | | ns | |
| Row Address Set-Up Time | t_{ASR} | 0 | | 0 | | 0 | | 0 | | ns | |
| Row Address Hold Time | t_{RAH} | 6 | | 8 | | 9 | | 10 | | ns | |
| Column Address Set-Up Time | t_{ASC} | 0 | | 0 | | 0 | | 0 | | ns | |
| Column Address Hold Time | t_{CAH} | 5 | | 6 | | 7 | | 10 | | ns | |
| Column Address to RAS Lead Time | t_{RAL} | 18 | | 20 | | 25 | | 30 | | ns | |
| Column Address Hold Time Referenced to RAS | t_{AR} | 25 | | 34 | | 44 | | 45 | | ns | |
| Read Command Set-Up Time | t_{RCS} | 0 | | 0 | | 0 | | 0 | | ns | |
| Read Command Hold Time Referenced to $\overline{\text{CAS}}$ | t_{RCH} | 0 | | 0 | | 0 | | 0 | | ns | 4 |
| Read Command Hold Time Referenced to RAS | t_{RRH} | 0 | | 0 | | 0 | | 0 | | ns | 4 |
| Write Command Set-Up Time | t_{WCS} | 0 | | 0 | | 0 | | 0 | | ns | 8,9 |
| Write Command Hold Time | t_{WCH} | 5 | | 6 | | 7 | | 10 | | ns | |
| Write Command Pulse Width | t_{WCP} | 5 | | 6 | | 7 | | 10 | | ns | |
| Write Command to RAS Lead Time | t_{RWL} | 10 | | 12 | | 13 | | 15 | | ns | |

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AC Characteristics

| Parameter | Symbol | 35 | | 40 | | 50 | | 60 | | Unit | Notes |
|---|-------------------|------|------|------|------|------|------|------|------|---------------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Write Command to $\overline{\text{CAS}}$ Lead Time | t_{CWL} | 8 | | 12 | | 13 | | 13 | | ns | |
| Data Set-Up Time | t_{DS} | 0 | | 0 | | 0 | | 0 | | ns | |
| Data Hold Time | t_{DH} | 5 | | 8 | | 9 | | 10 | | ns | |
| Data Hold Time Referenced to $\overline{\text{RAS}}$ | t_{DHR} | 25 | | 36 | | 46 | | 46 | | ns | |
| $\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time | t_{RWD} | 46 | | 54 | | 64 | | 79 | | ns | |
| $\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time | t_{CWD} | 23 | | 24 | | 25 | | 34 | | ns | |
| Column Address to $\overline{\text{WE}}$ Delay Time | t_{AWD} | 29 | | 32 | | 37 | | 49 | | ns | |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time | t_{RPC} | 0 | | 0 | | 0 | | 0 | | ns | |
| Access Time from $\overline{\text{CAS}}$ Precharge | t_{CPA} | | 20 | | 22 | | 30 | | 35 | ns | |
| EDO Page Mode Cycle Time | t_{PC} | 14 | | 15 | | 20 | | 25 | | ns | |
| EDO Page Mode Read-Modify-write Cycle Time | t_{PRWC} | 45 | | 50 | | 59 | | 59 | | ns | |
| $\overline{\text{CAS}}$ Precharge Time (EDO Page Mode) | t_{CP} | 4 | | 5 | | 8 | | 10 | | ns | |
| $\overline{\text{RAS}}$ Pulse Width (EDO Page Mode Only) | t_{RASP} | 35 | 100k | 40 | 100k | 50 | 100k | 60 | 100k | ns | |
| Access Time from $\overline{\text{OE}}$ | t_{OEA} | | 11 | | 12 | | 13 | | 15 | ns | |
| $\overline{\text{OE}}$ to Data Delay Time | t_{OED} | 5 | | 8 | | 8 | | 15 | | ns | |
| $\overline{\text{OE}}$ to Output High-Z | t_{OEZ} | 3 | 8 | 3 | 8 | 3 | 8 | 3 | 8 | ns | |
| $\overline{\text{OE}}$ Command Hold Time | t_{OEH} | 5 | | 7 | | 7 | | 15 | | ns | |
| Data Output Hold after $\overline{\text{CAS}}$ Low | t_{DOH} | 3 | | 3 | | 5 | | 5 | | ns | |
| $\overline{\text{RAS}}$ to Output High-Z | t_{REZ} | 3 | 8 | 3 | 8 | 3 | 8 | 3 | 15 | ns | |
| $\overline{\text{WE}}$ to Output High-Z | t_{WEZ} | 3 | 10 | 3 | 10 | 3 | 12 | 3 | 15 | ns | |
| $\overline{\text{OE}}$ to $\overline{\text{CAS}}$ Hold Time | t_{OCH} | 8 | | 8 | | 8 | | 5 | | ns | |
| $\overline{\text{CAS}}$ Hold Time to $\overline{\text{OE}}$ | t_{CHO} | 8 | | 8 | | 8 | | 5 | | ns | |
| $\overline{\text{OE}}$ Precharge Time | t_{OEP} | 8 | | 8 | | 8 | | 5 | | ns | |
| $\overline{\text{CAS}}$ Set-Up Time for $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Cycle | t_{CSR} | 8 | | 10 | | 10 | | 10 | | ns | |
| $\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Cycle | t_{CHR} | 8 | | 10 | | 10 | | 10 | | ns | |
| Transition Time | t_{T} | 2 | 50 | 2 | 50 | 2 | 50 | 2 | 50 | ns | |
| Refresh Period | t_{REF} | | 8 | | 8 | | 8 | | 8 | ms | |
| $\overline{\text{RAS}}$ pulse width ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Self refresh) | t_{RASS} | 100 | | 100 | | 100 | | 100 | | μs | |
| $\overline{\text{RAS}}$ precharge time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Self refresh) | t_{RPS} | 70 | | 75 | | 90 | | 110 | | ns | |
| $\overline{\text{CAS}}$ precharge time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Self refresh) | t_{CHS} | 50 | | 50 | | 50 | | 50 | | ns | |

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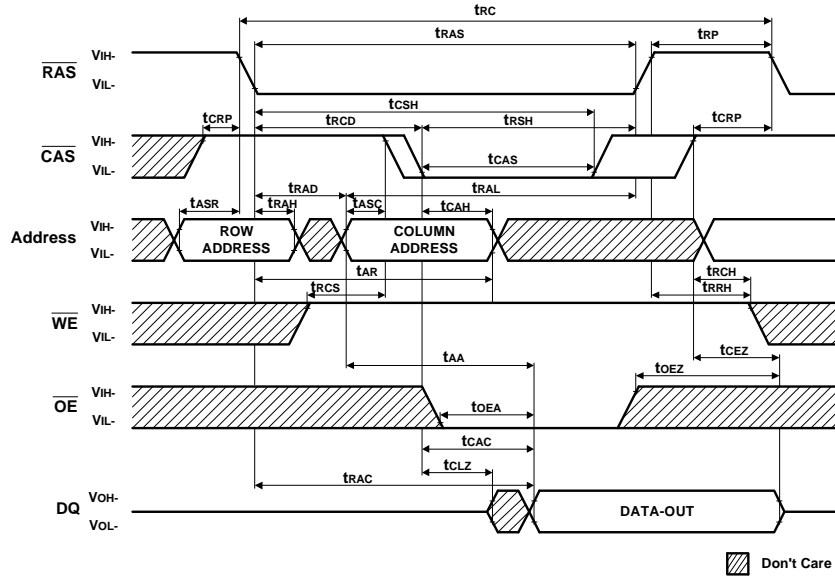
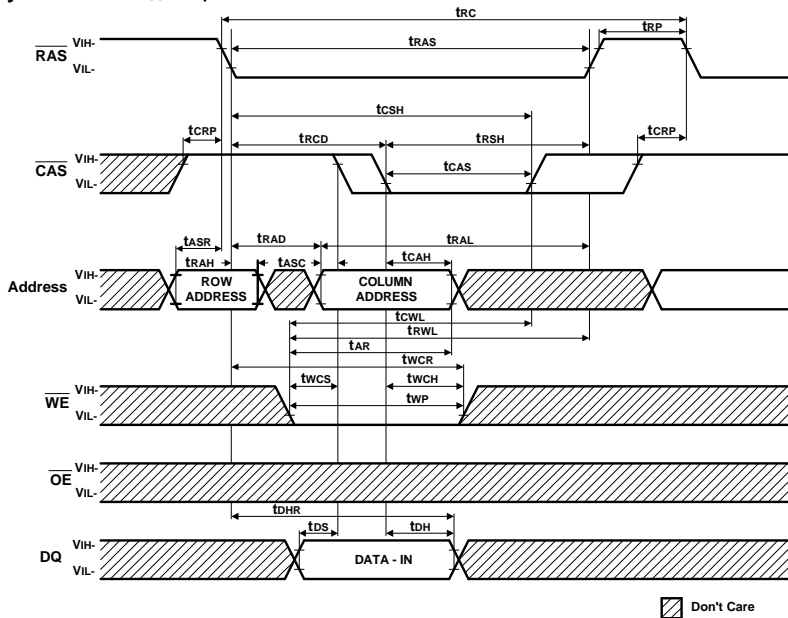
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- 7 -

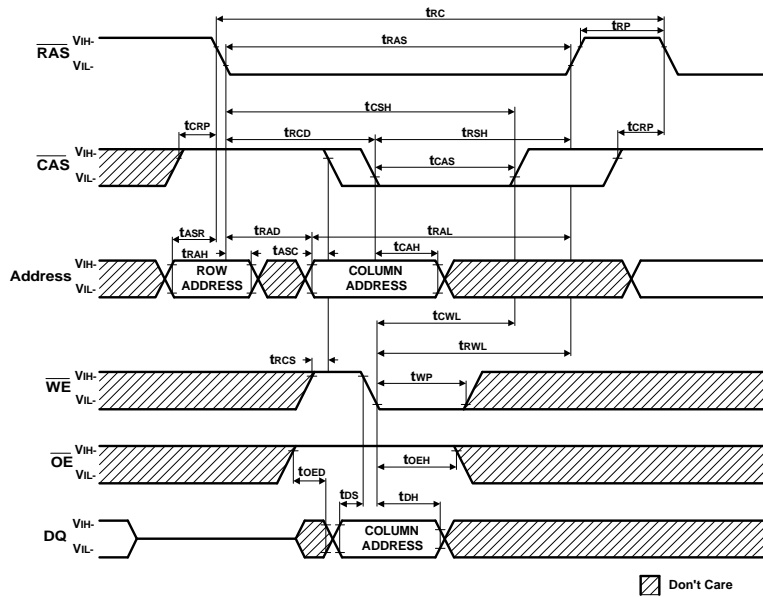
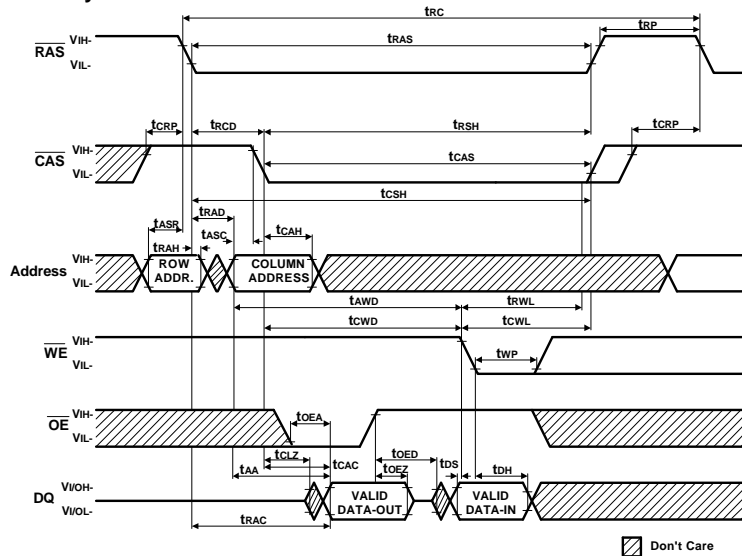
Notes:

1. Measure with a load equivalent to one TTL inputs and 50 pF.
2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max.})$. If t_{RCD} is greater than $t_{RCD}(\text{max.})$, access time will be t_{AA} dominant.
3. Assumes that $t_{RAD} \leq t_{RAD}(\text{max.})$. If t_{RAD} is greater than $t_{RCD}(\text{max.})$, access time will be controlled by t_{CAC} .
4. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle.
5. Access time is determined by the longest of t_{CAA} , t_{CAC} and t_{CPA} .
6. Assumes that $t_{RAD} \geq t_{RAD}(\text{max.})$.
7. Operation within the $t_{RAD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, the access time is controlled by t_{CAA} and t_{CAC} .
8. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are not restrictive operating parameters.
9. $t_{WCS}(\text{min.})$ must be satisfied in an Early Write Cycle.
10. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{\text{CAS}}$ of $\overline{\text{WE}}$. t_T is measured between $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$. AC-measurements assume $t_T = 1.5 \text{ ns}$.

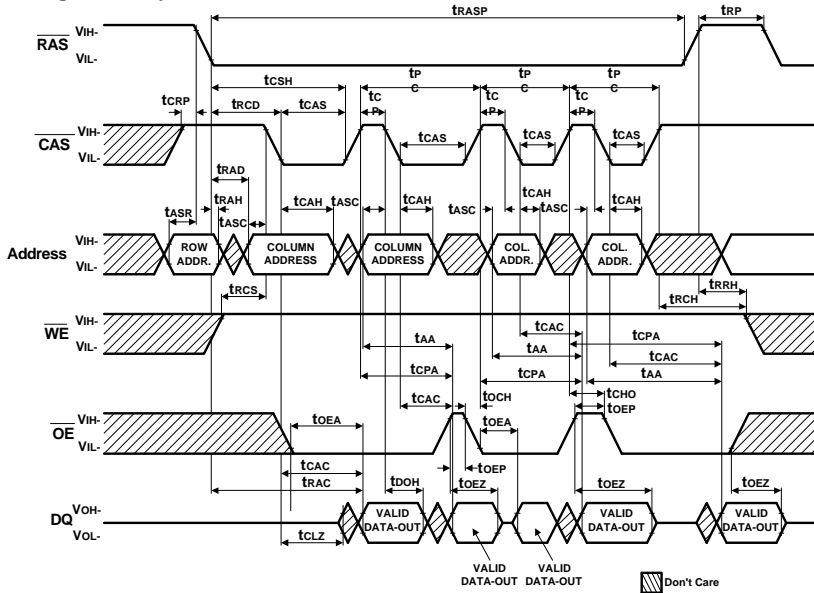
Read Cycle

Early Write Cycle NOTE : D_{OUT} = Open

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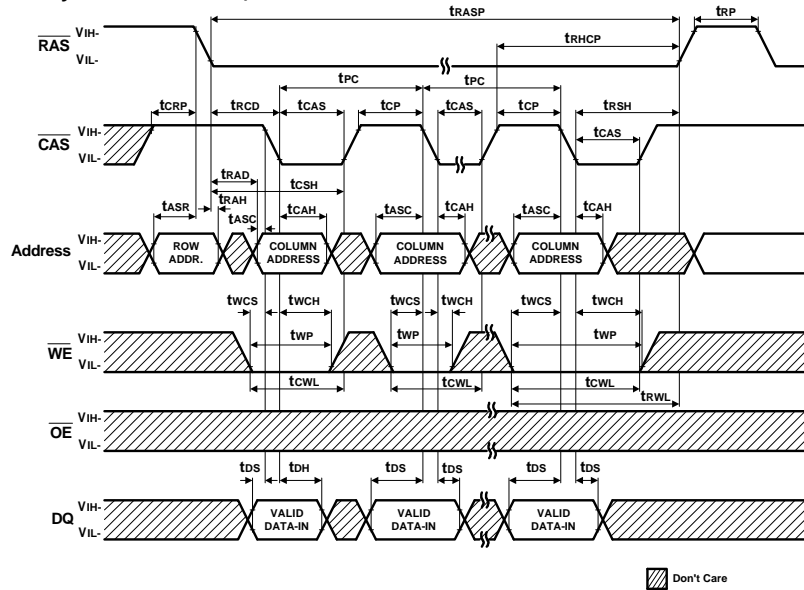
TEL : 886-2-27968078

Late Write Cycle (OE Controlled Write) NOTE : D_{OUT} = Open

Read - Modify - Write Cycle


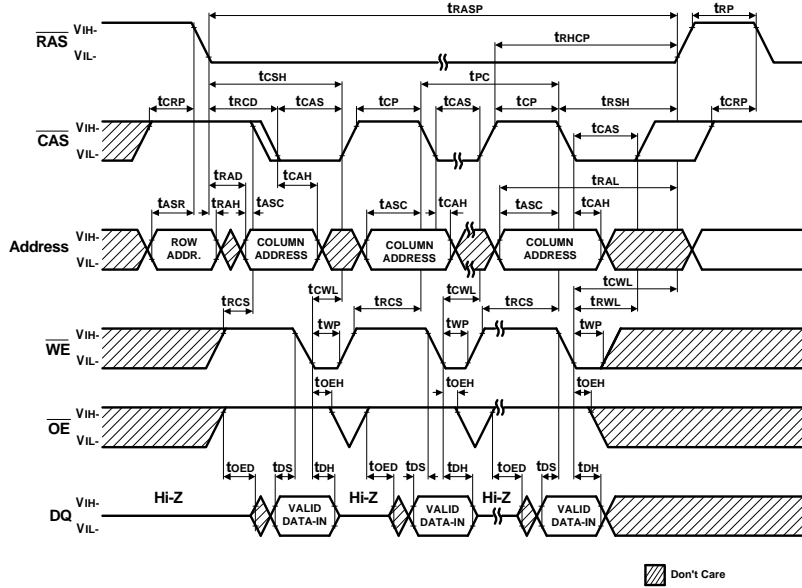
EDO Page Read Cycle



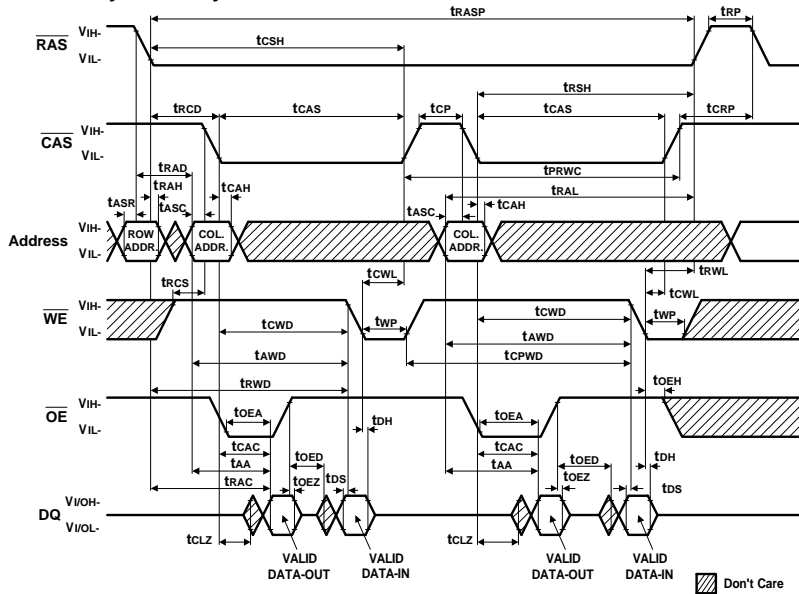
EDO Page Write Cycle NOTE : D_{out} = Open



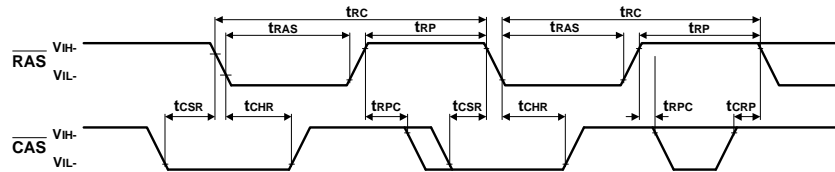
EDO Page Mode Late Write Cycle



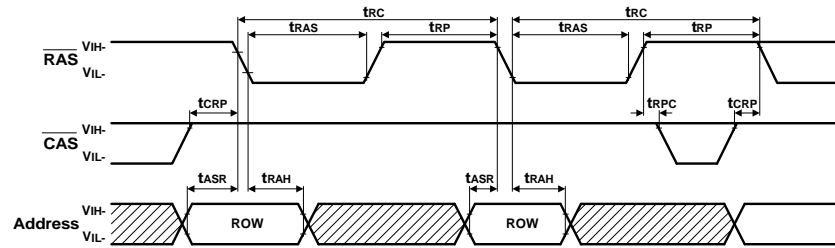
EDO Page Read - Modify - Write Cycle



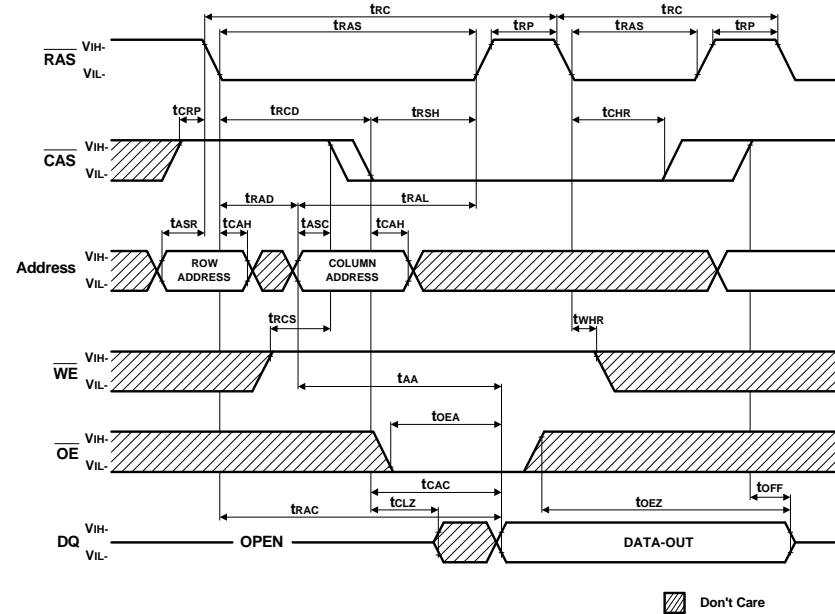
CAS Before RAS Refresh Cycle



RAS -Only Refresh Cycle

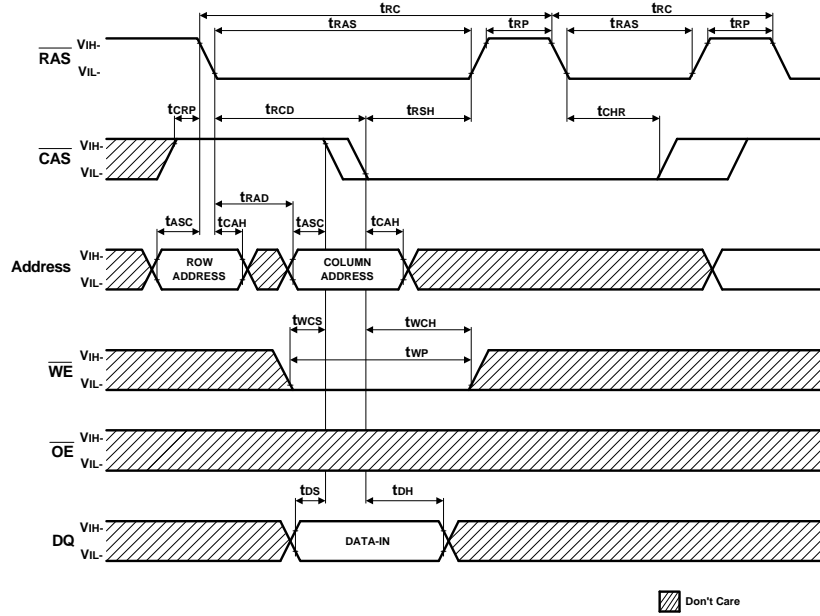


Hidden Refresh Cycle (Read)

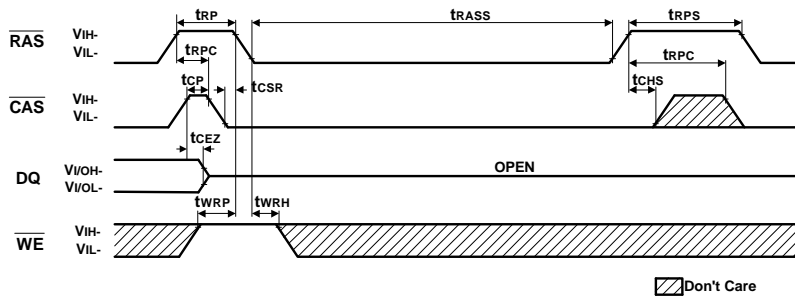


▨ Don't Care

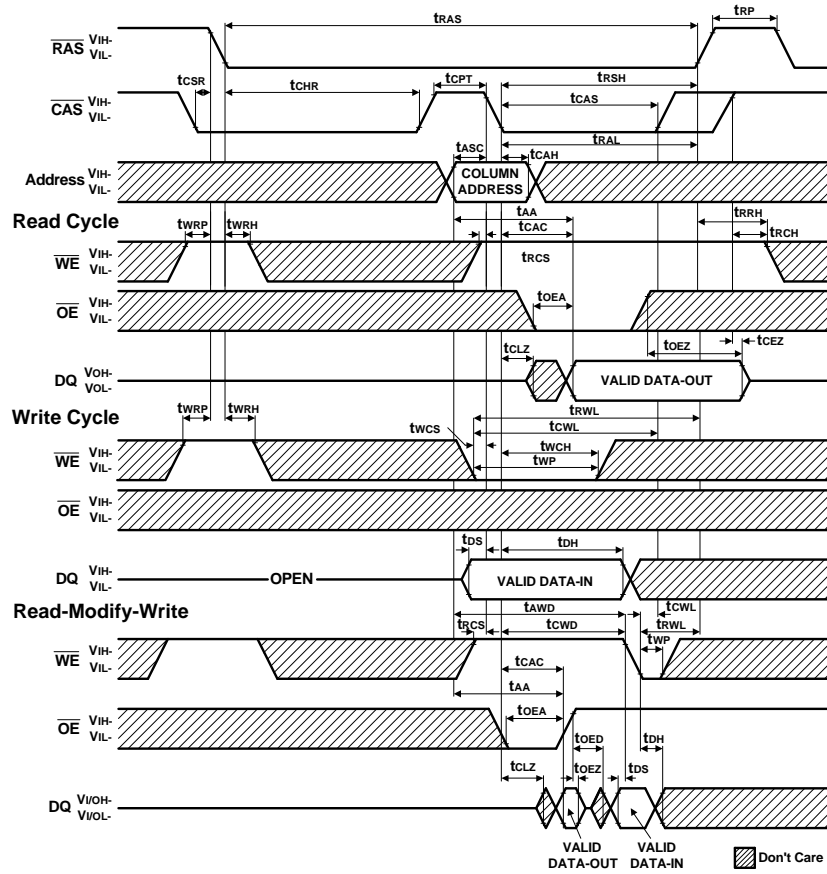
Hidden Refresh Cycle (Write) NOTE : D_{OUT} =Open



CAS-Before-RAS Self Refresh Cycle



CAS - Before RAS Refresh Counter Test Cycle





GLT440L16

256K X 16 CMOS DYNAMIC RAM WITH EXTENDED DATA OUTPUT

Nov. 2004 (Rev.2.6)

Ordering Information

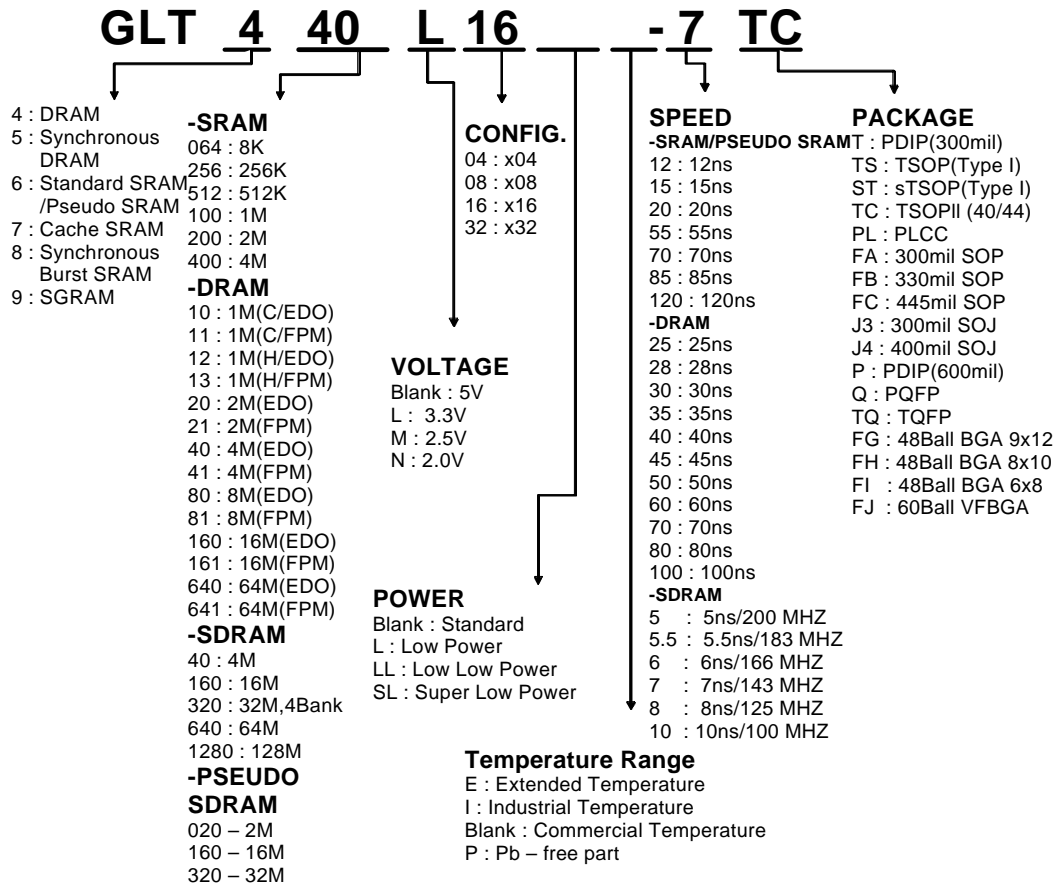
| Part Number | SPEED | POWER | FEATURE | TEMPERATURE | PACKAGE |
|-----------------|-------|--------------|---------|-------------|-------------------|
| GLT440L16-35J4 | 35ns | Normal | EDO | Commercial | 40L 400mil SOJ |
| GLT440L16-40J4 | 40ns | Normal | EDO | Commercial | 40L 400mil SOJ |
| GLT440L16-50J4 | 50ns | Normal | EDO | Commercial | 40L 400mil SOJ |
| GLT440L16-60J4 | 60ns | Normal | EDO | Commercial | 40L 400mil SOJ |
| GLT440L16S-35J4 | 35ns | Self Refresh | EDO | Commercial | 40L 400mil SOJ |
| GLT440L16S-40J4 | 40ns | Self Refresh | EDO | Commercial | 40L 400mil SOJ |
| GLT440L16S-50J4 | 50ns | Self Refresh | EDO | Commercial | 40L 400mil SOJ |
| GLT440L16S-60J4 | 60ns | Self Refresh | EDO | Commercial | 40L 400mil SOJ |
| GLT440L16P-35J4 | 35ns | Normal | EDO | Commercial | 40L 400mil SOJ |
| GLT440L16P-40J4 | 40ns | Normal | EDO | Commercial | 40L 400mil SOJ |
| GLT440L16P-50J4 | 50ns | Normal | EDO | Commercial | 40L 400mil SOJ |
| GLT440L16P-60J4 | 60ns | Normal | EDO | Commercial | 40L 400mil SOJ |
| GLT440L16-35TC | 35ns | Normal | EDO | Commercial | 44L 400mil TSOPII |
| GLT440L16-40TC | 40ns | Normal | EDO | Commercial | 44L 400mil TSOPII |
| GLT440L16-50TC | 50ns | Normal | EDO | Commercial | 44L 400mil TSOPII |
| GLT440L16-60TC | 60ns | Normal | EDO | Commercial | 44L 400mil TSOPII |
| GLT440L16S-35TC | 35ns | Self Refresh | EDO | Commercial | 44L 400mil TSOPII |
| GLT440L16S-40TC | 40ns | Self Refresh | EDO | Commercial | 44L 400mil TSOPII |
| GLT440L16S-50TC | 50ns | Self Refresh | EDO | Commercial | 44L 400mil TSOPII |
| GLT440L16S-60TC | 60ns | Self Refresh | EDO | Commercial | 44L 400mil TSOPII |
| GLT440L16P-35TC | 35ns | Normal | EDO | Commercial | 44L 400mil TSOPII |
| GLT440L16P-40TC | 40ns | Normal | EDO | Commercial | 44L 400mil TSOPII |
| GLT440L16P-50TC | 50ns | Normal | EDO | Commercial | 44L 400mil TSOPII |
| GLT440L16P-60TC | 60ns | Normal | EDO | Commercial | 44L 400mil TSOPII |

G-Link Technology Corporation, Taiwan

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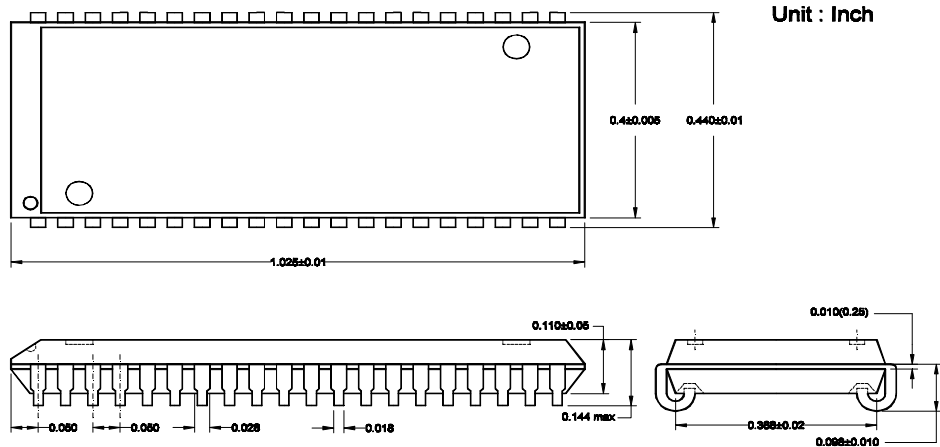
TEL : 886-2-27968078

- 16 -

Parts Numbers (Top Mark) Definition for DRAM :


Package Information

400 mil 40 pin Small Outline J-form Package (SOJ)



40/44 Lead Thin Small Outline Package TSOP(Type II)

