CH7302/CH7303 HDTV / DVI Transmitter

Features

- Digital Visual Interface (DVI) Transmitter up to 165M pixels/second
- DVI low jitter PLL with Emission Reduction
- DVI hot plug detection
- Analog YPrPb outputs for HDTV
- HDTV support for 525p, 625p, 720p, 1080i and 1080p
- Macrovision™ copy protection support for 525p and 625p **(CH7303 only)**
- Programmable digital input 16-bit D[15:0] interface supporting RGB (15, 16, 24 or 30 bit) and YCrCb input data formats
- Can output either RGB or YPrPb
- TV / Monitor connection detection
- Programmable power management
- Three 10-bit video DAC outputs
- Fully programmable through serial port
- Complete Windows and DOS driver support
- Low voltage interface support to graphics device
- Offered in a 64-pin LQFP package

General Description

The CH7302/CH7303 is a Display Controller device which accepts a digital graphics input signal, and encodes and transmits data through a DVI link (DFP can also be supported), VGA port (analog RGB) or an HDTV port (YPrPb). The device accepts data over one 16-bit wide variable voltage data port which supports different data formats including RGB and YCrCb.

The device is able to generate and insert synchronization signals for analog HDTV interface standards. Color space conversion from RGB and YCrCb to YPrPb is supported

The DVI processor includes a low jitter PLL for generation of the high frequency serialized clock, and all circuitry required to encode, serialize and transmit data. The CH7302/CH7303 is able to drive a DVI display at a pixel rate of up to 165MHz, supporting UXGA resolution displays. No scaling of input data is performed on the data output to the DVI device.

In addition to DVI encoder and HDTV modes, bypass modes are included which output VGA style analog RGB for use as a CRT DAC supporting graphics standards up to UXGA.

Color space conversion from YCrCb to RGB is supported in both DVI and VGA bypass modes.

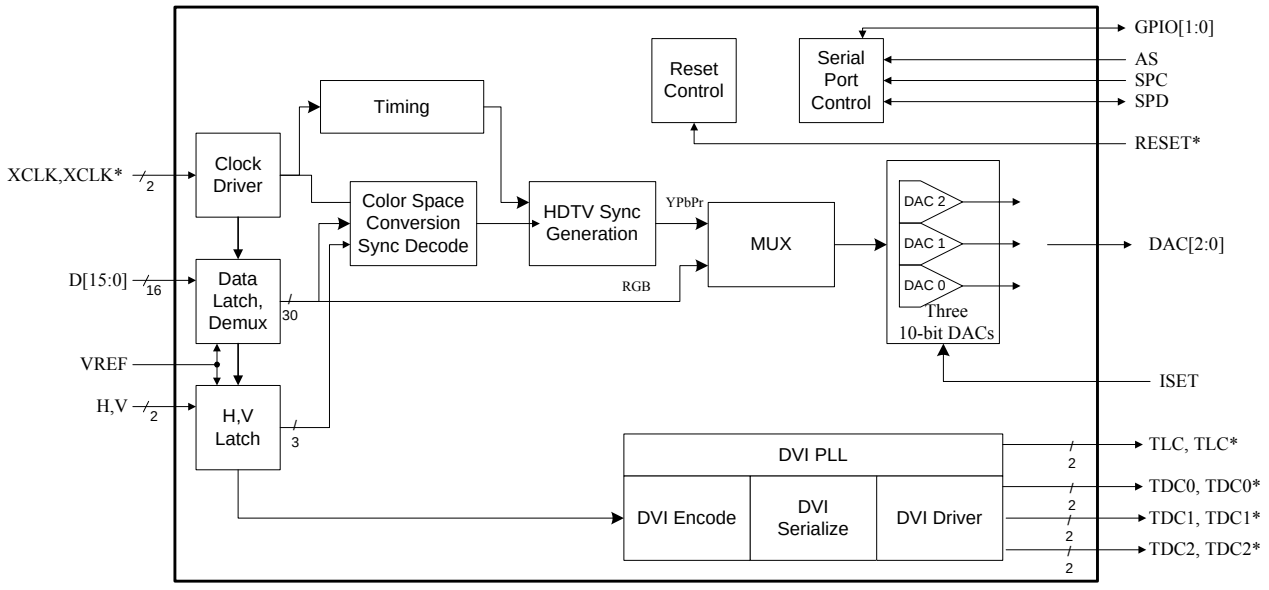

Figure 1: **Functional Block Diagram**

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1.0 Pin-Out

1.1 Package Diagram

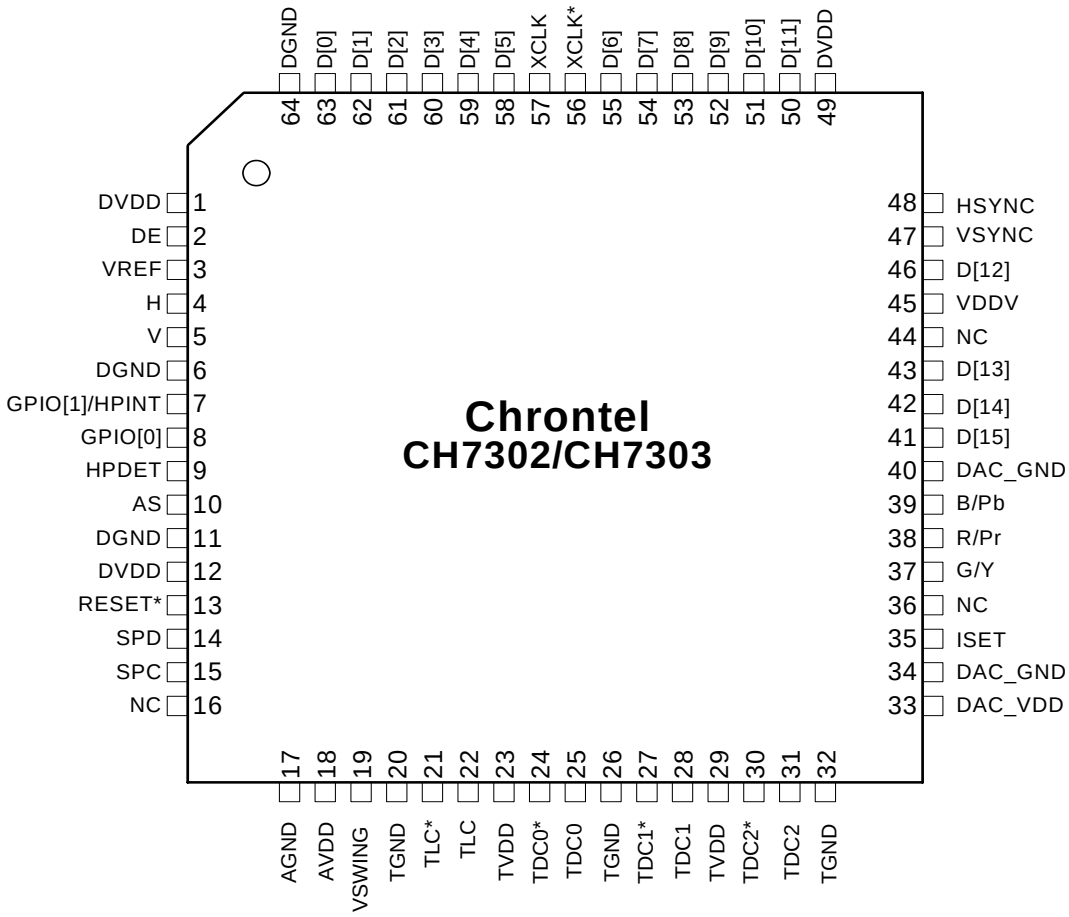

Figure 2: 64-Pin LQFP Package – CH7302/CH7303

1.2 Pin Description

Table 1: Pin Description

Pin #	Type	Symbol	Description
2	In	DE	**Data Enable** This pin accepts a data enable signal which is high when active video data is input to the device, and low all other times. The levels are 0 to VDDV, and the VREF signal is used as the threshold level. This input is used by the DVI. The TV-Out function uses H and V sync as reference to active video.
3	In	VREF	**Reference Voltage Input** The VREF pin inputs a reference voltage of VDDV / 2. The signal is derived externally through a resistor divider and decoupling capacitor, and will be used as a reference level for data, sync, data enable and clock inputs.
4	In	H	**Horizontal Sync Input** This pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDV and the VREF signal is used as the threshold level.
5	In	V	**Vertical Sync Input** This pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDV and the VREF signal is used as the threshold level.
7	In/Out	GPIO[1] / HPINT	**General Purpose Input - Output[1] / Hot Plug Interrupt** When the GPIO[1] pin is configured as an output, this pin can be used to output the DVI detect signal (pulls low when a termination change has been detected on the HPDET input). This is an open drain output. The output is released through serial port control.
8	In/Out	GPIO[0]	**General Purpose Input - Output[0]** (Weak internal pull-up) This pin provides a general purpose I/O controlled via the serial port. The internal pull-up will be to the DVDD supply.
9	In	HPDET	**Hot Plug Detect** (internal pull-down) This input pin determines whether the DVI is connected to a DVI monitor. When terminated, the monitor is required to apply a voltage greater than 2.4 volts. Changes on the status of this pin will be relayed to the graphics controller via GPIO[1]/HPINT pin pulling low. When the HPDET is pulled low, the DVI output driver will be shut down.
10	In	AS	**Address Select (Internal pull-up)** This pin determines the serial port address of the device (1,1,1,0,1,AS*,AS).
13	In	RESET*	**Reset* Input (Internal pull-up)** When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port register.
14	In/Out	SPD	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port and operates with inputs from 0 to VDDV. Outputs are driven from 0 to VDDV.
15	In	SPC	**Serial Port Clock Input** This pin functions as the clock input of the serial port and operates with inputs from 0 to VDDV.
19	In	VSWING	**DVI Swing Control** This pin sets the swing level of the DVI outputs. A 2.4K ohm resistor should be connected between this pin and TGND using short and wide traces.
22, 21	Out	TLC, TLC*	**DVI Clock Outputs** These pins provide the differential clock output for the DVI interface corresponding to data on the TDC[2:0] outputs.
25, 24	Out	TDC0, TDC0*	**DVI Data Channel 0 Outputs** These pins provide the DVI differential outputs for data channel 0 (blue).
28, 27	Out	TDC1, TDC1*	**DVI Data Channel 1 Outputs** These pins provide the DVI differential outputs for data channel 1 (green).
30, 31	Out	TDC2*, TDC2	**DVI Data Channel 2 Outputs** These pins provide the DVI differential outputs for data channel 2 (red).

Table 1: Pin Description (contd.)

Pin #	Type	Symbol	Description
35	In	ISET	**Current Set Resistor** This pin sets the DAC current. A 140 ohm resistor should be connected between this pin and DAC ground (pins 34 and 40) using short and wide traces.
37	Out	Y/G (DAC1)	**Luma / Green Output** This pin outputs a selectable video signal. The output is designed to drive a 75ohm doubly terminated load. The output can be selected to be the luminance component of YPrPb or Green component of RGB.
38	Out	R/Pr (DAC2)	**Red / Pr Output** This pin outputs a selectable video signal. The output is designed to drive a 75ohm doubly terminated load. The output can be selected to be the Pr component of YPrPb or Red component of RGB.
39	Out	B/Pb (DAC0)	**Blue / Pb Output** This pin outputs a selectable video signal. The output is designed to drive a 75ohm doubly terminated load. The output can be selected to be the Pb component of YPrPb or Blue component of RGB.
47	Out	VSYNC	**Vertical Sync Output** A buffered version of VGA vertical sync can be acquired from this pin. (Refer to **Register 21h**, bit [3] of DC register)
48	Out	HSYNC	**Horizontal Sync Output** A buffered version of VGA horizontal sync can be acquired from this pin. (Refer to **Register 21h**, bit [3] of DC register)
41 - 43, 46, 50 – 55, 58 –63	In/Out	D[15] - D[0]	**Data[15] through Data[0] Inputs** These pins accept the 16 data inputs from a digital video port of a graphics controller. The levels are 0 to VDDV, and the VREF signal is used as the threshold level.
57, 56	In	XCLK, XCLK*	**External Clock Inputs** These inputs form a differential clock signal input to the CH7302/CH7303 for use with the H, V, DE and D[15:0] data. If differential clocks are not available, the XCLK* input pin should be connected to VREF. The clock polarity used for latching data can be selected using the MCP control bit.
1, 12, 49	Power	DVDD	**Digital Supply Voltage** (3.3V)
6, 11, 64	Power	DGND	**Digital Ground**
45	Power	VDDV	**I/O Supply Voltage** (1.1V to 3.3V)
23, 29	Power	TVDD	**DVI Transmitter Supply Voltage** (3.3V)
20, 26, 32	Power	TGND	**DVI Transmitter Ground**
18	Power	AVDD	**PLL Supply Voltage** (3.3V)
17	Power	AGND	**PLL Ground**
33	Power	DAC_VDD	**DAC Supply Voltage** (3.3V)
34, 40	Power	DAC_GND	**DAC Ground**
16, 36, 44	–	NC	**No Connect**

2.0 Functional Description

2.1 TV Output Operation

The CH7302/CH7303 can be selected to operate in one of several bypass modes for driving monitors requiring component video signals (HDTV, multi-sync monitors, etc.). All modes make use of the same set of DACs, and therefore cannot be used simultaneously. **Table 2** describes the possible operating modes. A 'p' following a number in the Input Scan Type column indicates a progressive scan (non-interlaced) input where the number indicates the active number of lines per frame. An 'i' following a number in the Input Scan Type column indicates an interlaced input where the number indicates the active number of lines per frame. Detailed descriptions of each of the operating modes are listed in **Table 2**.

Table 2: Operating Modes

Input Scan Type	Input Data Format	Output scan Type	Output Format	Operating Mode	Described In section
non-interlaced	RGB	non-interlaced	RGB	RGB bypass	2.1.2
non-interlaced (480p, 576p, 720p)	RGB / YCrCb	non-interlaced	YPbPr	HDTV/EDTV bypass	2.1.1
Interlaced (1080i)	RGB / YCrCb	interlaced	YPbPr	HDTV bypass (1080i)	2.1.1
non-interlaced (1080p)	RGB / YCrCb	non-interlaced	YPbPr	HDTV bypass (1080p)	2.1.1

2.1.1 HDTV / EDTV Bypass

In HDTV / EDTV Bypass mode, data, sync and clock signals are input to the CH7302/CH7303 from a graphics device in the scanning method that matches the display device (interlaced data is sent to the CH7302/CH7303 to drive an interlaced display, non-interlaced data is sent to the CH7302/CH7303 to drive a non-interlaced display). The input data format can be YCrCb or RGB. Horizontal and vertical sync signals must either be sent to the CH7302/CH7303 from the graphics device or embedded in the data stream according to SMPTE standards. Data is 2X multiplexed, and the XCLK clock signal can be 1X or 2X times the pixel rate. Input data is color space converted to the selected video format, which has sync signals generated and is outputted from the video DACs. The output format is YPbPr. The graphics resolutions supported for HDTV Bypass mode are shown in **Table 3** below. The resolutions supported for EDTV Bypass mode are shown in **Table 4** below.

Table 3: HDTV Bypass

Active Resolution	Total Resolution	Scan Type	Pixel Clock (MHz)	Frame Rate (Hz)	Standard
1280x720	1650x750	Non-Interlaced	74.25 74.25/1.001	60 60/1.001	SMPTE 296M
1280x720	1648x750	Non-Interlaced	74.160	60	
1920x1080	2200x1125	Interlaced	74.25 74.25/1.001	30 30/1.001	SMPTE 274M
1920x1080	2640x1125	Interlaced	74.25	25	SMPTE 274M
1920x1080	2376x1250	Interlaced	74.25	25	SMPTE 295M
1920x1080	2200x1125	Non-Interlaced	148.5 148.5/1.001 74.25 74.25/1.001	60 60/1.001 30 30/1.001	SMPTE 274M
1920x1080	2640x1125	Non-Interlaced	148.5 74.25	50 25	SMPTE 274M
1920x1080	2750x1125	Non-Interlaced	74.25 74.25/1.001	24 24/1.001	SMPTE 274M
1920x1080	2752x1125	Non-Interlaced	74.304	24	
1920x1080	2376x1250	Non-Interlaced	148.5	50	SMPTE 295M

Table 4: EDTV Bypass

Active Resolution	Total Resolution	Scan Type	Pixel Clock (MHz)	Frame Rate (Hz)	Standard
720x480	858x525	Non-Interlaced	27.0	60/1.001	EIA-770.2-A
720x483	858x525	Non-Interlaced	27.027	60	SMPTE 293M
720x480	856x525	Non-Interlaced	26.937	60/1.001	
720x483	856x525	Non-Interlaced	26.964	60	
720x576	864x625	Non-interlaced	27.0	50	ITU-R BT.1358

2.1.2 RGB Bypass

In RGB Bypass mode, data, sync and clock signals are input to the CH7302/CH7303 from a graphics device, and bypassed directly to the D/A converters to implement a second CRT DAC function. External sync signals must be supplied from the graphics device. These sync signals are buffered internally, and can be output to drive the CRT. The input data format must be RGB in this operating mode. Input data is 2X multiplexed, and the XCLK clock signal can be 1X or 2X times the pixel rate. The CH7302/CH7303 can support a pixel rate of 165MHz. This operating mode uses all 10 bits of the DAC's 10-bit range, and provides a nominal signal swing of 0.661V (or 0.7V depending on DAC Gain setting in control registers) when driving a 75Ω doubly terminated load. No scaling, scan conversion or flicker filtering is applied in Bypass modes.

2.2 DVI Output

2.2.1 DVI Transmitter

In DVI Output mode, multiplexed input data, sync and clock signals are input to the CH7302/CH7303 from the graphics controller's digital output port. Data will be 2X multiplexed, and the clock inputs can be 1X or 2X times the pixel rate. Some examples of modes supported are shown in the table. For the table below, clock frequencies for given modes were taken from VESA DISPLAY MONITOR TIMING SPECIFICATIONS, not from VESA TIMING DEFINITION FOR FLAT PANEL MONITORS. The device is not dependent upon this set of timing specifications. Any values of pixels/line, lines/frame and clock rate are acceptable, as long as the pixel rate remains below 165MHz. The input format can be any RGB format or YCrCb (**Section 2.3.5**).

Table 5: DVI Output

Graphics Resolution	Active Aspect Ratio	Pixel Aspect Ratio	Refresh Rate (Hz)	Input pixel Frequency (MHz)	DVI Frequency (Mbits/Sec)
720x400	4:3	1.35:1.00	<85	<35.5	<355
640x400	8:5	1:1	<85	<31.5	<315
640x480	4:3	1:1	<85	<36	<360
720x480	4:3	9:8	59.94	27	270
720x576	4:3	15:12	50	27	270
800x600	4:3	1:1	<85	<57	<570
1024x768	4:3	1:1	<85	<95	<950
1280x720	16:9	1:1	<85	<110	<1100
1280x768	15:9	1:1	<85	<119	<1190
1280x1024	4:3	1:1	<85	<158	<1580
1366x768	16:9	1:1	<85	<140	<1400
1360x1024	4:3	1:1	<75	<145	<1450
1400x1050	4:3	1:1	<75	<156	<1560
1600x1200	4:3	1:1	<60	<165	<1650
1920X1080[1]	16:9	1:1	<60	<165	<1650

[1]This mode is implemented with reduced blanking.

2.3 Input Interface

2.3.1 Overview

Two distinct methods of transferring data to the CH7302/CH7303 are described. They are:

- Multiplexed data, clock input at 1X the pixel rate
- Multiplexed data, clock input at 2X the pixel rate

For the multiplexed data, clock at 1X pixel rate, the data applied to the CH7302/CH7303 is latched with both edges of the clock (also referred to as dual edge transfer mode or DDR). For the multiplexed data, clock at 2X pixel rate the data applied to the CH7302/CH7303 is latched with one edge of the clock (also known as single edge transfer mode or SDR). The polarity of the pixel clock can be reversed under serial port control. In single edge transfer modes, the clock edge used to latch data is programmable. In dual edge transfer modes, the clock edge used to latch the first half of each pixel is programmable.

2.3.2 Interface Voltage Levels

The graphics controller interface can operate at a variable voltage level controlled by the voltage on the VDDV pin. This should be set to the maximum voltage of the interface (typically 3.3V or adjustable between 1.1 and 1.8V). The VREF pin is the voltage reference for the data, data enable, clock and sync inputs and must be tied to VDDV/2. This is typically done using a resistor divider.

2.3.3 Input Clock and Data Timing Diagram

Figure 3 below shows the timing diagram for input data and clocks. The first XCLK/XCLK* waveform represents the input clock for single edge transfer (SDR) methods. The second XCLK/XCLK* waveform represents the input clock for the dual edge transfer (DDR) method. The timing requirements are given in **Section 4.6**.

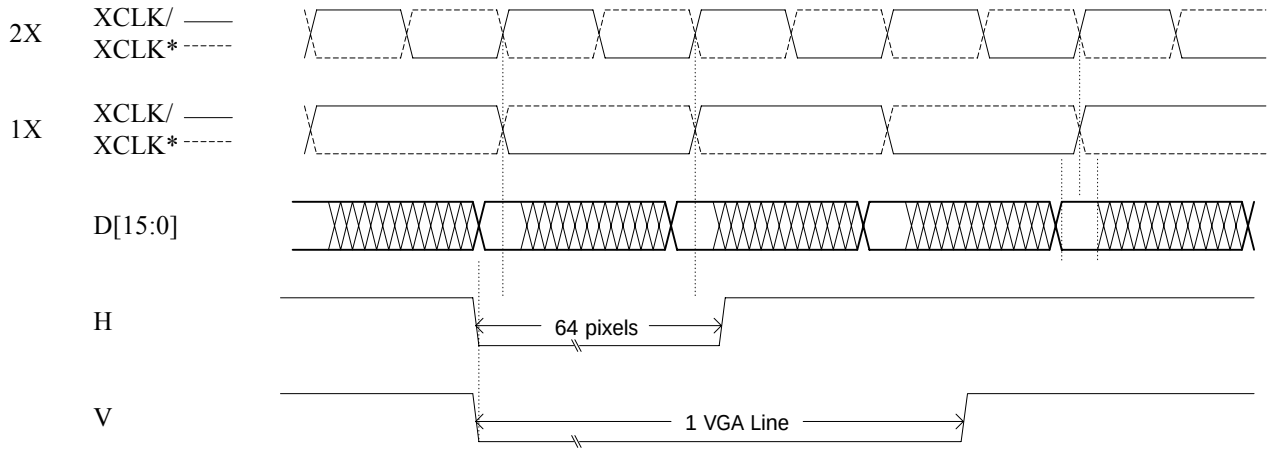

Figure 3: Clock, Data and Interface Timing

2.3.4 Data De-skew Feature

The de-skew feature allows timing adjustment to be made to the input setup and hold time. The input data D[15:0] can be latched slightly before or after the latching edge of XCLK, depending on the amount of the de-skew. Note that the XCLK is not changed, only the time at which the data is latch relative to XCLK. The de-skew feature is controlled through XCMD[3:0] bits located in **Register 1Dh**. The delay t_{CD} between clock and data is given by the following formula:

t_{CD} = - XCMD[3:0] * t_{STEP} for $0 \le$ XCMD[3:0] ≤ 7
t_{CD} = (XCMD[3:0] – 8) * t_{STEP} for $8 \le$ XCMD[3:0] ≤ 15

where XCMD is a number between 0 and 15 represented as a binary code
t_{STEP} is the adjustment increment (**Section 4.5**)

The delay is also tabulated in **Table 15.**

2.3.5 Input Data Formats

The CH7302/CH7303 supports 9 different data formats, each of which can be used with a 1X clock latching data on both clock edges, or a 2X clock latching data with a single edge (rising or falling depending on the value of the MCP bit (**Register 1Ch**) – rising refers to a rising edge on the XCLK signal, a falling edge on the XCLK* signal). The input data formats are (IDF[3:0]):

IDF	Description
0	12-bit multiplexed RGB input (24-bit color), (multiplex scheme 1)
1	12-bit multiplexed RGB input (24-bit color), (multiplex scheme 2)
2	8-bit multiplexed RGB input (16-bit color, 565)
3	8-bit multiplexed RGB input (15-bit color, 555)
4	8-bit multiplexed YCrCb input (24-bit color), (Y, Cr and Cb are multiplexed)
5	15-bit multiplexed RGB input (30-bit color), (multiplex scheme B1 - half-half mode)
6	15-bit multiplexed RGB input (30-bit color), (multiplex scheme B2 - half-color mode)
7	15-bit multiplexed RGB input (30-bit color), (multiplex scheme B3 - edge pair mode)
10	16-bit non-multiplexed RGB input (16-bit color, 565)
12	16-bit non-multiplexed YCrCb input (Cr and Cb are multiplexed)

The input data format is shown in **Figure 4** below. The Pixel Data bus represents a 16-bit, 15-bit, 12-bit or 8-bit data stream, which contains either RGB or YCrCb formatted data. The input data rate is 1X or 2X the pixel rate, and each pair of Pn values (e.g.; P0a and P0b) will contain one or two pixel encoded as shown in the following tables.

It is assumed that the first clock cycle following the leading edge of the incoming horizontal sync signal contains the first word (Pxa) of a pixel, if an active pixel was present immediately following the horizontal sync. This does not mean that active data should immediately follow the horizontal sync, however. When the input is a YCrCb data stream the color-difference data will be transmitted at half the data rate of the luminance data, with the sequence being set as Cb, Y, Cr, Y, where Cb0,Y0,Cr0 refers to co-sited luminance and color-difference samples and the following Y1 byte refers to the next luminance sample, per ITU-R BT.656 standards (the clock frequency is dependent upon the current mode, and is not 27MHz as specified in ITU-R BT.656). All non-active pixels should be 0 in RGB formats, and 16 for Y, 128 for Cr and Cb in YCrCb formats.

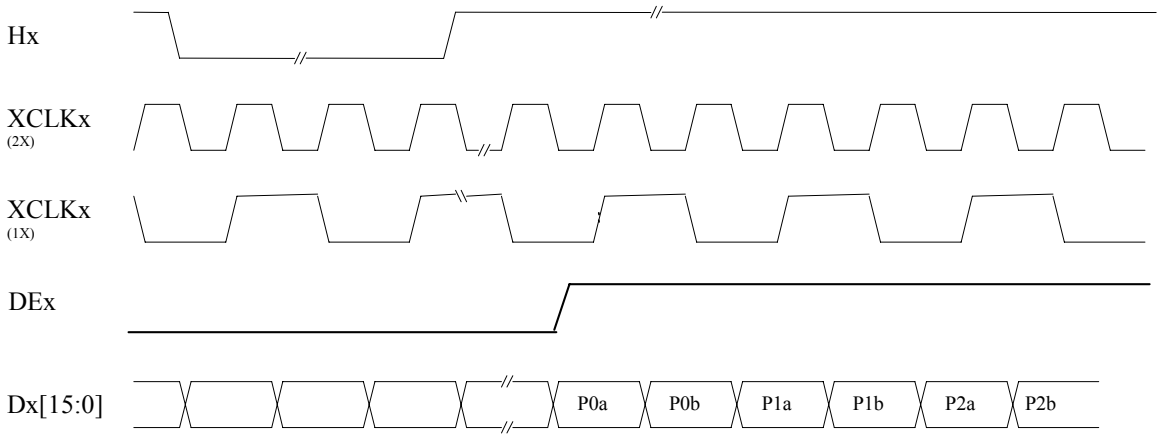

Figure 4: 12-bit Multiplexed Input Data Formats (IDFx = 0,1,2,3,4)

Table 6: Multiplexed Input Data Formats (IDF = 0, 1)

IDF = Format =		0 12-bit RGB				1 12-bit RGB			
Pixel #		**P0a**	**P0b**	**P1a**	**P1b**	**P0a**	**P0b**	**P1a**	**P1b**
Bus Data	D[11]	G0[3]	R0[7]	G1[3]	R1[7]	G0[4]	R0[7]	G1[4]	R1[7]
	D[10]	G0[2]	R0[6]	G1[2]	R1[6]	G0[3]	R0[6]	G1[3]	R1[6]
	D[9]	G0[1]	R0[5]	G1[1]	R1[5]	G0[2]	R0[5]	G1[2]	R1[5]
	D[8]	G0[0]	R0[4]	G1[0]	R1[4]	B0[7]	R0[4]	B1[7]	R1[4]
	D[7]	B0[7]	R0[3]	B1[7]	R1[3]	B0[6]	R0[3]	B1[6]	R1[3]
	D[6]	B0[6]	R0[2]	B1[6]	R1[2]	B0[5]	G0[7]	B1[5]	G1[7]
	D[5]	B0[5]	R0[1]	B1[5]	R1[1]	B0[4]	G0[6]	B1[4]	G1[6]
	D[4]	B0[4]	R0[0]	B1[4]	R1[0]	B0[3]	G0[5]	B1[3]	G1[5]
	D[3]	B0[3]	G0[7]	B1[3]	G1[7]	G0[0]	R0[2]	G1[0]	R1[2]
	D[2]	B0[2]	G0[6]	B1[2]	G1[6]	B0[2]	R0[1]	B1[2]	R1[1]
	D[1]	B0[1]	G0[5]	B1[1]	G1[5]	B0[1]	R0[0]	B1[1]	R1[0]
	D[0]	B0[0]	G0[4]	B1[0]	G1[4]	B0[0]	G0[1]	B1[0]	G1[1]

Table 7: Multiplexed Input Data Formats (IDF = 2, 3)

IDF = Format =		2 RGB 5-6-5				3 RGB 5-5-5			
Pixel #		**P0a**	**P0b**	**P1a**	**P1b**	**P0a**	**P0b**	**P1a**	**P1b**
Bus Data	D[11]	G0[4]	R0[7]	G1[4]	R1[7]	G0[5]	X	G1[5]	X
	D[10]	G0[3]	R0[6]	G1[3]	R1[6]	G0[4]	R0[7]	G1[4]	R1[7]
	D[9]	G0[2]	R0[5]	G1[2]	R1[5]	G0[3]	R0[6]	G1[3]	R1[6]
	D[8]	B0[7]	R0[4]	B1[7]	R1[4]	B0[7]	R0[5]	B1[7]	R1[5]
	D[7]	B0[6]	R0[3]	B1[6]	R1[3]	B0[6]	R0[4]	B1[6]	R1[4]
	D[6]	B0[5]	G0[7]	B1[5]	G1[7]	B0[5]	R0[3]	B1[5]	R1[3]
	D[5]	B0[4]	G0[6]	B1[4]	G1[6]	B0[4]	G0[7]	B1[4]	G1[7]
	D[4]	B0[3]	G0[5]	B1[3]	G1[5]	B0[3]	G0[6]	B1[3]	G1[6]

Table 8: Multiplexed Input Data Formats (IDF = 4)

IDF = Format =		4 YCrCb 8-bit							
Pixel #		**P0a**	**P0b**	**P1a**	**P1b**	**P2a**	**P2b**	**P3a**	**P3b**
Bus Data	D[7]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	Cb2[7]	Y2[7]	Cr2[7]	Y3[7]
	D[6]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	Cb2[6]	Y2[6]	Cr2[6]	Y3[6]
	D[5]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	Cb2[5]	Y2[5]	Cr2[5]	Y3[5]
	D[4]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	Cb2[4]	Y2[4]	Cr2[4]	Y3[4]
	D[3]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb2[3]	Y2[3]	Cr2[3]	Y3[3]
	D[2]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb2[2]	Y2[2]	Cr2[2]	Y3[2]
	D[1]	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb2[1]	Y2[1]	Cr2[1]	Y3[1]
	D[0]	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb2[0]	Y2[0]	Cr2[0]	Y3[0]

Table 9: Embedded Sync in Multiplexed Data Format (IDF=4)

IDF = Format =		4 YCrCb 8-bit							
Pixel #		**P0a**	**P0b**	**P1a**	**P1b**	**P2a**	**P2b**	**P3a**	**P3b**
Bus Data	D[7]	1	0	0	S[7]	Cb2[7]	Y2[7]	Cr2[7]	Y3[7]
	D[6]	1	0	0	S[6]	Cb2[6]	Y2[6]	Cr2[6]	Y3[6]
	D[5]	1	0	0	S[5]	Cb2[5]	Y2[5]	Cr2[5]	Y3[5]
	D[4]	1	0	0	S[4]	Cb2[4]	Y2[4]	Cr2[4]	Y3[4]
	D[3]	1	0	0	S[3]	Cb2[3]	Y2[3]	Cr2[3]	Y3[3]
	D[2]	1	0	0	S[2]	Cb2[2]	Y2[2]	Cr2[2]	Y3[2]
	D[1]	1	0	0	S[1]	Cb2[1]	Y2[1]	Cr2[1]	Y3[1]
	D[0]	1	0	0	S[0]	Cb2[0]	Y2[0]	Cr2[0]	Y3[0]

In this mode, the S[7:0] byte contains the following data:

S[6] = F = 1 during field 2, 0 during field 1
S[5] = V = 1 during field (frame) blank, 0 elsewhere
S[4] = H = 1 during EAV (synchronization reference at the end of active video)
0 during SAV (synchronization reference at the start of active video)

Table 10: Multiplexed Input Data Formats (IDF = 5, 6, 7)

IDF = Format =		5 15-bit RGB		6 15-bit RGB		7 15-bit RGB	
Pixel #		**P0a**	**P0b**	**P0a**	**P0b**	**P0a**	**P0b**
Bus Data	D[14]	G0[4]	R0[9]	R0[4]	R0[9]	R0[8]	R0[9]
	D[13]	G0[3]	R0[8]	R0[3]	R0[8]	R0[6]	R0[7]
	D[12]	G0[2]	R0[7]	R0[2]	R0[7]	R0[4]	R0[5]
	D[11]	G0[1]	R0[6]	R0[1]	R0[6]	R0[2]	R0[3]
	D[10]	G0[0]	R0[5]	R0[0]	R0[5]	R0[0]	R0[1]
	D[9]	B0[9]	R0[4]	G0[4]	G0[9]	G0[8]	G0[9]
	D[8]	B0[8]	R0[3]	G0[3]	G0[8]	G0[6]	G0[7]
	D[7]	B0[7]	R0[2]	G0[2]	G0[7]	G0[4]	G0[5]
	D[6]	B0[6]	R0[1]	G0[1]	G0[6]	G0[2]	G0[3]
	D[5]	B0[5]	R0[0]	G0[0]	G0[5]	G0[0]	G0[1]
	D[4]	B0[4]	G0[9]	B0[4]	B0[9]	B0[8]	B0[9]
	D[3]	B0[3]	G0[8]	B0[3]	B0[8]	B0[6]	B0[7]
	D[2]	B0[2]	G0[7]	B0[2]	B0[7]	B0[4]	B0[5]
	D[1]	B0[1]	G0[6]	B0[1]	B0[6]	B0[2]	B0[3]
	D[0]	B0[0]	G0[5]	B0[0]	B0[5]	B0[0]	B0[1]

Table 11: Non-multiplexed Input Data Formats (IDF = 10, 12)

IDF = Format =		10 16-bit RGB		12 16-bit YCrCb	
Pixel #		**P0a**	**P0b**	**P0a**	**P0b**
Bus Data	D[15]	R[7]	Not used	Y[7]	Not used
	D[14]	R[6]	Not used	Y[6]	Not used
	D[13]	R[5]	Not used	Y[5]	Not used
	D[12]	R[4]	Not used	Y[4]	Not used
	D[11]	R[3]	Not used	Y[3]	Not used
	D[10]	G[7]	Not used	Y[2]	Not used
	D[9]	G[6]	Not used	Y[1]	Not used
	D[8]	G[5]	Not used	Y[0]	Not used
	D[7]	G[4]	Not used	C[7]	Not used
	D[6]	G[3]	Not used	C[6]	Not used
	D[5]	G[2]	Not used	C[5]	Not used
	D[4]	B[7]	Not used	C[4]	Not used
	D[3]	B[6]	Not used	C[3]	Not used
	D[2]	B[5]	Not used	C[2]	Not used
	D[1]	B[4]	Not used	C[1]	Not used
	D[0]	B[3]	Not used	C[0]	Not used

3.0 Register Control

The CH7302/CH7303 is controlled via a serial control port. The serial bus uses only the SC clock to latch data into registers, and does not use any internally generated clocks so that the device can be written to in all power down modes. The device should retain all register values during power down modes. For details of CH7302/CH7303 registers read/write operation, please see AN-61.

3.1 Non-Macrovision Control Registers Index

The non-Macrovision controls are listed below.

Table 12: Control Register Index

Name	Description	Address
GENERAL & POWER DOWN CONTROLS		
DACPD[2:0]	DAC Power Down	**49h**
DID[7:0]	Device ID register	**4Bh**
ResetIB	Software SPP (serial port) reset	**48h**
ResetDB	Software datapath reset	**48h**
FPD	TV power down	**49h**
VID[7:0]	Version ID register	**4Ah**

INPUT/OUTPUT CONTROLS		
DACBP	DAC bypass	**21h**
DACG[1:0]	DAC gain control	**21h**
DACT[2:0]	DAC termination sense	**20h**
DES	Decode embedded sync	**1Fh**
GOENB[1:0]	Direction control for GPIO pins	**1Eh**
GPIOL[1:0]	Read or Write Data for GPIO pins	**1Eh**
HSP	H sync polarity control	**1Fh**
IDF[3:0]	Input Data Format for D[15:0]	**1Fh, 21h**
MCP	XCLK Polarity Control for D[15:0]	**1Ch**
SENSE	TV Sense	**20h**
SYNCO	Select Sync output on Hsync and Vsync	**21h**
T_RGB	YCrCb to RGB enable	**56h**
VSP	V sync polarity control for	**1Fh**
XCM	XCLK 1X / 2X select for D[15:0]	**1Ch**
XCMD[3:0]	Delay adjust between XCLK and D[15:0]	**1Dh**

DVI CONTROLS		
CTL[3:0]	DVI Control Inputs	**31h**
DVID[2:0]	DVI transmitter drive strength control	**33h**
DVII	DVI output invert	**33h**
DVIP	DVI Power Down Control	**49h**
DVIL	DVI Power Down Control	**49h**
DVIT	Hot Plug Detection Pin Level	**20h**
HPDD	Hot Plug Detection Disable	**23h**
HPIE	Hot Plug Interrupt Enable on GPIO[1]	**20h**
HPIR	Hot Plug Interrupt Reset	**1Eh**
TMSYO	DVI Sync Direction	**56h**
TPCP[1:0]	DVI PLL charge pump trim	**33h**
TPFBD[3:0]	DVI PLL feed back divider	**34h**
TPFFD[1:0]	DVI PLL feed forward divider	**34h**
TPLPF[3:0]	DVI PLL low pass filter	**36h**
TPPSD[1:0]	DVI PLL post scale divider	**33h**

TV-OUT CONTROLS		
BL[7:0]	TV-Out Black level control	**07h**
HDTV	Enable HDTV modes	**14h**
HP[8:0]	TV-Out horizontal position control	**05h, 03h**
IR[2:0]	Input data resolution	**00h**
SR[2:0]	TV-Out scaling ratio	**00h**
VOS[1:0]	TV-Out video standard	**00h**
VP[8:0]	TV-Out vertical position control	**06h, 03h**

3.2 Control Registers Map

Table 13: Serial Port Register Map

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	IR2	IR1	IR0	VOS1	VOS0	SR2	SR1	SR0
03h	Reserved	Reserved	Reserved	HP8	VP8	Reserved	Reserved	Reserved
05h	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
06h	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
07h	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0
14h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HDTV
1Ch	Reserved	Reserved	Reserved	Reserved	Reserved	MCP	Reserved	XCM
1Dh	Reserved	Reserved	Reserved	Reserved	XCMD3	XCMD2	XCMD1	XCMD0
1Eh	GOENB1	GOENB0	GPIOL1	GPIOL0	HPIR	Reserved	Reserved	Reserved
1Fh	Reserved	DES	Reserved	VSP	HSP	IDF2	IDF1	IDF0
20h	HPIE	Reserved	DVIT	Reserved	DACT2	DACT1	DACT0	SENSE
21h	Reserved	Reserved	IDF3	Reserved	SYNCO	DACG1	DACG0	DACBP
23h	Reserved	Reserved	Reserved	Reserved	Reserved	HPDD	Reserved	Reserved
31h	Reserved	Reserved	Reserved	Reserved	CTL3	CTL2	CTL1	CTL0
33h	DVID2	DVID1	DVID0	DVII	TPPSD1	TPPSD0	Reserved	TPCP0
34h	Reserved	Reserved	TPFFD1	TPFFD0	TPFBD3	TPFBD2	TPFBD1	TPFBD0
36h	TPLPF3	TPLPF2	TPLPF1	TPLPF0	Reserved	Reserved	Reserved	Reserved
48h	Reserved	Reserved	Reserved	ResetIB	ResetDB	Reserved	TSTP1	TSTP0
49h	DVIP	DVIL	Reserved	Reserved	DACPD2	DACPD1	DACPD0	FPD
4Ah	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
4Bh	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
56h	Reserved	Reserved	TMSYO	Reserved	Reserved	Reserved	Reserved	T_RGB

3.3 Control Registers Description

Display Mode Register **Symbol: DM**
Address: 00h

	7	6	5	4	3	2	1	0
SYMBOL:	IR2	IR1	IR0	VOS1	VOS0	SR2	SR1	SR0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0

Register DM provides programmable control of the CH7302/CH7303 TV display modes, including input resolution (IR[2:0]), video output standard (VOS[1:0]), and scaling ratio (SR[2:0]). The mode of operation is determined according to **Table 14** below when the HDTV bit (**register 14h**, bit 7) = '1'. These are the HDTV modes.

Table 14: Display Mode for HDTV/Component TV (HDTV = '1')

Mode	IR[2:0]	VOS [1:0]	SR [2:0]	Input Data Format (Active Video)	Total Pixels/Line x Total Lines/Frame	Output Standard [TV Standard]	Frame Rate [Hz]	Pixel Clock [MHz]
48	000	00	000	720x480	858x525	EIA-770.2-A	60/1.001	27.0
49	001	00	000	720x483	858x525	SMPTE293M	60	27.027
50	000	10	001	1280x720	1650x750	SMPTE296M	60	74.250
51	000	01	001	1920x1080	2376x1250	SMPTE295M	25	74.250
52	001	10	100	1920x1080	2376x1250	SMPTE295M	50	148.500
53	001	01	001	1920x1080	2200x1125	SMPTE274M	30	74.250
54	010	01	001	1920x1080	2640x1125	SMPTE274M	25	74.250
55	010	10	100	1920x1080	2200x1125	SMPTE274M	60	148.500
56	011	10	100	1920x1080	2640x1125	SMPTE274M	50	148.500
57	100	10	001	1920x1080	2200x1125	SMPTE274M	30	74.250
58	101	10	001	1920x1080	2750x1125	SMPTE274M	24	74.250
59	110	10	001	1920x1080	2640x1125	SMPTE274M	25	74.250
60	010	00	000	720x576	864x625	ITU-R BT.1358	50	27.000
63	000	00	010	720x480	858x525		60	26.937
64	001	00	010	720x483	856x525		60	26.964
65	000	10	011	1280x720	1648x750		60	74.160
66	101	10	011	1920x1080	2752x1125		24	74.304

Position Overflow Register **Symbol: PO**
Address: 03h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	HP8	VP8	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	0	0

HP8 and VP8 (bits 5-3) of register PO contain the MSB values for the horizontal position and vertical position controls. They are described in detail in HP (address 05h) and VP (address 06h) register descriptions.

Horizontal Position Register **Symbol: HP**
Address: 05h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	1	0	1	0	0	0	0

Register HP is used to shift the displayed TV image in a horizontal direction (left or right) to achieve a horizontally centered image on screen. The entire bit field, HP[8:0], is comprised of this register HP[7:0] plus HP[8] contained in the **PO register** (03h, bit 4). Increasing values move the displayed image position to the right, and decreasing values move the image position to the left.

Vertical Position Register **Symbol: VP**
Address: 06h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

Register VP is used to shift the displayed TV image in a vertical direction (up or down) to achieve a vertically centered image on screen. The entire bit field, VP[8:0], is comprised of this register VP[7:0] plus VP[8] contained in the **PO register** (03h, bit 3). The value represents the TV line number (relative to the VGA vertical sync) used to initiate the generation and insertion of the TV vertical interval (i.e. the first sequence of equalizing pulses). Increasing values delay the output of the TV vertical sync, causing the image position to move up on the TV screen. Decreasing values, therefore, move the image position DOWN. Each increment moves the image position by one 2 input line. The maximum value that should be programmed into VP[8:0] is the number of TV lines per field minus one half.

Black Level Register **Symbol: BL**
Address: 07h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	1	1	0	1	0	1

Register BL controls the black level. The default value is 117. The range of the black level is from 117 to 157.

HDTV Mode Register **Symbol: HDTVM**
Address: 14h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HDTV
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	0	0	1	0

HDTV (bit 0) enables the HDTV path.

Clock Mode Register **Symbol: CM**
Address: 1Ch

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	MCP	Reserved	XCM
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

XCM (bit 0) of register CM signifies the XCLK frequency for the data input. A value of '0' is used when XCLK is at the pixel frequency (dual edge clocking mode) and a value of '1' is used when XCLK is twice the pixel frequency (single edge clocking mode).

MCP (bit 2) of register CM controls the phase of the XCLK clock input for the data input. A value of '1' inverts the XCLK signal at the input of the device. This control is used to select which edge of the XCLK signal to use for latching input data.

Input Clock Register **Symbol: IC**
Address: 1Dh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	XCMD3	XCMD2	XCMD1	XCMD0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	1	0	0	0

XCMD[3:0] (bits 3-0) of register IC control the delay applied to the XCLK signal before latching input data D[15:0] per the following table. t_{STEP} is given is **Section 4.5**.

Table 15: Delay applied to XCLK before latching input data D[15:0]

XCMD3	XCMD2	XCMD1	XCMD0	Adjust phase of Clock relative to Data
0	0	0	0	0 * t_{STEP}, XCLK ahead of Data
0	0	0	1	1 * t_{STEP}, XCLK ahead of Data
0	0	1	0	2 * t_{STEP}, XCLK ahead of Data
0	0	1	1	3 * t_{STEP}, XCLK ahead of Data
0	1	0	0	4 * t_{STEP}, XCLK ahead of Data
0	1	0	1	5 * t_{STEP}, XCLK ahead of Data
0	1	1	0	6 * t_{STEP}, XCLK ahead of Data
0	1	1	1	7 * t_{STEP}, XCLK ahead of Data
1	0	0	0	0 * t_{STEP}, XCLK behind Data
1	0	0	1	1 * t_{STEP}, XCLK behind Data

1	0	1	0	2 * t_{STEP}, XCLK behind Data
1	0	1	1	3 * t_{STEP}, XCLK behind Data
1	1	0	0	4 * t_{STEP}, XCLK behind Data
1	1	0	1	5 * t_{STEP}, XCLK behind Data
1	1	1	0	6 * t_{STEP}, XCLK behind Data
1	1	1	1	7 * t_{STEP}, XCLK behind Data

GPIO Control Register **Symbol: GPIO**
Address: 1Eh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	GOENB1	GOENB0	GPIOL1	GPIOL0	HPIR	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	1	0	0	0	0	0	0

HPIR (bit 3) of register GPIO resets the hot plug detection circuitry. A value of '1' causes the CH7302/CH7303 to release the GPIO[1]/HPINT pin. When a hot plug interrupt is asserted by the CH7302/CH7303 (GPIO[1]/HPINT) the CH7302/CH7303 driver should read the DVIT bit in **Register 20h** to determine the state of the DVI termination. After having read this register, the HPIR bit should be set high to reset the circuit, and then set low again. In order to reset the HPIR bit high, DVIP and DVIL bits of register 49h[7:6] must first be set to '11'.

GPIOL[1:0] (bits 5-4) of register GPIO define the GPIO Read or Write Data bits [1:0]. When the corresponding GOENB bits (GOENB[1:0], are '0', the values in GPIOL[1:0] are driven out at the corresponding GPIO pins. When the corresponding GOENB bits are '1', the values in GPIOL[1:0] can be read to determine the level forced into the corresponding GPIO pins.

GOENB[1:0] (bits 7-6) of register GPIO define the GPIO Direction Control bits [1:0]. GOENB[1:0] control the direction of the GPIO[1:0] pins. A value of '1' sets the corresponding GPIO pin to an input, and a value of '0' sets the corresponding pin to a non-inverting output. The level at the output depends on the value of the corresponding bit GPIOL[1:0].

Input Data Format Register **Symbol: IDF**
Address: 1Fh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	DES	Reserved	VSP	HSP	IDF2	IDF1	IDF0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	0	0	0	0

IDF[2:0] (bits 2-0) of **Register IDF** plus IDF3 (bit 5 of **Register 21h**) select the input data format for the D[15:0] input. See **section 2.3.5** for a listing of available formats.

HSP (bit 3) of **Register IDF** controls the horizontal sync polarity. A value of '0' defines the horizontal sync to be active low, and a value of '1' defines the horizontal sync to be active high.

VSP (bit 4) of **Register IDF** controls the vertical sync polarity. A value of '0' defines the vertical sync to be active low, and a value of '1' defines the vertical sync to be active high.

DES (bit 6) of **Register IDF** signifies when the CH7302/CH7303 is to decode embedded sync signals present in the input data stream instead of using the H and V pins. This feature is only available for input data format # 4. A value of '0' selects the H and V pins to be used as the sync inputs, and a value of '1' selects the embedded sync signal.

Connection Detect Register **Symbol: CD**
Address: 20h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HPIE	Reserved	DVIT	Reserved	DACT2	DACT1	DACT0	SENSE
TYPE:	R/W	R/W	R	R/W	R	R	R	R/W
DEFAULT:	0	0	0	0	X	X	X	0

DACT[2:0] (bits 3-1) and SENSE (bit 0) of register CD provide a means to sense the connection of a TV to the three DAC outputs. The status bits, DACT[2:0] correspond to the termination of the four DAC outputs. However, the values contained in these status bits ARE NOT VALID until a sensing procedure is performed. Use of this register requires a sequence of events to enable the sensing of outputs, then reading out the applicable status bits. The detection sequence works as follows:

1) Set the power management register (address 49h) to enable all DACs, and set DACBP (bit 0) of register 21h to '0'.
2) Set the SENSE bit to '1'. This forces a constant output from the DACs. Note that during SENSE = 1, these 3 analog outputs are at steady state and no TV synchronization pulses are asserted.
3) Reset the SENSE bit to 0. This triggers a comparison between the voltage present on these analog outputs and the reference value. During this step, each of the four status bits corresponding to individual DAC outputs will be reset to "0" if they are NOT CONNECTED.
4) Read the status bits. The status bits, DACT[2:0] now contain valid information which can be read to determine which outputs are connected to a TV. A '1' indicates a valid connection, a '0' indicates an unconnected output.

DVIT (bit 5) of register CD can be read at any time to determine the level of the hot plug detection pin (**HPDET**). When the HPDET is low, the DVI output driver will be shut down. When the hot plug detection pin changes state, and the DVI output is selected, the GPIO[1]/HPINT output pin will be pulled low signifying a change in the DVI termination. At this point, the HPIR bit in **register 1Eh** should be set high, then low to reset the hot plug detect circuit.

HPIE (bit 7) of register CD enables the hot plug interrupt detection signal to be output from the GPIO[1]/HPINT pin. A value of '1' allows the hot plug detect circuit to pull the GPIO[1]/HPINT pin low when a change of state has taken place on the hot plug detection pin (**HPDET**). A value of '0' disables the interrupt signal. See also the description of the DVIT bit.

DAC Control Register **Symbol: DC**
Address: 21h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	IDF3	Reserved	SYNCO	DACG1	DACG0	DACBP
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

DACBP (bit 0) of register DC selects the DAC bypass mode. A value of '1' outputs the incoming data directly at the DAC[2:0] outputs for the VGA-Bypass RGB output. For the other TV output modes such as YPrPb, DACBP bit must be set to 0.

DACG[1:0] (bits 2-1) of **Register DC** control the DAC gain. DACG1 should be '1' when the input data format is YCrCb (IDF = 4), or '0' when the input data format is RGB.

SYNCO (bit 3) of **Register DC** enables the HSYNC and VSYNC outputs.

IDF3 (bit 5) of **Register DC** is the MSB of IDF[3:0] which is described in **Section 2.3.5**.

Hot Plug Detect Register **Symbol: HPD**
Address: 23h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	HPDD	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

HPDD (bit 2) of **Register HPD** disables the hardware hot plug detection function. This function (default on) tri-states the DVI outputs when the hot plug detect pin (HPDET) is pulled low in accordance with the DVI specification, revision 1.0. This function is independent of the hot plug interrupt function (HPIE, **Register 20h**, bit 7) controlled via the SPP interface.

HPDD = 0 => hardware hot plug interrupt is enabled
= 1 => hardware hot plug interrupt is disabled

DVI Control Input Register **Symbol: TCTL**
Address: 31h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	CTL3	CTL2	CTL1	CTL0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	0	0	0	0

CTL[3:0] (bits 3-0) of register TCTL set the DVI control inputs applied to the green and red channel during sync intervals. It is recommended to leave the controls at the default value. Refer to the DVI Specification, Revision 1.0, **section 3.2** for more details.

DVI PLL Charge Pump Control Register **Symbol: TPCP**
Address: 33h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	DVID2	DVID1	DVID0	DVII	TPPSD1	TPPSD0	Reserved	TPCP0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	1	1	0	0	1	0	0

TPCP0 (bit 0) of register TPCP controls the DVI PLL charge pump. The value should be set as shown in **Table 16.**

TPPSD[1:0] (bits 3-2) of register TPCP control the DVI PLL post scale divider. The value should set as shown in **Table 16** depending on the input frequency range.

DVII (bit 4) of register TPCP inverts the DVI outputs. A value of 1 inverts the output. A value of 0 is recommended.

DVID[2:0] (bits 7-5) of register TPCP control the DVI transmitter output drive level. The value should be set as shown in **Table 16.**

DVI PLL Divider Register **Symbol: TPD**
Address: 34h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	TPFFD1	TPFFD0	TPFBD3	TPFBD2	TPFBD1	TPFBD0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	0	1	1	0

TPFBD[3:0] (bits 3-0) of **register TPD** control the DVI PLL feedback divider. The value should be set as shown in **Table 16** depending on the input frequency range.

TPFFD[1:0] (bits 5-4) of **register TPD** control the DVI PLL feed forward divider. The value should be set as shown in **Table 16** depending on the input frequency range.

DVI PLL LPF Register **Symbol: TLPF**
Address: 36h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	TPLPF3	TPLPF2	TPLPF1	TPLPF0	Reserved	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

TPLPF[3:0] (bits 7-4) of **register TLPF** control the DVI PLL low pass filter. The value should be set as shown in **Table 16** depending on the input frequency range.

Table 16: DVI Register Settings for Different Frequency Ranges

Register		Lower than 65MHz	Higher than 65MHz
33h	TPCP	08h	04h
34h	TPD	16h	26h
36h	TLPF	60h	A0h

Reset Register **Symbol: RES**
Address: 48h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	ResetIB	ResetDB	Reserved	TSTP1	TSTP0
TYPE:	R/W	Reserved	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	1	0	0	0

TSTP[1:0] (bits 1:0) of **Register RES** enable and select test pattern generation (color bar, ramp). The pattern generated is determined by the table below:

Table 17: Test Pattern Selection

TSTP1	TSTP0	Test Pattern
0	0	No test pattern – Input data is used
0	1	Color Bars
1	0	Horizontal Luminance Ramp
1	1	Black Screen

ResetDB (bit 3) of **Register RES** resets the datapath. When ResetDB is '0' the datapath is reset. When ResetDB is '1' the datapath is enabled. The datapath is also reset at power on by an internally generated power-on-reset signal.

ResetIB (bit 4) of **Register RES** resets all control registers. When ResetIB is '0' the control registers are reset to the default values. When ResetIB is '1' the control registers operate normally. The control registers are also reset at power on by an internally generated power on reset signal.

Power Management Register **Symbol: PM**
Address: 49h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	DVIP	DVIL	Reserved	Reserved	DACPD2	DACPD1	DACPD0	FPD
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	1

FPD (bit 0) of **Register PM** controls power down of the entire chip except the serial port. When FPD is '1' the entire chip is in power down mode.

DACPD[2:0] (bits 3:1) of **Register PM** control DAC0 through DAC2 Power Down. DAC0 through DAC2 will be turned on only if FD bit is set to '0'. If FPD bit is set to '1', then DAC0 through DAC2 will be in power down state regardless of DACPD0 through DACPD2 state.

Table 18: DAC Power Down Control

FPD	DACPD[2:0]	Operating State	Functional Description
0	000	Normal (On)	All DACs on
0	001		DAC 0 powered down, DACs 1, 2 on
0	010		DAC 1 powered down, DACs 0, 2 on
0	100		DAC 2 powered down, DACs 0, 1 on
1	xxx	Full Power Down	All circuitry is powered down except serial port

Bit 7 – 6 of the PM register control the DVI path. A summary of the various bit operations for **Register 49h** is shown in the table below.

DVIP	DVIL	TV	DACPD[2:0]	FPD	Operating State	Functional Description
X	X	1	000	0	YPrPb On	Y Pr and Pb DACs on
1	1	X	XXX	0	DVI Encoder, Serializer, Transmitter and PLL on	DVI is in normal operation
X	X	X	XXX	1	Full Power Down	All circuitry powered down except serial port

Version ID Register **Symbol: VID**
Address: 4Ah

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	**Note**	0	0	0	0	0	0	0

Note: For CH7302 this bit is 0, for CH7303 this bit is 1.

Register VID is a read only register containing the version ID number of the CH7302/CH7303 family.

Product Number	Version ID
CH7302	00h
CH7303	80h

Device ID Register **Symbol: DID**
Address: 4Bh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	0	0	1	1	1	0	0	**Note**

Note: For CH7302 this bit is 0, for CH7303 this bit is 1.

Register DID is a read only register containing the device ID number of the CH7302/CH7303 family.

Product Number	Function	Device ID
CH7302	Single DVI Transmitter and HDTV without Macrovison	38h
CH7303	Single DVI Transmitter and HDTV with Macrovison	39h

DVI Sync Polarity Register **Symbol: DSP**
Address: 56h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	TMSYO	Reserved	Reserved	Reserved	Reserved	T_RGB
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

T_RGB (bit 0) of register DSP enables the YCrCb to RGB color space conversion
T_RGB = 0 => Disable YCrCb to RGB conversion
= 1 => Enable YCrCb to RGB conversion

TMSYO (bit 5) of register DSP determines the polarity of embedded sync for DVI, if 0, flip H, V for DVI.

4.0 Electrical Specifications

4.1 Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
	All power supplies relative to GND	-0.5		5.0	V
	Input voltage of all digital pins	GND – 0.5		VDD + 0.5	V
T_{SC}	Analog output short circuit duration		Indefinite		Sec
T_{AMB}	Ambient operating temperature	0		85	°C
T_{STOR}	Storage temperature	-65		150	°C
T_J	Junction temperature			150	°C
T_{VPS}	Vapor phase soldering (1 minute)			220	°C

Note:

1) Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2) The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5V can induce destructive latchup.

4.2 Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
AVDD	PLL Power Supply Voltage	3.1	3.3	3.6	V
DAC_VDD	DAC Power Supply Voltage	3.1	3.3	3.6	V
DVDD	Digital Power Supply Voltage	3.1	3.3	3.6	V
VDD	Generic for all of the above supplies	3.1	3.3	3.6	V
VDDV	I/O Power Supply Voltage	1.1	1.8	3.6	V
R_L	Output load to DAC Outputs		37.5		Ω
	Ambient operating temperature	0		70	°C

4.3 Electrical Characteristics

(Operating Conditions: T_A = 0°C – 70°C, VDD =3.3V ± 5%)

Symbol	Description	Min	Typ	Max	Units
	Video D/A Resolution	10	10	10	bits
	Full scale output current		33.9		mA
	Video level error			10	%
I_{VDD}	Total supply current		345	440	mA
I_{VDDV}	VDDV (1.8V) current (15pF load)		4		mA
I_{PD}	Total Power Down Current		0.06		mA

4.4 DC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
V_{SDOL}	SPD (serial port data) Output Low Voltage	I_{OL} = 2.0 mA			0.4	V
V_{SPIH}	Serial Port (SPC, SPD) Input High Voltage		1.0		VDD + 0.5	V
V_{SPIL}	Serial Port (SPC, SPD) Input Low Voltage		GND-0.5		0.4	V
V_{HYS}	Hysteresis of Inputs		0.25			V
V_{DATAIH}	D[0-15] Input High Voltage		Vref+0.25		DVDD+0.5	V
V_{DATAIL}	D[0-15] Input Low Voltage		GND-0.5		Vref-0.25	V
V_{MISCIH}	GPIOx, RESET*, AS, HPDET Input High Voltage	DVDD=3.3V	2.7		VDD + 0.5	V
V_{MISCIL}	GPIOx, RESET*, AS, HPDET Input Low Voltage	DVDD=3.3V	GND-0.5		0.6	V
I_{MISCPU}	Pull Up Current (GPIO, RESET*, AS)	V_{IN} = 0V	0.5		5.0	uA
I_{MISCPD}	Pull Down Current (HPDET)	V_{IN} = 3.3V	0.5		5.0	uA
V_{MISCOH}	GPIOx, VSYNC, HSYNC Output High Voltage	I_{OH} = -0.4mA	DVDD-0.2			V
V_{MISCOL}	GPIOx, VSYNC, HSYNC Output Low Voltage	I_{OL} = 3.2mA			0.2	V

Note :

V_{DATA} - refers to all digital data (D[15:0]), clock (XCLK, XCLK*), sync (H, V) and DE inputs. V_{MISC} - refers to GPIOx, RESET*, AS and HPDET inputs and GPIOx, VSYNC and HSYNC outputs.

4.5 AC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
f_{XCLK}	Input (XCLK) frequency		25		165	MHz
t_{PIXEL}	Pixel time period		6.06		40	ns
DC_{XCLK}	Input (XCLK) Duty Cycle	$T_S + T_H < 1.2ns$	30		70	%
t_{XJIT}	XCLK clock jitter tolerance			2		ns
t_{DVIR}	DVI Output Rise Time (20% - 80%)	f_{XCLK} = 165MHz	75		242	ps
t_{DVIF}	DVI Output Fall Time (20% - 80%)	f_{XCLK} = 165MHz	75		242	ps
t_{SKDIFF}	DVI Output intra-pair skew	f_{XCLK} = 165MHz			90	ps
t_{SKCC}	DVI Output inter-pair skew	f_{XCLK} = 165MHz			1.2	ns
t_{DVIJIT}	DVI Output Clock Jitter	f_{XCLK} = 165MHz			150	ps
t_S	Setup Time: D[11:0], H, V and DE to XCLK, XCLK*	XCLK = XCLK* to D[11:0], H, V, DE = Vref	0.50			ns
t_H	Hold Time: D[11:0], H, V and DE to XCLK, XCLK*	D[11:0], H, V, DE = Vref to XCLK = XCLK*	0.50			ns
t_R	H and V (when configured as outputs) Output Rise Time (20% - 80%)	15pF load VDDV = 3.3V			1.50	ns
t_F	H and V (when configured as outputs) Output Fall Time (20% - 80%)	15pF load VDDV = 3.3V			1.50	ns
t_{STEP}	De-skew time increment		50		80	ps

4.6 Timing Information

4.6.1 Clock - Slave, Sync - Slave Mode

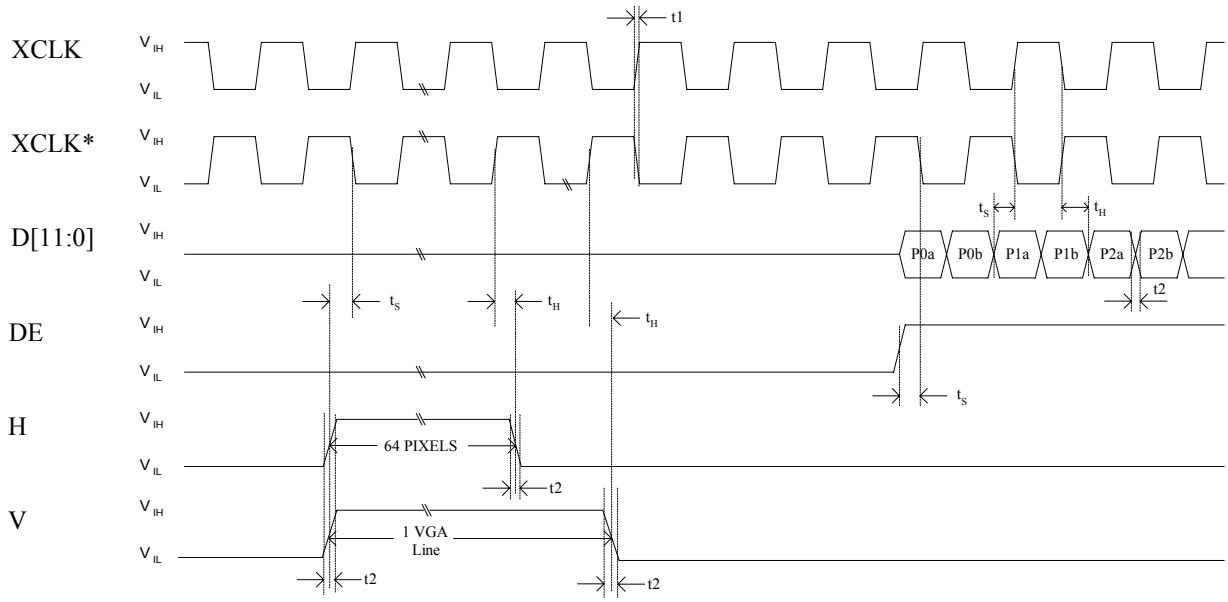

Figure 5: Timing for Clock - Slave, Sync - Slave Mode

Table 19: Timing for Clock - Slave, Sync - Slave Mode

Symbol	Parameter	Min	Typ	Max	Unit
t_S	Setup Time: D[11:0], H, V and DE to XCLK, XCLK*	see **section 4.5**			
t_H	Hold Time: D[11:0], H, V and DE to XCLK, XCLK*	see **section 4.5**			
t1	XCLK & XCLK* rise/fall time w/15pF load		1		ns
t2	D[11:0], H, V & DE rise/fall time w/ 15pF load		1		ns

5.0 Package Dimensions

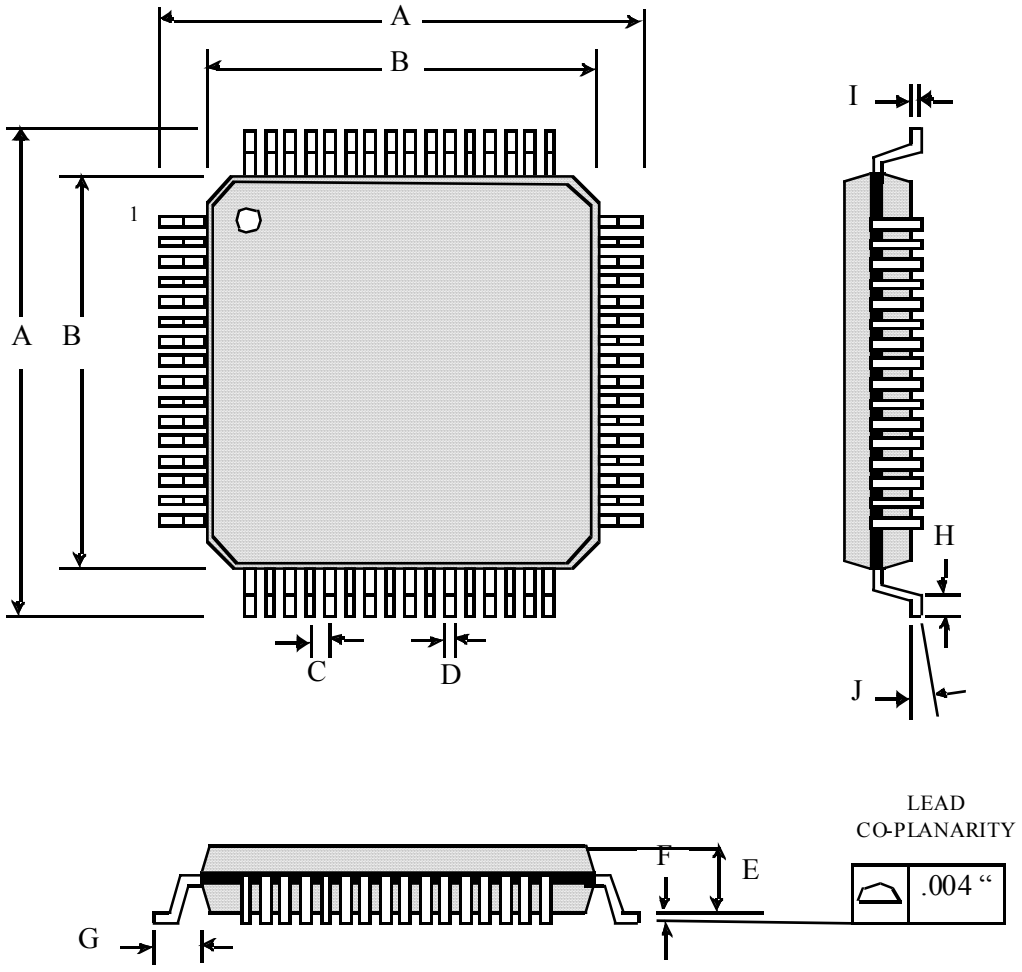

Table of Dimensions

No. of Leads		SYMBOL									
64 (10 X 10 mm)		A	B	C	D	E	F	G	H	I	J
Milli-meters	MIN	12	10	0.50	0.17	1.35	0.05	1.00	0.45	0.09	0°
	MAX				0.27	1.45	0.15		0.75	0.20	7°

Figure 6: 64 Pin LQFP Package

6.0 Revision History

Revision #	Date	Section	Description
1.0	3/11/2003	All	First official release
1.1	4/24/2003	Figure 2	Changed pin out configurations.
		Figure 1	Added 'AS' to Figure 1
		General Description	Revised description
	6/23/03		Table of Contents Added
1.11	7/10/03	Figure 1	Added reset control block
		Table 5	Added modes to Table 5
1.12	7/12/04	Register 1Eh	Updated DVI hotplug description
1.13	1/11/07	Register 4Bh, page24	Corrected function description in the Register 4Bh table.
		Ordering Information	Removed Voltage Supply: 2.5V.
2.0	1/17/07	All	Combined CH7302 and CH7303.
2.1	5/21/07	3.0	Corrected Application note reference.

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ORDERING INFORMATION

Part Number	Package Type	Number of Pins	Voltage Supply
CH7302A-TF	Lead Free - LQFP	64	3.3V
CH7302A-TF-TR	Lead Free - Tape and Reel LQFP	64	3.3V
CH7303A-TF	Lead Free - LQFP	64	3.3V
CH7303A-TF-TR	Lead Free - Tape and Reel LQFP	64	3.3V

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