Am25S10

Four-Bit Shifter with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

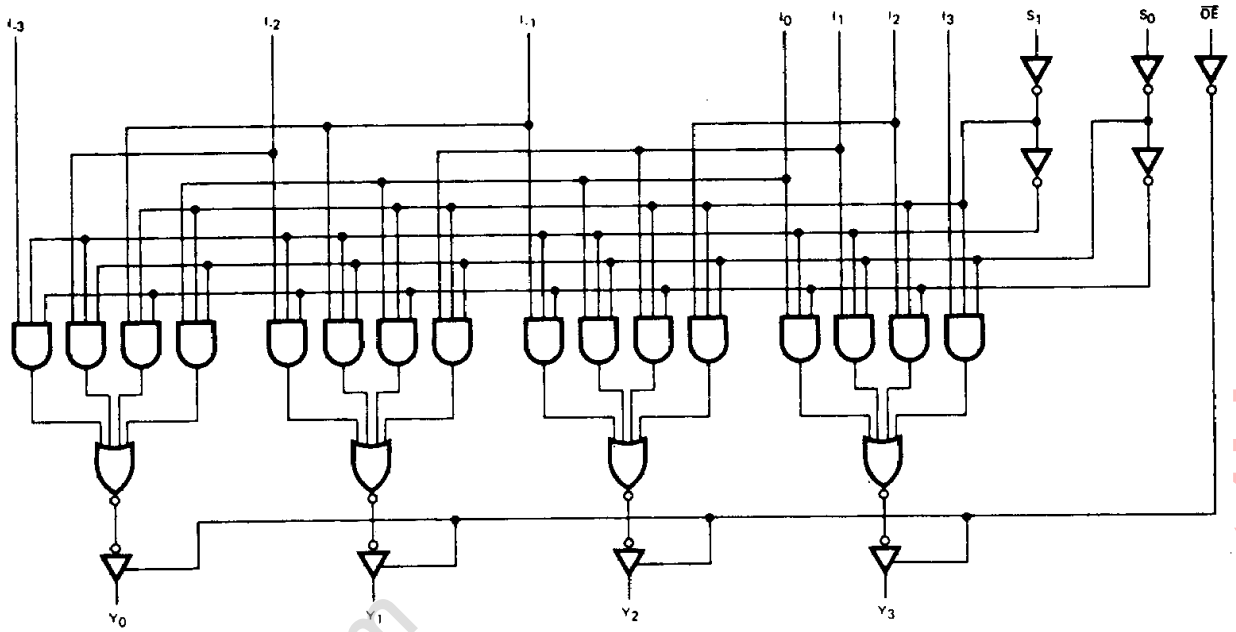
- Shifts 4-bits of data to 0, 1, 2 or 3 places under control of two select lines.
- Three-state outputs for bus organized systems.
- 6.5ns typical data propagation delay
- Alternate source is 54S/74S350

GENERAL DESCRIPTION

The Am25S10 is a combinatorial logic circuit that accepts a four-bit data word and shifts the word 0, 1, 2 or 3 places. The number of places to be shifted is determined by a two-bit select field S_0 and S_1. An active-LOW enable controls the three-state outputs. This feature allows expansion of shifting over a larger number of places with one delay.

By suitable interconnection, the Am25S10 can be used to shift any number of bits any number of places up or down. Shifting can be logical, with logic zeroes pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continuous loop.

BLOCK DIAGRAM



BD002480

RELATED PRODUCTS

Part No.	Description
Am2901	Bit Slice ALU
Am2903	Superslice
Am29501	Multiport Pipeline Processor

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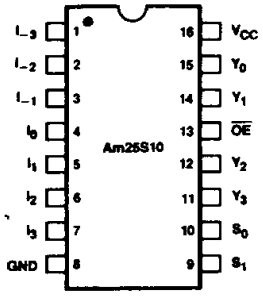
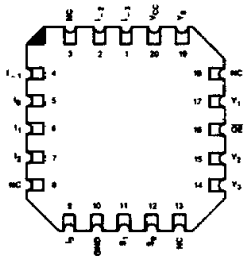
CONNECTION DIAGRAM
Top View

D-16, P-16



CD004060

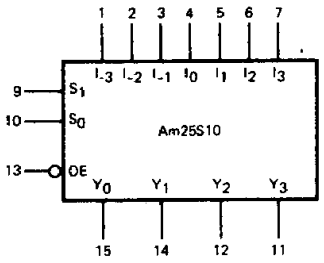
L-20-1



CD004050

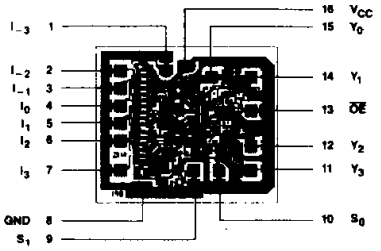
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000750

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.067" x 0.056"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25S10 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 16-pin CERDIP
  - F – 16-pin flatpak
  - L – 20-pin leadless chip carrier
  - P – 16-pin plastic DIP
  - X – Dice
- **Am25S10** — Device type
  - 4-Bit Shifter with Three-State Outputs

Valid Combinations	
Am25S10	PC DC, DM LC, LM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

9

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PIN DESCRIPTION

Pin No.	Name	I/O	Description
	I_i	I	The seven data inputs of the shifter.
13	$\overline{OE}$		Enable. When the enable is HIGH, the four outputs are in the high impedance state. When the enable is LOW, the selected I_i inputs are present at the outputs.
10, 9	S_0, S_1	I	Select inputs. Controls the number of places the inputs are shifted.
11, 12, 14, 15	Y_i	O	The four outputs of the shifter.

LOADING RULES (In Unit Loads)

Input/Output	Pin Nos.	Input Unit Load (Note 1)	Fan-out		
			Output HIGH		Output LOW
			XM	XC	
I-3	1	1	–	–	–
I-2	2	1.5	–	–	–
I-1	3	1.5	–	–	–
I_0	4	1.5	–	–	–
I_1	5	1.5	–	–	–
I_2	6	1.5	–	–	–
I_3	7	1	–	–	–
GND	8	–	–	–	–
S_1	9	1	–	–	–
S_0	10	1	–	–	–
Y_3	11	–	40	130	10
Y_2	12	–	40	130	10
$\overline{OE}$	13	1	–	–	–
Y_1	14	–	40	130	10
Y_0	15	–	40	130	10
V_{CC}	16	–	–	–	–

A Schottky TTL Unit Load is defined as 50μA at 2.7V at the HIGH and −2.0mA at 0.5V at the LOW.

Note 1. The fan-in on I_{-2}, I_{-1}, I_0, I_1 and I_2 will not exceed 1.5 Unit Loads when measured at $V_{IL} = 0.5V$. As V_{IL} is decreased to a 0V, the input current I_{IL} MAX. increases to −4, −6, −8, −6 and −4mA respectively due to the decrease in current sharing with the internal select buffer outputs.

LOGIC EQUATIONS

$$Y_0 = \overline{S}_0\overline{S}_1 I_0 + S_0\overline{S}_1 I_{-1} + \overline{S}_0 S_1 I_{-2} + S_0 S_1 I_{-3}$$

$$Y_1 = \overline{S}_0\overline{S}_1 I_1 + S_0\overline{S}_1 I_0 + \overline{S}_0 S_1 I_{-1} + S_0 S_1 I_{-2}$$

$$Y_2 = \overline{S}_0\overline{S}_1 I_2 + S_0\overline{S}_1 I_1 + \overline{S}_0 S_1 I_0 + S_0 S_1 I_{-1}$$

$$Y_3 = \overline{S}_0\overline{S}_1 I_3 + S_0\overline{S}_1 I_2 + \overline{S}_0 S_1 I_1 + S_0 S_1 I_0$$

TRUTH TABLE

$\overline{OE}$	S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_3	Y_2	Y_1	Y_0
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
L	L	L	D_3	D_2	D_1	D_0	X	X	X	D_3	D_2	D_1	D_0
L	L	H	X	D_2	D_1	D_0	D_{-1}	X	X	D_2	D_1	D_0	D_{-1}
L	H	L	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_1	D_0	D_{-1}	D_{-2}
L	H	H	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_0	D_{-1}	D_{-2}	D_{-3}

H = HIGH
L = LOW

X = Don't Care
Z = High Impedance State

D_n at input I_n may be either HIGH or LOW and output Y_m will follow the selected D_n input level.

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Refer to Page 13-1 for Essential Information on Military Devices

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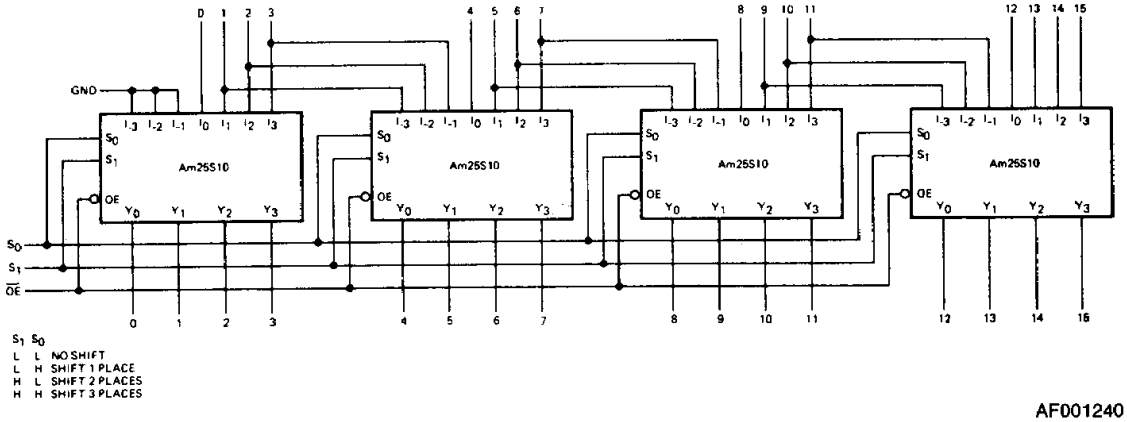
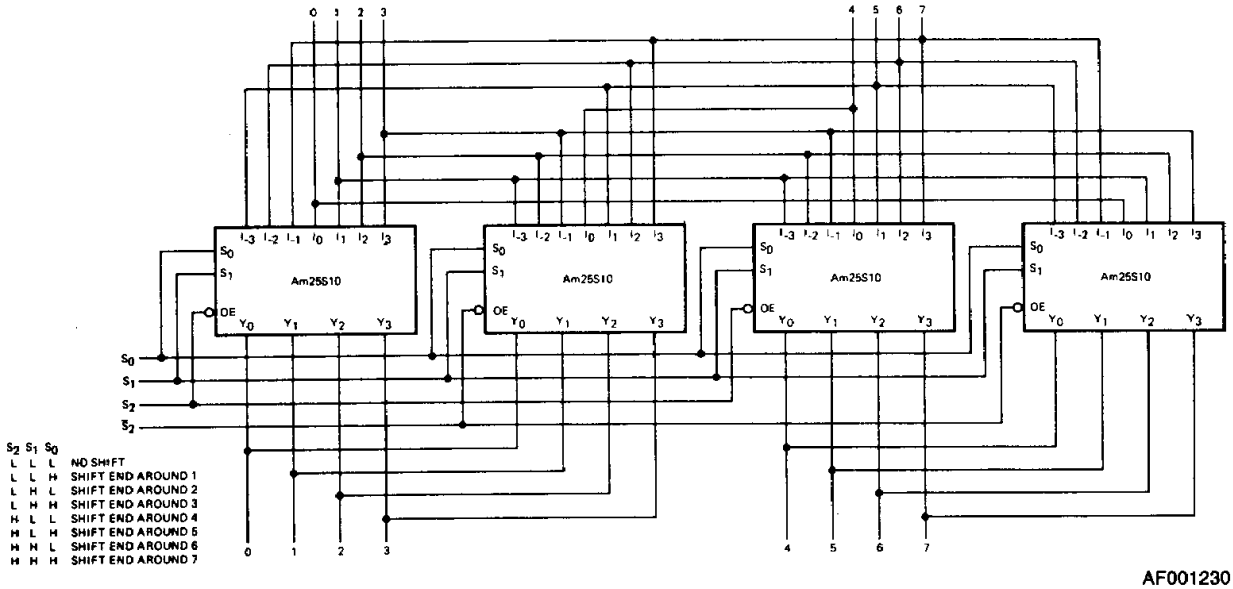
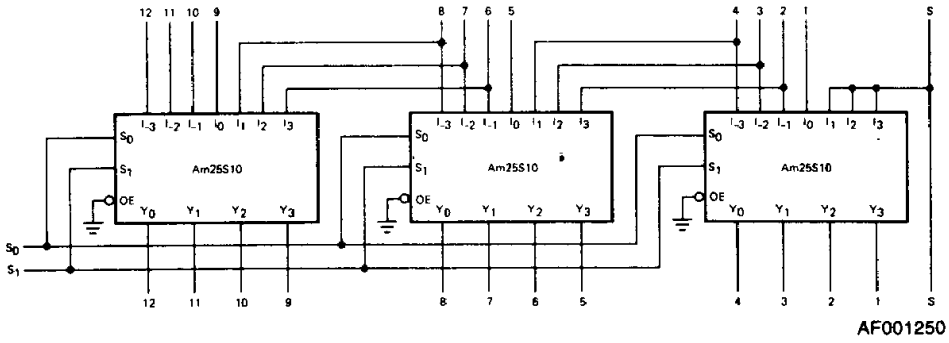
APPLICATIONS



16-Bit Shift-Up 0, 1, 2, or 3 Places.



8-Bit End Around Shift 0, 1, 2, 3, 4, 5, 6, 7 Places



13-Bit 2's Complement Scaler

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

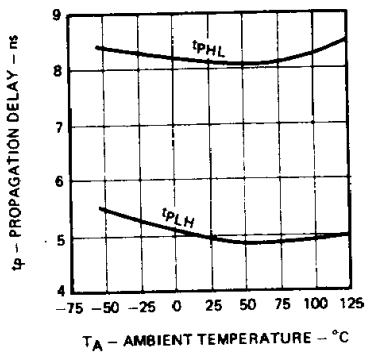
DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	XM I_{OH} = −2mA	2.4	3.4		Volts
			XC I_{OH} = −6.5mA	2.4	3.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V				−2.0	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				50	µA
I_O	Off State (High Impedance) Output Current	V_{CC} = MAX.	V_O = 2.4V			50	µA
			V_O = 0.5V			−50	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All outputs open, All inputs = GND			60	85	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN. or MAX., use the appropriate value specified under Operating Ranges for the applicable device type.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

PERFORMANCE CURVES
SWITCHING CHARACTERISTICS

Data to Output (Typical)



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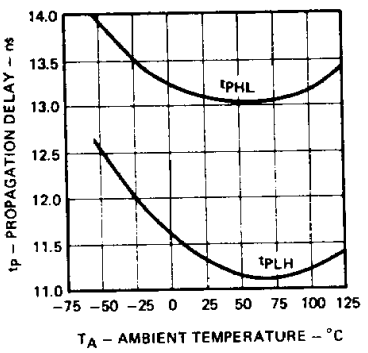
Select to Output (Typical)



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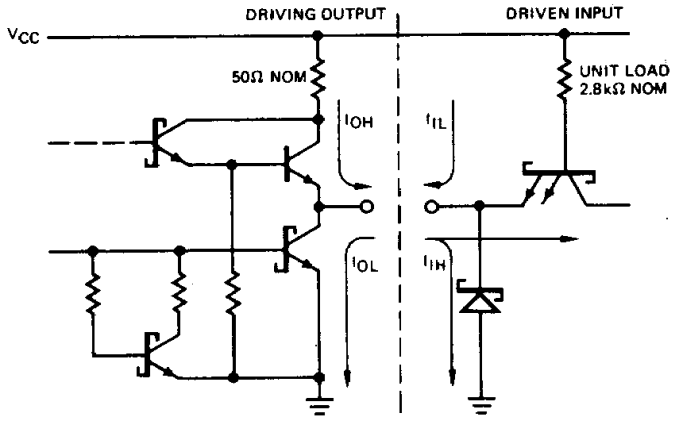
SWITCHING CHARACTERISTICS (T_A = +25°C)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Data Input to Output	V_{CC} = 5.0V, C_L = 15pF, R_L = 280Ω		5	7.5	ns
t_{PHL}				8	12	
t_{PLH}	Select to Output			11	17	ns
t_{PHL}				13	20	
t_{ZH}	Output Control $\overline{OE}$ to Output				19.5	ns
t_{ZL}					21	
t_{HZ}	Output Control $\overline{OE}$ to Output	V_{CC} = 5V, C_L = 5pF, R_L = 280Ω		5	8	ns
t_{LZ}				10	15	

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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