AK5353

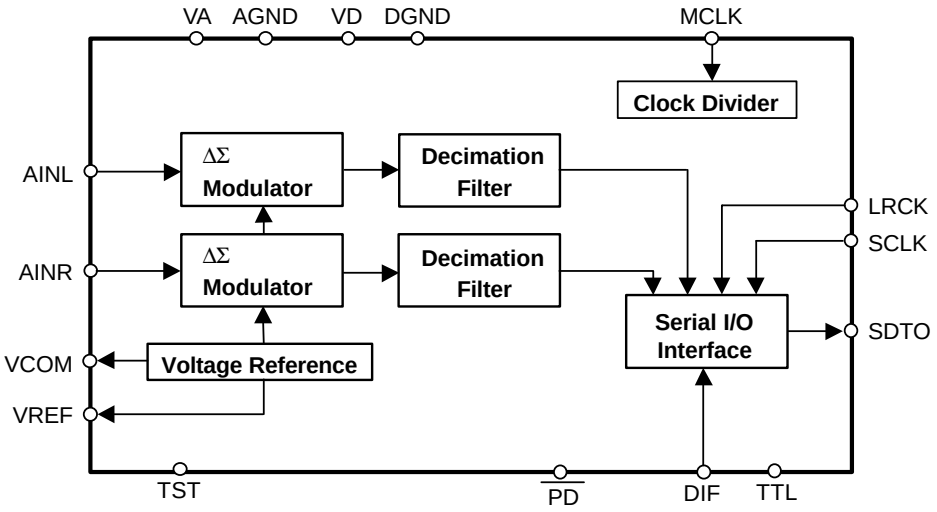
96kHz 24Bit ΔΣ ADC with Single–ended Input

GENERAL DESCRIPTION

The AK5353 is a stereo A/D Converter with wide sampling rate of 4kHz~96kHz and is suitable for multimedia audio system. The AK5353 achieves high accuracy and low cost by using Enhanced dual bit ΔΣ techniques. The AK5353 requires no external components because the analog inputs are single-ended. The audio interface has two formats (MSB justified, I^2S) and can correspond to many systems like Karaoke, surround.

FEATURES

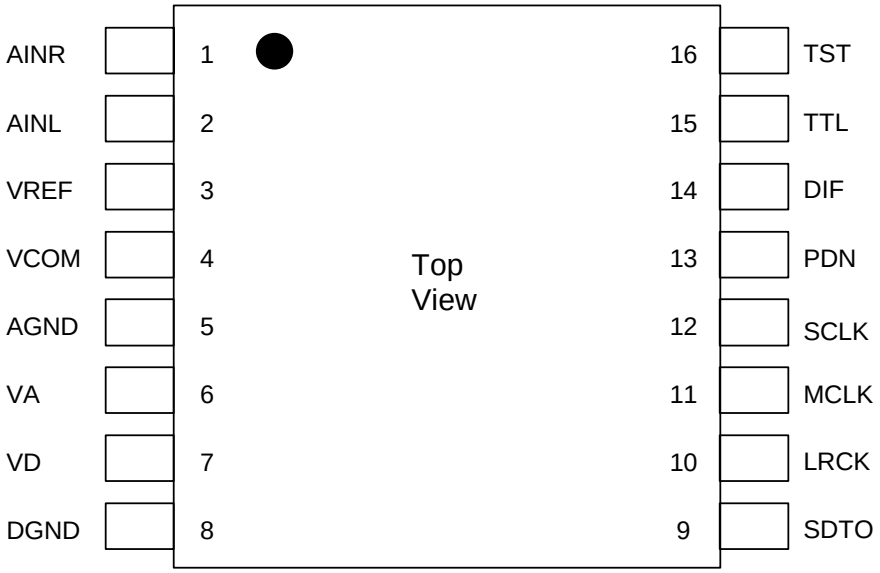
- ☐ **Stereo ΔΣ ADC**
- ☐ **On-Chip Digital Anti-Alias Filtering**
- ☐ **Single-ended Input**
- ☐ **Digital HPF for DC-Offset cancel**
- ☐ **S/(N+D): 84dB@5V, 80dB@3V for 48kHz**
- ☐ **DR: 96dB@5V, 92dB@3V for 48kHz**
- ☐ **S/N: 96dB@5V, 92dB@3V for 48kHz**
- ☐ **Sampling Rate Ranging from 4kHz to 96kHz**
- ☐ **Master Clock:**
  256fs/384fs/512fs (~48kHz)
  256fs/384fs (~96kHz)
- ☐ **Low Power Dissipation: 70mW**
- ☐ **Small 16pin TSSOP Package**
- ☐ **Power Supply: 2.7~5.5V (~48kHz)**
  4.5~5.5V (~96kHz)
- ☐ **Ta=-40~85°C**
- ☐ **Input level: TTL/CMOS selectable**
- ☐ **Output format: 24bit MSB justified / I^2S selectable**



■ Ordering Guide

AK5353VT	-40~+85°C	16pin TSSOP
AKD5353	Evaluation Board	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Description
1	AINR	I	Rch Analog Input Pin
2	AINL	I	Lch Analog Input Pin
3	VREF	O	Voltage Reference Output Pin Normally connected to AGND with a 0.1uF ceramic capacitor in parallel with an electrolytic capacitor less than 4.7uF.
4	VCOM	O	Common Voltage Output Pin Normally connected to AGND with a 0.1uF ceramic capacitor in parallel with an electrolytic capacitor less than 4.7uF.
5	AGND	-	Analog Ground Pin, 0V
6	VA	-	Analog Power Supply Pin, +2.7~+5.5V
7	VD	-	Digital Power Supply Pin, +2.7~+5.5V
8	DGND	-	Digital Ground Pin, 0V
9	SDTO	O	Serial Data Output Pin Data bits are presented MSB first, in 2 s complement format. This pin is L in the power-down mode.
10	LRCK	I	Left/Right Channel Select Pin The fs clock is input to this pin.
11	MCLK	I	Master Clock Input Pin
12	SCLK	I	Serial Data Input Pin Output data is clocked out on the falling edge of SCLK.
13	PDN	I	Power-Down Pin When L , the circuit is in power-down mode. The AK5353 should always be reset upon power-up.
14	DIF	I	Serial Interface Format Pin L : MSB justified, H : I^2S
15	TTL	I	Digital Input Level Select Pin L : CMOS level (VA,VD=2.7~5.5V), H : TTL level (VA,VD=4.5~5.5V)
16	TST	I	Test Pin (Internal pull-down pin) This pin should be left floating.

Note: All input pins except pull-down pins should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(AGND, DGND=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies	Analog (VA pin)	VA	-0.3	6.0	V
	Digital (VD pin)	VD	-0.3	6.0	V
	|AGND-DGND|	ΔGND	-	0.3	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage (AINL, AINR pins)		VINA	-0.3	VA+0.3	V
Digital Input Voltage		VIND	-0.3	VD+0.3	V
Ambient Temperature		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

Note:1. All voltages with respect to ground.
2. AGND and DGND must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may results in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (fs=48kHz)

(AGND, DGND=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog	VA	2.7	5.0	5.5	V
(Note 3)	Digital	VD	2.7	5.0	VA	V
Sampling Rate		fs	4		48	kHz

Note:1. All voltages with respect to ground.
3. The power up sequence between VA and VD is not critical.

RECOMMENDED OPERATING CONDITIONS (fs=96kHz)

(AGND, DGND=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog	VA	4.5	5.0	5.5	V
(Note 3)	Digital	VD	4.5	5.0	VA	V
Sampling Rate		fs	4		96	kHz

Note:1. All voltages with respect to ground.
3. The power up sequence between VA and VD is not critical.

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VA,VD=5V; fs=48kHz; I/F format=Mode 0; Signal Frequency =1kHz;
Measurement band width=20Hz~20kHz; unless otherwise specified)

Parameter		min	typ	max	Units
ADC Analog Input Characteristics: Analog source impedance=470Ω (BW=40Hz~40kHz at fs=96kHz)					
Resolution				24	Bits
S/(N+D) (-1dBFS) (Note 4)	fs=48kHz, VA=5V	76	84		dB
	fs=48kHz, VA=3V	76	84		dB
	fs=96kHz, VA=5V	-	84		dB
DR (-60dBFS) (Note 5)	fs=48kHz, VA=5V, A-weighted	90	96		dB
	fs=48kHz, VA=3V, A-weighted	86	92		dB
	fs=96kHz, VA=5V	-	93		dB
S/N	fs=48kHz, VA=5V, A-weighted	90	96		dB
	fs=48kHz, VA=3V, A-weighted	86	92		dB
	fs=96kHz, VA=5V	-	93		dB
Interchannel Isolation		78	90		dB
DC Accuracy					
Interchannel Gain Mismatch			0.1	0.3	dB
Gain Drift			100	150	ppm/°C
Input Voltage	(Note 6)	2.7	3.0	3.3	Vpp
Input Resistance	(Note 7)	40	60		kΩ
Power Supply Rejection	(Note 8)	-	30		dB
Power Supplies					
Power Supply Current					
Normal Operation (PDN= H)					
VA+VD	(Note 9)		14	21	mA
Power-Down Mode (PDN= L)					
VA+VD			10	100	μA

Note: 4. The ratio of the rms value of the signal to the rms sum of all the spectral components less than 20kHz bandwidth, including distortion components.
5. S/(N+D) which is measured with an input signal of -60dB below full-scale.
6. This value is the full scale(0dB) of the input voltage.
Input voltage is proportional to VA. (Vin=0.6xVA)
7. 40kΩ(typ) and 25kΩ(min) at fs=96kHz.
8. PSR is applied to VA,VD with 1kHz, 50mVpp.
9. VA=11mA; VD=3mA@48kHz,5V, 1.5mA@48kHz,3V, 6mA@96kHz,5V (typ).

FILTER CHARACTERISTICS (fs=48kHz)

(Ta=25°C; VA,VD=2.7~5.5V; fs=48kHz)

Parameter		Symbol	min	typ	max	Units
Digital Filter (Decimation LPF)						
Passband (Note 10)	±0.1dB	PB	0		18.9	kHz
	-0.2dB		-	20.0	-	kHz
	-1.0dB		-	21.8	-	kHz
	-3.0dB		-	23.0	-	kHz
Stopband (Note 10)		SB	29.4			kHz
Stopband Attenuation		SA	65			dB
Group Delay Distortion		ΔGD		0		μs
Group Delay (Note 11)		GD	-	17.0	-	1/fs
Digital Filter (HPF)						
Frequency Response:	-3 dB	FR	-	4	-	Hz
	-0.5dB		-	11	-	Hz
	-0.1dB		-	24	-	Hz

Note:10. The passband and stopband frequencies scale with fs.

11. The calculating delay time which occurred by digital filtering. This time is from the input of analog signal to setting the 24bit data of both channels to the output register for ADC.

FILTER CHARACTERISTICS (fs=96kHz)

(Ta=25°C; VA,VD=4.5~5.5V; fs=96kHz)

Parameter		Symbol	min	typ	max	Units
Digital Filter (Decimation LPF)						
Passband (Note 10)	±0.1dB	PB	0		37.8	kHz
	-0.2dB		-	40.0	-	kHz
	-1.0dB		-	43.6	-	kHz
	-3.0dB		-	46.0	-	kHz
Stopband (Note 10)		SB	58.8			kHz
Stopband Attenuation		SA	65			dB
Group Delay Distortion		ΔGD		0		μs
Group Delay (Note 11)		GD	-	17.0	-	1/fs
Digital Filter (HPF)						
Frequency Response:	-3 dB	FR	-	8	-	Hz
	-0.5dB		-	22	-	Hz
	-0.1dB		-	48	-	Hz

Note:10. The passband and stopband frequencies scale with fs.

11. The calculating delay time which occurred by digital filtering. This time is from the input of analog signal to setting the 24bit data of both channels to the output register for ADC.

DIGITAL CHARACTERISTICS (CMOS level input)

(Ta=25°C; VA,VD=2.7~5.5V; TTL= L)

Parameter	Symbol	min	typ	Max	Units
High-Level input voltage	VIH	0.7xVD	-	-	V
Low-Level input voltage	VIL	-	-	0.3xVD	V
High-Level output voltage (Iout= -100μA)	VOH	VD-0.5	-	-	V
Low-Level output voltage (Iout= 100μA)	VOL	-	-	0.5	V
Input leakage current (exclude TST pin)	Iin	-	-	±10	μA

DIGITAL CHARACTERISTICS (TTL level input; except for TTL pin)

(Ta=25°C; VA,VD=4.5~5.5V; TTL= H)

Parameter	Symbol	min	typ	Max	Units
High-Level input voltage (TTL pin)	VIH	0.7xVD	-	-	V
(All pins except for TTL pin)	VIH	2.2	-	-	V
Low-Level input voltage (TTL pin)	VIL	-	-	0.3xVD	V
(All pins except for TTL pin)	VIL	-	-	0.8	V
High-Level output voltage (Iout= -100μA)	VOH	VD-0.5	-	-	V
Low-Level output voltage (Iout= 100μA)	VOL	-	-	0.5	V
Input leakage current (exclude TST pin)	Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS (VA,VD=4.5~5.5V)

(Ta=25°C; VA,VD=4.5~5.5V; C_L=20pF)

Parameter		Symbol	min	typ	max	Units
Control Clock Frequency						
Master Clock 256fs:		fCLK	1.024	12.288	24.576	MHz
Pulse Width Low		tCLKL	16			ns
Pulse Width High		tCLKH	16			ns
384fs:		fCLK	1.536	18.432	36.864	MHz
Pulse Width Low		fCLKL	10			ns
Pulse Width High		fCLKH	10			ns
512fs:		fCLK	2.048	24.576	24.576	MHz
Pulse Width Low		fCLKL	16			ns
Pulse Width High		fCLKH	16			ns
SCLK Frequency		fSLK			6.144	MHz
LRCK Frequency		fs	4	48	96	kHz
Serial Interface Timing	(Note 12)					
SCLK Period		tSLK	160			ns
SCLK Pulse Width Low		tSLKL	65			ns
Pulse Width High		tSLKH	65			ns
LRCK Edge to SCLK ↑	(Note 13)	tLRSH	30			ns
SCLK ↑ to LRCK Edge	(Note 13)	tSHLR	30			ns
LRCK Edge to SDTO Valid	(Note 14)	tDLR			50	ns
SCLK ↓ to SDTO Valid		tDSS			50	ns
Power-Down & Reset Timing						
PDN Pulse Width		tPDW	150			ns
PDN ↓ to SDTO delay	(Note 15)	tPDV		4129		1/fs

Note: 12. Refer to the operating overview section Serial Data Interface .
13. SCLK rising edge must not occur at the same time as LRCK edge.
14. In case of MSB justified format.
15. These cycles are the number of LRCK rising from PDN falling.

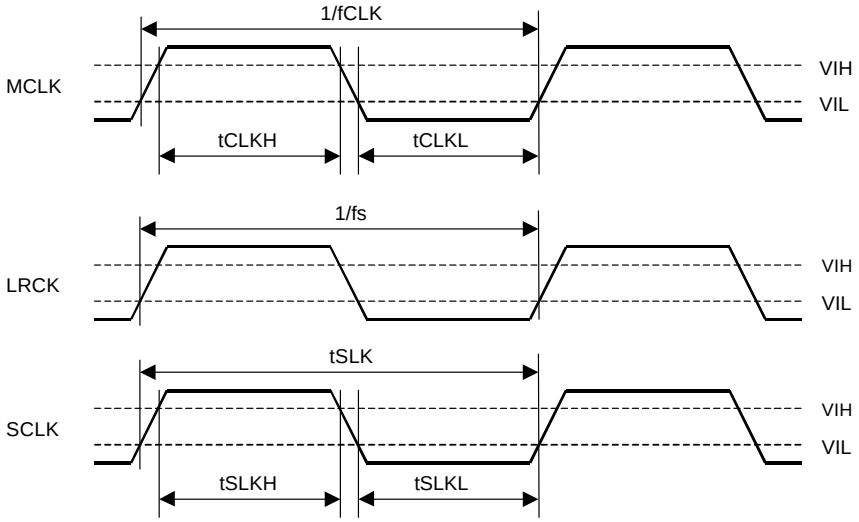
SWITCHING CHARACTERISTICS (VA,VD=2.7~4.5V)

(Ta=25°C; VA,VD=2.7~4.5V; C_L=20pF)

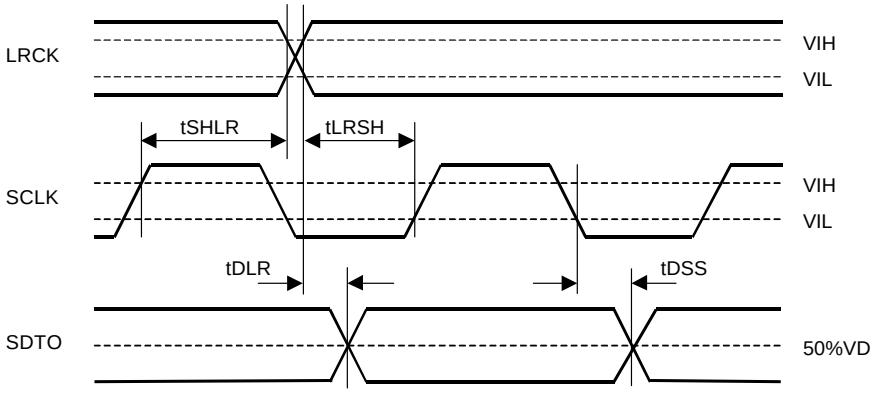
Parameter		Symbol	min	typ	max	Units
Control Clock Frequency						
Master Clock 256fs:		fCLK	1.024		12.288	MHz
Pulse Width Low		tCLKL	32			ns
Pulse Width High		tCLKH	32			ns
384fs:		fCLK	1.536		18.432	MHz
Pulse Width Low		fCLKL	21			ns
Pulse Width High		fCLKH	21			ns
512fs:		fCLK	2.048		24.576	MHz
Pulse Width Low		fCLKL	16			ns
Pulse Width High		fCLKH	16			ns
SCLK Frequency		fSLK			6.144	MHz
LRCK Frequency		fs	4		48	kHz
Serial Interface Timing	(Note 12)					
SCLK Period		tSLK	160			ns
SCLK Pulse Width Low		tSLKL	65			ns
Pulse Width High		tSLKH	65			ns
LRCK Edge to SCLK ↑	(Note 13)	tLRSH	30			ns
SCLK ↑ to LRCK Edge	(Note 13)	tSHLR	30			ns
LRCK Edge to SDTO Valid	(Note 14)	tDLR			50	ns
SCLK ↓ to SDTO Valid		tDSS			50	ns
Power-Down & Reset Timing						
PDN Pulse Width		tPDW	150			ns
PDN ↓ to SDTO delay	(Note 15)	tPDV		4129		1/fs

Note: 12. Refer to the operating overview section Serial Data Interface .
13. SCLK rising edge must not occur at the same time as LRCK edge.
14. In case of MSB justified format.
15. These cycles are the number of LRCK rising from PDN falling.

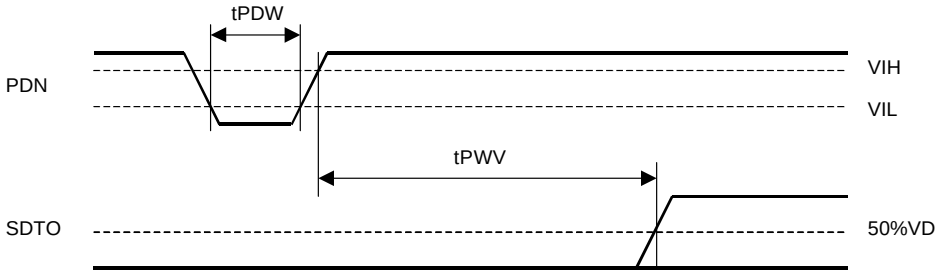
■ Timing Diagram



Clock Timing



Serial Interface Timing



Power-down & Reset Timing

OPERATION OVERVIEW

■ System Clock Input

The external clocks which are required to operate the AK5353 are MCLK(256fs/384fs/512fs), LRCK(1fs), SCLK. MCLK should be synchronized with LRCK but the phase is not critical. When 384fs or 512fs clock is input to MCLK pin, the internal master clock becomes 256fs(=384fs*2/3=512fs*1/2). Table 1 illustrates standard audio word rates and corresponding frequencies used in the AK5353.

All external clocks (MCLK,BICK,LRCK) should always be present whenever the AK5353 is in normal operation mode (PDN= H). If these clocks are not provided, the AK5353 may draw excess current and may not possibly operate properly because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK5353 should be in the power-down mode (PDN= L). After exiting reset at power-up etc., the AK5353 is in the power-down mode until MCLK and LRCK are input.

fs	MCLK			SCLK		
	256fs	384fs	512fs	32fs	64fs	128fs
32.0kHz	8.1920MHz	12.2880MHz	16.3840MHz	1.0240MHz	2.0480MHz	4.0960MHz
44.1kHz	11.2896MHz	16.9344MHz	22.5792MHz	1.4112MHz	2.8224MHz	5.6448MHz
48.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	1.5360MHz	3.0720MHz	6.1440MHz
96.0kHz	24.5760MHz	36.8640MHz	N/A	3.0720MHz	6.1440MHz	N/A

Table 1. Example of System Clock

■ Serial Data Interface

2 kinds of data format can be selected by DIF pin. The data is clocked out via the SDTO pin by SCLK corresponding to the setting of DIF pin. The format of output data is 2 s complement MSB first.

Mode	DIF	Format
0	0	24bit, MSB justified, L/R, SCLK ≥48fs (16bit, MSB justified, L/R, SCLK ≥32fs)
1	1	24bit, I2S, SCLK ≥48fs (16bit, I2S, SCLK ≥32fs)

Table 2. Audio Serial Interface Formats

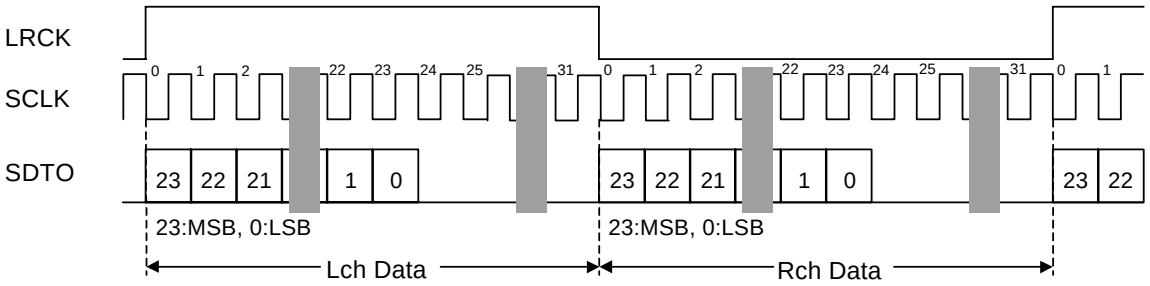


Figure 1. Mode 0 Timing

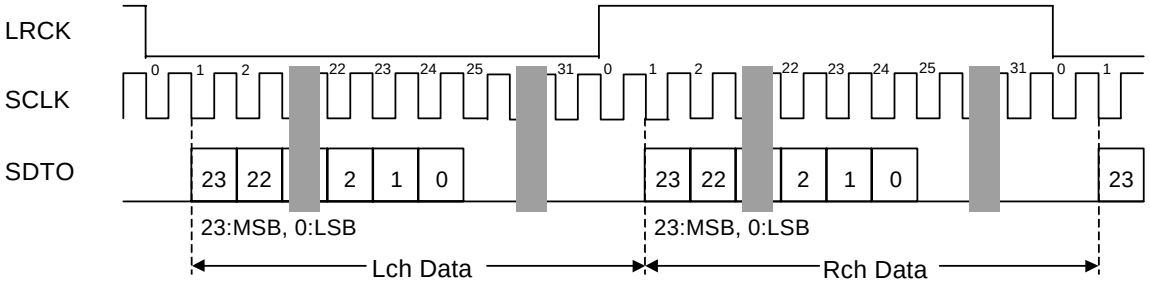
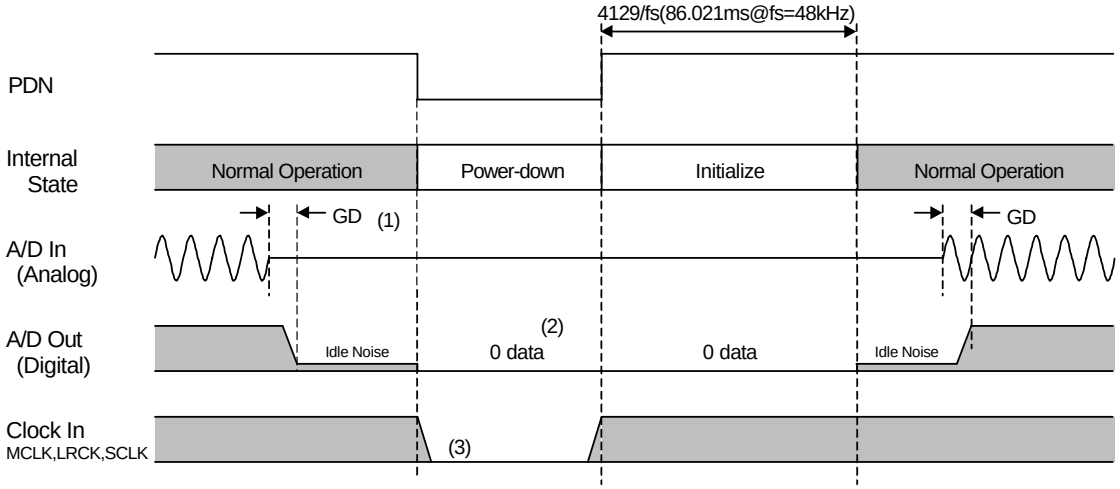


Figure 2. Mode 1 Timing

■ Power down

The AK5353 is placed in the power-down mode by bringing PDN L and the digital filter is also reset at the same time. This reset should always be done after power-up. In the power-down mode, the VREF and VCOM are AGND level. An analog initialization cycle starts after exiting the power-down mode. Therefore, the output data SDTO becomes available after 4129 cycles of LRCK clock. During initialization, the ADC digital data outputs of both channels are forced to a 2 s complement 0 . The ADC outputs settle in the data corresponding to the input signals after the end of initialization (Settling approximately takes the group delay time).



Notes:

(1) Digital output corresponding to analog input has the group delay (GD).

(2) A/D output is 0 data at the power-down state.

(3) When the external clocks (MCLK,SCLK,LRCK) are stopped, the AK5353 should be in the power-down state.

Figure 3. Power-down/up sequence example

■ System Reset

The AK5353 should be reset once by bringing PDN L after power-up. The internal timing starts clocking by the rising edge (falling edge at mode1) of LRCK upon exiting from reset.

SYSTEM DESIGN

Figure 4 shows the system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

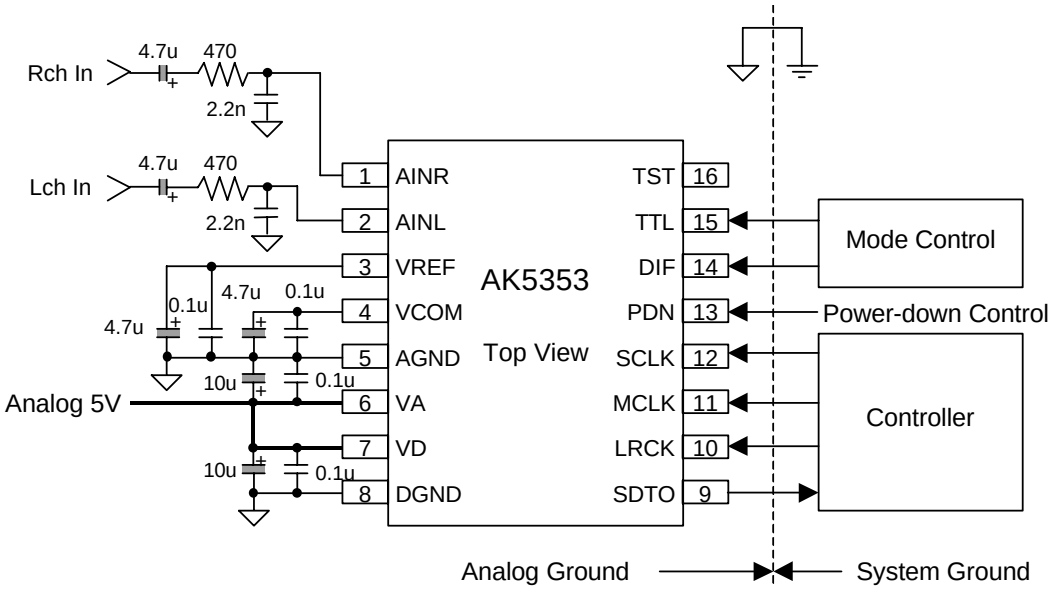


Figure 4. Typical Connection Diagram

Note: The value of electrolytic capacitor at VCOM depends on the low-frequency noise of power supply.

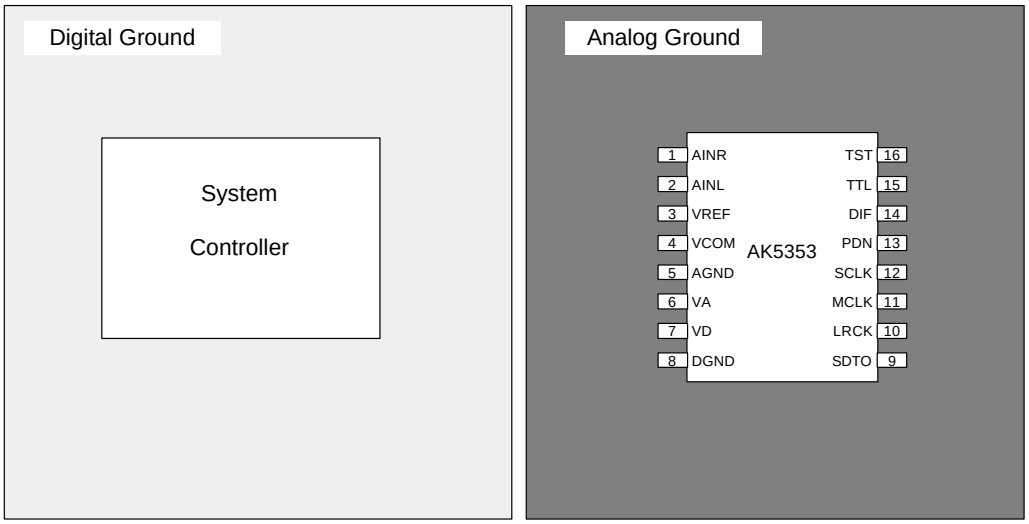


Figure 5. Ground Layout

Note: AGND and DGND must be connected to the same analog ground plane.

1. Grounding and Power Supply decoupling

The AK5353 requires careful attention to power supply and grounding arrangements. VA and VD are usually supplied from analog supply in system. Alternatively if VA and VD are supplied separately, the power up sequence is not critical. **AGND and DGND of the AK5353 must be connected to analog ground plane.** System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK5353 as possible, with the small value ceramic capacitor being the nearest.

2. On-chip voltage reference

The voltage input to VA sets the analog input range. VREF and VCOM are 55%VA and normally connected to VA with a 0.1uF ceramic capacitor. An electrolytic capacitor 10uF parallel with a 0.1uF ceramic capacitor attached to VREF and VCOM pins eliminates the effects of high frequency noise. No load current may be drawn from these pins. All signals, especially clocks, should be kept away from the VREF and VCOM pins in order to avoid unwanted coupling into the AK5353.

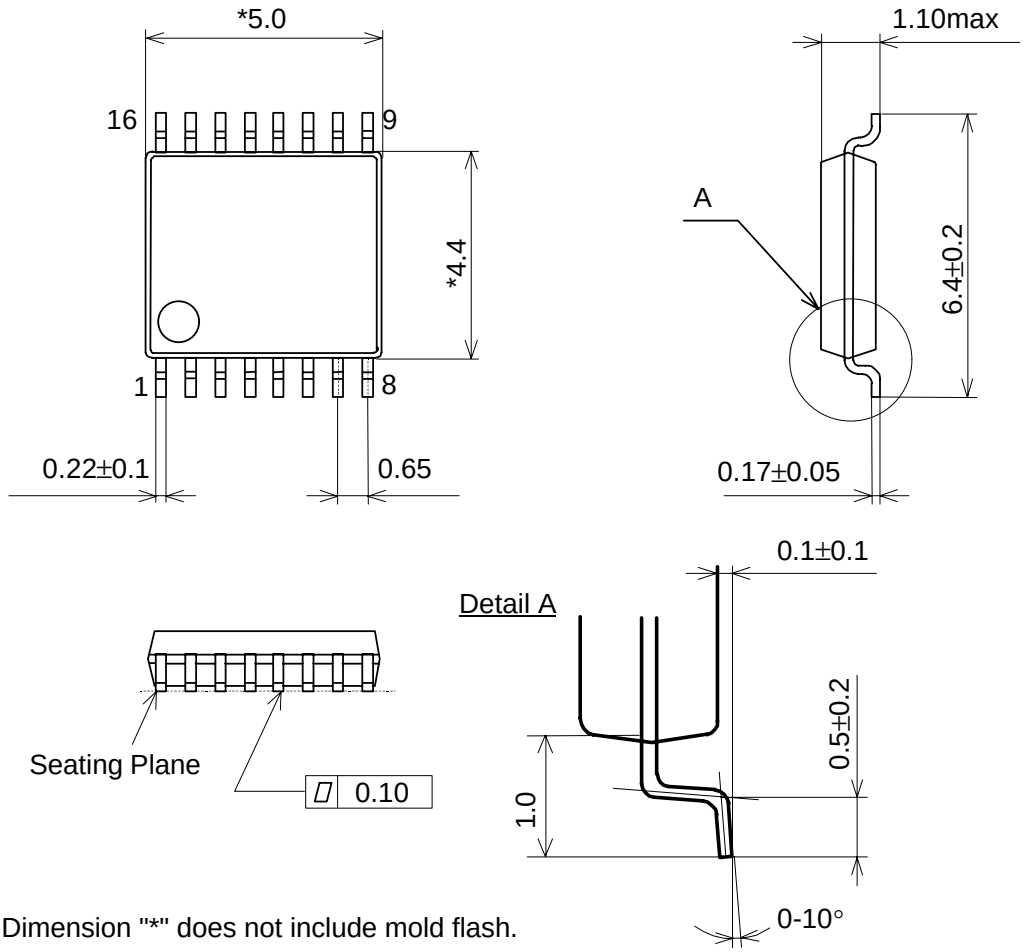
3. Analog Inputs

The ADC inputs are single-ended and internally biased to the common voltage (55%VA) with 100kΩ (typ) resistance. The input signal range scales with the supply voltage and nominally 0.6xVA Vpp. The ADC output data format is 2 s complement. The output code is 7FFFFFH(@24bit) for input above a positive full scale and 800000H(@24bit) for input below a negative full scale. The ideal code is 000000H(@24bit) with no input signal. The DC offset is removed by the internal HPF.

The AK5353 samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of 64fs. A simple RC filter (fc=150kHz) may be used to attenuate any noise around 64fs and most audio signals do not have significant energy at 64fs.

PACKAGE

16pin TSSOP (Unit: mm)

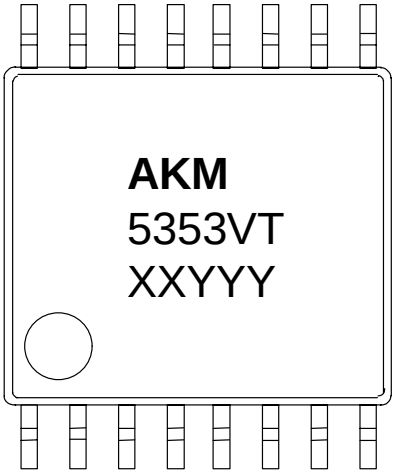


NOTE: Dimension "*" does not include mold flash.

■ Package & Lead frame material

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate

MARKING



1) Pin #1 indication
2) Date Code : XXYYY (5 digits)
   XX: lot#
   YYY: Date Code
3) Marketing Code : 5353VT
4) Asahi Kasei Logo