Signetics

7496, LS96
Shift Registers

5-Bit Shift Register
Product Specification

Logic Products

FEATURES
- **5-bit parallel-to-serial or serial-to-parallel converter**
- **Asynchronous ones transfer preset entry**
- **Buffered positive-triggered clock**
- **Buffered active LOW Clear (Master Reset)**

DESCRIPTION
The '96 is a 5-bit shift register with both serial and parallel (ones transfer) data entry. Since the '96 has the output of each stage available as well as a D-type serial input and ones transfer inputs on each stage, it can be used in 5-bit serial-to-parallel, serial-to-serial and some parallel-to-serial data operations.

The '96 is five master/slave flip-flops connected to perform right shift. The flip-flops change state on the LOW-to-HIGH transition of the clock. The Serial (S) input is edge-triggered and must be stable only one set-up time before the LOW-to-HIGH clock transition.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7496	25ns	48mA
74LS96	25ns	12mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N7496N, N74LS96N

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

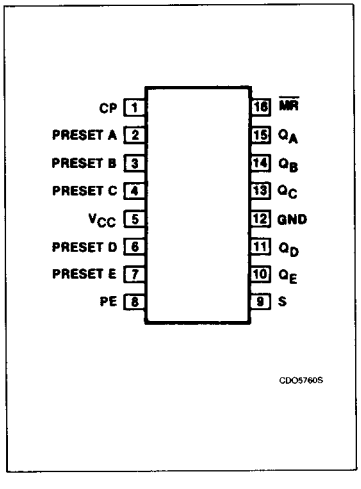
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
Preset enable	Inputs	5ul	5LSul
All other	Inputs	1ul	1LSul
Q	Outputs	10ul	10LSul

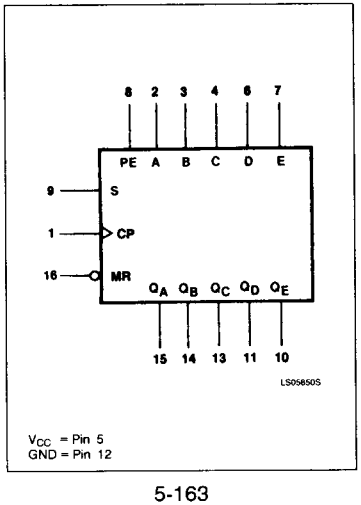
NOTE:
A 74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

5

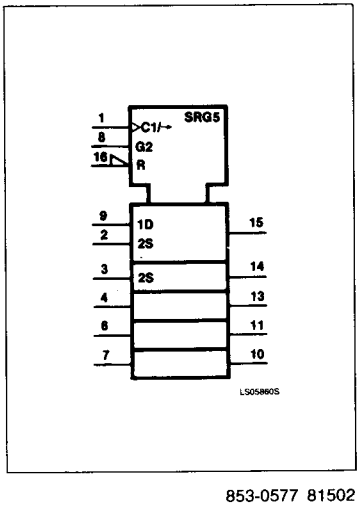
PIN CONFIGURATION



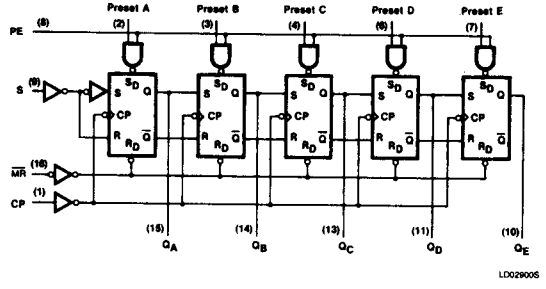
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



( ) = Pin number
V_{CC} = Pin 5
GND = Pin 12

Each flip-flop has asynchronous set inputs, allowing them to be independently set HIGH. The set inputs are controlled by a common active HIGH Preset Enable (PE) input. The PE input is not buffered, and care must be taken not to overload the driving element. When the PE is HIGH, a HIGH on the Preset (A – E) inputs will set the associated flip-flops HIGH. A LOW on the A – E inputs will cause "no change" in the appropriate flip-flops.

The asynchronous active LOW Clear ($\overline{MR}$) is buffered. When LOW, the $\overline{MR}$ overrides the clock and clears the register if the PE is not active. The Preset inputs override the $\overline{MR}$, forcing the flip-flops HIGH if both are activated simultaneously. However, for predictable operation, both signals should not be deactivated simultaneously.

FUNCTION TABLE

INPUTS								OUTPUTS				
Master Reset	Preset Enable	Preset					Clock	Serial	Q_A	Q_B	Q_C	Q_D	Q_E
		A	B	C	D	E							
L	L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	H	H	L	H	L	H	L	X	H	Q_{B0}	H	Q_{D0}	H
H	L	X	X	X	X	X	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	L	X	X	X	X	X	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}
H	L	X	X	X	X	X	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}

H = HIGH voltage level, (steady state)
L = LOW voltage level (steady state)
X = Irrelevant (any input, including transitions)
↑ = Transition from LOW-to-HIGH level
Q_{A0}, Q_{B0}, etc = The level of Q_A, Q_B, etc, respectively before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, etc = The level of Q_A, Q_B, etc, respectively before the most recent ↑ transition of the clock.

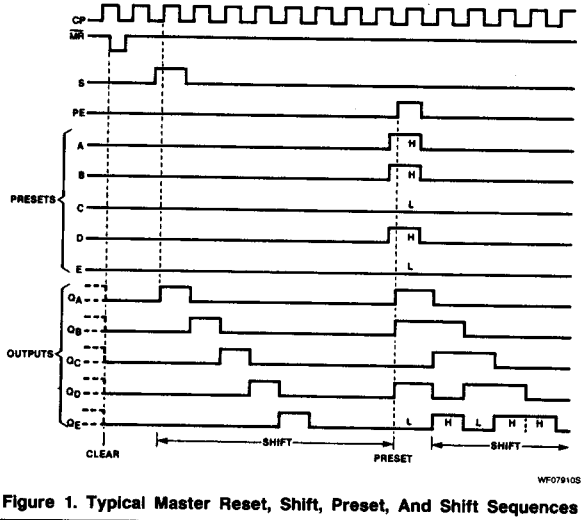


Figure 1. Typical Master Reset, Shift, Preset, And Shift Sequences

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			V
V_{IL}	LOW-level input voltage			+0.8			+0.8	V
I_{IK}	Input clamp current			−12			−18	mA
I_{OH}	HIGH-level output current			−400			−400	μA
I_{OL}	LOW-level output current			16			8	mA
T_A	Operating free-air temperature	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			7496			74LS96			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX			2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX			0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA (74LS)						0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5			−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V	PE inputs						0.5	mA
				Other inputs						0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	PE inputs			200				μA
				Other inputs			40				μA
			V_I = 2.7V	PE inputs						100	μA
				Other inputs						20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX V_I = 0.4V		PE inputs			−8			−2	mA
				Other inputs			−1.6			−0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−18		−57	−20		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				48	79		12	20	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with Clear grounded and all other inputs and outputs open.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

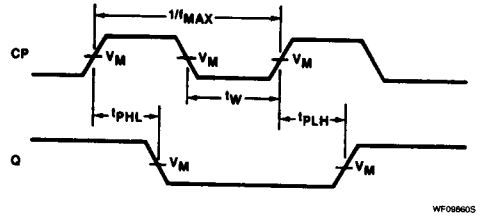
PARAMETER		TEST CONDITIONS	74		74LS		UNIT
			$C_L = 15pF$, $R_L = 400\Omega$		$C_L = 15pF$, $R_L = 2k\Omega$		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	10		25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		40 40		40 40	ns
t_{PLH}	Propagation delay Preset or preset enable to output	Waveform 2		35		35	ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 2		55		55	ns

NOTE:
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

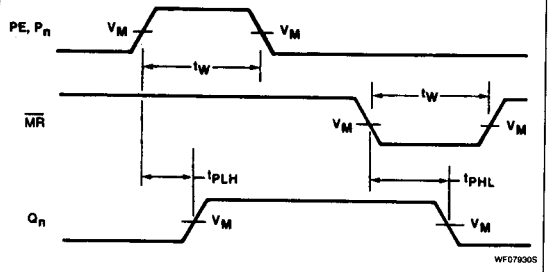
AC SET-UP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	74		74LS		UNIT
			Min	Max	Min	Max	
$t_W(L)$	Clock pulse width, LOW	Waveform 1	35		20		ns
$t_W(L)$	$\overline{MR}$ pulse width, LOW	Waveform 2	30		30		ns
$t_W(H)$	Preset or preset enable pulse width, HIGH	Waveform 2	30		30		ns
t_s	Set-up time, S to CP	Waveform 3	30		30		ns
t_h	Hold time, S to CP	Waveform 3	0		0		ns

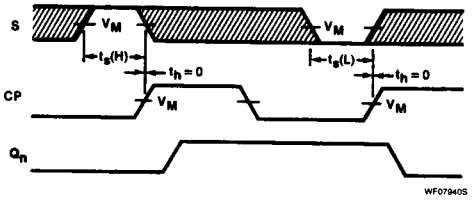
AC WAVEFORMS



Waveform 1. Clock To Output Delays And Clock Pulse Width



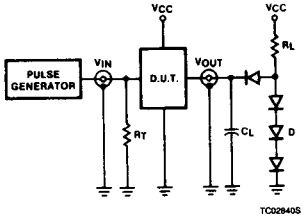
Waveform 2. Parallel Load And Parallel Data To Output Delays And Master Reset To Output Delay

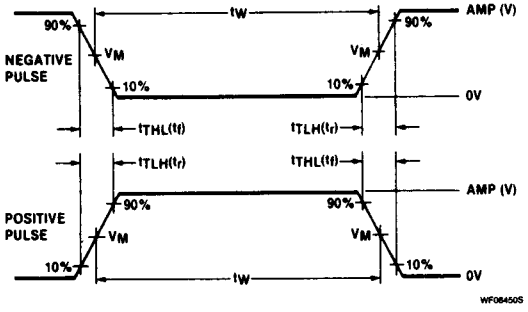


For all waveforms, $V_M = 1.5V$ for 74 and 74S; $V_M = 1.3V$ for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.
The number of Clock Pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Truth Table.

Waveform 3. Data Set-up And Hold Time

TEST CIRCUITS AND WAVEFORMS





Test Circuit For 74 Totem-Pole Outputs

V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

5