General Description

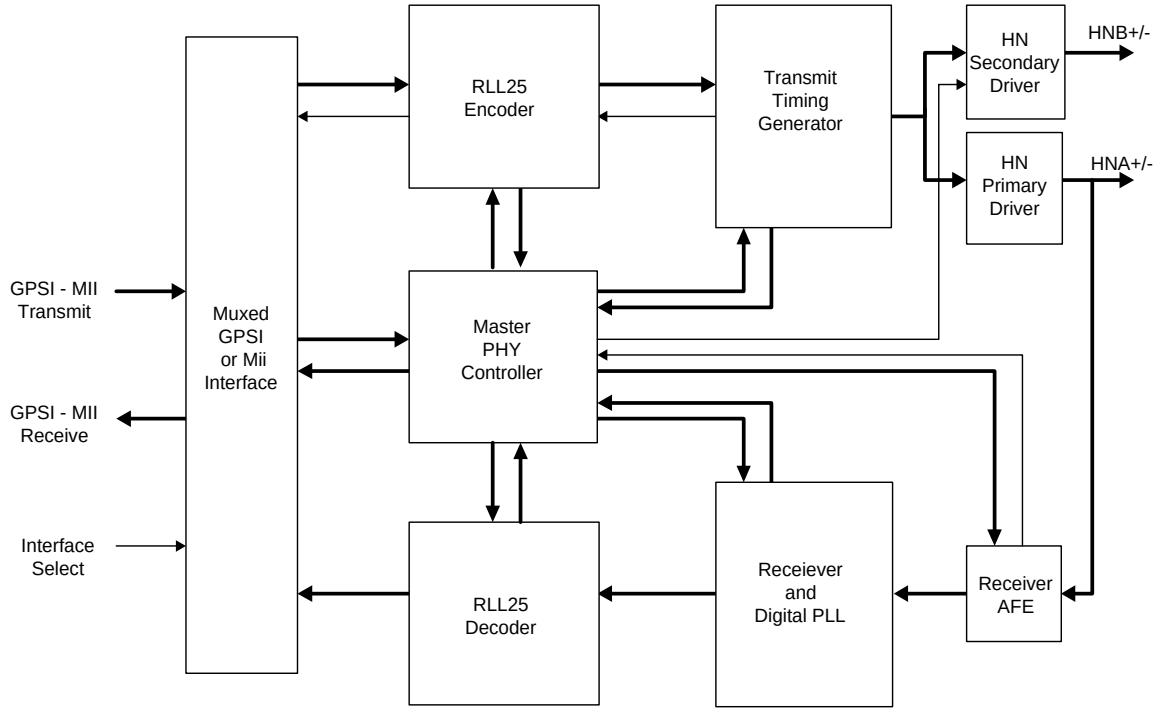
The DM9801A is a physical-layer, single-chip, low-power transceiver for 1M Home Phoneline Network applications. On the media side, it provides an interface to a Home Phoneline wiring system. The reconciliation layer interfaces to the DM9801A either through an IEEE802.3u subset Media Independent Interface (MII) or a pseudo-standard General Purpose Serial Interface (GPSI). A management interface is provided by MDIO/MDC when operating in MII mode, or a Serial Peripheral Interface bus when operating in GPSI mode.

The DM9801A uses a low-power and high-performance CMOS process. It contains the entire physical layer functions of 1M as defined by Home Phoneline Network Alliance, Rev. 1.1, including the Physical Coding Sublayer, (RLL25) Encoder/Decoder (ENC/DEC), 4-wire HN Driver circuit and receiver analog front end (AFE).

Patent-Pending Circuitry Includes:

Enhanced 4-wire Home Network transceiver circuit. Compatible with HomePNA 1M PHY specification version 1.1 and HomePNA certification document version 1.0

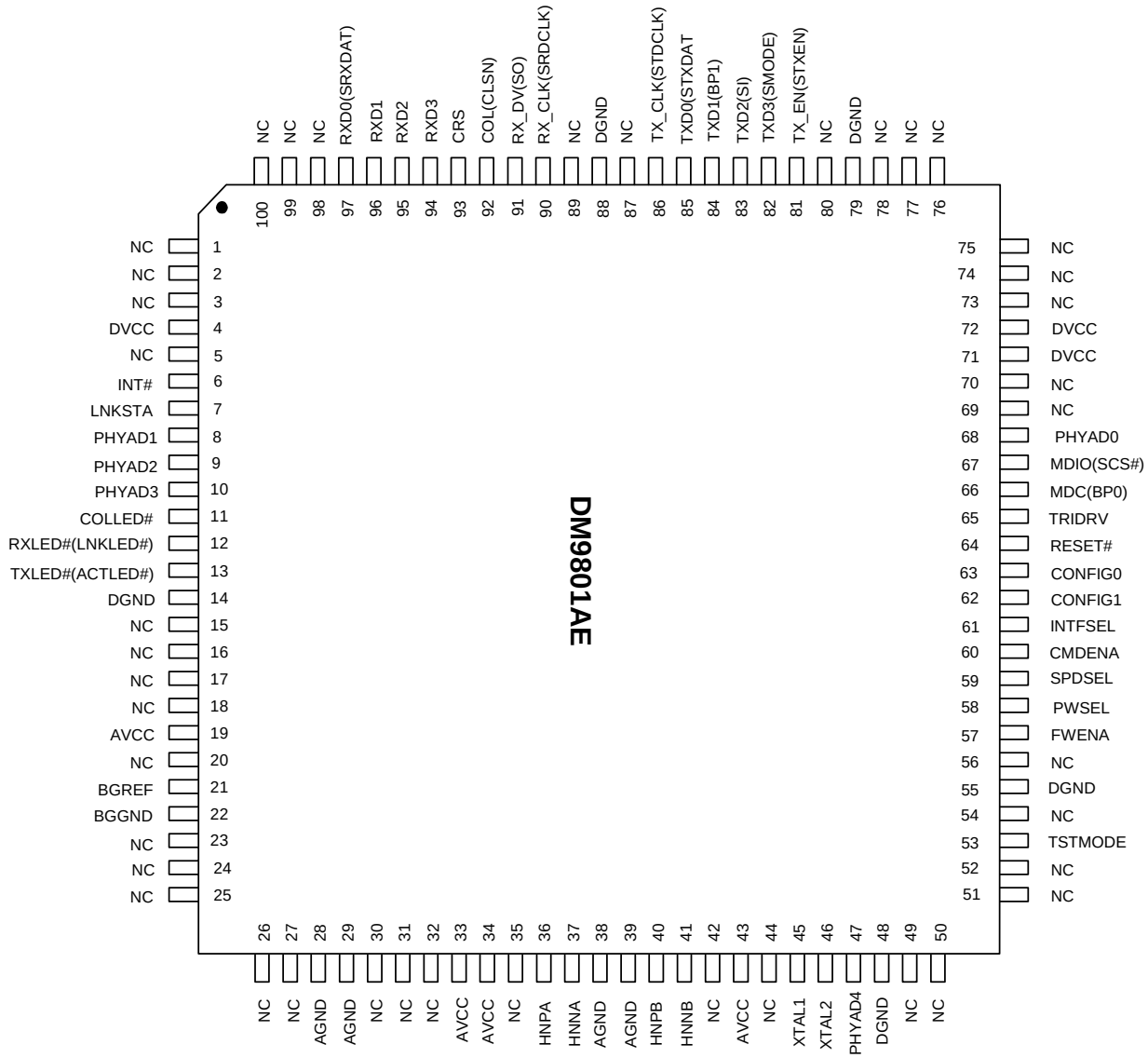
Block Diagram



Features

- 1M Home Phoneline Network physical-layer, single-chip transceiver
- Compatible with HomePNA 1M PHY specification version 1.1 and HomePNA certification document version 1.0
- Supports the MII including the MDIO/MDC serial management interface
- Supports the GPSI including a SPI serial management interface
- Supports Link Integrity function
- Smart equalizer circuit for 1M receiver
- Supports Patent Pending 4-wire operation
- Supports hardware or software speed select
- Supports Interrupt on change, eliminates management polling
- Flexible built-in LED support for TX Activity, RX Activity and Collision Indication or Activity, Link state and Collision
- Digital PLL circuit using advanced digital algorithm to reduce jitter
- Low-power, high-performance CMOS process
- Available in a small outline 100-pin LQFP
- 3.3V DC power with 5V DC tolerant I/O

Pin Configuration: DM9801A, 100-pin LQFP



Pin Description

Pin No.	Pin Name	I/O	Description
Station Interface: Receive Data, Transmit Data and Management			
85	TXD0 or STXDAT	I	**Transmit Data Bit 0 (MII Mode, INTFSEL = 0):** Transmit data input pin, bit 0, for nibble data from the MII **Serial Transmit Data Bit (GPSI Mode, INTFSEL = 1):** Transmit data input pin for serial data from the GPSI.
84	TXD1 or BP1	I	**Transmit Data Bit 1 (MII Mode, INTFSEL = 0):** Transmit data input pin, bit 1, for nibble data from the MII **SPROM Boot Page Select 1 (GPSI Mode, INTFSEL = 1):** Most significant bit of a 2-bit encoded select. The BP1 and BP0 inputs, select one of four, 64-byte, SPROM pages to initialize the DM9801A management registers. Master mode must be selected using the SMODE input.
83	TXD2 or SI	I	**Transmit Data Bit 2 (MII Mode, INTFSEL = 0):** Transmit data input pin, bit 2, for nibble data from the MII **Serial Data Input (GPSI Mode, INTFSEL = 1):** This is the serial data input pin to the DM9801A for the SPI bus. The SPI bus operation is only valid if GPSI mode is selected.
82	TXD3 or SMODE	I	**Transmit Data Bit 3 (MII Mode, INTFSEL = 0):** Transmit data input pin, bit 3, for nibble data from the MII **Serial Mode Select (GPSI Mode, INTFSEL = 1):** This input pin selects the SPI buses mode of operation. The SPI bus modes of operation are: **Master Mode (SMODE = 0)** **Slave Mode (SMODE = 1)** The SPI bus operation is only valid if GPSI mode is selected.
86	TX_CLK or STDCLK	O,Z	**MII Transmit Clock (MII Mode, INTFSEL = 0):** TX_CLK is an output pin from the DM9801A. Used as the transmit data reference clock, to clock in nibble data from the MII when in MII interface mode. **Serial Transmit Data Clock (GPSI Mode, INTFSEL = 1):** STDCLK is an output from the DM9801A. Used as the transmit reference clock to clock in the STXDATA when in GPSI interface mode.
81	TX_EN or STXEN	I	**MII Transmit Enable (MII Mode, INTFSEL = 0):** MII Transmit enable input, used to enable the transmit function of the MII when in MII interface mode. **Serial Transmit Enable (GPSI Mode, INTFSEL = 1):** Used to enable the transmit function of the GPSI when in GPSI interface mode.
66	MDC or BP0	I	**MII Serial Management Clock (MII Mode, INTFSEL = 0):** Synchronous clock to the MDIO management data input/output serial interface which is asynchronous to transmit and receive clocks. The maximum clock rate is 2.5MHz. **SPROM Boot Page Select 0 (GPSI Mode, INTFSEL = 1):** Least significant bit of a 2-bit encoded select. The BP1 and BP0 inputs, select one of four, 64-byte, SPROM pages to initialize the DM9801A management registers. Master mode must be selected using the SMODE input.

Pin Description (Continued)

Pin No.	Pin Name	I/O	Description
Station Interface: Receive Data, Transmit Data and Management (Continued)			
67	MDIO Or SCS#	I/O,Z	**MII Serial Management Data (MII Mode, INTFSEL = 0):** Bi-directional management instruction/data signal that may be driven by the station management entity or the PHY. This pin requires a 1.5KΩ pull-up resistor. **Serial Interface Chip Select (GPSI Mode, INTFSEL = 1):** SCS# is a bi-directional management chip select signal that may be driven by the station management entity or the PHY. **(Active low)**
97	RXD0 Or SRXDAT	O,Z	**Receive Data Bit 0 (MII Mode, INTFSEL = 0):** Receive data output pin, bit 0, for nibble data to the MII **Serial Receive Data Bit (GPSI Mode, INTFSEL = 1):** Receive data output pin for serial data to the GPSI.
96	RXD1	O,Z	**Receive Data Bit 1:** Receive data output pin, bit 1, for nibble data to the
95	RXD2	O,Z	**Receive Data Bit 2:** Receive data output pin, bit 2, for nibble data to the MII
94	RXD3	O,Z	**Receive Data Bit 3:** Receive data output pin, bit 3, for nibble data to the MII
90	RX_CLK Or SRDCLK	O,Z	**MII Receive Clock (MII Mode, INTFSEL = 0):** RX_CLK is an output pin from the DM9801A. Used as the receive data reference clock, to clock out nibble data from the MII when in MII interface mode. **Serial Receive Data Clock (GPSI Mode, INTFSEL = 1):** SRDCLK is an output from the DM9801A. Used as the receive reference clock to clock out the SRXDATA when in GPSI interface mode.
91	RX_DV Or SO	O,Z	**Receive Data Valid (MII Mode, INTFSEL = 0):** RX_DV is asserted high to indicate that valid data is present on RXD[3:0]. **Serial Data Output (GPSI Mode, INTFSEL = 1):** This is the serial data output pin from the DM9801A for the SPI bus. The SPI bus operation is only valid if GPSI mode is selected.
93	CRS	O,Z	**Carrier Sense:** This pin is asserted high to indicate the presence of carrier due to receive or transmit activities.
92	COL or CLSN	O,Z	**Collision Detect MII Mode, INTFSEL = 0):** COL is asserted high to indicate detection of collision condition. **Collision Detect (GPSI Mode, INTFSEL = 1):** CLSN is asserted high to indicate detection of collision condition.

Pin Description (Continued)

PHY Address Interface: PHYAD[4:0] provides up to 32 unique PHY address. An address selection of all zeros (00000) will result in a PHY isolation condition. See the isolate bit description in the BMCR, address 00.			
68	PHYADSEL (PHYAD0) Or SCLK	I/O,Z	**MII Serial Management PHY Address Select (MII Mode, INTFSEL = 0):** PHYADSEL is an input signal that selects one of two PHY addresses within the 32 address range for the DM9801A MII management interface when both CONFIG1 and CONFIG0 are not set to 1. **0 = 0x01 address** **1 = 0x1F address** **PHY Address 0 (MII Mode, i.e. INTFSEL = 0 or GM_MODE, i.e. INTFSEL=1, CONFIG1=1, and CONFIG0=1):** PHY address bit 0 for multiple PHY address applications. Both CONFIG1 and CONFIG0 must be set to 1. **Serial Interface Clock (Standard GPSI Mode, INTFSEL = 1):** SCLK is a bi-directional clock signal used to synchronize SI, SO and SCS# to and from the DM9801A SPI bus.
8	PHYAD1	I/O, Z	**PHY Address 1 (MII Mode, INTFSEL = 0, or GM_MODE, i.e. INTFSEL=1, CONFIG1=1, and CONFIG0=1):** PHY address bit 1 for multiple PHY address applications. Both CONFIG1 and CONFIG0 must be set to 1. Leave unconnected when both CONFIG1 and CONFIG0 are not 1.
9	PHYAD2	I/O, Z	**PHY Address 2 (MII Mode, INTFSEL = 0, or GM_MODE, i.e. INTFSEL=1, CONFIG1=1, and CONFIG0=1):** PHY address bit 2 for multiple PHY address applications. Both CONFIG1 and CONFIG0 must be set to 1. Leave unconnected when both CONFIG1 and CONFIG0 are not 1.
10	PHYAD3	I/O, Z	**PHY Address 3 (MII Mode, INTFSEL = 0), or GM_MODE, i.e. INTFSEL=1, CONFIG1=1, and CONFIG0=1:** PHY address bit 3 for multiple PHY address applications. Both CONFIG1 and CONFIG0 must be set to 1. Leave unconnected when both CONFIG1 and CONFIG0 are not 1.
47	PHYAD4	I/O, Z	**PHY Address 4 (MII Mode, INTFSEL = 0), or GM_MODE, i.e. INTFSEL=1, CONFIG1=1, and CONFIG0=1:** PHY address bit 4 for multiple PHY address applications. Both CONFIG1 and CONFIG0 must be set to 1. Leave unconnected when both CONFIG1 and CONFIG0 are not 1.

Pin Description (Continued)

Pin No.	Pin Name	I/O	Description
Configuration and Control Interface:			
64	RESET#	I	**Reset:** Active Low input that initializes the DM9801A. Should remain low for 10ms after VCC has stabilized at 3.3Vdc (nominal) before it transitions to high.
63 62	CONFIG0 CONFIG1	I	**Configuration Select 1:0:** These input pins select the DM9801A configuration from a reset condition.

<table>
<tr><td></td><td></td><td></td><td>
<table>
<tr><th>CONFIG1</th><th>CONFIG0</th><th>Configuration Selected</th></tr>
<tr><td>0</td><td>0</td><td>TXLED, RXLED and COLLED configuration *</td></tr>
<tr><td>0</td><td>1</td><td>ACTLED, LNKLED and COLLED configuration *</td></tr>
<tr><td>1</td><td>0</td><td>ACTLED, LNKLED and COLLED configuration with MII Management Register 0-6 emulation support *</td></tr>
<tr><td>1</td><td>1</td><td>ACTLED, LNKLED and COLLED Configuration with MII Management Register 0-6 emulation and 32 PHY address support</td></tr>
</table>
*see the DM9801A description for a more detailed explanation
</td></tr>
<tr><td>61</td><td>INTFSEL</td><td>I</td><td>
Interface Select:
This pin, when combined with pin 62, 63 (CONFIG1, CONFIG0),selects among the following different data interfaces and management interfaces:
<table>
<tr><td></td><td>INTFSEL</td><td>CONFIG0</td><td>CONFIG1</td><td>INTERFACE</td><td>MANAGEMENT</td></tr>
<tr><td>MII Mode</td><td>0</td><td>X</td><td>X</td><td>MII</td><td>MDC/MDIO</td></tr>
<tr><td rowspan="2">GPSI Mode</td><td>1</td><td>0</td><td>X</td><td rowspan="2">GPSI</td><td rowspan="2">SPI</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
<tr><td>GM Mode</td><td>1</td><td>1</td><td>1</td><td>GPSI</td><td>MDC/MDIO</td></tr>
</table>
</td></tr>
<tr><td>60</td><td>CMDENA</td><td>I</td><td>Command Enable:
This pin enables a remote master node to alter the management register values of the local DM9801A.</td></tr>
<tr><td>59</td><td>SPDSEL</td><td>I</td><td>Speed Select:
This pin will select the 1M network speed.
0 = Low Speed
1 = High Speed</td></tr>
<tr><td>58</td><td>PWRSEL</td><td>I</td><td>Power Select:
This pin will select the 1M network power.
0 = Low Power
1 = High Power</td></tr>
<tr><td>65</td><td>TRIDRV</td><td>I</td><td>Tri-state all Outputs:
This pin, when asserted high, will tri-state all outputs (no effect on open-drain outputs).</td></tr>
<tr><td>57</td><td>FWENA</td><td>I</td><td>Four Wire Interface Enable:
This pin, when asserted high, will enable the HNPB and HNNB driver pair for operation. When low, the secondary drivers are powered down.</td></tr>
<tr><td>6</td><td>INT#</td><td>OD</td><td>Interrupt Request:
This pin will be asserted low when an interrupt condition exists in the DM9801A.</td></tr>
</table>

Pin Description (Continued)

Pin No.	Pin Name	I/O	Description
LED Interface : These outputs can directly drive LEDs or provide status information to a network management device.			
13	TXLED# or ACTLED#	OD	**Transmit LED:** Indicates the DM9801A is transmitting data (Active low, Open drain). *Config0 = 0 and Config1 = 0* **Activity LED:** Indicates the DM9801A is either transmitting or receiving data (Active low, Open drain).
12	RXLED# or LNKLED#	OD	**Receive LED:** Indicates the presence of receive data activity by the DM9801A(Active low, Open drain). *Config0 = 0 and Config1 = 0* **Link LED:** Indicates Good Link status and that the Link Integrity Timer has not expired (Active low, Open drain).
11	COLLED#	OD	**Collision LED:** Indicates the presence of collision activity on the 1M network (Active low, Open drain).
Home Phoneline Network Media Interface:			
36	HNPA	ALG	**Home Network Interface, Positive, Primary:** This is the positive interface connection of the primary 1M network interface.
37	HNNA	ALG	**Home Network Interface, Negative, Primary:** This is the negative interface connection of the primary 1M network interface.
40	HNPB	ALG	**Home Network Interface, Positive, Secondary:** This is the positive interface connection of the secondary 1M network interface.
41	HNNB	ALG	**Home Network Interface, Negative, Secondary:** This is the negative interface connection of the secondary 1M network interface.

Pin Description (Continued)

Pin No.	Pin Name	I/O	Description
Miscellaneous:			
7	LNKSTA	I/O,Z	**Link Status:** Output, positive true logic. Indication of Link Status.
45	XTAL1	ALG	**Crystal Pin 1:** This pin should be connected to one side of a 20MHz (±50 ppm) crystal.
46	XTAL2	ALG	**Crystal Pin 2:** This pin should be connected to the other side of a 20MHz (±50 ppm) crystal.
21	BGREF	ALG	**Bandgap Voltage Reference:** Connect a 6.20_KΩ, 1% resistor between this pin and the BGGND pin to provide an accurate current reference for the DM9801A.
22	BGGND	ALG	**Bandgap Voltage Reference Return:** Return pin for the 6.20_KΩ resistor connection.
53	TSTMODE	I	**Test Mode Control Pin:** TSTMODE=0: Normal operating mode. TSTMODE=1: Enable test mode.
1, 2, 3,5, 15 – 18, 20, 23 – 27, 30 - 32, 35, 42, 44, 49 – 52, 54, 56, 69, 70, 73 – 78, 80, 87, 89, 98, 99, 100	NC		**No Connect:** These pins are reserved. Leave these pins unconnected (floating).
Power and Ground: The power (VCC) and ground (GND) pins of the DM9801A are grouped in pairs of two categories - Digital Circuitry Power/Ground Pairs and Analog Circuitry Power/Ground Pair.			
14, 48, 55, 79, 88,	DGND	P	Digital logic ground
4, 71, 72	DVCC	P	Digital logic power supply
28, 29, 38, 39	AGND	P	Analog circuit ground
19, 33, 34, 43	AVCC	P	Analog circuit power supply

Functional Description

The DM9801A is a single-chip Home Phoneline Network transceiver .The DM9801A provides an IEEE 802.3u subset Media Independent Interface (MII) or a pseudo-standard General Purpose Serial Interface (GPSI).

The DM9801A enables home networking by allowing Ethernet packets to be transported over common home telephone wiring with no modifications, using Ethernet CSMA/CD media access control procedures as defined in the IEEE 802.3 standard. Figure 1 shows the major functional blocks implemented in the DM9801A.

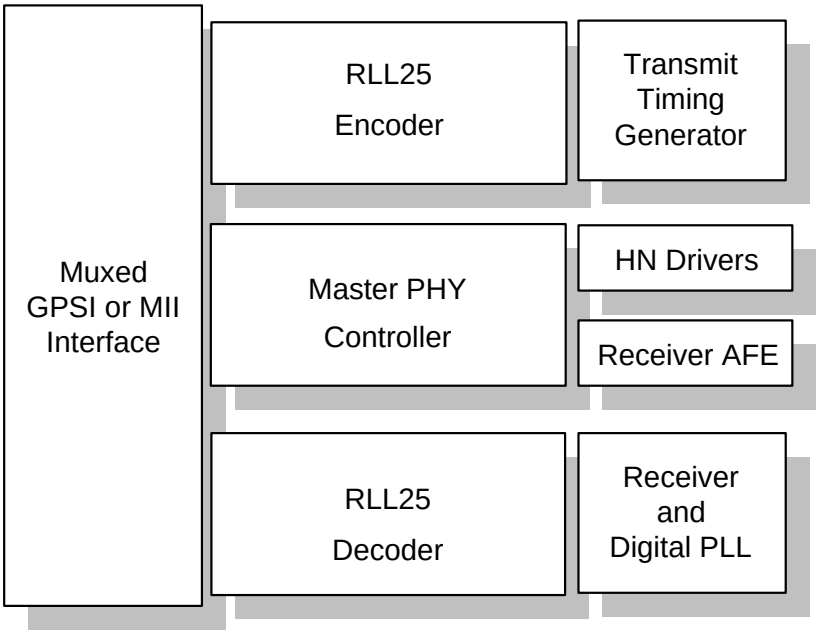


Figure 1

MII Interface

The DM9801A provides a subset Media Independent Interface (MII) or a pseudo-standard General Purpose Serial Interface (GPSI). The MII interface provides a simple, easy way to implement connection between the MAC Reconciliation layer and the DM9801A transceiver. The MII is designed to make the differences between various media transparent to the MAC sublayer.
The MII consists of a nibble wide receive data bus, a nibble wide transmit data bus, and control signals to facilitate data transfers between the PHY and the Reconciliation layer.

TXD (transmit data) is a nibble (4 bits) of data that are driven by the reconciliation sublayer synchronously with respect to TX_CLK. For each TX_CLK period, which TX_EN is asserted, TXD (3:0) are accepted for transmission by the PHY.

TX_CLK (transmit clock) output to the MAC reconciliation sublayer is a clock that provides the timing reference for the transfer of the TX_EN, TXD, and TX_ER signals.

TX_EN (transmit enable) input from the MAC reconciliation sublayer to indicate nibbles are being presented on the MII for transmission on the physical medium.

MII Interface (continued)

RXD (receive data) is a nibble (4 bits) of data that are sampled by the reconciliation sublayer synchronously with respect to RX_CLK. For each RX_CLK period that RX_DV is asserted, RXD (3:0) are transferred from the PHY to the MAC reconciliation sublayer.

RX_CLK (receive clock) output to the MAC reconciliation sublayer is a clock that provides the timing reference for the transfer of the RX_DV, RXD, and RX_ER signals.

RX_DV (receive data valid) input from the PHY to indicate the PHY is presenting recovered and decoded nibbles to the MAC reconciliation sublayer. To interpret a receive frame correctly by the reconciliation sublayer, RX_DV must encompass the frame starting no later than the Start-of-Frame delimiter and excluding any End-Stream delimiter.

CRS (carrier sense) is asserted by the PHY when either the transmit or receive medium is non-idle and deasserted by the PHY when the transmit and receive medium are idle.

MII Serial Management

The MII serial management interface consists of a data interface, basic register set, and a serial management interface to the register set. Through this interface it is possible to control and configure multiple PHY devices, get status and error information, and determine the type and capabilities of the attached PHY device(s).

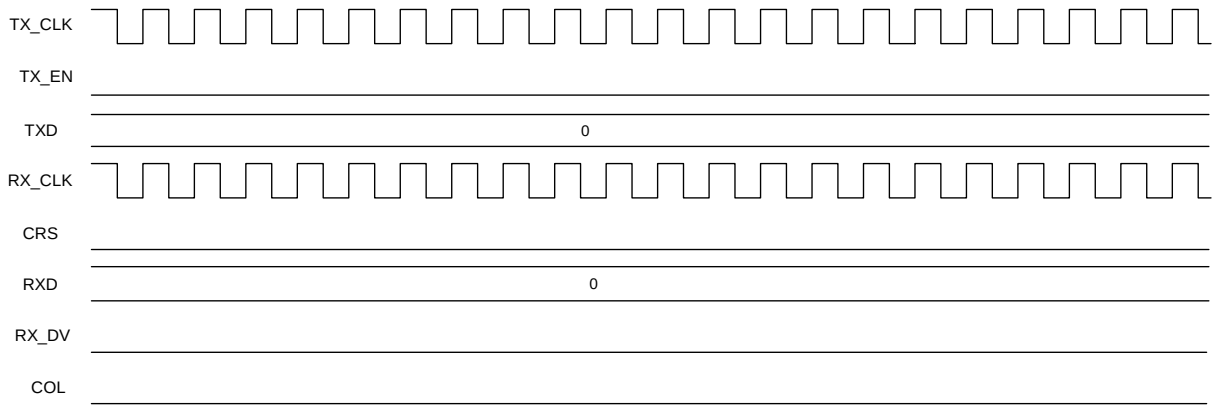
The DM9801A management functions correspond to MII specification for IEEE 802.3u-1995 (Clause 22) for registers 0 through 6 with vendor-specific registers 16 through 31.

In read/write operation, the management data frame is 64-bits long and starts with 32 contiguous logic one bits (preamble) synchronization clock cycles on MDC. The Start of Frame Delimiter (SFD) is indicated by a <01> pattern followed by the operation code (OP):<10> indicates Read operation and <01> indicates Write operation. For read operation, a 2-bit turnaround (TA) filing between Register Address field and Data field is provided for MDIO to avoid contention. Following the turnaround time, 16-bit data is read from or written to the management registers.

Serial Management Interface

The serial control interface uses a simple two-wired serial interface to obtain and control the status of the physical layer through the MII interface. The serial control interface consists of MDC (Management Data Clock), and MDI/O (Management Data Input/Output) signals.
The MDIO pin is bi-directional and may be shared by up to 32 devices.

MII Interface Transmit and Receive Timing Diagram

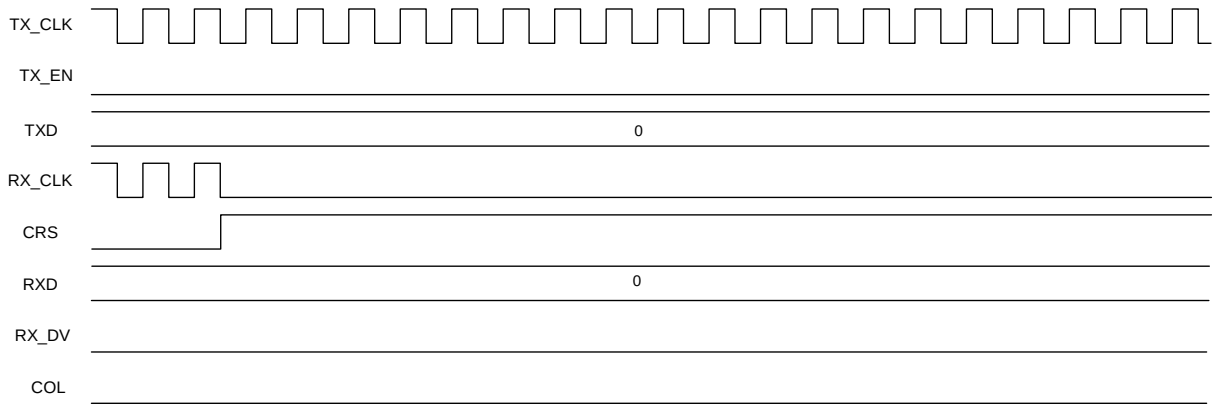


RX_CLK and TX_CLK are synchronized. All signals are inactive. The period of the two clock is 2333.3 ns.

Idle State

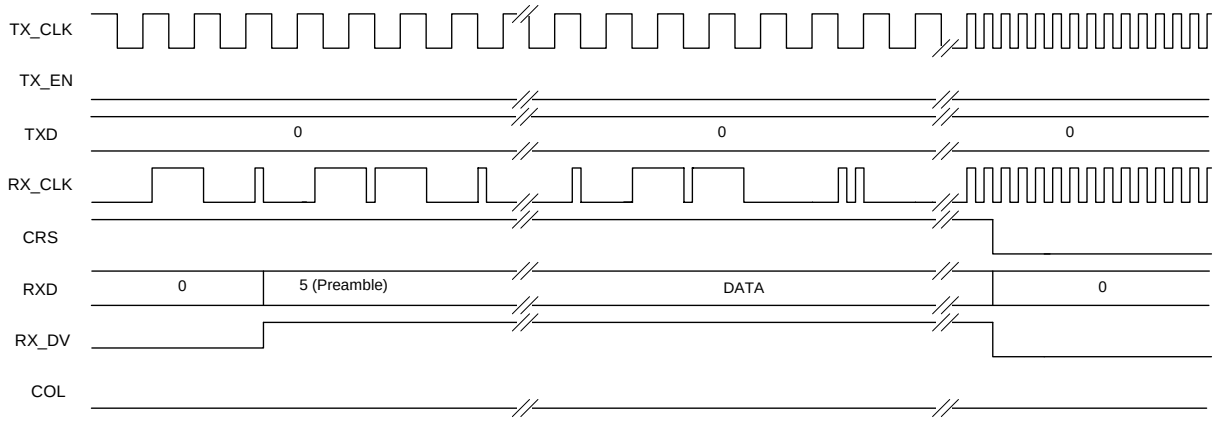
Figure 2

MII Interface Transmit and Receive Timing Diagram (continued)



RX_CLK becomes disabled (and left in the low state) as soon as CRS is asserted. The clock is re-enabled about 140 uS into the packet.

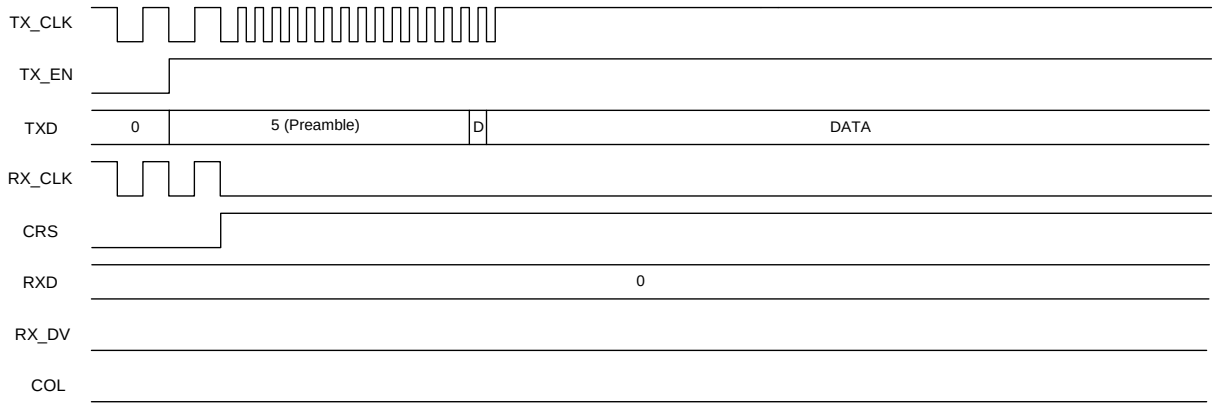
RXPKT – CRS Asserted
Figure 3



RX_CLK and TX_CLK are unrelated to each other during this time. When a symbol has been received and decoded, RX_CLK toggles at various frequencies depending on what data have been received. Once CRS falls, RX_CLK and TX_CLK are toggled continuously at 933.3 ns for 22 cycles, after which DM9801A returns to the Idle State.

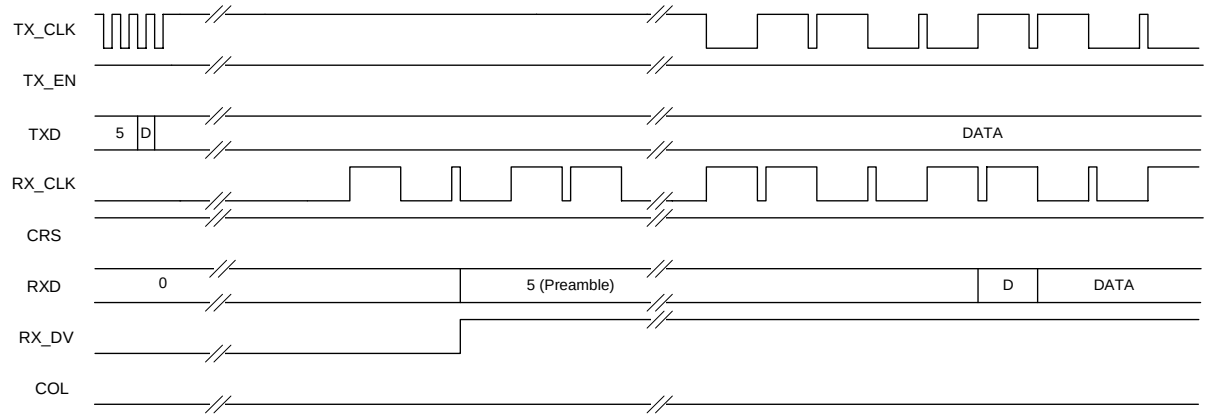
RXPKT – RX_CLK Active and CRS Cleared
Figure 4

MII Interface Transmit and Receive Timing Diagram (continued)



Once TX_EN is asserted, DM9801A stops RX_CLK, asserts CRS, and toggles TX_CLK at 933.3 ns.

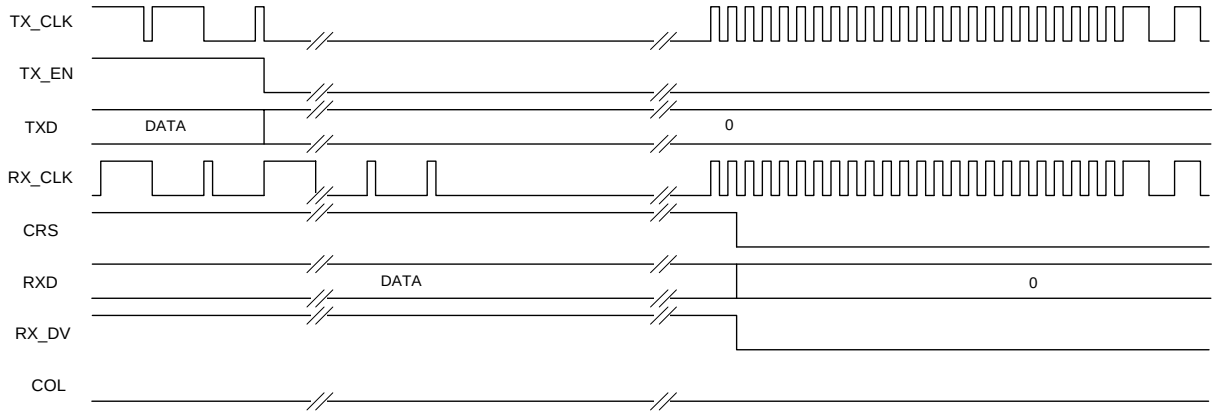
TXPKT – TX_EN Asserted
Figure 5



TX_CLK continues to toggle at 933.3 ns until the SFD is observed, as shown in the first section of the above diagram. At this point, TX_CLK is disabled (high) until AID header has been transmitted on the wire (or until a COL has been detected). This takes about 120 us, at which time RX_CLK starts toggling, thereby shifting 32 bits of preamble and SFD back to the MAC. Sometime later, the TX_CLK restarts as symbols get sent onto the wire in an analogous manner as RX_CLK during packet reception.

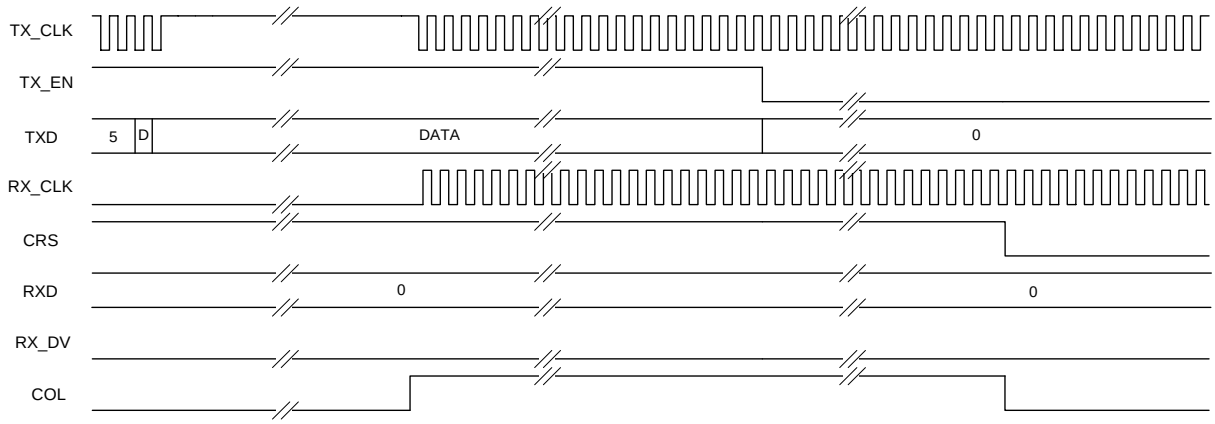
TXPKT – RX_CLK Active
Figure 6

MII Interface Transmit and Receive Timing Diagram (continued)



Once TX_EN is cleared, the last symbol gets encoded and transmitted, the looped-back data is presented back to the MAC, and CRS falls. Once CRS falls, TX_CLK and RX_CLK toggles with a period of 933.3 ns for 22 clocks, after which the system returns to the Idle State.

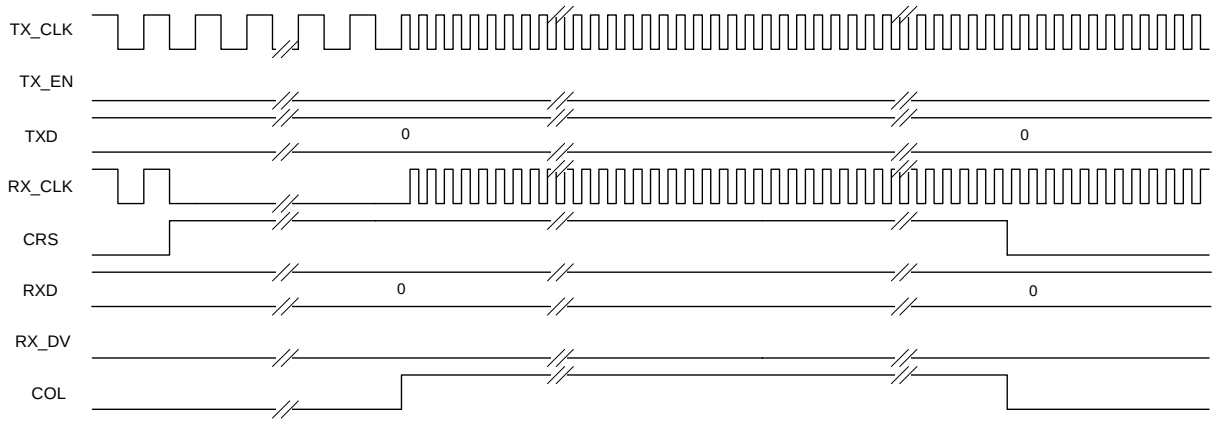
TXPKT – TX_EN Cleared
Figure 7



COL will be asserted sometime after the preamble and SFD have been clocked in. TX_CLK and RX_CLK are then clocked with a period 933.3 ns until CRS drops. TX_EN drops sometime after COL was asserted. CRS and COL are dropped after more than 80 clocks. TX_CLK and RX_CLK keep toggling at 933.3 ns period for roughly another 25 clock cycles, when the system returns to the Idle State.

TXPKT – COL Asserted
Figure 8

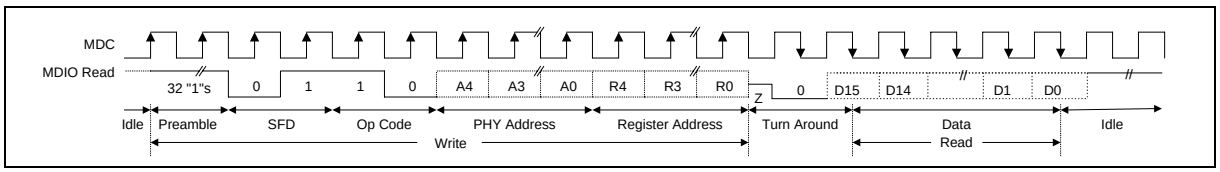
MII Interface Transmit and Receive Timing Diagram (continued)



COL may be asserted up to 120 us after CRS has been asserted. Once COL has been asserted, TX_CLK and RX_CLK run at a period of 933.3 ns until COL and CRS are cleared. It can take up to about 600 us for CRS to clear.

RXPKT – COL Asserted
Figure 9

Management Interface - Read Frame Structure



Management Interface - Write Frame Structure

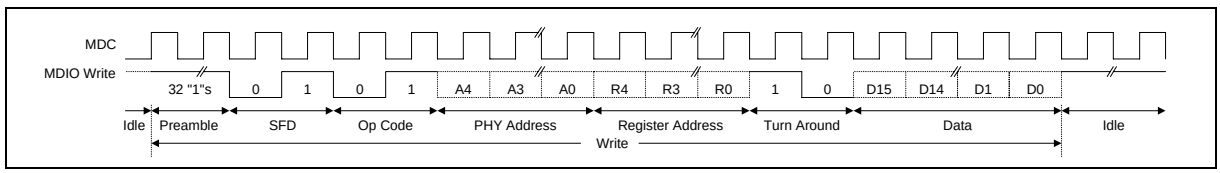


Figure 10

General Purpose Serial Interface

The DM 9801 provides a subset Media Independent Interface (MII) or a pseudo-standard General Purpose Serial Interface (GPSI). The GPSI interface provides a simple, easy way to implement connection between the MAC Reconciliation layer and the DM9801A transceiver. The GPSI is designed to make the differences between various media transparent to the MAC sublayer.
The GPSI interface provides a serial receive data bus, a serial transmit data bus, and control signals to facilitate data transfers between the DM9801A transceiver and the Reconciliation layer. The seven signals which comprise the GPSI are STXDAT, STDCLK, STXEN, SRXDAT, SRXCLK, CLSN, and CRS. Of these, only STXEN and STXDAT are inputs to the DM9801A, the other five are outputs from the DM9801A.

STXDAT (serial transmit data) is a serial stream of data that are driven by the reconciliation sublayer synchronously with respect to STDCLK. For each STDCLK period, which STXEN is asserted, STXDAT is accepted for transmission by the PHY.

STDCLK (serial transmit data clock) is an output to the MAC reconciliation sublayer. STDCLK is a clock that provides the timing reference for the transfer of the STXDAT in GPSI mode.

STXEN (serial transmit enable) input from the MAC reconciliation sublayer to indicate serial data is being presented on the GPSI for transmission on the physical medium.

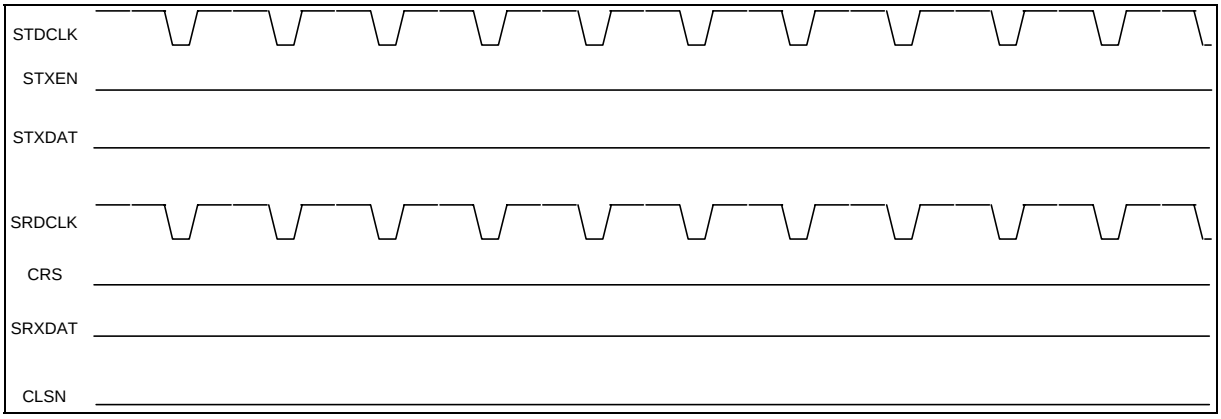
SRXDAT (serial receive data) is a serial stream of data that is sampled by the reconciliation sublayer synchronously with respect to SRXCLK.

SRXCLK (serial receive data clock) is an output to the MAC reconciliation sublayer. SRDCLK is a clock that provides the timing reference for the transfer of the SRXDAT in GPSI mode.

CLSN (collision detect) is an output to the MAC reconciliation sublayer. CLSN is asserted high to indicate detection of collision condition

CRS (carrier sense) is an output to the MAC reconciliation sublayer that is asserted high to indicate the presence of carrier due to receive or transmit activities.

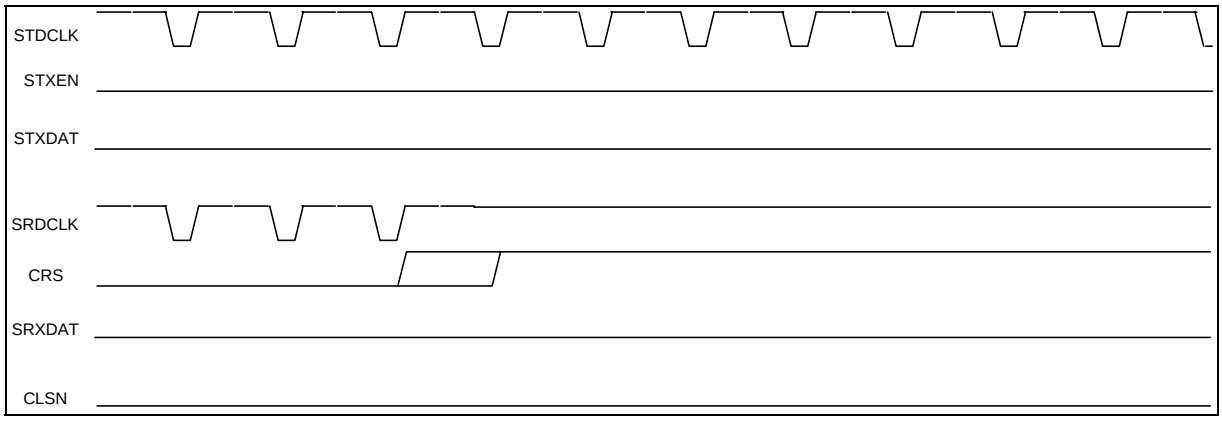
The subsequent sections analyze each GPSI related state of the DM9801A in detail.



SRDCLK and STDCLK are synchronized. All other signals are inactive.

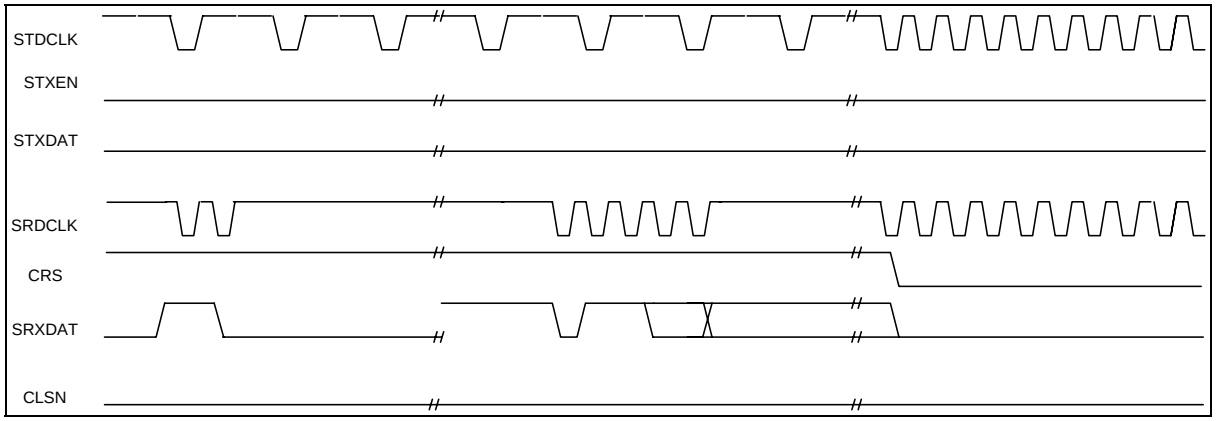
Idle State
Figure 11

General Purpose Serial Interface (continued)



SRDCLK becomes disabled as soon as CRS is asserted.

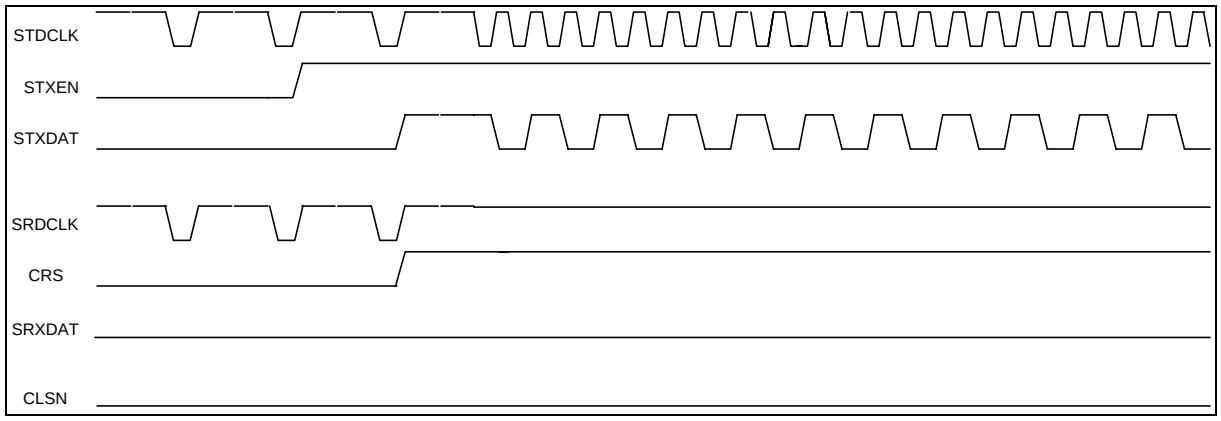
RXPKT- CRS Asserted
Figure 12



SRDCLK and STDCLK are unrelated to each other during this time. When a symbol has been received and decoded, SRDCLK toggles in order to shift out the three to six bits encoded in the symbol. The middle portion of this diagram shows the end of the preamble, followed by the SFD and the beginning of the datagram. CRS will fall after the last received symbol. Once CRS falls, SRDCLK and STDCLK are toggled continuously for 97 cycles after which the DM9801A returns to the Idle state.

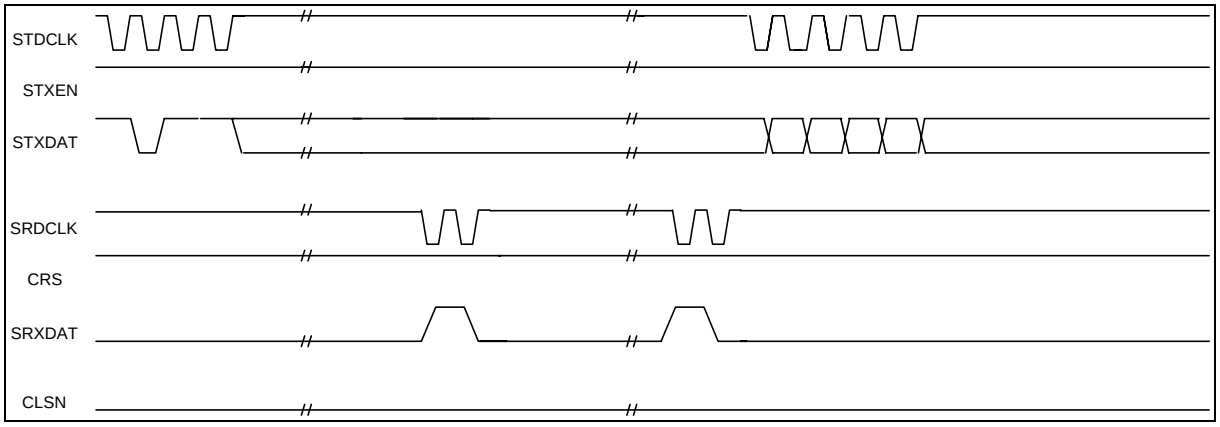
RXPKT - SRDCLK Active and CRS Cleared
Figure 13

General Purpose Serial Interface (continued)



Once STXEN is asserted, the DM9801A stops SRDCLK, asserts CRS, and toggles STDCLK.

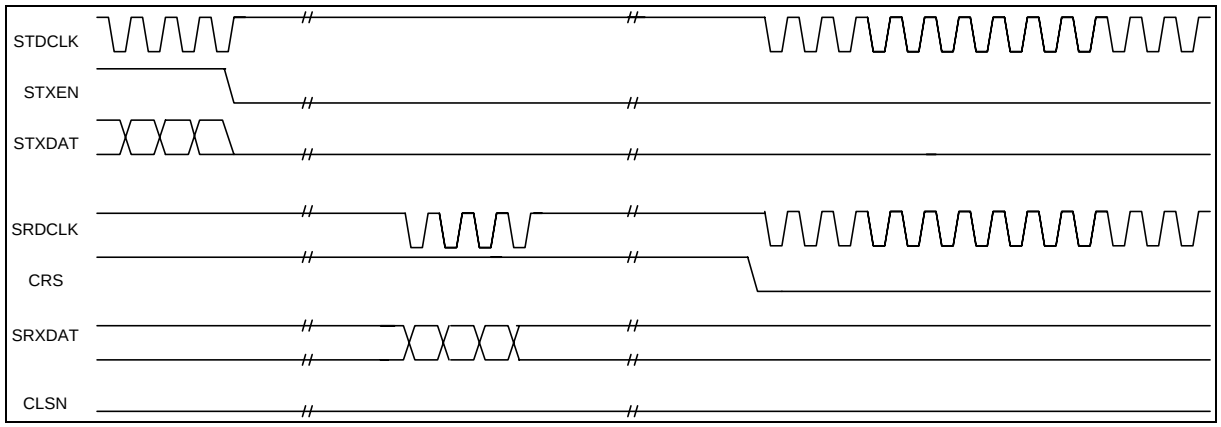
TXPKT - STXEN Asserted
Figure 14



STDCLK continues to toggle until SFD is observed, as shown in the first section on the above diagram. At this point, STDCLK is disabled until the AID header has been transmitted on the wire or until CLS has been detected. At this time SRDCLK starts toggling, thereby shifting 32 bits of preamble and SFD back to the MAC. Sometime later, the STDCLK restarts as symbols get sent onto the wire in an analogous manner as SRDCLK during packet reception.

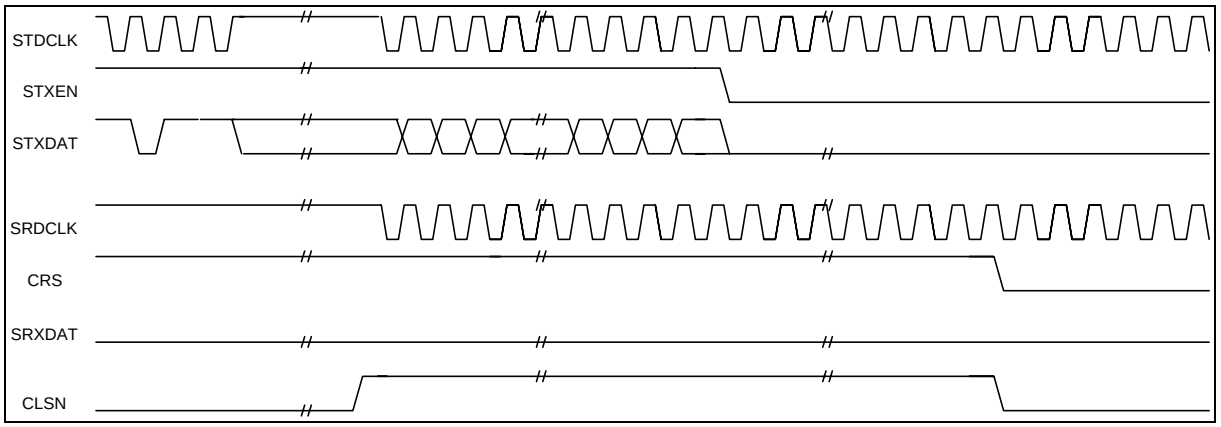
TXPKT - SRDCLK Active
Figure 15

General Purpose Serial Interface (continued)



Once STXEN is cleared, the last symbol gets encoded and transmitted. The looped-back data is presented back to the MAC and sometime later CRS falls. Once CRS falls, STDCLK and SRDCLK toggle for 97 clocks after which the system returns to the Idle state.

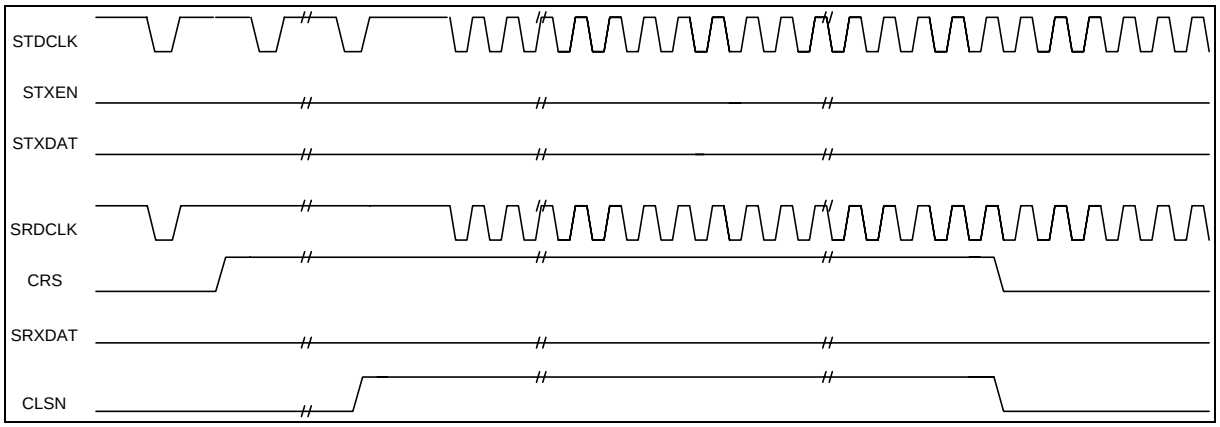
TXPKT - STXEN Cleared
Figure 16



CLSN will be asserted some time after the preamble and SFD have been clocked in. STDCLK and SRDCLK are then clocked until CRS drops. STXEN drops sometime after CLSN was asserted. CRS and CLSN are dropped together after more than 500 clocks. STDCLK and SRDCLK keep toggling for approximately another 100 clock cycles, then the system returns to the idle state.

TXPKT - CLSN Asserted
Figure 17

General Purpose Serial Interface (continued)



CLSN may be asserted up to 120us after CRS has been asserted. Once CLSN has been asserted STDCLK and SRDCLK run at a period of 233.3ns per cycle until 97 cycles after CLSN and CRS are cleared. It can take up to about 60us for CRS to clear.

RXPKT - CLSN Cleared
Figure 18

Serial Peripheral Interface (SPI) Bus

When INTFSEL is asserted, the DM9801A is configured to operate in SPI mode. While configured to operate in SPI mode, the DM9801A can act as a SPI Slave or SPI Master. Asserting SMODE places the DM9801A in SPI Slave mode. Clearing SMODE places the DM9801A in SPI Master Mode.

The SPI (Serial Peripheral Interface) Bus uses a four-wired serial interface to obtain and control the status of the physical layer through the SPI Bus interface. The serial control interface consists of SI (serial data input), SO (serial data output), SCLK (serial clock), and SCS# (serial interface chip select) signals. When operating in Master mode the DM9801A drives the SCLK and SCS# signals, when operating in Slave mode these signals are inputs.

SPI-Slave Mode (Valid only in GPSI Mode)

When SMODE is asserted the DM9801A is configured for SPI Slave operation. Commands are issued to the DM9801A by asserting the SCS# signal, shifting in an 8-bit opcode followed by a register address and an end delimiter. If the operation is a write, the address is followed by an 8-bit data byte. If the operation is a read, the SO pin will shift out an 8-bit data byte representing the contents of the register referenced by the address field. Only one command can be sent in one SCS# cycle. The DM9801A does not support multiple byte reads or writes.

SPI-Master Mode (Valid only in GPSI Mode)

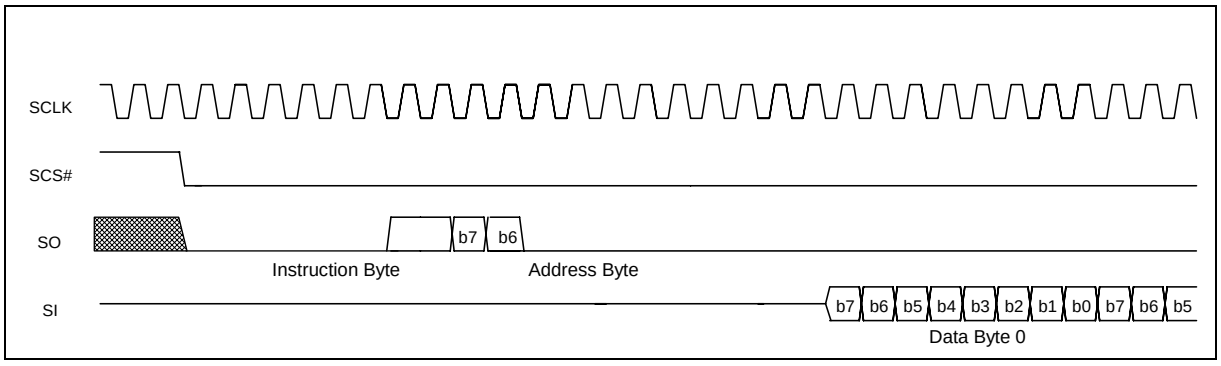
When SMODE is cleared the DM9801A is configured for SPI Master operation. When the DM9801A is configured for SPI-Master operation, it will load all programmable registers from an external SPI type EEPROM. The memory locations loaded may be offset via the boot page pins, BP[1:0], allowing a single 256 byte serial EEPROM to hold four distinct sets of default register values.

After RESET# has cleared the DM9801A will assert SCS#, shift out a Read opcode (0x03), followed by the initial address to be read (as modified by the Boot Page pins). The DM9801A will then shift in the memory contents, auto incrementing the register address being programmed every 8-bits. Once all 64-bytes have been read, the DM9801A releases SCS#. The SCLK continues to run. Opcodes are shown in Table 1.

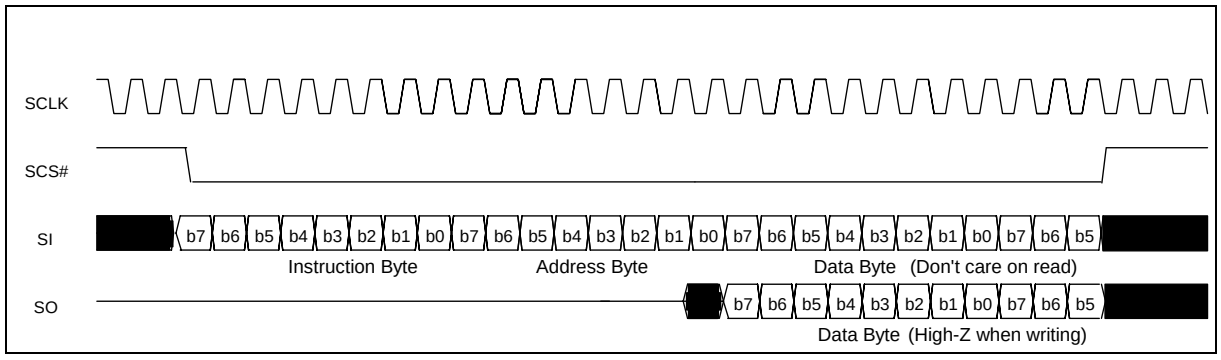
Instruction Format	Instruction Name
0000 0110	Set WE
0000 0100	Clear WE
0000 0011	Read
0000 0010	Write

OPCODES
Table 1

Serial Peripheral Interface (SPI) Bus (continued)



SPI Master Mode Timing
Figure 19



SPI Slave Mode Timing
Figure 20

MII and GM_Mode Serial Management Register Map

Register Address	Register Name	Access Type	Default Value	Description
0	BMCR	RW	0x0000	Basic Mode Control Register (valid only when MII Emulation Support is enabled, Config1 = 1).
1	BMSR	RO	0x0820	Basic Mode Status Register (valid only when MII Emulation Support is enabled, Config1 = 1).
2	PHYIDR1	RO	0x0181	PHY Identifier Register #1 (valid only when MII Emulation Support is enabled, Config1 = 1).
3	PHYIDR2	RO	0xB903	PHY Identifier Register #2 (valid only when MII Emulation Support is enabled, Config1 = 1).
4	ANAR	RO	0x0021	Auto-negotiation Advertisement Register (valid only when MII Emulation Support is enabled, Config1 = 1).
5	ANLPAR	RO	0x0021	Auto-negotiation Link Partner Ability Register (valid only when MII Emulation Support is enabled, Config1 = 1). When LINK is down, default value becomes 0x0000.
6	ANER	RO	0x0000	Auto-Negotiation Expansion Register (valid only when MII Emulation Support is enabled, Config1 = 1).
16	CNTRL	RW	0x1005	Control Register
17	STATUS	RW	0x0005	Status Register
18	IMASK	RW	0x0000	Interrupt Mask Register
19	ISTAT	RW	0x0080	Interrupt Status Register
20	TX_PCOM_HI	RW	0x0000	Transmit PHY Communication Hi Word
21	TX_PCOM_LO	RW	0x0000	Transmit PHY Communication Lo Word
22	RX_PCOM_HI	RW	0x0000	Receive PHY Communication Hi Word
23	RX_PCOM_LO	RW	0x0000	Receive PHY Communication Lo Word
24	PEAK_NOISE	RW	0xFF07	Peak Level and Noise Level Register
25	NOISE_CNTRL_A	RW	0xC207	Noise Ceiling and Noise Floor Register
26	NOISE_CNTRL_B	RW	0x00F4	Noise Events and Noise Attack Register
27	FWENA	RW	0x0000	Four Wire Enable and Disable Link Register
28	AID_ADDRESS	RW	0x0000	AID Address Register
29	AID_CNTRL	RW	0x4014	AID Interval and AID ISBI Register
30	SYM_CNTRL	RW	0x1C2C	DATA ISBI Control Register
31	TX_SIG_CNTRL	RW	0x4404	Transmit Pulse Control Register

Key to Default

In the register description that follows, the default column takes the form:

<Reset Value>, <Access Type> / <Attribute(s)>

Where

<Reset Value>:

1	Bit set to logic one
0	Bit set to logic zero
X	No default value
(PIN#)	Value latched in from pin # at reset

<Access Type>:

RO = Read only

RW = Read/Write

<Attribute (s)>:

SC = Self clearing

P = Value permanently set

LL = Latching low

LH = Latching high

Basic Mode Control Register (BMCR) - Register 0

Bit	Bit Name	Default	Description
0.15	Reset	0, RW/SC	**Reset:** 1=Software reset 0=Normal operation When set this bit configures the PHY status and control registers to their default states. This bit will return a value of one until the reset process is complete
0.14	Loopback	0, RW	**Loopback:** Loopback control register for MII operation. Always disabled (Loopback = 0) for GM_MODE operation. 1=Loopback enabled 0=Normal operation
0.13	Speed Selection	0, RO/P	**Speed Select:** The DM9801A does not support this function. This bit is permanently set to 0
0.12	Auto-negotiation Enable	0,RO/P	**Auto-negotiation Enable:** The DM9801A does not support this function. This bit is permanently set to 0
0.11	Power Down	0,RW	**Power Down:** 1=Power down enabled 0=Normal operation Setting this bit will power down the DM9801A with the exception of the crystal oscillator circuit.
0.10	Isolate	0,RW	**Isolate:** 1= Isolate 0= Normal Operation When this bit is set the data path will be isolated from the MII interface. TX_CLK, RX_CLK, RX_DV, RXD[3:0], COL and CRS will be placed in a high impedance state. The management interface is not effected by this bit. When the PHY address is set to 00000 the isolate bit will be set upon power-up/reset.
0.9	Restart Auto-negotiation	0,RO/P	**Restart Auto-negotiation:** The DM9801A does not support this function. This bit is permanently set to 0
0.8	Duplex Mode	0,RO/P	**Duplex Mode:** The DM9801A does not support this function. This bit is permanently set to 0
0.7	Collision Test	0,RO/P	**Collision Test:** The DM9801A does not support this function. This bit is permanently set to 0
0.6-0.0	Reserved	0,RO	**Reserved:** Write as 0, ignore on read

Basic Mode Status Register (BMSR) - Register 1

Bit	Bit Name	Default	Description
1.15	100Base-T4	0,RO/P	**Reserved:** The DM9801A does not support this function. This bit is permanently set to 0
1.14	100Base-TX Full Duplex	0,RO/P	**Reserved:** The DM9801A does not support this function. This bit is permanently set to 0
1.13	100Base-TX Half Duplex	0,RO/P	**Reserved:** The DM9801A does not support this function. This bit is permanently set to 0
1.12	10Base-T Full Duplex	0,RO/P	**Reserved:** The DM9801A does not support this function. This bit is permanently set to 0
1.11	10Base-T Half Duplex	1,RO/P	**Reserved:** The DM9801A supports half Duplex Operation only. This bit is permanently set to 1
1.10-1.7	Reserved	0,RO	**Reserved:** Write as 0, ignore on read
1.6	MF Preamble Suppression	0,RO/P	**MII Frame Preamble Suppression:** 1=PHY will accept management frames with preamble suppressed 0=PHY will not accept management frames with preamble suppressed
1.5	Auto-negotiation Complete	1,RO/P	**Auto-negotiation Complete:** The DM9801A does not support this function. This bit is permanently set to 1
1.4	Remote Fault	0,RO/P	**Remote Fault:** The DM9801A does not support this function. This bit is permanently set to 0
1.3	Auto-negotiation Ability	0,RO/P	**Auto Configuration Ability:** The DM9801A does not support this function. This bit is permanently set to 0
1.2	Link Status	0,RO/LL	**Link Status:** 1=Valid link established 0=Link not established The link status bit is implemented with a latching function, so that the occurrence of a link failure condition causes the Link Status bit to be cleared and remain cleared until it is read via the management interface
1.1	Jabber Detect	0,RO/P	**Jabber Detect:** The DM9801A does not support this function. This bit is permanently set to 0
1.0	Extended Capability	0,RO/P	**Extended Capability:** The DM9801A does not support this function. This bit is permanently set to 0

PHY ID Identifier Register #1 (PHYIDR1) - Register 2

The PHY Identifier Registers #1 and #2 work together in a single identifier of the DM9801A. The Identifier consists of a concatenation of the **Organizationally Unique Identifier** (OUI), a vendor's model number, and a model revision number. DAVICOM Semiconductor's IEEE assigned OUI is 00606E.

Bit	Bit Name	Default	Description
2.15-2.0	OUI_MSB	<0181H>	**OUI Most Significant Bits:** This register stores bits 3 - 18 of the OUI (00606E) to bits 15 - 0 of this register respectively. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bit 1 and 2)

PHY Identifier Register #2 (PHYIDR2) - Register 3

Bit	Bit Name	Default	Description
3.15-3.10	OUI_LSB	<101110>,RO/P	**OUI Least Significant Bits:** Bits 19 - 24 of the OUI (00606E) are mapped to bits 15 - 10 of this register respectively
3.9-3.4	VNDR_MDL	<010000>,RO/P	**Vendor Model Number:** Six bits of the vendor model number mapped to bits 9 - 4 (most significant bit to bit 9)
3.3-3.0	MDL_REV	<0011>,RO/P	**Model Revision Number:** Four bits of the vendor model revision number mapped to bits 3 - 0 (most significant bit to bit 3)

Auto-negotiation Advertisement Register(ANAR) - Register 4

This register contains the advertised abilities of the DM9801A device as they will be transmitted to link partners during Auto-negotiation.

Bit	Bit Name	Default	Description
4.15	NP	0,RO/P	**Next Page Indication:** The DM9801A does not support the next page function. This bit is permanently set to 0
4.14	ACK	0,RO/P	**Acknowledge:** 1=Link partner ability data reception acknowledged 0=Not acknowledged The DM9801A's state machine will automatically control this bit. Software should not attempt to write to this bit.
4.13	RF	0, RO/P	**Remote Fault:** The DM9801A does not support this function. This bit is permanently set to 0
4.12-4.11	Reserved	0, RO	**Reserved:** Write as 0, ignore on read
4.10	FCS	0, RO/P	**Flow Control Support:** The DM9801A does not support this function. This bit is permanently set to 0
4.9	T4	0, RO/P	**100Base-T4 Support:** The DM9801A does not support this function. This bit is permanently set to 0
4.8	TX_FDX	0, RO/P	**100Base-TX Full Duplex Support:** The DM9801A does not support this function. This bit is permanently set to 0
4.7	TX_HDX	0, RO/P	**100Base-TX Support:** The DM9801A does not support this function. This bit is permanently set to 0

Auto-negotiation Advertisement Register(ANAR) - Register 4 (continued)

Bit	Bit Name	Default	Description
4.6	10_FDX	0, RO/P	**10Base-T Full Duplex Support:** The DM9801A does not support this function. This bit is permanently set to 0
4.5	10_HDX	1, RO/P	**10Base-T Support:** 1=10Base-T Half Duplex supported by the link partner 0=10Base-T Half Duplex not supported by the link partner
4.4-4.0	Selector	<00001>, RO/P	**Protocol Selection Bits:** These bits contain the binary encoded protocol selector supported by this node. <00001> indicates that this device supports IEEE 802.3 CSMA/CD.

Auto-negotiation Link Partner Ability Register (ANLPAR) - Register 5

This register contains the advertised abilities of the link partner as they are received during Auto-negotiation.

Bit	Bit Name	Default	Description
5.15	NP	0, RO/P	**Next Page Indication:** 0= Link partner, no next page available 1= Link partner, next page available
5.14	ACK	0, RO/P	**Acknowledge:** 1=Link partner ability data reception acknowledged 0=Not acknowledged The DM9801A's state machine will automatically control this bit. Software should not attempt to write to this bit.
5.13	RF	0, RO/P	**Remote Fault:** 1=Remote fault indicated by link partner 0=No remote fault indicated by link partner
5.12-5.10	Reserved	0, RO	**Reserved:** Write as 0, ignore on read
5.9	T4	0, RO/P	**100Base-T4 Support:** The DM9801A does not support this function. This bit is permanently set to 0
5.8	TX_FDX	0, RO/P	**100Base-TX Full Duplex Support:** The DM9801A does not support this function. This bit is permanently set to 0
5.7	TX_HDX	0, RO/P	**100Base-TX Support:** The DM9801A does not support this function. This bit is permanently set to 0
5.6	10_FDX	0, RO/P	**10Base-T Full Duplex Support:** The DM9801A does not support this function. This bit is permanently set to 0
5.5	10_HDX	1, RO	**10Base-T Support:** 1=10Base-T Half Duplex supported by the link partner 0=10Base-T Half Duplex not supported by the link partner
5.4-5.0	Selector	<00001>, RO	**Protocol Selection Bits:** Link partner binary encoded protocol selector

Auto-negotiation Expansion Register (ANER) - Register 6

Bit	Bit Name	Default	Description
6.15-6.5	Reserved	0, RO	**Reserved:** Write as 0, ignore on read
6.4	PDF	0, RO/P	**Local Device Parallel Detection Fault:** PDF=1: A fault detected via parallel detection function. PDF=0: No fault detected via parallel detection function DM9801A does not support this function, so this bit is always 0.
6.3	LP_NP_ABLE	0, RO/P	**Link Partner Next Page Able:** LP_NP_ABLE=1: Link partner, next page available LP_NP_ABLE=0: Link partner, no next page DM9801A does not support this function, so this bit is always 0.
6.2	NP_ABLE	0,RO/P	**Local Device Next Page Able:** NP_ABLE=1: DM9801A, next page available NP_ABLE=0: DM9801A, no next page DM9801A does not support this function, so this bit is always 0.
6.1	PAGE_RX	0, RO/P	**New Page Received:** A new link code word page received. This bit will be automatically cleared when the register (Register 6) is read by management. DM9801A does not support this function, so this bit is always 0.
6.0	LP_AN_ABLE	0, RO/P	**Link Partner Auto-negotiation Able:** LP_AN_ABLE=1 indicates that the link partner supports Auto-negotiation. DM9801A does not support this function, so this bit is always 0.

Control Register - Register 16

Bit	Bit Name	Default	Description
16.15	IG_RMT_CMDS	0,RW	**Ignore Remote Commands:** 1=Remote commands are ignored 0=Remote commands will be accepted from any node in the network. The value of the CMDENA pin is latched into this bit at power-up/reset.
16.14	AVG_PEAK_RL	0,RW	**Average Peak Rule:** 1= Average peak with measured noise instead of noise + 25% 0= Normal operation
16.13	EN_SHORT_CD	0,RW	**Enable Short CD:** 1= Enable short CD noise rule Do not count bad SYNC if CD is longer than 160uS 0= Normal operation
16.12	DIS_INC_NOISE	1,RW	**Disable Increment of Noise:** 1= Disable 25% increase of noise slice when in a packet 0= Normal operation
16.11	CMD_LO_PWR	0,RW	**Command Low Power:** 1= Transmit power is set to low 0= Normal operation Remote commands will be issued if this bit is set
16.10	CMD_HI_PWR	0,RW	**Command High Power:** 1= Transmit power is set to high 0= Normal operation Remote commands will be issued if this bit is set

16.9	CMD_LO_SPD	0,RW	**Command Low Speed:** 1= Transmit speed is set to low 0= Normal operation Remote commands will be issued if this bit is set
16.8	CMD_HI_SPD	0,RW	**Command High Speed:** 1= Transmit speed is set to high 0= Normal operation Remote commands will be issued if this bit is set
16.7	AID_ADR_NEG	0,RW	**AID Address Negotiation:** 1= Stop AID address negotiation 0= Normal operation
16.6	CLR_NS_EVNT	0,RW	**Clear Noise Event Register:** 1= Clear the Noise Event Register 0= Normal operation
16.5	SLC_LVL_ADP	0,RW	**Slice Level Adaptation:** 1= Slice level adaptation is disabled (stopped). 0= Slice level adaptation is enabled
16.4	PWR_DWN	0,RW	**Power Down:** Writing a 1 to this bit will cause DM9801A to enter Sleep mode and power down all circuits except the oscillator and clock generator circuit. To exit Sleep mode, write 0 to this bit position. The prior configuration will be retained when the sleep state is terminated, but the state machine will be reset
16.3	Reserved	0,RW	**Reserved:** This bit must be written as 0
16.2	Speed	1, RW	**Speed:** 1= high speed 0= low speed This bit indicates the network speed is set to high as selected by the status of the SPDSEL pin during power-up/reset.
16.1	Power	0, RW	**Power:** 1= high power 0= low power This bit indicates the network power is set to high as selected by the status of the PWRSEL pin during power-up/reset.
16.0	Reserved	1,RW	**Reserved:** This bit must be written as 1

Status Register - Register 17

Bit	Bit Name	Default	Description
17.15 – 17.11	Reserved	0, RW	**Reserved:** Write as 0, ignore on read
17.10	LINK_STA	0, RO	**Link Status:** This bit reports the Link Status of the DM9801A
17.9	DIS_LED_STR	0, RW	**Disable LED Stretchers:** This bit disables LED pulse stretchers
17.8	Reserved	0, RW	**Reserved:** Write as 0, ignore on read
17.7	RX_RESERVED	0, RW	**Receiving station reserved.**

17.6	RX_PWR	0, RO	**Receive Power:** This bit is an indication of the current receive signal power. 1= The receive signal power is high. 0= The receive signal power is low.
17.5	RX_SPD	0, RO	**Receive Speed:** This bit is an indication of the current receive speed. 1= The receive speed is high. 0= The receive speed is low.
17.4	RX_VER	0, RO	**Receive Version:** This bit is an indication of the current receive version. 1= The receive version is not version 0. 0= The receive version is version 0.
17.3 - 17.0	Reserved	<0101>, RW	**Reserved:** Write as 0, ignore on read

IMASK (Interrupt Mask) Register - Register 18

Bit	Bit Name	Default	Description
18.15 – 18.10	Software Interrupts	0,RW	**Software Interrupts:** 1= Software interrupts will not activate the INT# pin 0= Software interrupts will activate the INT# pin
18.9	MSK_RX_PCOM	0,RW	**Mask RXPCOM Valid:** 1= RX_PCOM_VAL will not activate the INT# pin 0= RX_PCOM_VAL will activate the INT# pin
18.8	MSK_TX_PCOM	0,RW	**Mask TXPCOM Ready:** 1= TX_PCOM_RDY will not activate the INT# pin 0= TX_PCOM_RDY will activate the INT# pin
18.7 – 18.4	Reserved	0,RW	**Reserved:** Write as 0, ignore on read
18.3	MSK_PKT_RCV	0,RW	**Mask Packet Received:** 1= Packet Received will not activate the INT# pin 0= Packet Received will activate the INT# pin
18.2	MSK_PKT_XMIT	0,RW	**Packet Transmitted:** 1= Packet Transmitted will not activate the INT# pin 0= Packet Transmitted will activate the INT# pin
18.1	MSK_RMT_RCV	0,RW	**Remote Command Received:** 1= Remote Command Received will not activate the INT# pin 0= Remote Command Received will activate the INT# pin
18.0	MSK_CMD_SNT	0,RW	**Remote Command Sent:** 1= Remote Command Sent will not activate the INT# pin 0= Remote Command Sent will activate the INT# pin.

ISTAT (Interrupt Status) Register - Register 19

This register reports the state of each interrupt source regardless of the state of the IMASK Register.

Bit	Bit Name	Default	Description
19.15 – 19.10	Software Interrupts	0,RW	**Software Interrupts:** When set any bit of those registers indicates software interrupt is on.
19.9	RX_PCOM_VAL	0,RW	**RXPCOM Valid:** When set this bit indicates a non-null RX_PCOM has been received. Accessing the high byte of the RX_PCOM register clears this bit.

19.8	TX_PCOM_RDY	0,RW	**TXPCOM Ready:** When set this bit indicates a non-null TX_PCOM has been loaded into the TX_PCOM register.
19.7 – 19.4	Reserved	<1000>,RW	**Reserved:** Write as 0, ignore on read
19.3	PKT_RCVD	0,RW	**Packet Received:** When set this bit indicates a packet has been received
19.2	PKT_XMITD	0,RW	**Packet Transmitted:** When set this bit indicates a packet has been transmitted
19.1	RMT_CMD_RCV	0,RW	**Remote Command Received:** When set this bit indicates a valid remote command has been received.
19.0	RMT_CMD_SNT	0,RW	**Remote Command Sent:** When set this bit indicates a valid remote command has been sent.

TX_PCOM High Register - Register 20

Bit	Bit Name	Default	Description
20.15 – 20.0	TX_PCOM_HI	0, RW	**TX_PCOM_HI:** The high order word of the 32-bit transmitted data field to be used for out-of-band communications between PHY management entities. The PHY will send all-0 PCOMs until the high byte has been accessed. An access of any of the four TX_PCOM bytes will clear the TX_PCOM_RDY bit in the ISTAT register.

TX_PCOM Low Register - Register 21

Bit	Bit Name	Default	Description
21.15 – 21.0	TX_PCOM_LO	0, RW	**TX_PCOM_LO:** The low order word of the 32-bit transmitted data field to be used for out-of-band communications between PHY management entities. The PHY will send all-0 PCOMs until the high byte in TX_PCOM_HI has been accessed. An access of any of the four TX_PCOM bytes will clear the TX_PCOM_RDY bit in the ISTAT register.

RX_PCOM High Register - Register 22

Bit	Bit Name	Default	Description
22.15 – 22.0	RX_PCOM_HI	0, RW	**RX_PCOM_HI:** The high order word of the 32-bit receive data field to be used for out-of-band communications between PHY management entities. A non-null receive PCOM will set the RX_PCOM_VAL bit in the ISTAT register. An access of the high byte of this register will clear the RX_PCOM_VAL bit in the ISTAT register.

RX_PCOM Low Register - Register 23

Bit	Bit Name	Default	Description
23.15 – 23.0	RX_PCOM_LO	0, RW	**RX_PCOM_LO:** The low order word of the 32-bit receive data field to be used for out-of-band communications between PHY management entities. A non-null receive PCOM will set the RX_PCOM_VAL bit in the ISTAT register. An access of the high byte of the RX_PCOM_HI register will clear the RX_PCOM_VAL bit in the ISTAT register.

Peak Noise Register - Register 24

Bit	Bit Name	Default	Description
24.15 - 24.8	PEAK_LEVEL	0xFF, RW	**Peak Level:** This is a measurement of the peak level of the last valid (non-collision) AID received also, the maximum allowable value of the noise measurement. If NOISE_LEVEL exceeds PEAK_LEVEL, NOISE_LEVEL is reset to NOISE_FLOOR.
24.7 - 24.0	NOISE_LEVEL	0x07, RW	**NOISE LEVEL:** This is the digital value of the SLICE_LVL_NOISE output. It is effectively a measure of the noise level on the wire. When auto-adaptation is enabled (bit 5 of the Control register is false) this register is updated with the current noise count every 50n Secs. When adaptation is disabled, this register can be written and is used to generate both the SLICE_LVL_NOISE and the SLICE_LVL_DATA signals.

Noise Control A Register - Register 25

Bit	Bit Name	Default	Description
25.15 - 25.8	NSE_CEILING	0xC2, RW	**Noise Ceiling:** The maximum value of the NOISE_LEVEL measurement.
25.7 - 25.0	NSE_FLOOR	0x07, RW	**Noise Floor:** The minimum value of the NOISE_LEVEL measurement.

Noise Control B Register - Register 26

Bit	Bit Name	Default	Description
26.15 - 26.8	NSE_EVENTS	0x00, RW	**Noise Events:** An 8 bit counter that records the number of noise events detected. Overflows are held as 0xFF. This register is cleared by setting bit 6 of the Control register (CLR_NS_EVNT).
26.7 - 26.0	NSE_ATTACK	0xF4, RW	**Noise Attack:** Sets the attack characteristics of the noise algorithm. The high nibble sets the number of noise events needed to raise the NOISE_LEVEL immediately, while the low nibble is the number of noise events needed to raise the NOISE_LEVEL at the end of an 870 msec period.

Aid Address Register - Register 27

Bit	Bit Name	Default	Description
27.15 - 27.2	Reserved	0, RW	**Reserved:** These bits will always be read as 0.

27.1	DIS_LNK	0, RW	**Disable Link:** This bit disables link integrity feature.
27.0	FWENA	0, RW	**Four Wire Enable:** When read this bit will indicate the status of FWENA (pin 57) as read during power up. If the FWENA pin status is 1 on power up, this bit can be written to change the FWENA status. If the FWENA pin status is 0 on power up, writes to this bit are ignored.

Aid Address Register - Register 28

Bit	Bit Name	Default	Description
28.15 - 28.8	Reserved	0x00, RW	**Reserved:** These bits will always be read as 0.
28.7 - 28.0	AID_ADDRESS	0x00, RW	**AID Address:** Unless bit 7 of the Control register is set, the DM9801A is assured to select a unique AID Address. Addresses above 0xEF are reserved. Address 0xFF is defined to indicate a Remote Command.

Aid Control Register - Register 29

Bit	Bit Name	Default	Description
29.15 - 29.8	AID_ISBI	0x40, RW	**AID Inter Symbol Blanking Interval:** This value defines the number of TCLKs (116.7ns) between AID pulses for symbol 0.
29.7 - 29.0	AID_INTERVAL	0x14, RW	**AID Interval:** This value defines the number of TCLKs (116.7ns) separating AID symbols.

Symbol Control Register - Register 30

Bit	Bit Name	Default	Description
30.15 - 30.8	ISBI_FAST	0x1C, RW	**Inter Symbol Blanking Interval (High Speed):** This value defines the number of TCLKs (116.7ns) between data pulses for symbol 0 in High speed
30.7 - 30.0	ISBI_SLOW	0x2C, RW	**Inter Symbol Blanking Interval (Low Speed):** This value defines the number of TCLKs (116.7ns) between data pulses for symbol 0 in low speed

TX Signal Control Register - Register 31

Bit	Bit Name	Default	Description
31.15 - 31.8	TX_PLS_CYCLS	0x44, RW	**Transmit Pulse Cycles:** The low nibble of this register indicates the number of pulses on the HNN pins while the high nibble indicates the number of pulses on the HNP pins.
31.7 - 31.0	TX_PLS_WIDTH	0x04, RW	**Transmit Pulse Width:** This value determines the duration in OSC cycles (16.7 ns) that a transmit pulse lasts.

SPI Serial Management Register Map (INTFSEL = 1, GPSI Mode)

Register Address	Register Name	Access Type	Default Value	Description
1-0	CNTRL	RW	0x1005	Control Registers
3-2	STATUS	RW	0x0005	Status Registers
5-4	IMASK	RW	0x0000	Interrupt Mask Registers
7-6	ISTAT	RW	0x0080	Interrupt Status Registers
9-8	TX_PCOM_LO	RW	0x0000	Transmit PHY Communication Low Word
11-10	TX_PCOM_HI	RW	0x0000	Transmit PHY Communication High Word
13-12	RX_PCOM_LO	RW	0x0000	Receive PHY Communication Low Word
15-14	RX_PCOM_HI	RW	0x0000	Receive PHY Communication High Word
17-16	PEAK_NOISE	RW	0xFF07	PEAK Level and Noise Level Registers
19-18	NOISE_CNTRL_A	RW	0xC207	Noise Ceiling and Noise Floor Registers
21-20	NOISE_CNTRL_B	RW	0x00F4	Noise Events and Noise Attack Registers
22	FWENA	RW	0x00	Four Wire Enable and Link Disable Registers
25	AID_ADDRESS	RW	0x00	AID Address Register
27-26	AID_CNTRL	RW	0x4014	AID Interval and AID ISBI Registers
29-28	SYM_CNTRL	RW	0x1C2C	DATA ISBI Control Registers
31-30	TX_SIG_CNTRL	RW	0x4404	Transmit Pulse Control Registers

SPI Serial Management Control Register - Register 0 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
0.7	AID_ADR_NEG	0,RW	**AID Address Negotiation:** 1= Stop AID address negotiation 0= Normal operation
0.6	CLR_NS_EVNT	0,RW	**Clear Noise Event Register:** 1= Clear the Noise Event Register 0= Normal operation
0.5	SLC_LVL_ADP	0,RW	**Slice Level Adaptation:** 1= Slice level adaptation is disabled (stopped). 0= Slice level adaptation is enabled
0.4	PWR_DWN	0,RW	**Power Down:** Writing a 1 to this bit will cause DM9801A to enter Sleep mode and power down all circuits except the oscillator and clock generator circuit. To exit Sleep mode, write 0 to this bit position. The prior configuration will be retained when the sleep state is terminated, but the state machine will be reset
0.3	Reserved	0,RW	**Reserved:** This bit must be written as 0
0.2	Speed	1,RW	**Speed:** 1= high speed 0= low speed This bit indicates the network speed is set to high as selected by the status of the SPDSEL pin during power-up/reset.
0.1	POWER	0,RW	**Power:** 1= high power 0= low power This bit indicates the network power is set to high as selected by the status of the PWRSEL pin during power-up/reset.

SPI Serial Management Control Register - Register 0 (continued) **(INTFSEL = 1, GPSI Mode)**

Bit	Bit Name	Default	Description
0.0	Reserved	1,RW	**Reserved:** This bit must be written as 1

SPI Serial Management Control Register - Register 1 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
1.7	IG_RMT_CMDS	0,RW	**Ignore Remote Commands:** 1=Remote commands are ignored 0=Remote commands will be accepted from any node in the network. The value of the CMDENA pin is latched into this bit at power-up/reset.
1.6	AVG_PEAK_RL	0,RW	**Average Peak Rule:** 1= Average peak with measured noise instead of noise + 25% 0= Normal operation
1.5	EN_SHORT_CD	0,RW	**Enable Short CD:** 1= Enable short CD noise rule Do not count bad SYNC if CD is longer than 160uS 0= Normal operation
1.4	DIS_INC_NOISE	1,RW	**Disable Increment of Noise:** 1= Disable 25% increase of noise slice when in a packet 0= Normal operation
1.3	CMD_LO_PWR	0,RW	**Command Low Power:** 1= Transmit power is set to low 0= Normal operation Remote commands will be issued if this bit is set
1.2	CMD_HI_PWR	0,RW	**Command High Power:** 1= Transmit power is set to high 0= Normal operation Remote commands will be issued if this bit is set
1.1	CMD_LO_SPD	0,RW	**Command Low Speed:** 1= Transmit speed is set to low 0= Normal operation Remote commands will be issued if this bit is set
1.0	CMD_HI_SPD	0,RW	**Command High Speed:** 1= Transmit speed is set to high 0= Normal operation Remote commands will be issued if this bit is set

SPI Serial Management Status Register - Register 2 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
2.7	RX_RESERVED	0, RW	**Receiving station reserved.**
2.6	RX_PWR	0, RO	**Receive Power:** This bit is an indication of the current receive signal power. 1= The receive signal power is high. 0= The receive signal power is low.
2.5	RX_SPD	0, RO	**Receive Speed:** This bit is an indication of the current receive speed. 1= The receive speed is high. 0= The receive speed is low.

SPI Serial Management Status Register - Register 2 (continued) **(INTFSEL = 1, GPSI Mode)**

Bit	Bit Name	Default	Description
2.4	RX_VER	0, RO	**Receive Version:** This bit is an indication of the current receive version. 1= The receive version is not version 0. 0= The receive version is version 0.
2.3 – 2.0	Reserved	<0101>, RW	**Reserved:** Write as 0, ignore on read

SPI Serial Management Status Register - Register 3 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
3.7	INVRT_CRS	0, RW	**Invert CRS Signal:** When this bit is set the CRS signal on the DM9801A will be inverted.
3.6	INVRT_COL	0, RW	**Invert COL Signal:** When this bit is set the COL signal on the DM9801A will be inverted.
3.5	INVRT_TXCLK	0, RW	**Invert Transmit Clock:** When this bit is set the TX_CLK signal on the DM9801A will be inverted.
3.4	INVRT_RXCLK	0, RW	**Invert Receive Clock:** When this bit is set the RX_CLK signal on the DM9801A will be inverted.
3.3	Reserved	0, RW	**Reserved:** Write as 0, ignore on read
3.2	LINK_STA	0, RO	**Link Status:** This bit reports the Link Status of the DM9801A
3.1	DIS_LED_STR	0, RW	**Disable LED Stretchers:** This bit disables LED pulse stretchers
3.0	Reserved	0, RW	**Reserved:** Write as 0, ignore on read

IMASKA (Interrupt Mask A) Register - Register 4 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
4.7 – 4.4	Reserved	0,RW	**Reserved:** Write as 0, ignore on read
4.3	MSK_PKT_RCV	0,RW	**Mask Packet Received:** 1= Packet Received will not activate the INT# pin 0= Packet Received will activate the INT# pin
4.2	MSK_PKT_XMIT	0,RW	**Packet Transmitted:** 1= Packet Transmitted will not activate the INT# pin 0= Packet Transmitted will activate the INT# pin
4.1	MSK_RMT_RCV	0,RW	**Remote Command Received:** 1= Remote Command Received will not activate the INT# pin 0= Remote Command Received will activate the INT# pin
4.0	MSK_CMD_SNT	0,RW	**Remote Command Sent:** 1= Remote Command Sent will not activate the INT# pin 0= Remote Command Sent will activate the INT# pin.

IMASKB (Interrupt Mask B) Register - Register 5 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description

5.7 – 5.2	Software Interrupts	0,RW	**Software Interrupts:** 1= Software interrupts will not activate the INT# pin 0= Software interrupts will activate the INT# pin
5.1	MSK_RX_PCOM	0,RW	**Mask RXPCOM Valid:** 1= RX_PCOM_VAL will not activate the INT# pin 0= RX_PCOM_VAL will activate the INT# pin
5.0	MSK_TX_PCOM	0,RW	**Mask TXPCOM Ready:** 1= TX_PCOM_RDY will not activate the INT# pin 0= TX_PCOM_RDY will activate the INT# pin

ISTAT (Interrupt Status A) Register - Register 6 (INTFSEL = 1, GPSI Mode)

This register reports the state of each interrupt source regardless of the state of the IMASK Register.

Bit	Bit Name	Default	Description
6.7 – 6.4	Reserved	<1000>,RW	**Reserved:** Write as 0, ignore on read
6.3	PKT_RCVD	0,RW	**Packet Received:** When set this bit indicates a packet has been received
6.2	PKT_XMITD	0,RW	**Packet Transmitted:** When set this bit indicates a packet has been transmitted
6.1	RMT_CMD_RCV	0,RW	**Remote Command Received:** When set this bit indicates a valid remote command has been received.
6.0	RMT_CMD_SNT	0,RW	**Remote Command Sent:** When set this bit indicates a valid remote command has been sent.

ISTAT (Interrupt Status B) Register - Register 7 (INTFSEL = 1, GPSI Mode)

This register reports the state of each interrupt source regardless of the state of the IMASK Register.

Bit	Bit Name	Default	Description
7.7 – 7.2	Software Interrupts	0,RW	**Software Interrupts:** When set any bit of those registers indicates software interrupt is on.
7.1	RX_PCOM_VAL	0,RW	**RXPCOM Valid:** When set this bit indicates a non-null RX_PCOM has been received. Accessing the high byte of the RX_PCOM register clears this bit.
7.0	TX_PCOM_RDY	0,RW	**TXPCOM Ready:** When set this bit indicates a non-null TX_PCOM has been loaded into the TX_PCOM register.

TX_PCOM Low B Register - Register 8 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
8.7 – 8.0	TX_PCOM_LOB	0, RW	**TX_PCOM_LOB:** The 7th through the LSB of the 32-bit transmitted data field to be used for out-of-band communications between PHY management entities. The PHY will send all-0 PCOMs until the high byte in TX_PCOM_HI has been accessed. An access of any of the four TX_PCOM bytes will clear the TX_PCOM_RDY bit in the ISTAT register.

TX_PCOM Low A Register - Register 9 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
9.7 – 9.0	TX_PCOM_LOA	0, RW	**TX_PCOM_LOA:** The 15th through 8th bits of the 32-bit transmitted data field to be used for out-of-band communications between PHY management entities. The PHY will send all-0 PCOMs until the high byte in TX_PCOM_HI has been accessed. An access of any of the four TX_PCOM bytes will clear the TX_PCOM_RDY bit in the ISTAT register.

TX_PCOM High B Register - Register 10 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
10.7 – 10.0	TX_PCOM_HIB	0, RW	**TX_PCOM_HIB:** The 23rd through the 16th bits transmitted data field to be used for out-of-band communications between PHY management entities. The PHY will send all-0 PCOMs until the high byte has been accessed. An access of any of the four TX_PCOM bytes will clear the TX_PCOM_RDY bit in the ISTAT register.

TX_PCOM High A Register - Register 11 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
11.7 – 11.0	TX_PCOM_HIA	0, RW	**TX_PCOM_HIA:** The MSB of the 32-bit transmitted data field to be used for out-of-band communications between PHY management entities. The PHY will send all-0 PCOMs until the high byte has been accessed. An access of any of the four TX_PCOM bytes will clear the TX_PCOM_RDY bit in the ISTAT register.

RX_PCOM Low B Register - Register 12 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
12.7 – 12.0	RX_PCOM_LOB	0, RW	**RX_PCOM_LOB:** The LSB of the 32-bit receive data field to be used for out-of-band communications between PHY management entities. A non-null receive PCOM will set the RX_PCOM_VAL bit in the ISTAT register. An access of the high byte of the RX_PCOM_HI register will clear the RX_PCOM_VAL bit in the ISTAT register.

RX_PCOM Low A Register - Register 13 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
13.7 – 13.0	RX_PCOM_LOA	0, RW	**RX_PCOM_LOA:** The 15th through the 8th bits of the 32-bit receive data field to be used for out-of-band communications between PHY management entities. A non-null receive PCOM will set the RX_PCOM_VAL bit in the ISTAT register. An access of the high byte of the RX_PCOM_HI register will clear the RX_PCOM_VAL bit in the ISTAT register.

RX_PCOM High B Register - Register 14 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
14.7 – 14.0	RX_PCOM_HIB	0, RW	**RX_PCOM_HIB:** The 23rd through the 16th bits of the 32-bit receive data field to be used for out-of-band communications between PHY management entities. A non-null receive PCOM will set the RX_PCOM_VAL bit in the ISTAT register. An access of the high byte of this register will clear the RX_PCOM_VAL bit in the ISTAT register.

RX_PCOM High A Register - Register 15 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
15.7 - 15.0	RX_PCOM_HIA	0, RW	**RX_PCOM_HIA:** The MSB of the 32-bit receive data field to be used for out-of-band communications between PHY management entities. A non-null receive PCOM will set the RX_PCOM_VAL bit in the ISTAT register. An access of the high byte of this register will clear the RX_PCOM_VAL bit in the ISTAT register.

Noise Level Register - Register 16 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
16.7 - 16.0	NOISE_LEVEL	0x07, RW	**NOISE LEVEL:** This is the digital value of the SLICE_LVL_NOISE output. It is effectively a measure of the noise level on the wire. When auto-adaptation is enabled (bit 5 of the Control register is false) this register is updated with the current noise count every 50n Secs. When adaptation is disabled, this register can be written and is used to generate both the SLICE_LVL_NOISE and the SLICE_LVL_DATA signals.

Peak Level Register - Register 17 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
17.7 - 17.0	PEAK_LEVEL	0xFF, RW	**Peak Level:** This is a measurement of the peak level of the last valid (non-collision) AID received also, the maximum allowable value of the noise measurement. If NOISE_LEVEL exceeds PEAK_LEVEL, NOISE_LEVEL is reset to NOISE_FLOOR.

Noise Floor Register - Register 18 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
18.7 - 18.0	NSE_FLOOR	0x07, RW	**Noise Floor:** The minimum value of the NOISE_LEVEL measurement.

Noise Ceiling Register - Register 19 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
19.7 - 19.0	NSE_CEILING	0xC2, RW	**Noise Ceiling:** The maximum value of the NOISE_LEVEL measurement.

Noise Attack Register - Register 20 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
20.7 - 20.0	NSE_ATTACK	0xF4, RW	**Noise Attack:** Sets the attack characteristics of the noise algorithm. The high nibble sets the number of noise events needed to raise the NOISE_LEVEL immediately, while the low nibble is the number of noise events needed to raise the NOISE_LEVEL at the end of an 870 msec period.

Noise Events Register - Register 21 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
21.7 - 21.0	NSE_EVENTS	0x00, RW	**Noise Events:** An 8 bit counter that records the number of noise events detected. Overflows are held as 0xFF. This register is cleared by setting bit 6 of the Control register (CLR_NS_EVNT).

Four Wire Enable Register - Register 22 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
22.7 - 22.2	Reserved	0, RW	**Reserved** These bits will always be read as 0.
22.1	DIS_LNK	0, RW	**Disable Link:** This bit disables link integrity feature.
22.0	FWENA	0, RW	**Four Wire Enable:** When read this bit will indicate the status of FWENA (pin 57) as read during power up. If the FWENA pin status is 1 on power up, this bit can be written to change the FWENA status. If the FWENA pin status is 0, on power up, writes to this bit are ignored.

Aid Address Register - Register 25 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
25.7 - 25.0	AID_ADDRESS	0x00, RW	**AID Address:** Unless bit 7 of the Control register is set, the DM9801A is assured to select a unique AID Address. Addresses above 0xEF are reserved. Address 0xFF is defined to indicate a Remote Command.

Aid Interval Register - Register 26 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
26.7 - 26.0	AID_INTERVAL	0x14, RW	**AID Interval:** This value defines the number of TCLKs (116.7ns) separating AID symbols.

Aid Inter-Symbol Blanking Interval Register - Register 27 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
27.7 - 27.0	AID_ISBI	0x40, RW	**AID Inter Symbol Blanking Interval:** This value defines the number of TCLKs (116.7ns) between AID pulses for symbol 0.

ISBI Slow Register - Register 28 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
28.7 - 28.0	ISBI_SLOW	0x2C, RW	**Inter Symbol Blanking Interval (Low Speed):** This value defines the number of TCLKs (116.7ns) between DATA pulses for symbol 0 in low speed

ISBI Fast Register - Register 29 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
29.7 - 29.0	ISBI_FAST	0x1C, RW	**Inter Symbol Blanking Interval (High Speed):** This value defines the number of TCLKs (116.7ns) between DATA pulses for symbol 0 in High speed

TX Pulse Width Register - Register 30 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
30.7 - 30.0	TX_PLS_WIDTH	0x04, RW	**Transmit Pulse Width:** This value determines the duration in OSC cycles (16.7 ns) that a transmit pulse lasts.

TX Pulse Cycles Register - Register 31 (INTFSEL = 1, GPSI Mode)

Bit	Bit Name	Default	Description
31.7 - 31.0	TX_PLS_CYCLS	0x44, RW	**Transmit Pulse Cycles:** The low nibble of this register indicates the number of pulses on the HNN pins while the high nibble indicates the number of pulses on the HNP pins.

1 Mbps Home Phoneline Network PHY

The integrated DM9801A transceiver is a physical layer device supporting home phoneline networking. It provides all of the PHY layer functions required to support 1 Mbps data transfers over existing residential phone wiring.

All data bits are encoded into the relative time position of a pulse with respect to the previous one. The wave-form on the wire consists of a 7.5 MHz carrier sinusoid enclosed within an exponential (bell shaped) envelope. The waveform is produced by generating four 7.5 MHz square wave cycles and passing them through an external bandpass filter.

The Home Phoneline Network PHY frame consists of a Home Phoneline Network header that replaces the normal Ethernet 64-bit preamble and delimiter. The frame header is prepended to a standard Ethernet packet starting with the destination address and ending with the CRC. Only the PHY layer and its parameters are modified from that of the standard Ethernet implementation. The Home Phoneline Network PHY layer is designed to operate with a standard Ethernet MAC layer controller implementing all the CSMA/CD protocol features.

The frame begins with a characteristic SYNC interval that delineates the beginning of a Home Phoneline Network frame followed by an Access ID (AID) which encodes 8 bits of AID and 4 bits of control word. The AID is used to detect collisions and is dynamically assigned, while the control word carries speed and power information. The AID is followed by a silence interval, then 32 bits of data reserved for PHY layer communication. These bits are accessible via internal registers and are for future use.

Data encoding consists of two symbol types: an AID symbol and a data symbol. The AID symbol is always transmitted at the same speed and encodes 2 bits that determine the pulse position (one of four) relative to the previous pulse. These bits are transmitted LSB first. The access symbol interval is fixed.

The data symbol interval is variable. The arriving bit stream is blocked into from 3-bit to 6-bit blocks according to a proprietary (RLL25) algorithm. The bits in each block are then used to encode a data symbol. Each symbol consists of a Data Inter Symbol Blanking Interval (DISBI) and then a pulse at one of 25 possible positions. The pulse position and polarity within the interval is determined by the bits in the data block. Immediately after the pulse a new symbol interval begins. During the DISBI the receiver ignores all incoming pulses to allow network reflections to die out.

Any station may be programmed to assume the role of a PHY master and remotely command, via the control word, the rest of the units on the network to change their transmit speed or power level.

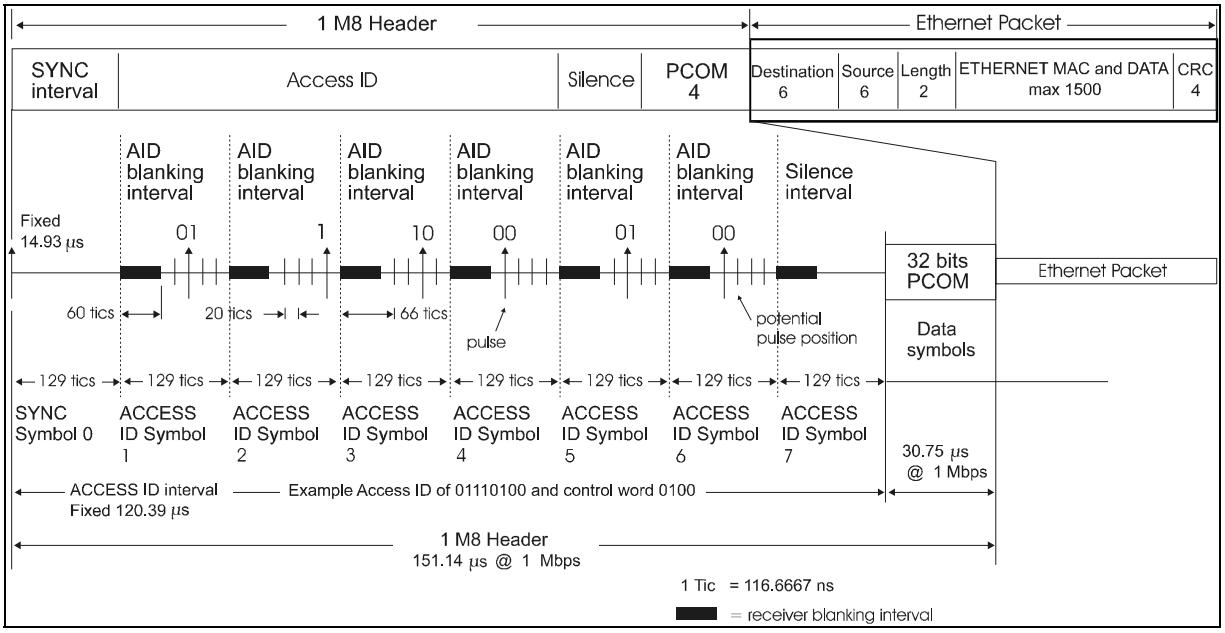
Many of the framing parameters are programmable in the Home Phoneline Network PHY and will allow modifications to transmission speed center frequency as well as noise and reflection rejection algorithms.

Two default speeds are provided, low at 0.7 Mbps and high at 1 Mbps.

Home Phoneline Network PHY Medium Interface Framing

The Home Phoneline Network frame on the phone wire network consists of a header generated in the PHY prepended to an IEEE 802.3 Ethernet data packet received from the MAC layer.

When transmitting on the wire pair, the DM9801A first receives an Ethernet MAC frame from the MAC. The 8 octets of preamble and delimiter are stripped off and replaced with the Home Phoneline Network PHY header, then transmitted on the home network with the LSB of each symbol being transmitted first. During a receive operation, the reverse process is executed. When a Home Phoneline Network PHY frame is received by the DM9801A, the header is stripped off and replaced with the 4 octets of preamble and delimiter of the IEEE 802.3 Ethernet MAC frame specification and then passed on to the MAC layer.



DM9801A 1M Framing
Figure 21

DM9801A Symbol Waveform

All DM9801A symbols are composed at the transmitter of a silence interval and a pulse formed of an integer number of cycles (CYCLES_PER_PULSE) of a frequency square wave (CENTER_FREQUENCY) that has been filtered with a bandpass filter. Data is encoded in the same time interval from the preceding pulse.

The DM9801A pulse parameters are shown below.

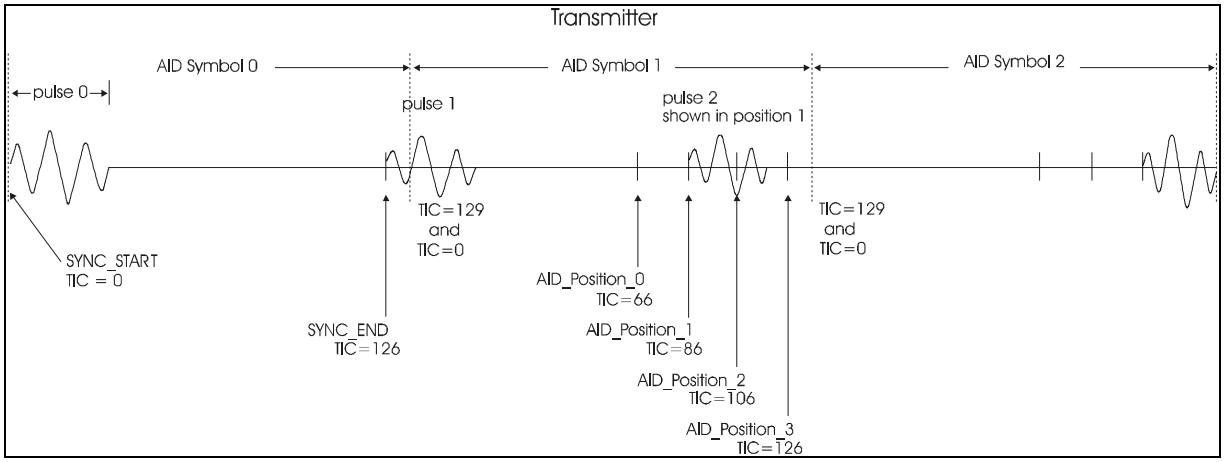
Parameter	Value	Tolerance	Unit
CENTER_FREQUENCY	7.5	500 PPM	MHz
CYCLES_PER_PULSE	4		Cycle

DM9801A 1M time intervals are expressed in Tine Interval Clock (TIC) units. One TIC is defined as 7/(60E6) seconds or approximately 116.67 nano-seconds (ns).

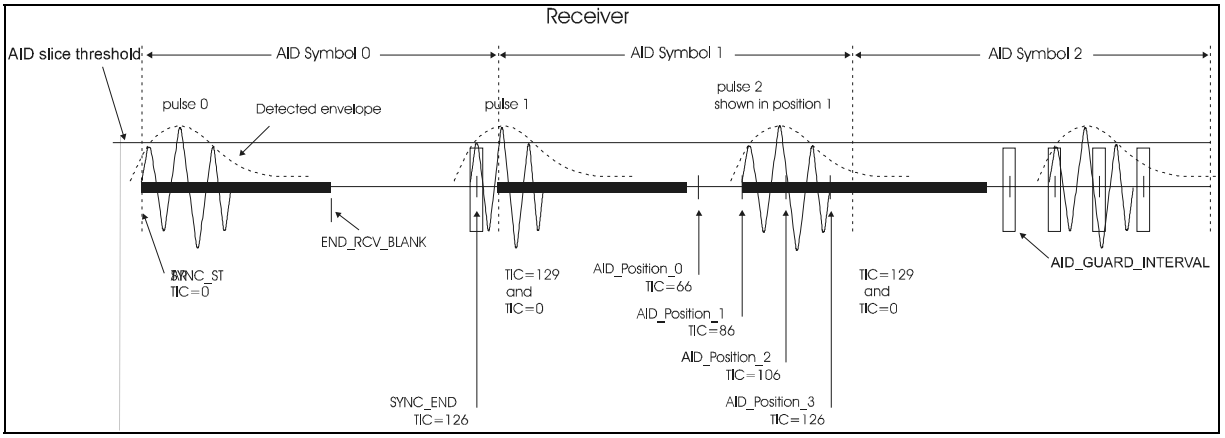
Access ID Intervals

The DM9801A 1M frame begins with an Access ID interval which is composed of eight equally spaced subintervals termed AID symbols 0 through 7. (refer to figure 21 above)

An Access ID symbol is 129 TICs long. Transmit timing is shown in figure 22 below. Timing starts at the beginning of each AID symbol and ends at TIC = 129.



AID Symbol Transmit Timing
Figure 22



AID symbol Receive Timing
Figure 23

Sync Transmit Timing

The Sync interval (AID symbol 0) delineates the beginning of a frame and is composed of a SYNC_START pulse followed by a SYNC_END pulse after a fixed silence interval as shown in figure 22 above. Timing for this (AID symbol 0) starts (TIC = 0) at the beginning of the SYNC_START pulse. The SYNC_END pulse starts at TIC = 126.

At TIC = 129, this AID symbol 0 ends and the next AID symbol begins with the symbol timing reference reset to TIC = 0. No information bits are coded in the SYNC (AID symbol 0 interval).

Sync Receive Timing

As soon as the SYNC_START pulse is detected, the receiver disables (Blanks) further detection until AID_END_BLANK (located at TIC = 61) after which detection is re-enabled for the next received pulse. The receiver allows for jitter by establishing a window around each legal pulse position. This window AID_GUARD_INTERVAL is 2 TICS wide on either side of the position.

A SYNC_END pulse which arrives outside AID_GUARD_INTERVAL of the legal TIC = 126 is considered a NOISE_EVENT that may be used in setting the adaptive Squelch level, aborts the packet, and sets the receiver in search of a new SYNC_START pulse and SYNC interval. If it is a transmitting station, the Collision event is asserted.

The SYNC interval is followed by six Access ID symbols (symbols 1 through6). Transmit timing is shown in figure 22 and receive timing in figure 23(above). Data is encoded in the relative position of each pulse with respect to the previous one. A pulse may occur at one and only one of the four possible positions within the AID symbol yielding two bits of data coded per AID symbol.

The decoded bits from the AID symbols 1 to 4 produce 8 bits of Access ID which are used to identify individual stations and to detect collisions. The MSB is encoded in AID symbol 1 and is the leftmost bit in Table 2.

Pulse Position	Tics From Beginning of AID Symbol	Bit Encoding
1	66	00
2	86	01
3	106	10
4	126	11

Access ID Symbol Pulse Position and Encoding
Table 2

The next two AID symbols (5 and 6) encode four bits of control information. The MSB is encoded in AID Symbol 5.

Collisions

A Collision is detected only during Access ID and silent intervals (AID Symbols 0 through 7). In general during a collision a transmitting station will read back an AID value that does not match its own and recognizes the event as a collision alerting other stations with a Jam signal. Non-transmitting stations may also detect non-conforming AID pulses as collisions.

With two transmitters colliding, each transmitter normally blanks its receive input immediately after transmitting and simultaneously receiving a pulse. Therefore, only when a transmitting station receives pulses in a position earlier than the position it transmitted will it recognize it as a pulse transmitted by another station and signal a collision.

For this reason guaranteed collision is possible only as long as the spacing between successive possible pulse positions in an AID symbol (20 TICS or 2.3 μs) is greater than the round trip delay between the colliding nodes. At approximately 1.5 ns propagation delay per foot, the maximum distance between two stations must not be greater than 500 feet for collision detection purposes (1.5μs round trip delay plus margin).

The following criteria must be met to guarantee reliable collision detection:

At least one station of a colliding group must always detect a collision when the delay between the beginning of its transmitted packed and the beginning of the received colliding packed is between -1.5 μs and +1.5 μs

Collisions (continued)

In general, any received pulse at a station that does not conform to the pulse position requirements of AID symbols 0 through 7 shall indicate a collision on the wire. When a transmitting station senses a collision, it emits a Jam signal to alert all other stations to the collision. The following conditions signify a collision event:

1. A station receives an AID that does not match the one being sent.
2. A station receives a pulse outside of the AID_GUARD_INTERVAL in AID intervals 0 to 7.
3. A station receives a pulse inside the SILENT_INTERVAL (AID symbol 7).

As in all cases, pulses received inside the blanking interval are ignored.

Passive stations (stations not actively transmitting during the collision) cannot reliably detect collisions. Therefore, once an collision is detected by a transmitting station, the station must inform the rest of the stations of the collision with a Jam pattern. Only a transmitting station emits a Jam signal.

Once a collision is detected, the COLLISION signal to the MAC interface is asserted and is not reset until the MAC deactivates the TX_EN signal and CRS is inactive.

Jam Signal

A Jam pattern consists of one pulse every 32 TICs and continues until at least the end of the AID intervals. After the AID intervals, the jam pattern is continued until TX_EN from the MAC is deactivated.

Access ID Values

The Access ID values for slave stations must be picked by each individual station randomly from a set a AID slave numbers. During operation each station monitors the frames received on the wire. If it detects another station using the same AID, it must randomly select a new AID.

Silence Interval (AID Symbol 7)

The Access ID symbols are followed by a fixed SILENCE_INTERVAL on 129 TICs. The receive blanking interval is the same as that of the AID symbols (1 through 6). Any pulses detected in the SILENCE_INTERVAL are considered as Collision event and are handled as described in the Collisions section.

Data Symbols

Data symbols are less robust than Access ID symbols and do not allow collision detection. However, they encode data for a much higher transmission rate.

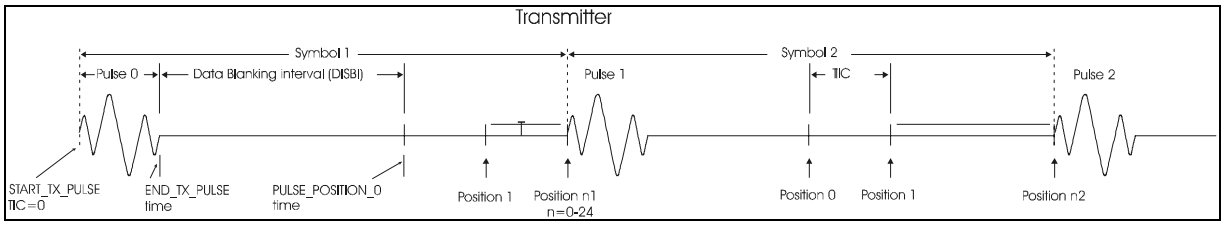
Data Transmit Timing

Data transmission begins with the beginning of a transmission of a pulse as shown in figure 24 below. Transmit timing in TICs is measured from this point (TIC = 0).

Depending on the data code, the next pulse may begin at any PULSE_POSITION_N, where n = 0 to 24. Each position is separated from the previous one by one TIC. PULSE_POSITION_0 occurs at a value defined in Table 3 below. This value determines the transmission speed. When a pulse begins transmission, the previous symbol interval ends and a new one immediately begins.

SPEED Setting	Nominal Data Rate	PULSE_POSITION_0 Value (in TICs)
LOW_SPEED	0.7 MB/s	44
HIGH_SPEED	1.0 MB/s	28

Blanking Interval Speed Settings
Table 3



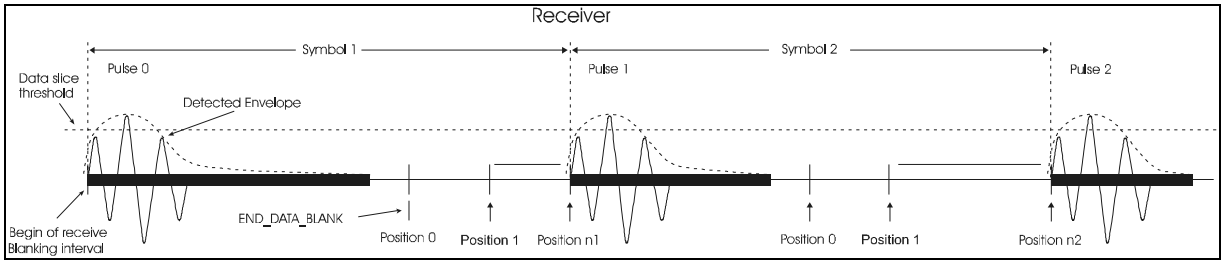
Transmit Data Symbol Timing
Figure 24

Data Receive Timing

The incoming waveform is formed from the transmitted pulse along with any distortions and reflections that occur in the wiring network. The receiver detects the point at which the envelope of the received waveform crosses a set threshold as described in the Receiver Functions section.

Immediately after the receive threshold crossing, the receiver disables any further detection for a period of END_DATA_BLANK = PULSE_POSITION_0 - (minus) 3 TICs, starting with the detection of the pulse peak.

The receiver is then re-enabled for pulse detection and, upon reception of the next pulse measures the elapsed time (RX_PULSE_INTERVAL) from the previous pulse. The value is then placed in the nearest pulse position bin (one of 25), where pulse position 0 is at PULSE_POSITION_0, and each subsequent position is spaced 1 TIC from the previous one as defined in the Data Transmit Timing section. Data symbols are therefore variable and depend on the encoded data.



Receive Symbol Timing
Figure 25

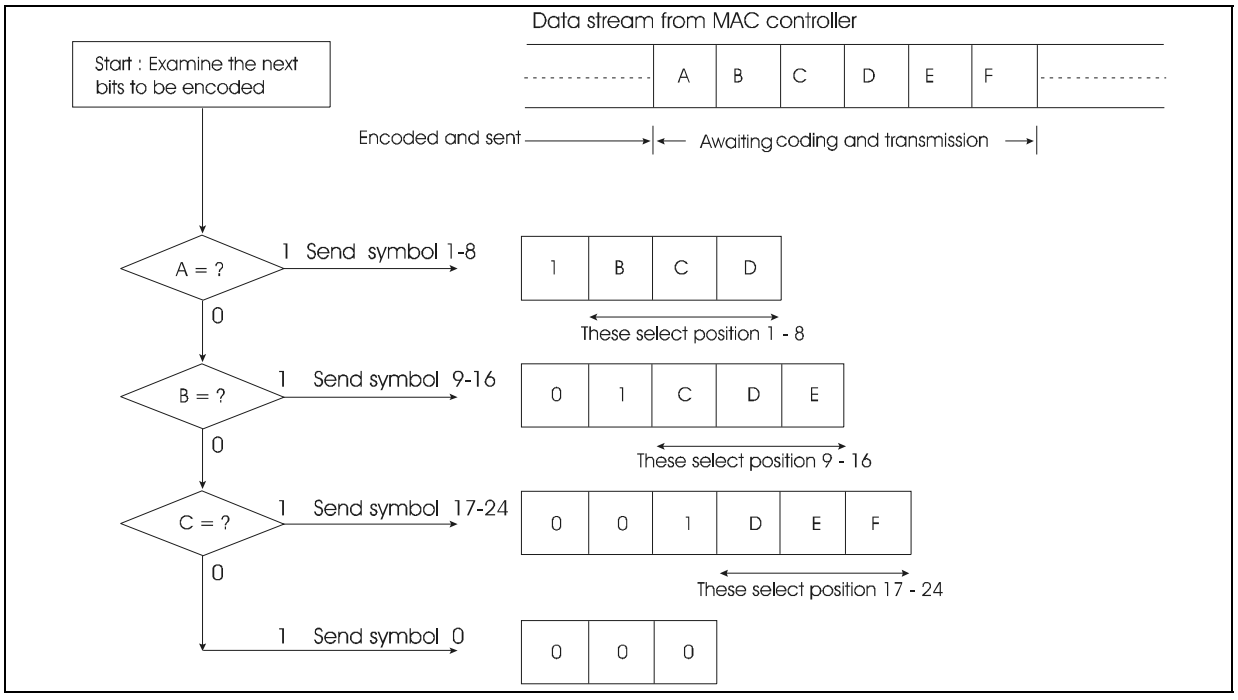
Data Symbol RLL25 Encoding

The Run Length Limit (RLL25)code was developed for the Home Networking PHY. It produces highest bit rate for a given value of ISBI (Inter-Symbol Blanking Interval) and TIC size. In a manor similar to run length limited disk coding, RLL27 encodes data bits in groups of various sizes, specifically, 3, 4, 5, and 6 bits. Pulse positions are assigned to the encoded bit groups in a manor that causes more data bits to be encoded in positions that ate farther apart. This keeps both the average and minimum bit rates higher.

RLL25 codes data by traversing a tree as shown in figure 26 below. Assuming that successive data bits to be encoded are labeled A, B, C, D…,etc. The encoding process begins at the root node and proceeds as follows:

- If the first bit (bit A) is a one, the next 3 bits (B, C, and D) select which one of the eight positions (1-8) is transmitted. The encoding process then continues at the root node.
- If bit A is a zero and bit B is a one, the next 3 bits (C, D, and E) select which one of eight positions (9-16) is transmitted. The encoding process then continues at the root node.
- If bit A is a zero, bit B is a zero, and bit C is a one, the next 3 bits (D, E, and F) select which one of eight positions (17-24) is transmitted. The encoding process then continues at the root node.
- Finally, if bits A, B, and C are all zeros, position 0 is transmitted. The encoding process then continues at the root node.

As a result, Symbol 0 encodes the 3-bit data pattern 000, positions 1-8 encode the 4-bit data pattern 1BCD, positions 9-16 encode the 5-bit data pattern 01CDE, and positions 17-24 encode the 6-bit data pattern 001DEF. If the data encoded is random, 50% of the positions used will be for 4-bit data patterns, 25% will be for 5-bit data patterns, 12.5% will be for 6-bit data patterns, and 12.5% will be for 3-bit data patterns.



RLL 25 Coding Tree
Figure 26

Management Interfaces

The DM9801A may be managed from either of two interfaces with managed parameters varying depending on the interface:

1. Remote control-word management commands embedded in the AID header on the wire network.
2. Management messages from the local management entity.

AID Header Remote Control-Word Commands

Home Phoneline Networking stations may be configured either as master stations or slave stations. Only one master may exist on a given Home Phoneline Network over which the header is preserved. Operation is master station mode is optional while operation is slave mode is a requirement.

The master station may send commands embedded in the header control word to remotely set various parameters of the remote slave stations. Stations are identified via the AID as follows:

1. The master station is identified on the Home Phoneline Network with an AID of 0xFF (hex).
2. The slave is identified with an AID of 0x00 (hex) to 0xEF (hex).
3. AID values of 0xF0 to 0xFE are reserved for future use.

Once a command has been transmitted, the master station must revert to a slave AID so that subsequent control words are not interpreted by the slave stations as new commands.

A master remote command must consist of three frames with an AID header of 0xFF (hex). Since the header is appended (piggy-backed) to packets received from the MAC that are normally transmitted independently of the DM9801A, master control frames are transmitted only when the MAC sends packets to the DM9801A. Therefore, packets from the master station may be separated by long intervals during which other (slave) stations may transmit their frames.

A remote master Control-Word command must be recognized and executed by a Home Phoneline Networking PHY when it receives three consecutive valid frames with an AID of 0xFF (hex). Valid commands are as follows:

1. SET_VERSION - Commands slave devices to operate according to 1M Home Networking version.
2. SET_POWER - commands slave stations to set their transmit level to a prescribed level until another master command is received.
3. SET_SPEED - commands slave stations to set their transmit speed to a prescribed value until another master command is received.

The control word bit encoding and possible values are described in Table 4 below.

Bit #	Indicated Status
0	0 = This station is version 0 1 = This station is not version 0
1	0 = Frame transmitted at low power 1 = Frame transmitted at high power
2	0 = Frame transmitted at low speed 0 = Frame transmitted at high speed
3	Reserved

Master/Slave Station Control Word Functions
Table 4

Note: Master and Slave control word bit encoding are identical.

Absolute Maximum Ratings*

Symbol	Parameter	Min.	Max.	Unit	Conditions
DVCC,AVCC	Supply Voltage	-0.3	3.6	V	
VIN	DC Input Voltage (VIN)	-0.5	5.5	V	
VOUT	DC Output Voltage(VOUT)	-0.3	3.6	V	
T_A	Ambient Temperature Range	0	70	°C	
Tc	Case Temperature Range	0	85	°C	@ T_A = 70°C
Tstg	Storage Temperature Rang (Tstg)	-65	150	°C	EIAJ-ED-4701
LT	Lead Temp. (TL, Soldering, 10 sec.)	---	220	°C	J-STD-020
ESD	ESD rating (Rzap=1.5K,Czap=100pF)	--	2000	V	EIAJ-ED-4701

Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Power Consumption:

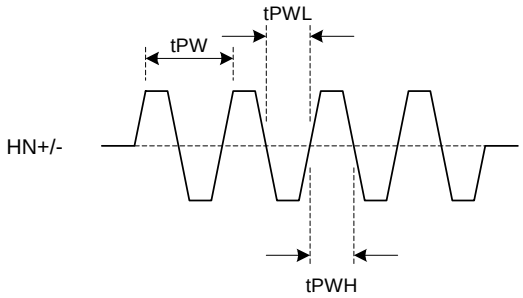
Symbol	Parameter	Min.	Max.	Unit	Conditions
PD	High Power, 2 drivers		125	mA	3.3V
	High Power, 1 driver		80	mA	3.3V
	Low Power, 2 drivers		70	mA	3.3V
	Low Power, 1 driver		45	mA	3.3V

DC Electrical Characteristics (VCC = 3.3Vdc, ±5%, TA = 25°C, unless specified otherwise)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
TTL Inputs						
VIL	Input Low Voltage			0.8	V	IIL = -400uA
VIH	Input High Voltage	2.0			V	IIH = 100uA
IIL	Input Low Current			10	uA	VIN = 0.4V
IIH	Input High Current			-10	uA	VIN = 2.7V
MII/GPSI TTL Outputs						
VOL	Output Low Voltage			0.4	V	IOL = 4mA
VOH	Output High Voltage	2.4			V	IOH = -4mA
LED Outputs						
VOL	Output Low Voltage			0.4	V	IOL = 1mA
VOH	Output High Voltage	2.4			V	IOH = -0.1mA

AC Electrical Characteristics & Timing Waveforms (Over full range of operating condition unless specified otherwise)

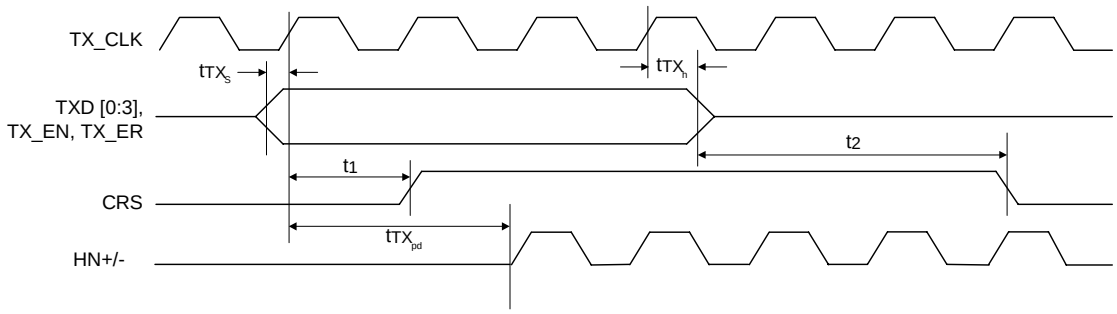
Analog Transmitter Timing Diagram



Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Transmitter (Analog)						
tPW	Pulse Width		133		ns	
tPWH	Pulse Width High		67		ns	
tPWL	Pulse Width Low		67		ns	
tPWH	OSC Pulse Width High		25		ns	
tPWL	OSC Pulse Width Low		25		ns	
MII (Media-Independent Interface) Clock Timing						
Idle (excluding IFG time)						
tPWH	TX_CLK/RX_CLK Pulse Width High	1168			ns	
tPWL	TX_CLK/RX_CLK Pulse Width Low	1165			ns	
Preamble (first 64 bits of TX MAC frame)						
tTPWH	TX_CLK Pulse Width High	468			ns	
tTPWL	TX_CLK Pulse Width Low	466			ns	
tRPWH	RX_CLK Pulse Width High	-			ns	
tRPWL	RX_CLK Pulse Width Low	-			ns	
Data (throughout the data phase)						
tPWH	TX_CLK/RX_CLK Pulse Width High	468 ns	3us	5.6us		
tPWL	TX_CLK/RX_CLK Pulse Width Low	466 ns	3us	23us		
IFG (88 bit times following CRS falling edge)						
tPWH	TX_CLK/RX_CLK Pulse Width High	468			ns	
tPWL	TX_CLK/RX_CLK Pulse Width Low	466			ns	

Notes: 1) During AID interval, RX_CLK and TX_CLK stop for up to 140 us.
2) During Preamble state, RX_CLK stays at Low.

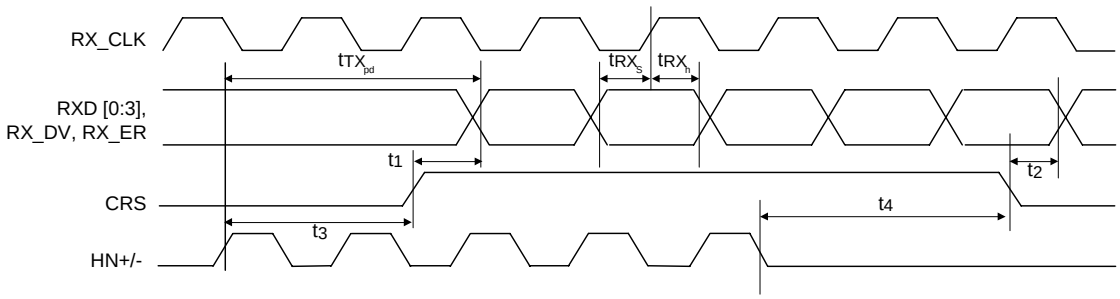
MII-1M Nibble Transmit Timing Diagram



MII-1M Nibble Transmit Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tTX_s	TXD[0:3], TX_EN, TX_ER Setup To TX_CLK High	10			ns	
tTX_h	TXD[0:3], TX_EN, TX_ER Hold From TX_CLK High	10			ns	
t_1	TX_EN Sampled To CRS Asserted			1.3	us	
t_2	TX_EN Sampled To CRS De-asserted			36.1	us	
tTX_{pd}	TX_EN Sampled To HN+/- Out (Tx Latency)			1.3	us	

MII-1M Receive Nibble Timing Diagram



MII-1M Receive Nibble Timing Parameters

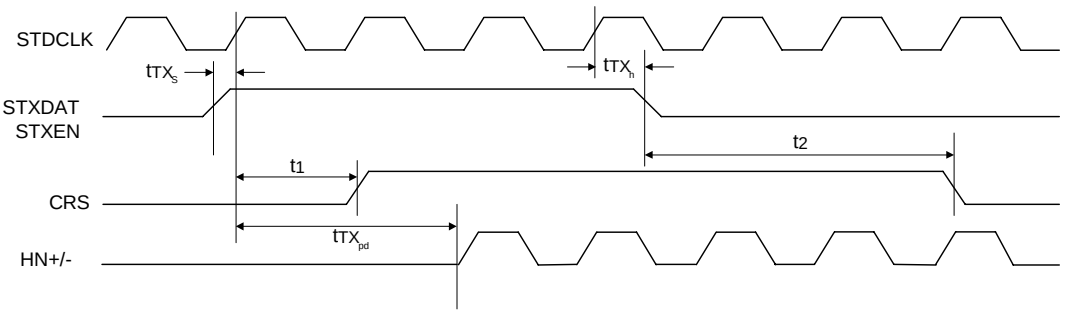
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tRX_S	RXD[0:3), RX_DV, RX_ER Setup To RX_CLK High	10			ns	
tRX_h	RXD[0:3], RX_DV, RX_ER Hold From RX_CLK High	10			ns	
tRX_{pd}	HN+/- In To RXD[0:3] Out (Rx Latency)			154	us	
t1	CRS Asserted To RXD[0:3], RX_DV, RX_ER			153	us	
t2	CRS De-asserted To RXD[0:3], RX_DV, RX_ER			0	ns	
t3	HN+/- In To CRS Asserted			474	ns	
t4	HN+/- Quiet To CRS De-asserted			20.1	us	

GPSI-1M Clock Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
GPSI (General Purpose Serial Interface)						
Idle (excluding IFG time)						
tPWH	STDCLK/SRDCLK Pulse Width High	468			ns	
tPWL	STDCLK/SRDCLK Pulse Width Low	115.3			ns	
Preamble (first 64 bits of TX MAC frame)						
tTPWH	STDCLK Pulse Width High	118			ns	
tTPWL	STDCLK Pulse Width Low	115.3			ns	
tRPWH	SRDCLK Pulse Width High	-			ns	
tRPWL	SRDCLK Pulse Width Low	-			ns	
Data (throughout the data phase)						
tPWH	STDCLK/SRDCLK Pulse Width High	115.3 ns		8.17 us		
tPWL	STDCLK/SRDCLK Pulse Width Low	115.3		115.3	ns	
IFG (96 bit times following CRS falling edge)						
tPWH	STDCLK/SRDCLK Pulse Width High	118			ns	
tPWL	STDCLK/SRDCLK Pulse Width Low	115.3			ns	

Notes: 1) During AID interval, SRDCLK and STDCLK stop for up to 140 us.
2) During Preamble state, SRDCLK stays at Low.

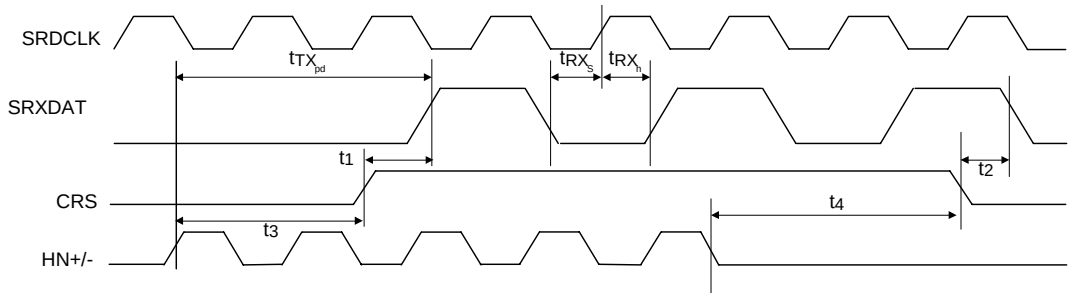
GPSI-1M Transmit Timing Diagram



GPSI-1M Transmit Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tTX_s	STXDATA STXEN, Setup To STDCLK High	10			ns	
tTX_h	STXDAT, STXEN, Hold From STDCLK High	10			ns	
t_1	STXEN Sampled To CRS Asserted			810	ns	
t_2	STXEN Sampled To CRS De-asserted	33.83		43.16	us	
tTX_{pd}	STXEN Sampled To HN+/- Out (Tx Latency)			819.3	ns	

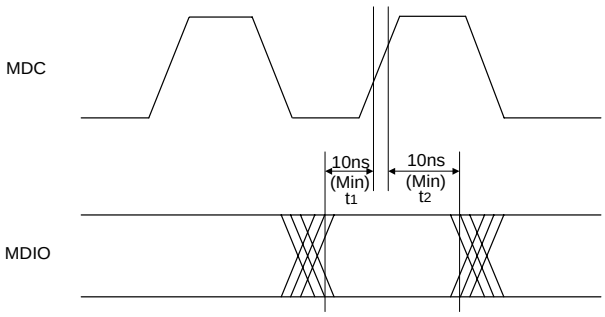
GPSI-1M Receive Timing Diagram



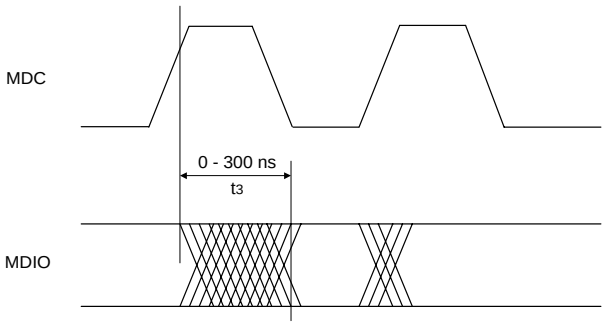
GPSI-1M Receive Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tRX_S	SRXDAT Setup To SRDCLK High	10			ns	
tRX_h	SRXDAT Hold From SRDCLK High	10			ns	
tRX_{pd}	HN+/- In To SRXDAT Out (Rx Latency)			143.8	us	
t1	CRS Asserted To SRXDAT			142.3	us	
t2	CRS De-asserted To SRXDAT			233	ns	
t3	HN+/- In To CRS Asserted			458.5	ns	
t4	HN+/- Quiet To CRS De-asserted			17.7	us	

MDIO Timing when OUTPUT by STA



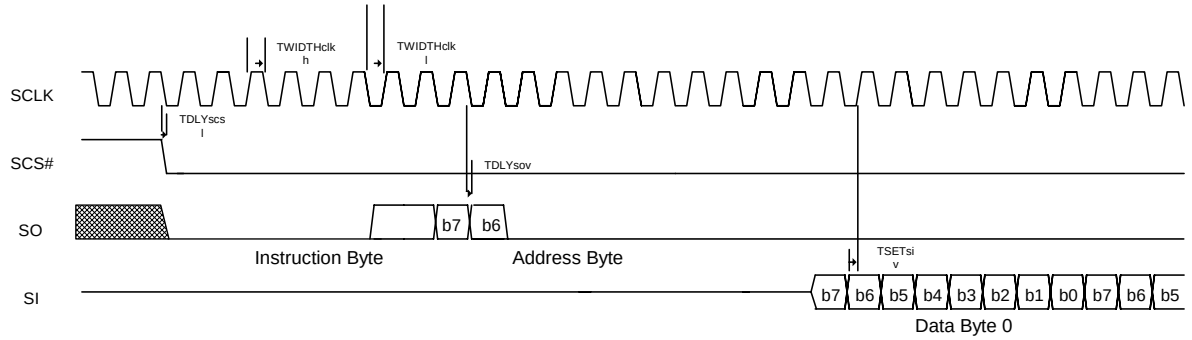
MDIO Timing when OUTPUT by DM9801A



MII Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t1	MDIO Setup Before MDC	10	-	-	ns	When OUTPUT By STA
t2	MDIO Hold After MDC	10	-	-	ns	When OUTPUT By STA
t3	MDC To MDIO Output Delay	0	-	100	ns	When OUTPTU By DM9801A

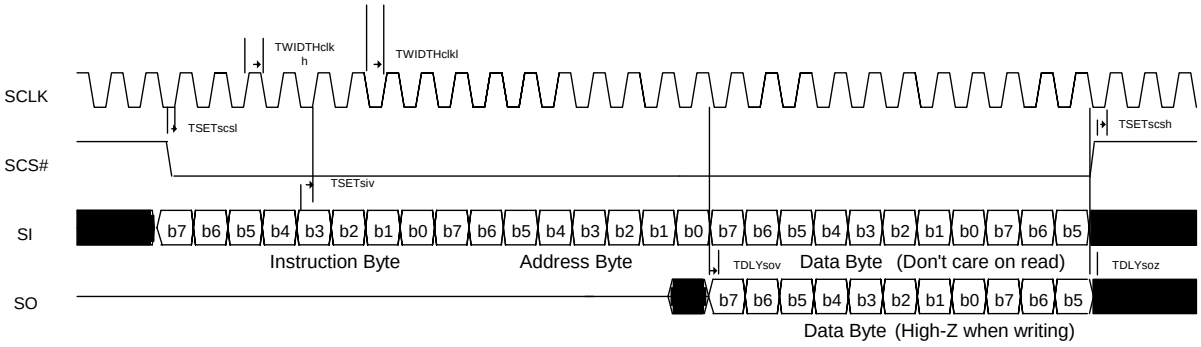
SPI Master Mode Timing Diagram



SPI Master Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
TWIDTHclkh	Positive half-cycle pulse width	790		810	ns	
TWIDTHclkl	Negative half-cycle pulse width	790		810	ns	
TDLYscsl	Falling clock edge to SCS# low			40	ns	
TDLYsov	Falling clock edge to SO valid	40		60	ns	
TSETsiv	SI valid to rising clock edge	20			ns	

SPI Slave Mode Timing Diagram



SPI Master Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
TWIDTHclkh	Positive half-cycle pulse width	400			ns	
TWIDTHclkl	Negative half-cycle pulse width	400			ns	
TSETscsl	SCS# low to rising clock edge	50			ns	
TSETscsh	SCS# high to rising edge clock	50			ns	
TDLYsov	Falling edge clock to SO valid			50	ns	
TDLYsoz	Falling edge clock to SO tri-state			100	ns	
TSETsiv	SI valid to rising clock edge	50			ns	

Magnetics Selection Guide

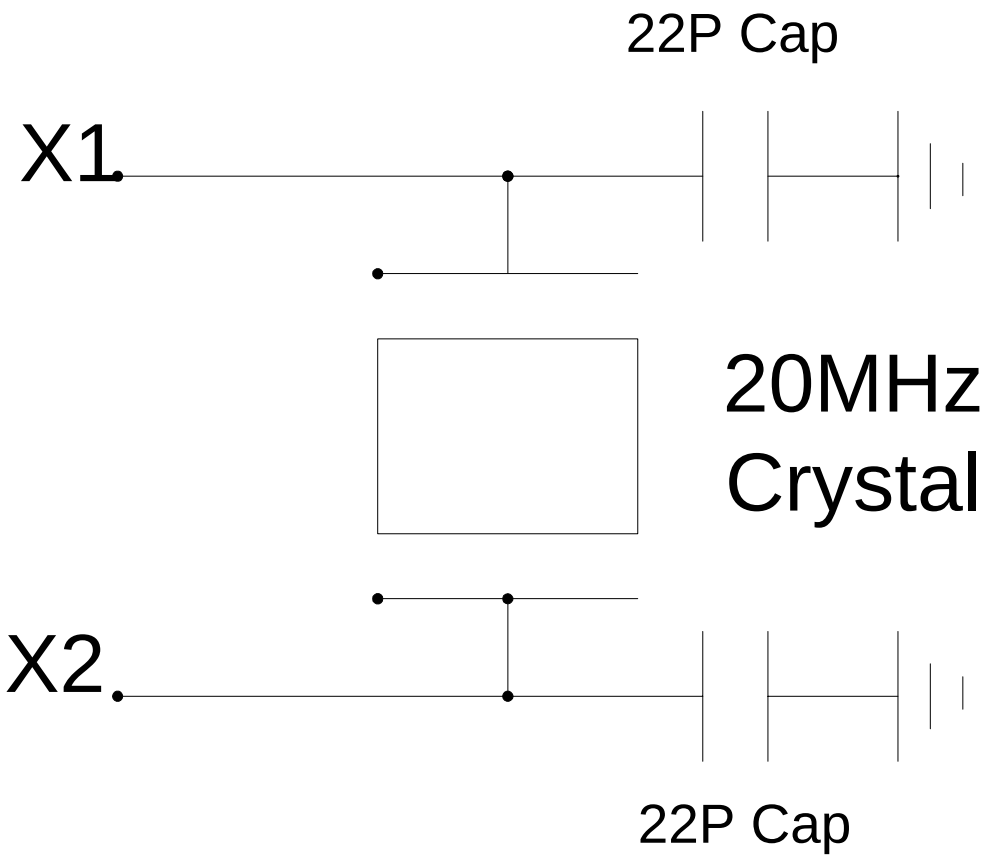
The DM9801A requires an external bandpass filter to interface to the telephone line.

Manufacturer	Part Number
PULSE	B6003
DELTA	LF8114

Table 5

Crystal Selection Guide
A crystal can be used to generate

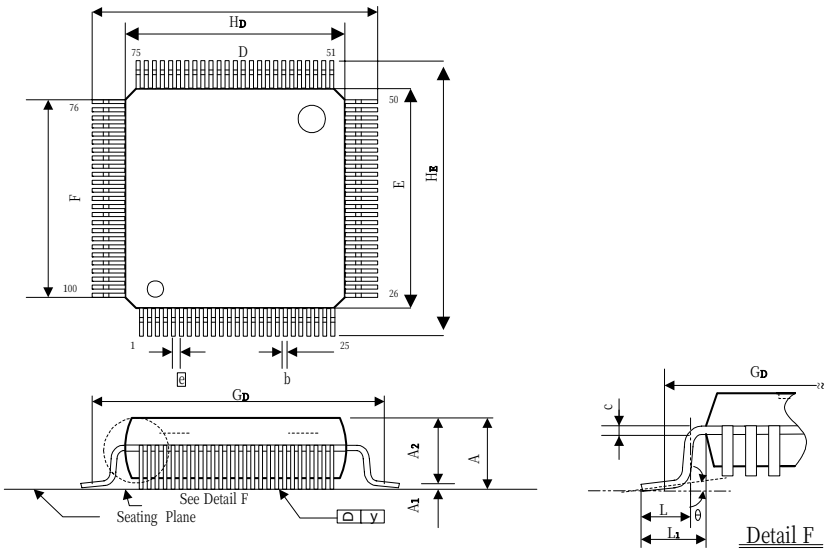
Figure 27
Crystal Circuit Diagram



Package Information

LQFP 100L Outline Dimensions

Unit: Inches/mm



Symbol	Dimensions In Inches	Dimensions In mm
A	0.063 Max.	1.60 Max.
A_1	0.004 ± 0.002	0.1 ± 0.05
A_2	0.055 ± 0.002	1.40 ± 0.05
b	0.009 ± 0.002	0.22 ± 0.05
c	0.006 ± 0.002	0.15 ± 0.05
D	0.551 ± 0.005	14.00 ± 0.13
E	0.551 ± 0.005	14.00 ± 0.13
e	0.020 BSC.	0.50 BSC.
F	0.481 NOM.	12.22 NOM.
G_D	0.606 NOM.	15.40 NOM.
H_D	0.630 ± 0.006	16.00 ± 0.15
H_E	0.630 ± 0.006	16.00 ± 0.15
L	0.024 ± 0.006	0.60 ± 0.15
L_1	0.039 Ref.	1.00 Ref.
y	0.004 Max.	0.1 Max.
θ	0° ~ 12°	0° ~ 12°

Notes:
1. Dimension D & E do not include resin fins.
2. Dimension GD is for PC Board surface mount pad pitch design reference only.
3. All dimensions are based on metric system.

Ordering Information

Part Number	Pin Count	Package
DM9801AE	100	LQFP

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