

## 512K x 8 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

APRIL 2003

### FEATURES

- High-speed access time: 55ns, 70ns
- CMOS low power operation
  - 36 mW (typical) operating
  - 9  $\mu$ W (typical) CMOS standby
- TTL compatible interface levels
- Single power supply
  - 1.65V – 2.2V  $V_{DD}$  (IS62WV5128ALL)
  - 2.5V – 3.6V  $V_{DD}$  (IS62WV5128BLL)
- Fully static operation: no clock or refresh required
- Three state outputs
- Industrial temperature available

### DESCRIPTION

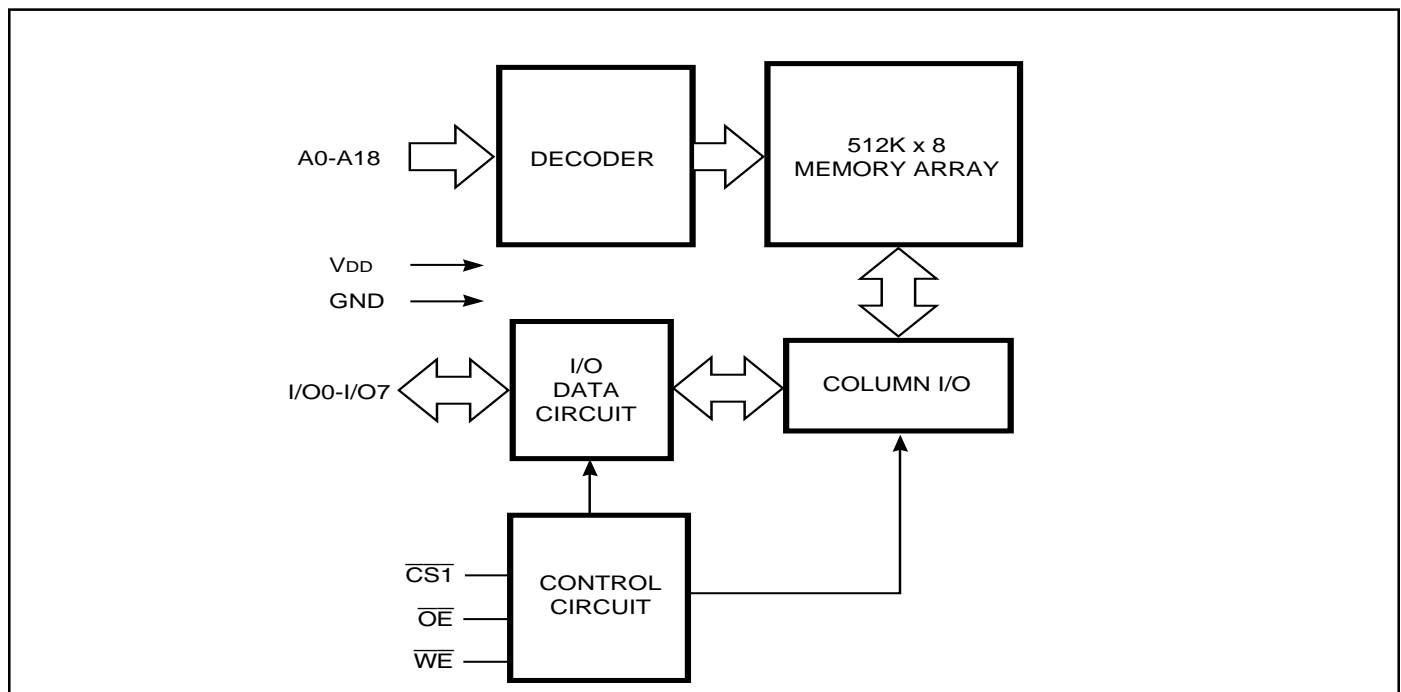
The *ISSI* IS62WV5128ALL / IS62WV5128BLL are high-speed, 4M bit static RAMs organized as 512K words by 8 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When  $\overline{CS1}$  is HIGH (deselected) the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ( $\overline{WE}$ ) controls both writing and reading of the memory.

The IS62WV5128ALL and IS62WV5128BLL are packaged in the JEDEC standard 32-pin TSOP (TYPE I), 32-pin sTSOP (TYPE I), and 32-pin TSOP (Type II).

### FUNCTIONAL BLOCK DIAGRAM



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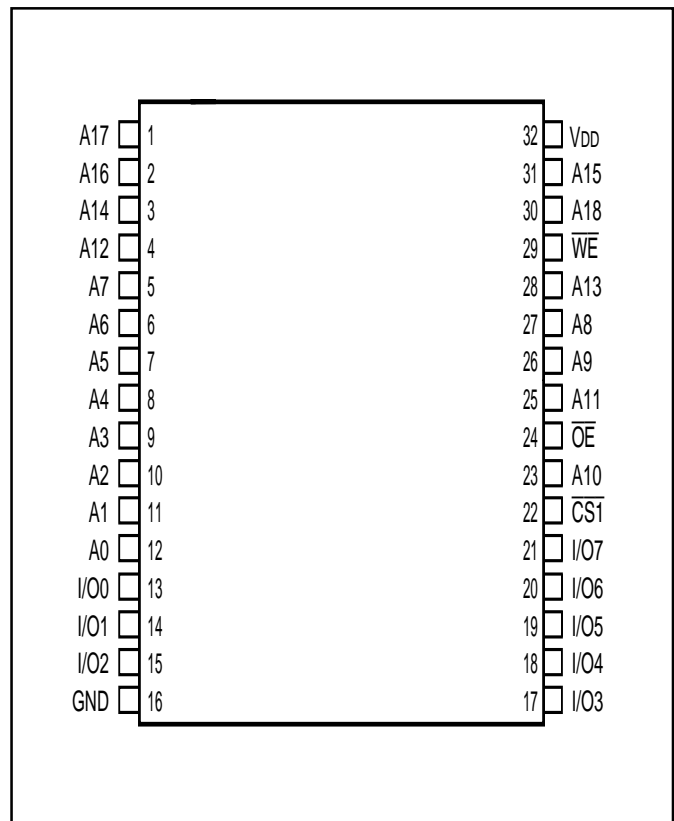
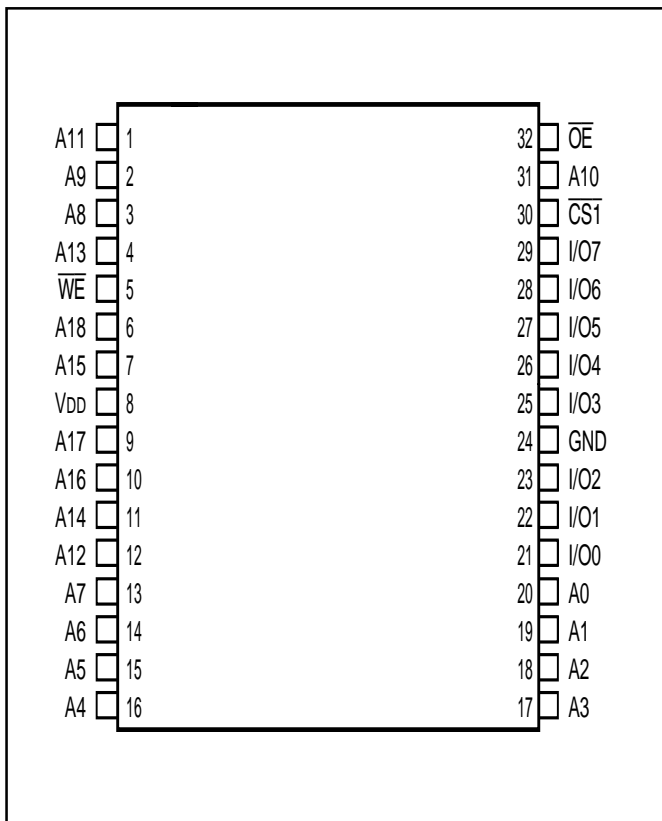
**PIN DESCRIPTIONS**

A0-A18	Address Inputs
$\overline{CS1}$	Chip Enable 1 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
NC	No Connection
V <sub>DD</sub>	Power
GND	Ground

**PIN CONFIGURATION**

**32-pin TSOP (TYPE I), (Package Code T)**  
**32-pin sTSOP (TYPE I) (Package Code H)**

**32-pin TSOP (TYPE II)**  
**(Package Code T2)**



OPERATING RANGE (V<sub>DD</sub>)

Range	Ambient Temperature	IS62WV5128ALL	IS62WV5128BLL
Commercial	0°C to +70°C	1.65V - 2.2V	2.5V - 3.6V
Industrial	-40°C to +85°C	1.65V - 2.2V	2.5V - 3.6V

ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Parameter	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.2 to V <sub>DD</sub> +0.3	V
V <sub>DD</sub>	V <sub>DD</sub> Related to GND	-0.2 to V <sub>DD</sub> +0.3	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	W

**Note:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	V <sub>DD</sub>	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA	1.65-2.2V	1.4	—	V
		I <sub>OH</sub> = -1 mA	2.5-3.6V	2.2	—	V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA	1.65-2.2V	—	0.2	V
		I <sub>OL</sub> = 2.1 mA	2.5-3.6V	—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage		1.65-2.2V	1.4	V <sub>DD</sub> + 0.2	V
			2.5-3.6V	2.2	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub> <sup>(1)</sup>	Input LOW Voltage		1.65-2.2V	-0.2	0.4	V
			2.5-3.6V	-0.2	0.6	V
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>		-1	1	μA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> , Outputs Disabled		-1	1	μA

**Notes:**

1. V<sub>IL</sub> (min.) = -1.0V for pulse width less than 10 ns.

**CAPACITANCE<sup>(1)</sup>**

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	8	pF
C <sub>OUT</sub>	Input/Output Capacitance	V <sub>OUT</sub> = 0V	10	pF

**Note:**

1. Tested initially and after any design or process changes that may affect these parameters.

**AC TEST CONDITIONS**

Parameter	IS62WV5128ALL (Unit)	IS62WV5128BLL (Unit)
Input Pulse Level	0.4V to V <sub>DD</sub> -0.2V	0.4V to V <sub>DD</sub> -0.3V
Input Rise and Fall Times	5 ns	5ns
Input and Output Timing and Reference Level	V <sub>REF</sub>	V <sub>REF</sub>
Output Load	See Figures 1 and 2	See Figures 1 and 2

	IS62WV5128ALL 1.65 - 2.2V	IS62WV5128BLL 2.5V - 3.6V
R1(Ω)	3070	3070
R2(Ω)	3150	3150
V <sub>REF</sub>	0.9V	1.5V
V <sub>TM</sub>	1.8V	2.8V

**AC TEST LOADS**

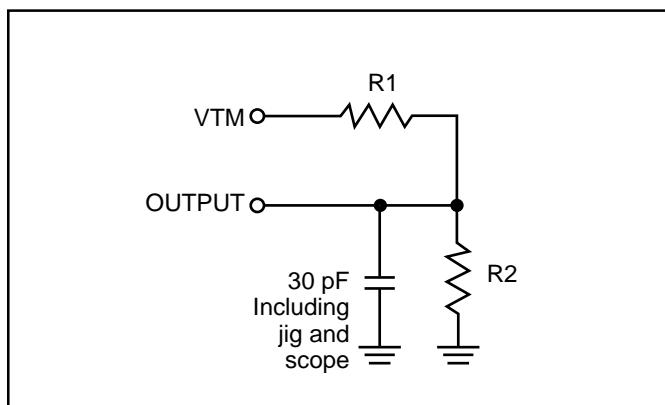


Figure 1

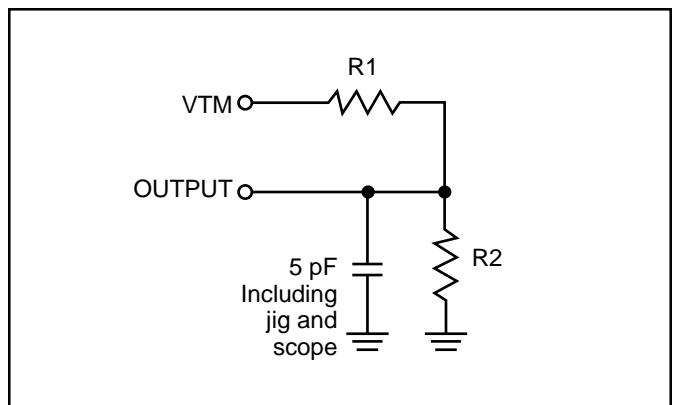


Figure 2

**POWER SUPPLY CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)**62WV5128ALL** (1.65V - 2.2V)

Symbol	Parameter	Test Conditions	Max.		Unit
			70 ns		
I <sub>CC</sub>	V <sub>DD</sub> Dynamic Operating Supply Current	V <sub>DD</sub> = Max.,	Com.	25	mA
		I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Ind.	30	
I <sub>CC1</sub>	Operating Supply Current	V <sub>DD</sub> = Max., $\overline{CS1} = 0.2V$	Com.	10	mA
		$\overline{WE} = V_{DD} - 0.2V$ f = 1 MHz	Ind.	10	
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>DD</sub> = Max.,	Com.	0.35	mA
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CS1} = V_{IH}$ , f = 1 MHz	Ind.	0.35	
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = Max.,	Com.	15	μA
		$\overline{CS1} \geq V_{DD} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0	Ind.	15	

**Note:**

1. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

**POWER SUPPLY CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)**62WV5128BLL** (2.5V - 3.6V)

Symbol	Parameter	Test Conditions	Max.		Unit	
			55 ns	70 ns		
I <sub>CC</sub>	V <sub>DD</sub> Dynamic Operating Supply Current	V <sub>DD</sub> = Max.,	Com.	40	35	mA
		I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Ind.	45	40	
I <sub>CC1</sub>	Operating Supply Current	V <sub>DD</sub> = Max., $\overline{CS1} = 0.2V$	Com.	15	15	mA
		$\overline{WE} = V_{DD} - 0.2V$ f = 1 MHz	Ind.	15	15	
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>DD</sub> = Max.,	Com.	0.35	0.35	mA
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CS1} = V_{IH}$ , f = 1 MHz	Ind.	0.35	0.35	
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = Max.,	Com.	15	15	μA
		$\overline{CS1} \geq V_{DD} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0	Ind.	15	15	

**Note:**

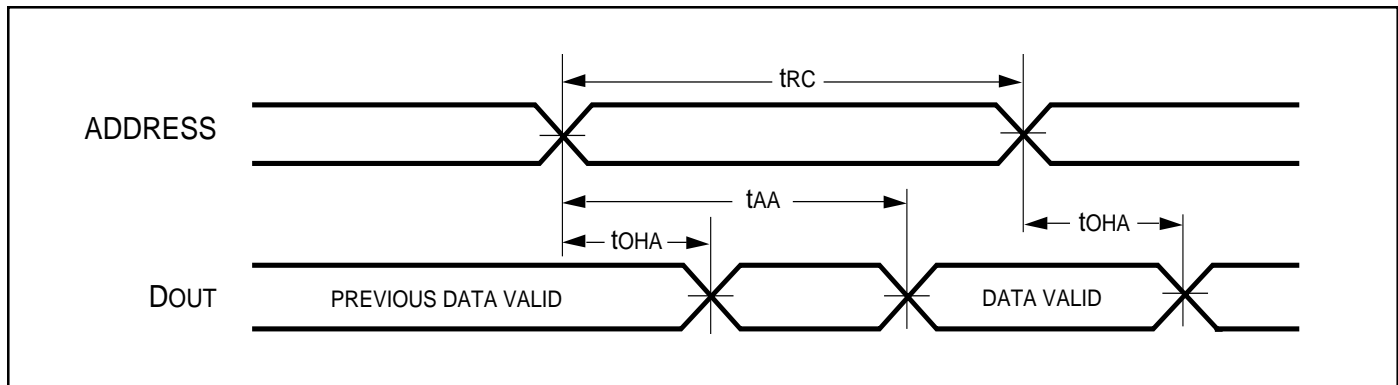
1. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

Symbol	Parameter	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	55	—	70	—	ns
t <sub>AA</sub>	Address Access Time	—	55	—	70	ns
t <sub>OHA</sub>	Output Hold Time	10	—	10	—	ns
t <sub>ACS1</sub>	$\overline{CS1}$ Access Time	—	55	—	70	ns
t <sub>DOE</sub>	$\overline{OE}$ Access Time	—	25	—	35	ns
t <sub>HZOE</sub> <sup>(2)</sup>	$\overline{OE}$ to High-Z Output	—	20	—	25	ns
t <sub>LZOE</sub> <sup>(2)</sup>	$\overline{OE}$ to Low-Z Output	5	—	5	—	ns
t <sub>HZCS1</sub>	$\overline{CS1}$ to High-Z Output	0	20	0	25	ns
t <sub>LZCS1</sub>	$\overline{CS1}$ to Low-Z Output	10	—	10	—	ns

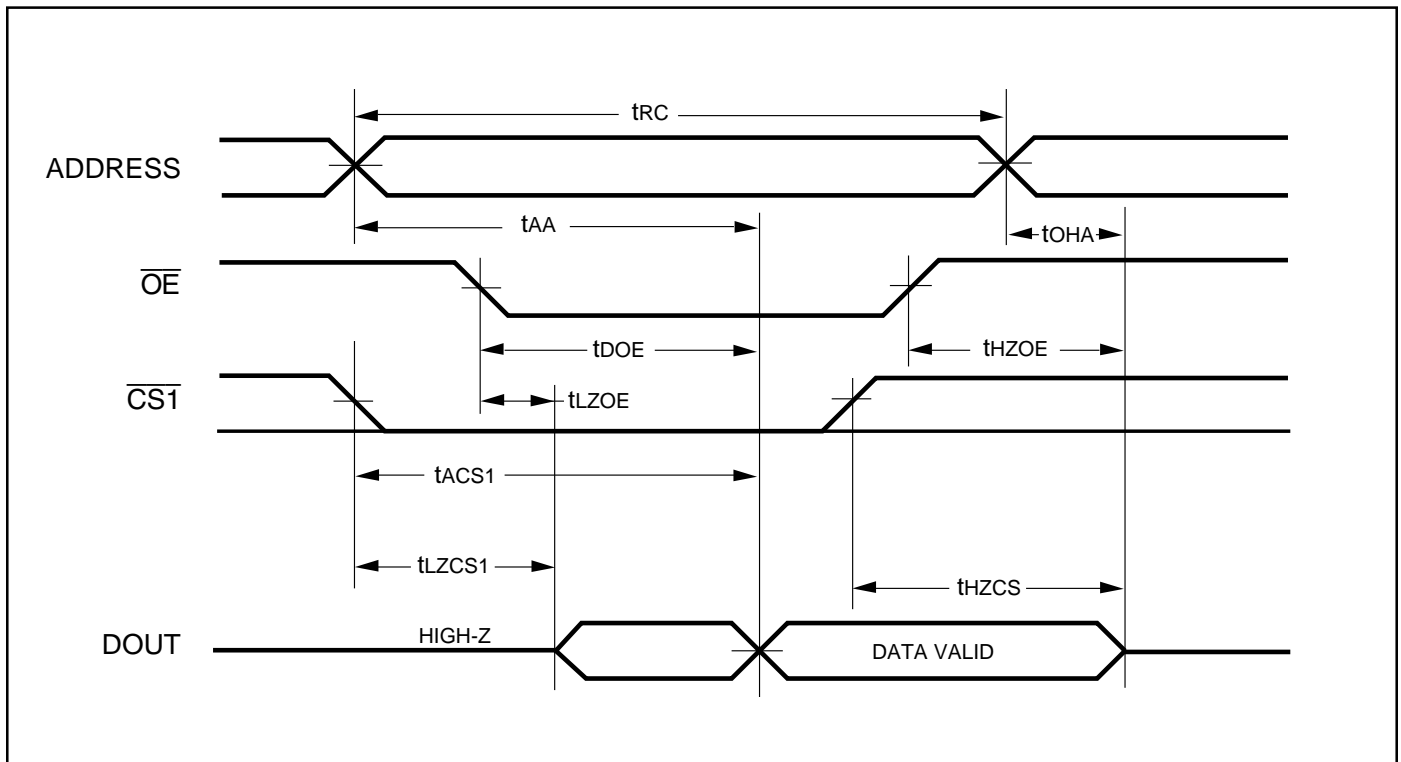
**Notes:**

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to  $V_{DD}-0.2V/V_{DD}-0.3V$  and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.

**AC WAVEFORMS****READ CYCLE NO. 1<sup>(1,2)</sup>** (Address Controlled) ( $\overline{CS1} = \overline{OE} = V_{IL}$ ,  $\overline{WE} = V_{IH}$ )

AC WAVEFORMS

READ CYCLE NO. 2<sup>(1,3)</sup> ( $\overline{CS1}$ ,  $\overline{OE}$  Controlled)



Notes:

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CS1} = V_{IL}$ .  $\overline{WE} = V_{IH}$ .
3. Address is valid prior to or coincident with  $\overline{CS1}$  LOW transition.

**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,2)</sup>** (Over Operating Range)

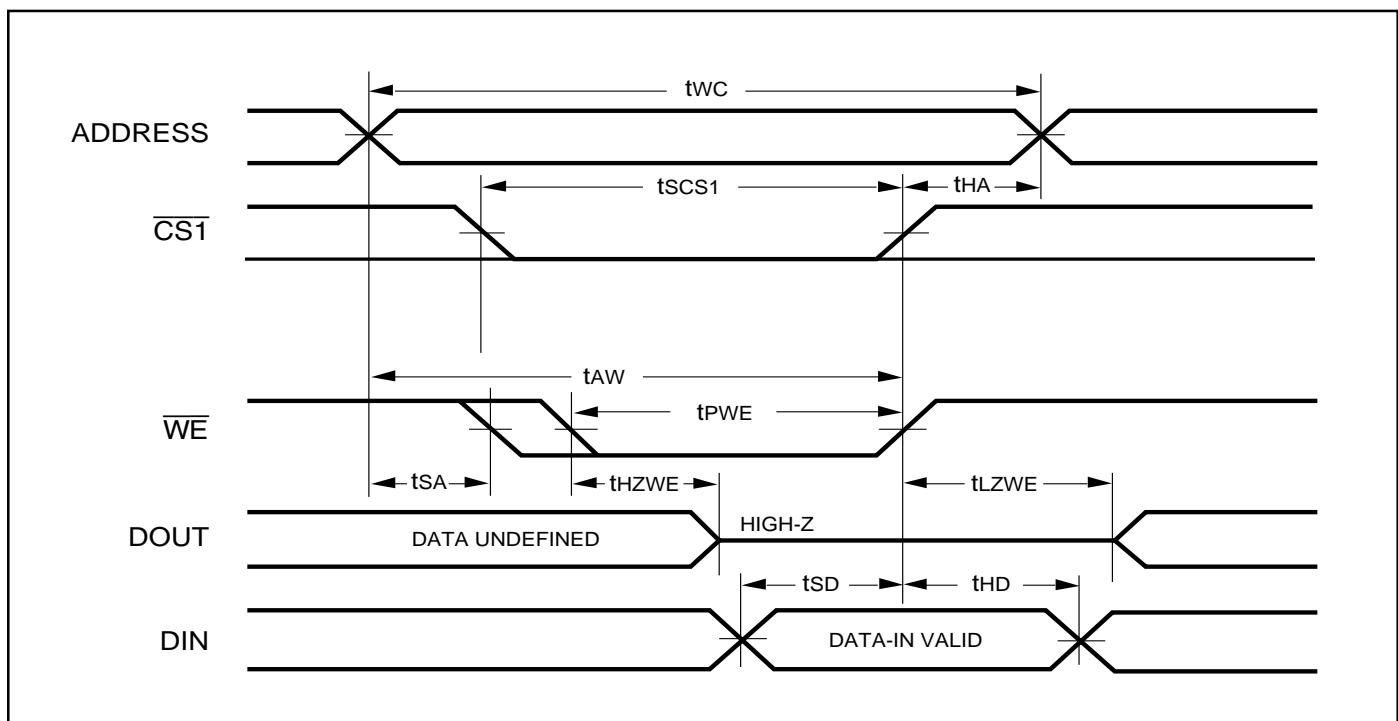
Symbol	Parameter	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time	55	—	70	—	ns
t <sub>SCS1</sub>	$\overline{CS1}$ to Write End	45	—	60	—	ns
t <sub>AW</sub>	Address Setup Time to Write End	45	—	60	—	ns
t <sub>HA</sub>	Address Hold from Write End	0	—	0	—	ns
t <sub>SA</sub>	Address Setup Time	0	—	0	—	ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	40	—	50	—	ns
t <sub>SD</sub>	Data Setup to Write End	25	—	30	—	ns
t <sub>HD</sub>	Data Hold from Write End	0	—	0	—	ns
t <sub>HZWE<sup>(3)</sup></sub>	$\overline{WE}$ LOW to High-Z Output	—	20	—	20	ns
t <sub>LZWE<sup>(3)</sup></sub>	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	ns

**Notes:**

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4V to V<sub>DD</sub>-0.2V/V<sub>DD</sub>-0.3V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of  $\overline{CS1}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

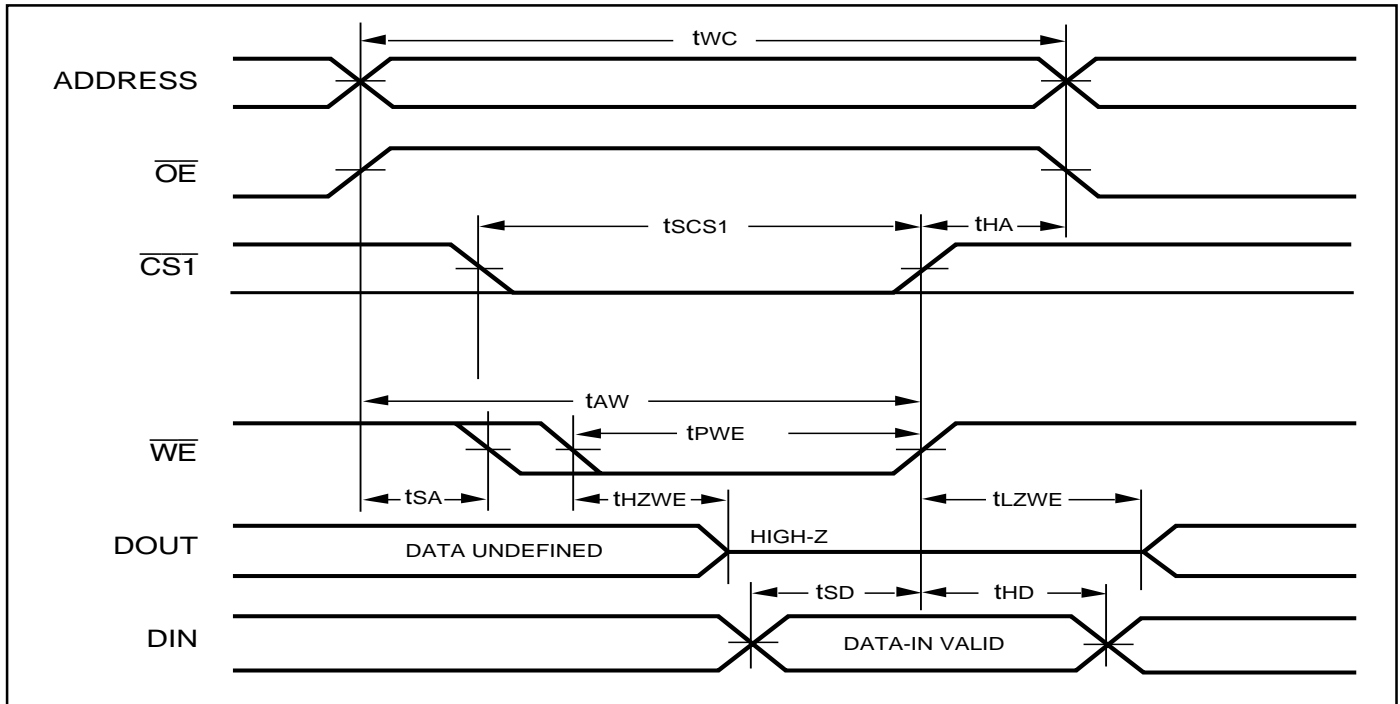
**AC WAVEFORMS**

**WRITE CYCLE NO. 1** ( $\overline{CS1}$  Controlled,  $\overline{OE}$  = HIGH or LOW)

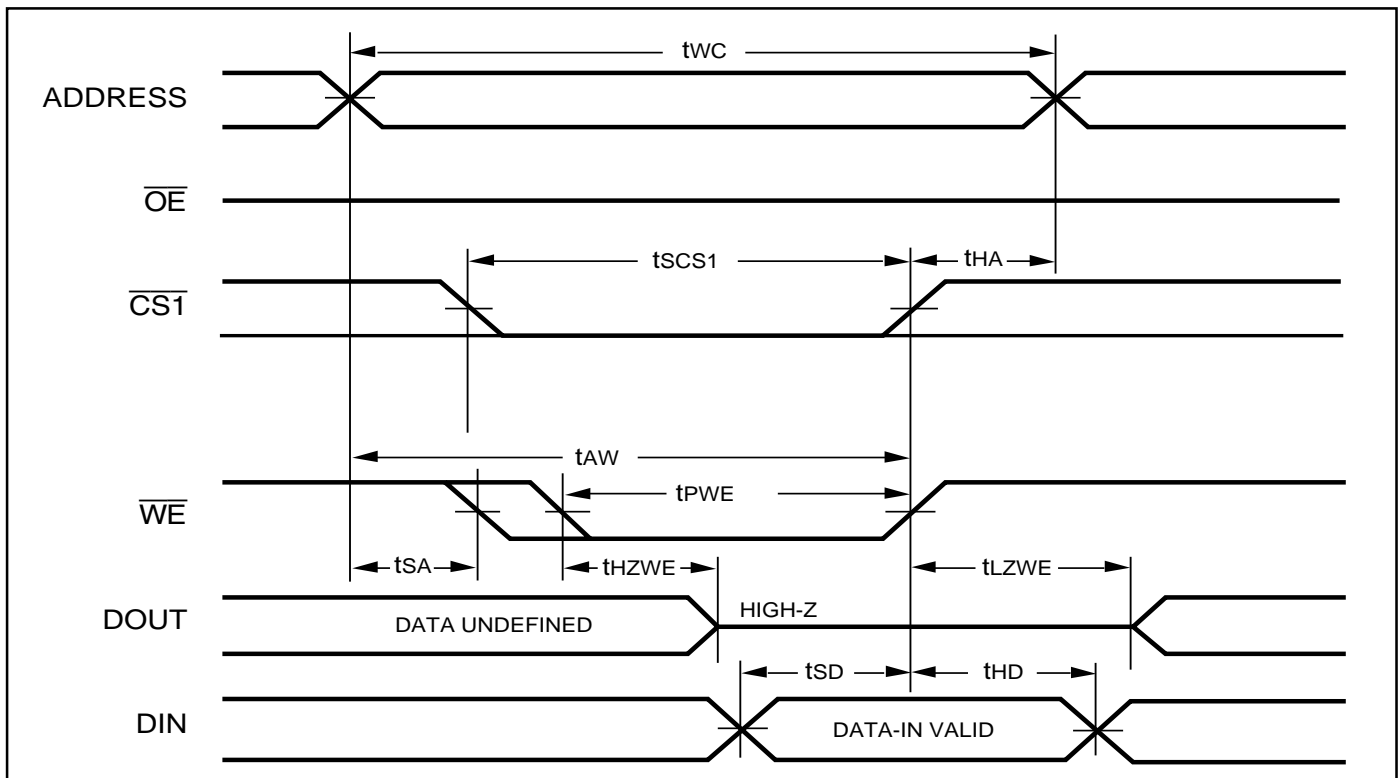




**WRITE CYCLE NO. 2** ( $\overline{WE}$  Controlled:  $\overline{OE}$  is HIGH During Write Cycle)



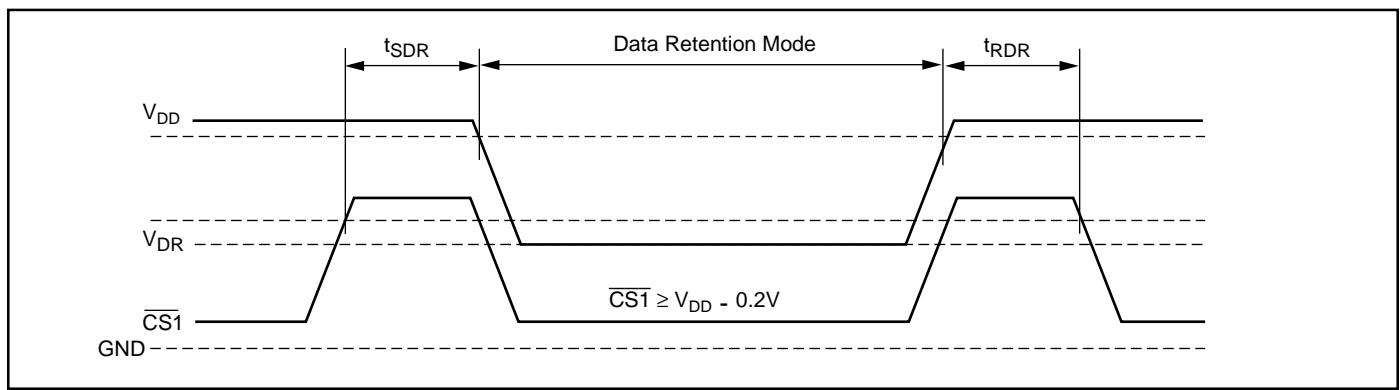
**WRITE CYCLE NO. 3** ( $\overline{WE}$  Controlled:  $\overline{OE}$  is LOW During Write Cycle)



**DATA RETENTION SWITCHING CHARACTERISTICS**

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V <sub>DR</sub>	V <sub>DD</sub> for Data Retention	See Data Retention Waveform	1.2	3.6	V
I <sub>DR</sub>	Data Retention Current	V <sub>DD</sub> = 1.2V, $\overline{CS1} \geq V_{DD} - 0.2V$	—	15	μA
t <sub>SDR</sub>	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t <sub>RDR</sub>	Recovery Time	See Data Retention Waveform	t <sub>RC</sub>	—	ns

**DATA RETENTION WAVEFORM ( $\overline{CS1}$  Controlled)**



**ORDERING INFORMATION****IS62WV5128ALL (1.65V - 2.2V)****Commercial Range: 0°C to +70°C**

Speed (ns)	Order Part No.	Package
70	IS62WV5128ALL-70T	TSOP, TYPE I
70	IS62WV5128ALL-70T2	TSOP, TYPE II
70	IS62WV5128ALL-70H	sTSOP, TYPE I

**Industrial Range: -40°C to +85°C**

Speed (ns)	Order Part No.	Package
70	IS62WV5128ALL-70TI	TSOP, TYPE I
70	IS62WV5128ALL-70T2I	TSOP, TYPE II
70	IS62WV5128ALL-70HI	sTSOP, TYPE I

**ORDERING INFORMATION****IS62WV5128BLL (2.5V - 3.6V)****Commercial Range: 0°C to +70°C**

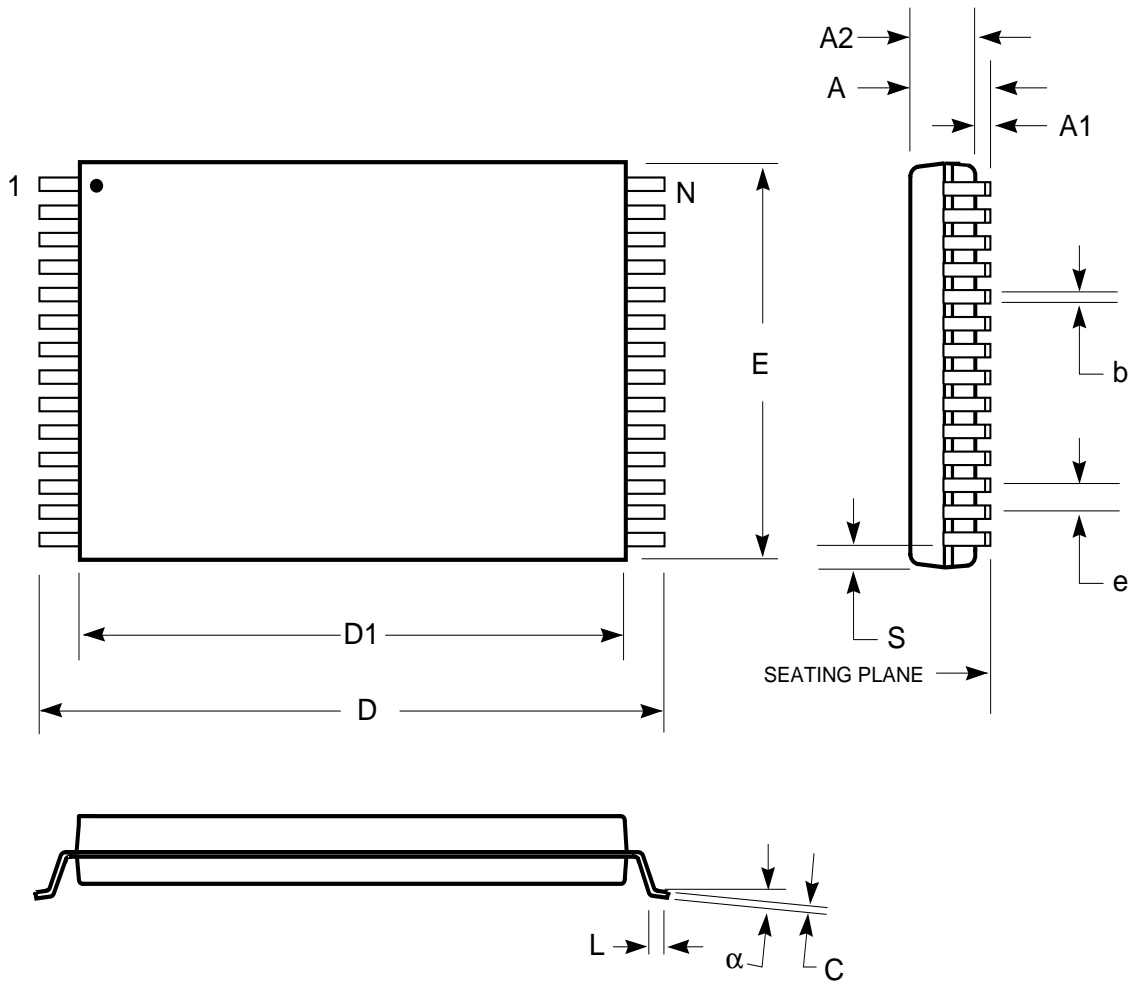
Speed (ns)	Order Part No.	Package
55	IS62WV5128BLL-55T2	TSOP, TYPE II
55	IS62WV5128BLL-55H	sTSOP, TYPE I
70	IS62WV5128BLL-70T	TSOP, TYPE I
70	IS62WV5128BLL-70T2	TSOP, TYPE II
70	IS62WV5128BLL-70H	sTSOP, TYPE I

**Industrial Range: -40°C to +85°C**

Speed (ns)	Order Part No.	Package
55	IS62WV5128BLL-55TI	TSOP, TYPE I
55	IS62WV5128BLL-55T2I	TSOP, TYPE II
55	IS62WV5128BLL-55HI	sTSOP, TYPE I
70	IS62WV5128BLL-70TI	TSOP, TYPE I
70	IS62WV5128BLL-70HI	sTSOP, TYPE I

## PACKAGING INFORMATION

Plastic STSOP - 32 pins  
 Package Code: H (Type I)



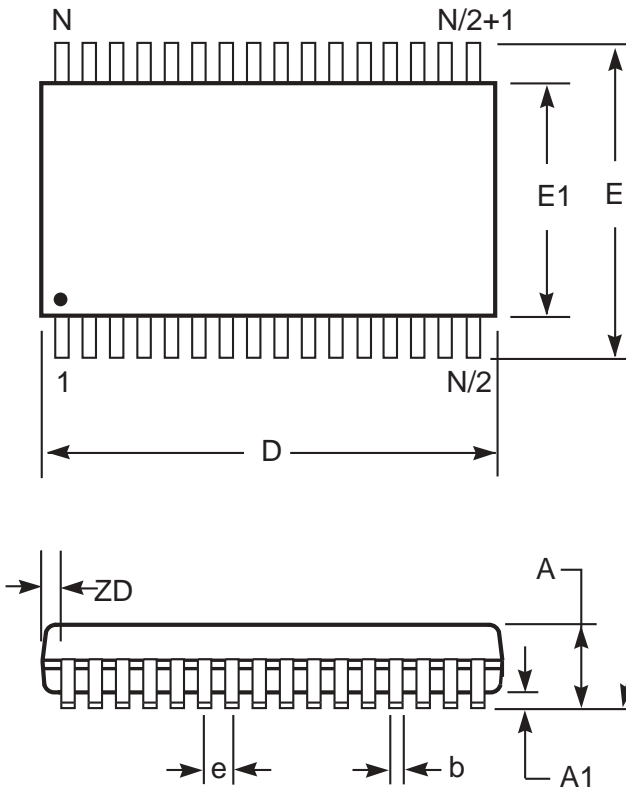
Plastic STSOP (H - Type I)				
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
Ref. Std.				
N	32			
A	—	1.25	—	0.049
A1	0.05	—	0.002	—
A2	0.95	1.05	0.037	0.041
b	0.17	0.23	0.007	0.009
C	0.14	0.16	0.0055	0.0063
D	13.20	13.60	0.520	0.535
D1	11.70	11.90	0.461	0.469
E	7.90	8.10	0.311	0.319
e	0.50 BSC		0.020 BSC	
L	0.30	0.70	0.012	0.028
S	0.28 Typ.		0.011 Typ.	
alpha	0°	5°	0°	5°

**Notes:**

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D1 and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

# PACKAGING INFORMATION

## Plastic TSOP Package Code: T (Type II)



- Notes:**
1. Controlling dimension: millimeters, unless otherwise specified.
  2. BSC = Basic lead spacing between centers.
  3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
  4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

Plastic TSOP (T - Type II)

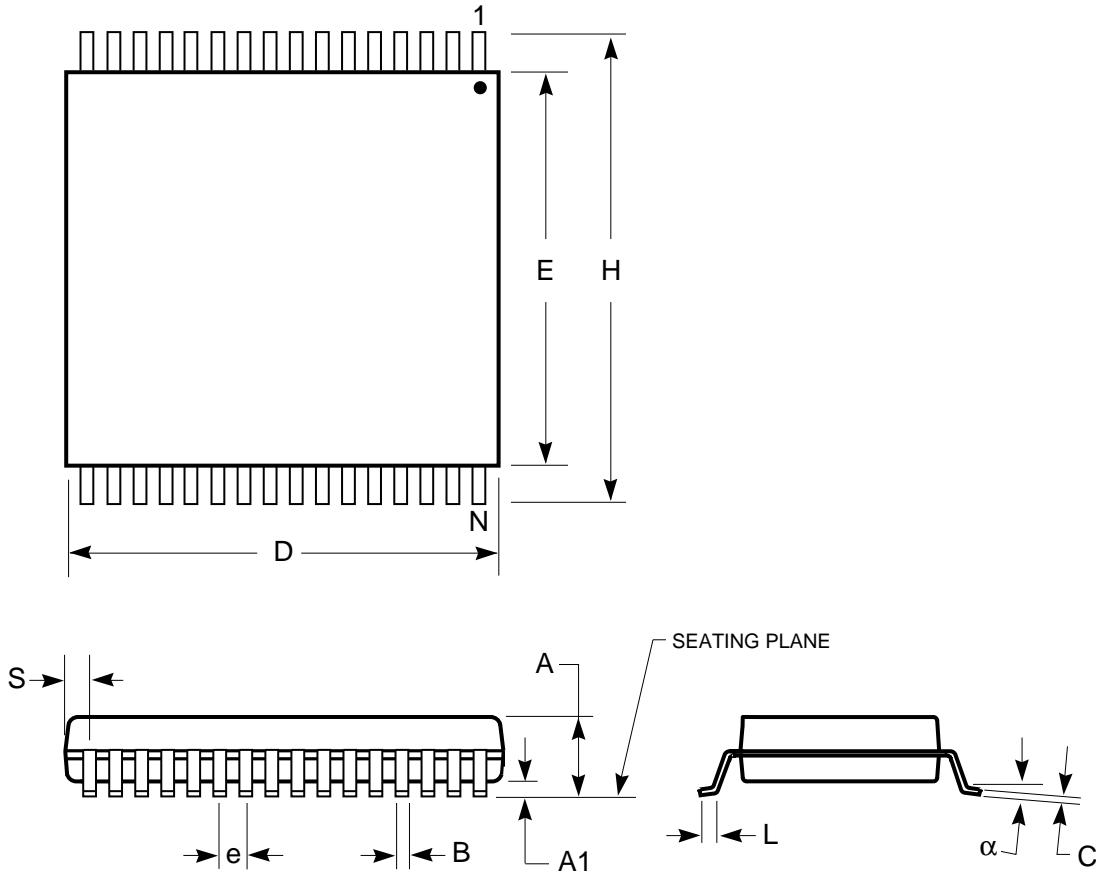
Symbol	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Ref. Std.												
No. Leads (N)	32				44				50			
A	—	1.20	—	0.047	—	1.20	—	0.047	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006
b	0.30	0.52	0.012	0.020	0.30	0.45	0.012	0.018	0.30	0.45	0.012	0.018
C	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008
D	20.82	21.08	0.820	0.830	18.31	18.52	0.721	0.729	20.82	21.08	0.820	0.830
E1	10.03	10.29	0.391	0.400	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E	11.56	11.96	0.451	0.466	11.56	11.96	0.455	0.471	11.56	11.96	0.455	0.471
e	1.27 BSC		0.050 BSC		0.80 BSC		0.032 BSC		0.80 BSC		0.031 BSC	
L	0.40	0.60	0.016	0.024	0.41	0.60	0.016	0.024	0.40	0.60	0.016	0.024
ZD	0.95 REF.		0.037 REF.		0.81 REF.		0.032 REF.		0.88 REF.		0.035 REF.	
α	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°

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Rev. E  
02/20/03

Plastic TSOP - 32 pins  
 Package Code: T (Type I)



Plastic TSOP (T—Type I)				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
Ref. Std.				
No. Leads	32			
A	—	1.20	—	0.047
A1	0.05	0.25	0.002	0.010
B	0.17	0.23	0.007	0.009
C	0.12	0.17	0.006	0.014
D	7.90	8.10	0.308	0.316
E	18.30	18.50	0.714	0.722
H	19.80	20.20	0.772	0.788
e	0.50 BSC		0.020 BSC	
L	0.40	0.60	0.016	0.024
$\alpha$	0°	8°	0°	8°

**Notes:**

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.