

HD74LS273 Octal D-type Positive-edge-triggered Flip-Flops (with Clear)

The HD74LS273, positive-edge-triggered flip-flops utilize LS TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse.

Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse.

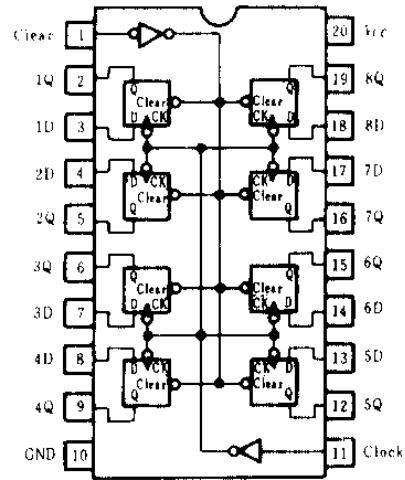
When the clock input is at either the high or low level, the D input signal has no effect at the output.

FUNCTION TABLE

Inputs			Output
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q ₀

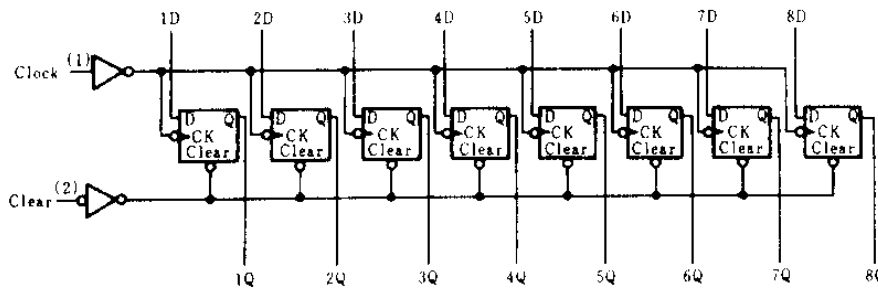
Notes: H = high level, L = low level,
 X = irrelevant
 ↑ = transition from low to high level
 Q₀ = level of Q before the indicated steady-state input conditions were established.

PIN ARRANGEMENT



(Top View)

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply voltage	V _{CC}	4.75	5.00	5.25	V
Output current	I _{OH}	—	—	-400	μA
	I _{OL}	—	—	8	mA
Clock frequency	f _{clock}	0	—	30	MHz
Clock and clear pulse width	t _w	20	—	—	ns
Setup time	Data	20 ↑	—	—	ns
	Clear inactive-state	25 ↑	—	—	
Data hold time	t _h	5 ↑	—	—	ns

Note) ↑ : The arrow indicates the rising edge of clock pulse.



ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input voltage	V_{IH}		2.0	—	—	V
	V_{IL}		—	—	0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}, I_{OH}=-400\mu\text{A}$	2.7	—	—	V
	V_{OL}	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}$	—	—	0.5	V
		$I_{OL}=8\text{mA}$	—	—	0.4	
Input current	I_i	$V_{CC}=5.25\text{V}, V_i=7\text{V}$	—	—	0.1	mA
	I_{IH}	$V_{CC}=5.25\text{V}, V_i=2.7\text{V}$	—	—	20	μA
	I_{IL}	$V_{CC}=5.25\text{V}, V_i=0.4\text{V}$	—	—	-0.4	mA
Short-circuit output current	I_{OS}	$V_{CC}=5.25\text{V}$	-20	—	-100	mA
Supply current	I_{CC}^{**}	$V_{CC}=5.25\text{V}$	—	17	27	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75\text{V}, I_{IN}=-18\text{mA}$	—	—	-1.5	V

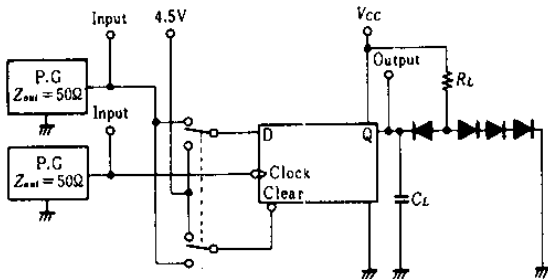
* $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$

** : With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V is applied to clock.

SWITCHING CHARACTERISTICS ($V_{CC}=5\text{V}, T_a=25^\circ\text{C}$)

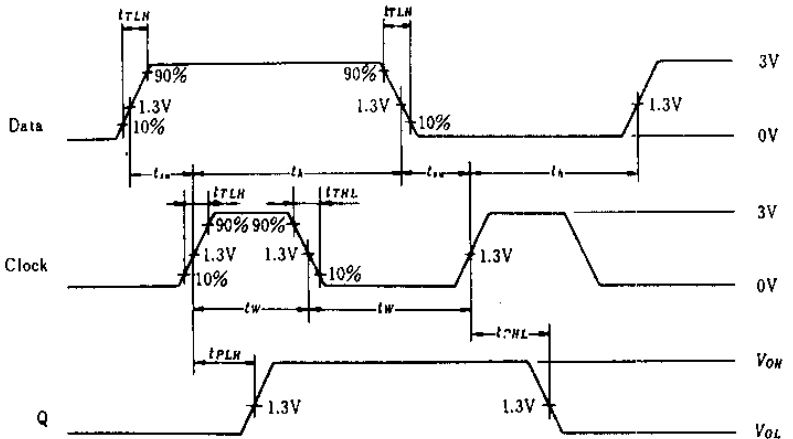
Item	Symbol	Inputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}	Clock		30	—	—	MHz
Propagation Delay Time	t_{PHL}	Clear	$C_L=15\text{pF}, R_L=2\text{k}\Omega$	—	18	27	ns
	t_{PLH}	Clock		—	17	27	
	t_{PHL}			—	18	27	

TESTING METHOD



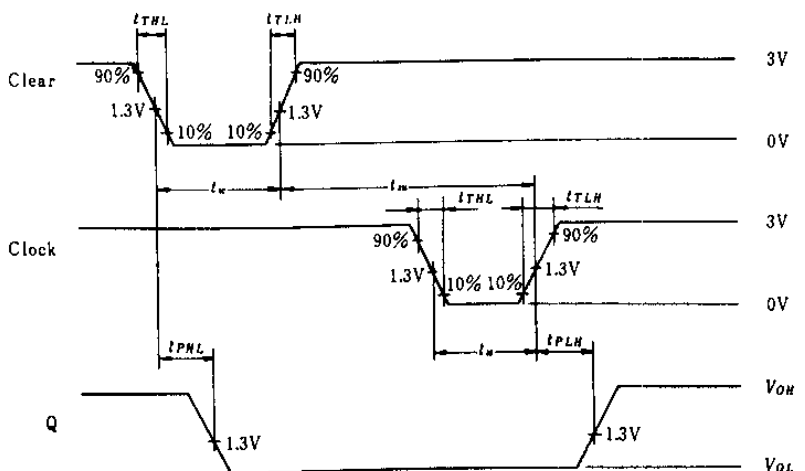
- Notes:
- C_L includes probe and jig capacitance.
 - All diodes are 1S2074 \oplus .

Waveform-1



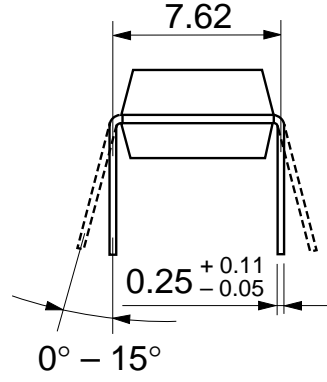
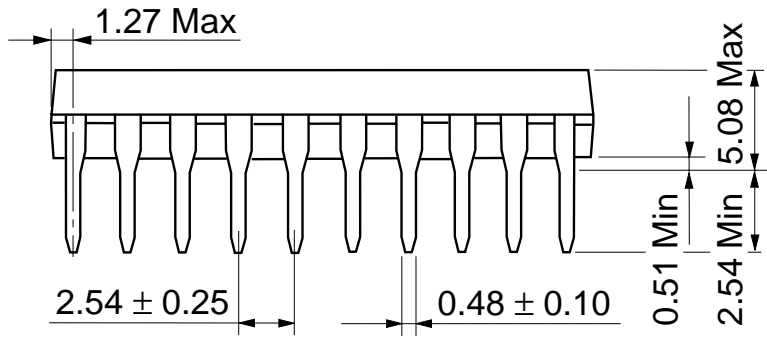
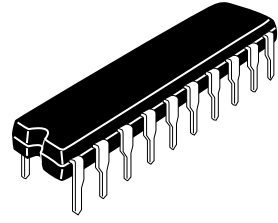
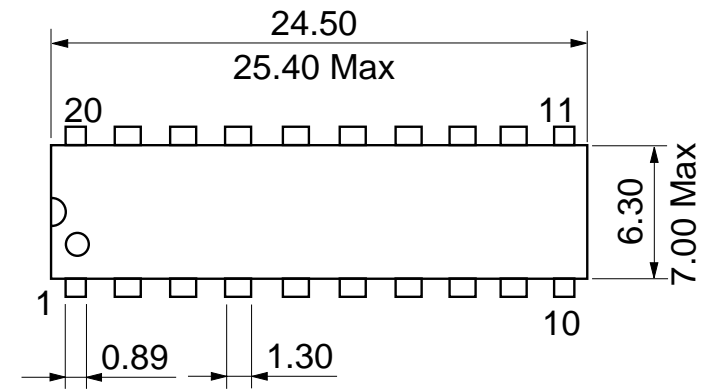
- Notes:
- Input pulse; $t_{TLH} \leq 15\text{ns}$, $t_{TLH} \leq 6\text{ns}$
 Clock input; $PRR = 1\text{MHz}$, duty cycle 50%
 Data input; $PRR = 500\text{kHz}$, duty cycle 50%

Waveform-2



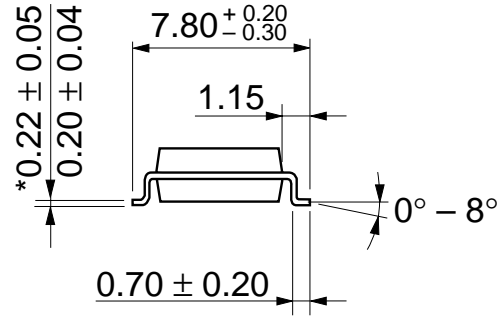
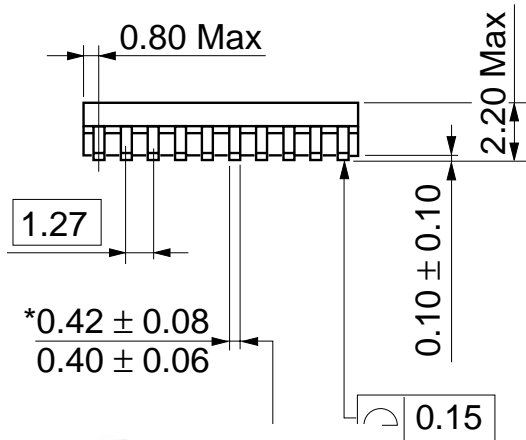
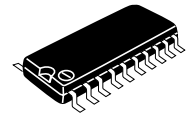
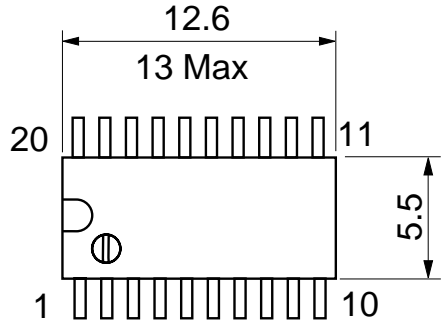
- Note: Input pulse; $t_{TLH} \leq 15\text{ns}$, $t_{THL} \leq 6\text{ns}$, $PRR = 1\text{MHz}$.

Unit: mm



Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Weight (reference value)	1.26 g

Unit: mm

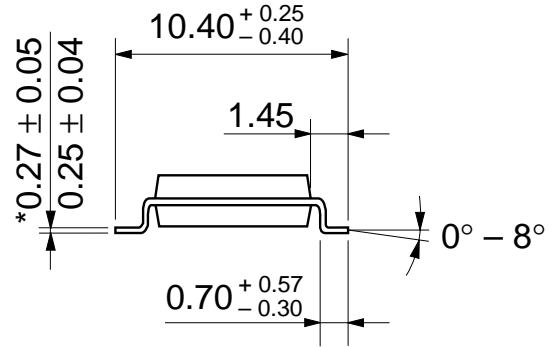
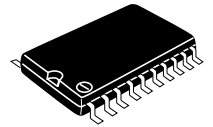
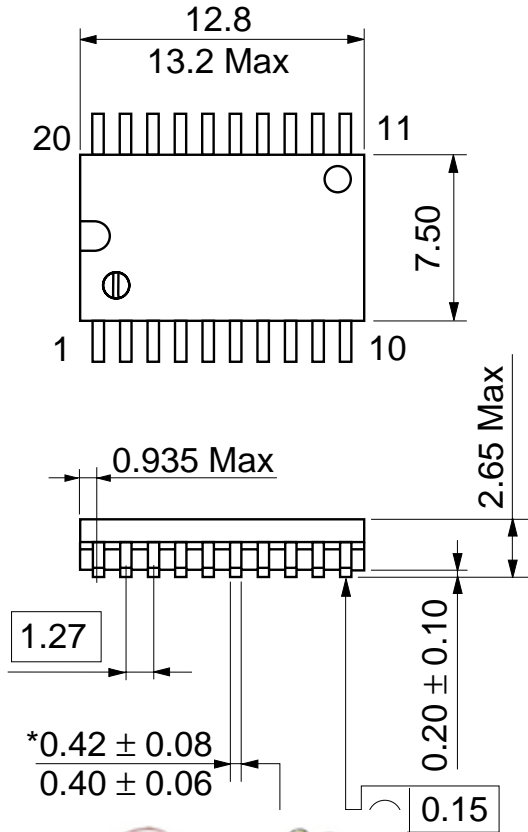


12 (M)

Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.31 g

*Dimension i
Bas

Unit: mm



2 (M)

Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.52 g

*Dimension i
Bas

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HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL NorthAmerica : <http://semiconductor.hitachi.com/>
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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1> (408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher StraÙe 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building, No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

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