Military Plastic pASIC 3 Family Data Sheet

60,000 Usable PLD Gate pASIC 3 FPGA Combining High Performance and High Density

Device Highlights

High Performance & High Density

- 60,000 usable PLD gates with 316 I/Os
- 300 MHz 16-bit counters, 400 MHz datapaths
- 0.35 µm four-layer metal non-volatile CMOS process for smallest die sizes

Easy to Use/Fast Development Cycles

- 100% routable with 100% utilization and complete pin-out stability
- Variable-grain logic cells provide high performance and 100% utilization
- Comprehensive design tools include high quality Verilog/VHDL synthesis

Advanced I/O Capabilities

- Interfaces with 3.3 V and 5.0 V devices
- PCI compliant with 3.3 V and 5.0 V buses for -1/-2 speed grades
- Full JTAG boundary scan
- Registered I/O cells with individually controlled clocks and output enables

Total of 180 I/O pins

- 308 bidirectional input/output pins, PCI-compliant for 5.0 volt and 3.3 volt buses for -1/-2 speed grades
- 8 high-drive input/distributed network pins

Eight Low-Skew Distributed Networks

- Two array clock/control networks are available to the logic cell flip-flop; clock, set, and reset inputs — each can be driven by an input-only pin
- Up to six global clock/control networks are available to the logic cell; F1, clock, set, and reset inputs and the data input, I/O register clock, reset, and enable inputs as well as the output enable control — each can be driven by an input-only pin, I/O pin, any logic cell output, or I/O cell feedback

High Performance

- Input + logic cell + output total delays under 6 ns
- Data path speeds over 400 MHz
- Counter speeds over 300 MHz

Figure 1: Up to 1,584 pASIC 3 Logic Cells

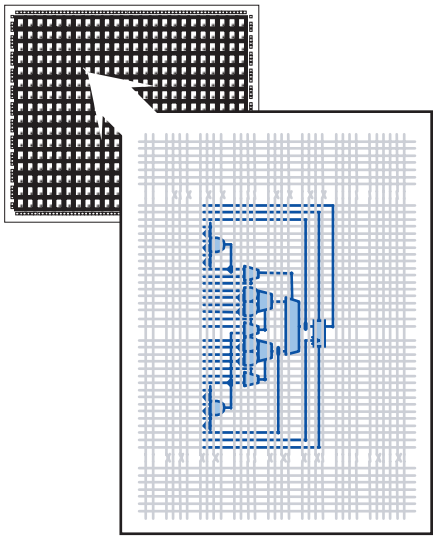


Table 1: Military pASIC 3 Product Family Members

		QL3012	QL3025	QL3040	QL3060
Max Gates		15,740	32,616	48,684	75,232
Logic Array		20x16	28x24	36x28	44x36
Logic Cells		320	672	1,008	1,584
Max Flip-Flops		388	846	1,182	1,758
Max I/O		68	174	174	174
Packages	PLCC	84	-	-	-
	PQFP	-	208	208	208

Table 2: Selector Table

Device	ASIC Gates	PLD Gates	Package	Max I/O	Qualification Level	Supply Voltage
QL3012	8,000	12,000	84 PLCC	68	M[a]	3.3 V
QL3025	16,000	25,000	208 PQFP	174	M[a]	3.3 V
QL3040	24,000	40,000	208 PQFP	174	M[a]	3.3 V
QL3060	36,000	60,000	208 PQFP	174	M[a]	3.3 V

a. M = Military Temperature (-55°C to +125°C)

Architecture Overview

The Military pASIC 3 family of devices have a range of 8,000 to 60,000 usable PLD gates. Military pASIC 3 FPGAs are fabricated on a 0.35 µm four-layer metal process using QuickLogic's patented ViaLink technology to provide a unique combination of high performance, high density, low cost, and extreme ease-of-use.

The Military pASIC 3 family of devices contain a range of 320 to 1,584 logic cells (see **Table 1**). With a range of 68 to 174 I/Os, the Military pASIC 3 family is available in 208-PQFP and 84-PLCC packages. **Table 2** contains the specifications of the Military pASIC 3 family of devices.

Software support for the complete pASIC 3 family is available through two basic packages. The turnkey Quick*Works*® package provides the most complete FPGA software solution from design entry to logic synthesis, to place and route, to simulation. The QuickTools™ for Workstations package provides a solution for designers who use Cadence®, Exemplar™, Mentor®, Synopsys®, Synplicity®, Viewlogic™, Aldec™, or other third-party tools for design entry, synthesis, or simulation.

Electrical Specifications

AC Characteristics at V_{CC} = 3.3 V, TA = 25°C (K = 1.00)

To calculate delays, multiply the appropriate K factor from **Table 12** by the numbers provided in **Table 3** through **Table 10**.

Table 3: Logic Cells

Symbol	Parameter	Propagation Delays (ns) Fanout[a]				
		1	2	3	4	8
t_{PD}	Combinatorial Delay [b]	1.4	1.7	1.9	2.2	3.2
t_{SU}	Setup Time [b]	1.7	1.7	1.7	1.7	1.7
t_{H}	Hold Time	0.0	0.0	0.0	0.0	0.0
t_{CLK}	Clock to Q Delay	0.7	1.0	1.2	1.5	2.5
t_{CWHI}	Clock High Time	1.2	1.2	1.2	1.2	1.2
t_{CWLO}	Clock Low Time	1.2	1.2	1.2	1.2	1.2
t_{SET}	Set Delay	1.0	1.3	1.5	1.8	2.8
t_{RESET}	Reset Delay	0.8	1.1	1.3	1.6	2.6
t_{SW}	Set Width	1.9	1.9	1.9	1.9	1.9
t_{RW}	Reset Width	1.8	1.8	1.8	1.8	1.8

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage, and temperature settings as specified in **Table 12**.
b. These limits are derived from a representative selection of the slowest paths through the pASIC 3 logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of your particular design.

Table 4: Input-Only/Clock Cells

Symbol	Parameter	Propagation Delays (ns) Fanout [a]						
		1	2	3	4	8	12	24
t_{IN}	High Drive Input Delay	1.5	1.6	1.8	1.9	2.4	2.9	4.4
t_{INI}	High Drive Input, Inverting Delay	1.6	1.7	1.9	2.0	2.5	3.0	4.5
t_{ISU}	Input Register Set-Up Time	3.1	3.1	3.1	3.1	3.1	3.1	3.1
t_{IH}	Input Register Hold Time	0.0	0.0	0.0	0.0	0.0	0.0	0.0
t_{ICLK}	Input Register Clock To Q	0.7	0.8	1.0	1.1	1.6	2.1	3.6
t_{IRST}	Input Register Reset Delay	0.6	0.7	0.9	1.0	1.5	2.0	3.5
t_{IESU}	Input Register clock Enable Set-Up Time	2.3	2.3	2.3	2.3	2.3	2.3	2.3
t_{IEH}	Input Register Clock Enable Hold Time	0.0	0.0	0.0	0.0	0.0	0.0	0.0

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage, and temperature settings as specified in **Table 12**.

Table 5: Military QL3012 Clock Cells

Symbol	Parameter	Propagation Delays (ns) Loads per Half Column [a]						
		1	2	3	4	8	10	11
t_{ACK}	Array Clock Delay	1.2	1.2	1.3	1.3	1.5	1.6	1.7
t_{GCKP}	Global Clock Pin Delay	0.7	0.7	0.7	0.7	0.7	0.7	0.7
t_{GCKB}	Global Clock Buffer Delay	0.8	0.8	0.9	0.9	1.1	1.2	1.3

a. The array distributed networks consist of 40 half columns and the global distributed networks consist of 44 half columns, each driven by an independent buffer. The number of half columns used does not affect clock buffer delay. The array clock has up to 8 loads per half column. The global clock has up to 11 loads per half column.

Table 6: Military QL3025 Clock Cells

Symbol	Parameter	Propagation Delays (ns) Loads per Half Column [a]							
		1	2	3	4	8	10	12	15
t_{ACK}	Array Clock Delay	1.2	1.2	1.3	1.3	1.5	1.6	1.7	1.8
t_{GCKP}	Global Clock Pin Delay	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7
t_{GCKB}	Global Clock Buffer Delay	0.8	0.8	0.9	0.9	1.1	1.2	1.3	1.4

a. The array distributed networks consist of 56 half columns and the global distributed networks consist of 60 half columns, each driven by an independent buffer. The number of half columns used does not affect clock buffer delay. The array clock has up to 12 loads per half column. The global clock has up to 15 loads per half column.

Table 7: Military QL3040 Clock Cells

Symbol	Parameter	Propagation Delays (ns) Loads per Half Column [a]								
		1	2	3	4	8	10	12	14	16
t_{ACK}	Array Clock Delay	1.2	1.2	1.3	1.3	1.5	1.6	1.7	1.8	1.9
t_{GCKP}	Global Clock Pin Delay	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7
t_{GCKB}	Global Clock Buffer Delay	0.8	0.8	0.9	0.9	1.1	1.2	1.3	1.4	1.5

a. The array distributed networks consist of 72 half columns and the global distributed networks consist of 76 half columns, each driven by an independent buffer. The number of half columns used does not affect clock buffer delay. The array clock has up to 14 loads per half column. The global clock has up to 16 loads per half column.

Table 8: Military QL3060Clock Cells

Symbol	Parameter	Propagation Delays (ns) Loads per Half Column [a]										
		1	2	3	4	8	10	12	14	16	18	20
t_{ACK}	Array Clock Delay	1.2	1.2	1.3	1.3	1.5	1.6	1.7	1.8	1.9	2.0	2.1
t_{GCKP}	Global Clock Pin Delay	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7
t_{GCKB}	Global Clock Buffer Delay	0.8	0.8	0.9	0.9	1.1	1.2	1.3	1.4	1.5	1.6	1.7

a. The array distributed networks consist of 88 half columns and the global distributed networks consist of 92 half columns, each driven by an independent buffer. The number of half columns used does not affect clock buffer delay. The array clock has up to 18 loads per half column. The global clock has up to 20 loads per half column.

Table 9: Input-Only I/O Cells

Symbol	Parameter	Propagation Delays (ns) Fanout [a]					
		1	2	3	4	8	10
$t_{I/O}$	Input Delay (bidirectional pad)	1.3	1.6	1.8	2.1	3.1	3.6
t_{ISU}	Input Register Set-Up Time	3.1	3.1	3.1	3.1	3.1	3.1
t_{IH}	Input Register Hold Time	0.0	0.0	0.0	0.0	0.0	0.0
t_{IOCLK}	Input Register Clock To Q	0.7	1.0	1.2	1.5	2.5	3.0
t_{IORST}	Input Register Reset Delay	0.6	0.9	1.1	1.4	2.4	2.9
t_{IESU}	Input Register clock Enable Set-Up Time	2.3	2.3	2.3	2.3	2.3	2.3
t_{IEH}	Input Register Clock Enable Hold Time	0.0	0.0	0.0	0.0	0.0	0.0

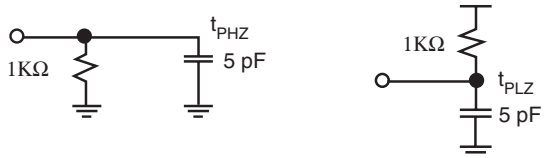
a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage, and temperature settings as specified in **Table 12**.

Table 10: Output-Only I/O Cells

Symbol	Parameter	Propagation Delays (ns) Output Load Capacitance (pF)				
		30	50	75	100	150
t_{OUTLH}	Output Delay Low to High	2.1	2.5	3.1	3.6	4.7
t_{OUTHL}	Output Delay High to Low	2.2	2.6	3.2	3.7	4.8
t_{PZH}	Output Delay Tri-state to High	1.2	1.7	2.2	2.8	3.9
t_{PZL}	Output Delay Tri-state to Low	1.6	2.0	2.6	3.1	4.2
t_{PHZ}	Output Delay High to Tri-State[a]	2.0	-	-	-	-
t_{PLZ}	Output Delay Low to Tri-State[a]	1.2	-	-	-	-

a. The loads presented in **Figure 2** are used for t_{PXZ}:

Figure 2: Loads used for t_{PXZ}



DC Characteristics

The DC specifications are provided in **Table 11** through **Table 13**.

Table 11: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
V_{CC} Voltage	-0.5 V to 4.6 V	DC Input Current	±20 mA
V_{CCIO} Voltage	-0.5 V to 7.0 V	ESD Pad Protection	±2000 V
Input Voltage	-0.5 V to V_{CCIO} +0.5 V	Storage Temperature	-65°C to +150°C
Latch-up Immunity	±200 mA	Lead Temperature	300°C

Table 12: Operating Range

Symbol	Parameter		Military		Unit
			Min.	Max.	
V_{CC}	Supply Voltage		3.0	3.6	V
V_{CCIO}	I/O Input Tolerance Voltage		3.0	5.5	V
TA	Ambient Temperature		-55	-	°C
TC	Case Temperature		-	125	°C
K	Delay Factor	-0 Speed Grade	0.42	2.03	n/a
		-1 Speed Grade	0.42	1.64	n/a
		-2 Speed Grade	0.42	1.37	n/a

Table 13: DC Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{IH}	Input HIGH Voltage		0.5 V_{CC}	V_{CCIO}+0.5	V
V_{IL}	Input LOW Voltage		-0.5	0.3 V_{CC}	V
V_{OH}	Output HIGH Voltage	IOH = -12 mA	2.4	V_{CC}	V
		IOH = -500 µA	0.9 V_{CC}	V_{CC}	V
V_{OL}	Output LOW Voltage	IOL = 8 mA[a]		0.45	V
		IOL = 1.5 mA		0.1 V_{CC}	V
I_I	I or I/O Input Leakage Current	VI = V_{CCIO} or GND	-10	10	µA
I_{OZ}	3-State Output Leakage Current	VI = V_{CCIO} or GND	-10	10	µA
C_I	Input Capacitance[b]			10	pF
I_{OS}	Output Short Circuit Current[c]	VO = GND	-15	-180	mA
		VO = V_{CC}	40	210	mA
I_{CC}	D.C. Supply Current[d]	VI, VIO = V_{CCIO} or GND	0.50 (typ)	5	mA
I_{CCIO}	D.C. Supply Current on V_{CCIO}		0	100	µA

a. Military devices have 8 mA IOL specifications.
b. Capacitance is sample tested only. Clock pins are 12 pF maximum.
c. Only one output at a time. Duration should not exceed 30 seconds.
d. Maximum I_{CC} is 5 mA for all military grade devices. For AC conditions, contact QuickLogic customer applications group (see "Contact Information" on page 21).

Kv and Kt Graphs

Figure 3: Voltage Factor vs. Supply Voltage

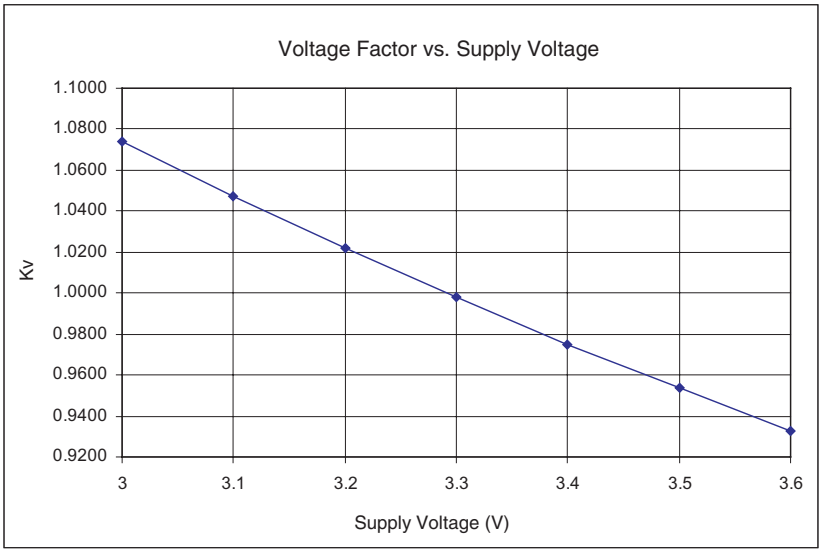
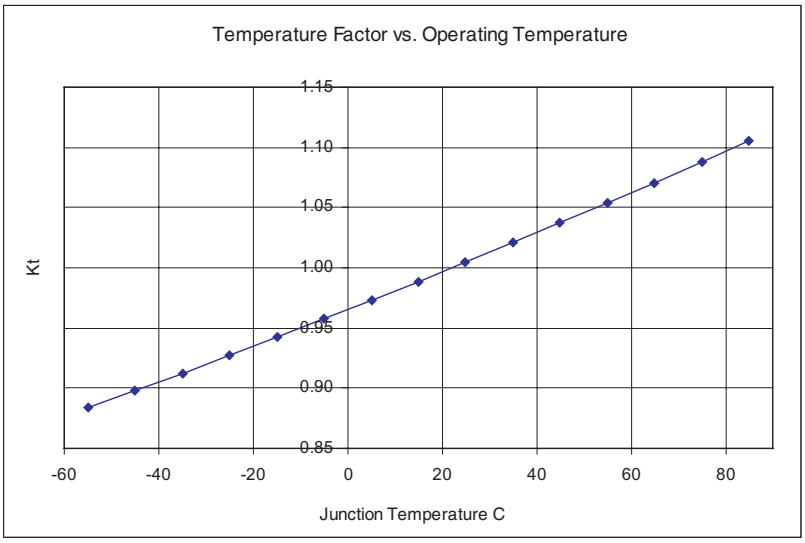
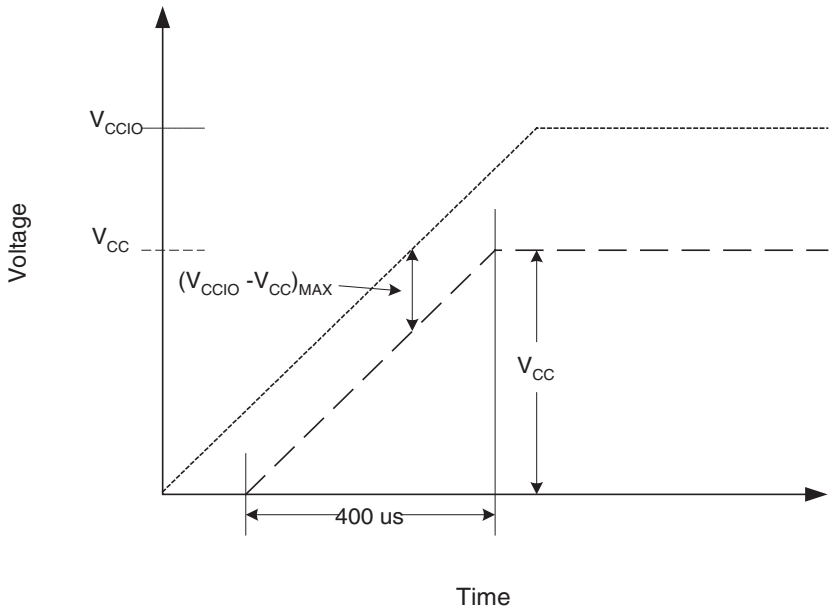


Figure 4: Temperature Factor vs. Operating Temperature



Power-Up Sequencing

Figure 5: Power-Up Requirements



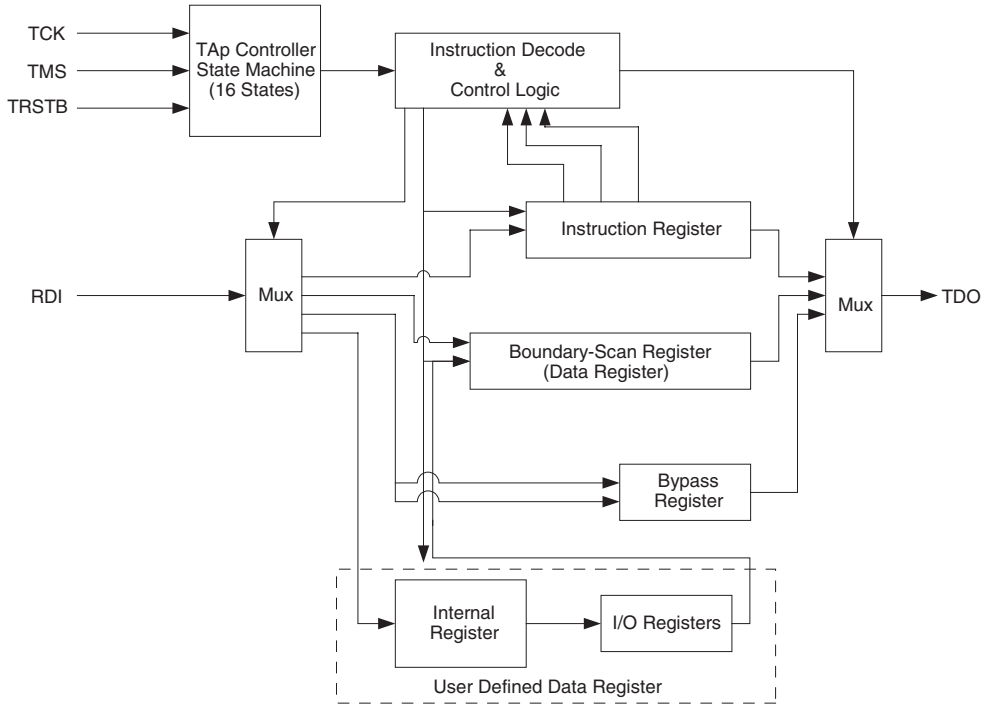
When powering up a device, the V_{CC}/V_{CCIO} rails must take 400 µs or longer to reach the maximum value (refer to **Figure 5**).

NOTE: Ramping V_{CC}/V_{CCIO} to the maximum voltage faster than 400 µs can cause the device to behave improperly.

For users with a limited power budget, keep $(V_{CCIO} - V_{CC})_{MAX} \leq 500$ mV when ramping up the power supply.

JTAG

Figure 6: JTAG Block Diagram



Microprocessors and Application Specific Integrated Circuits (ASICs) pose many design challenges, not the least of which concerns the accessibility of test points. The Joint Test Access Group (JTAG) formed in response to this challenge, resulting in IEEE standard 1149.1, the Standard Test Access Port and Boundary Scan Architecture.

The JTAG boundary scan test methodology allows complete observation and control of the boundary pins of a JTAG-compatible device through JTAG software. A Test Access Port (TAP) controller works in concert with the Instruction Register (IR); these allow users to run three required tests, along with several user-defined tests.

JTAG tests allow users to reduce system debug time, reuse test platforms and tools, and reuse subsystem tests for fuller verification of higher level system elements.

The 1149.1 standard requires the following three tests:

- **Extest Instruction.** The Extest Instruction performs a printed circuit board (PCB) interconnect test. This test places a device into an external boundary test mode, selecting the boundary scan register to be connected between the TAP Test Data In (TDI) and Test Data Out (TDO) pins. Boundary scan cells are preloaded with test patterns (via the Sample/Preload Instruction), and input boundary cells capture the input data for analysis.
- **Sample/Preload Instruction.** The Sample/Preload Instruction allows a device to remain in its functional mode, while selecting the boundary scan register to be connected between the TDI and TDO pins. For this test, the boundary scan register can be accessed via a data scan operation, allowing users to sample the functional data entering and leaving the device.

- **Bypass Instruction.** The Bypass Instruction allows data to skip a device boundary scan entirely, so the data passes through the bypass register. The Bypass instruction allows users to test a device without passing through other devices. The bypass register is connected between the TDI and TDO pins, allowing serial data to be transferred through a device without affecting the operation of the device.

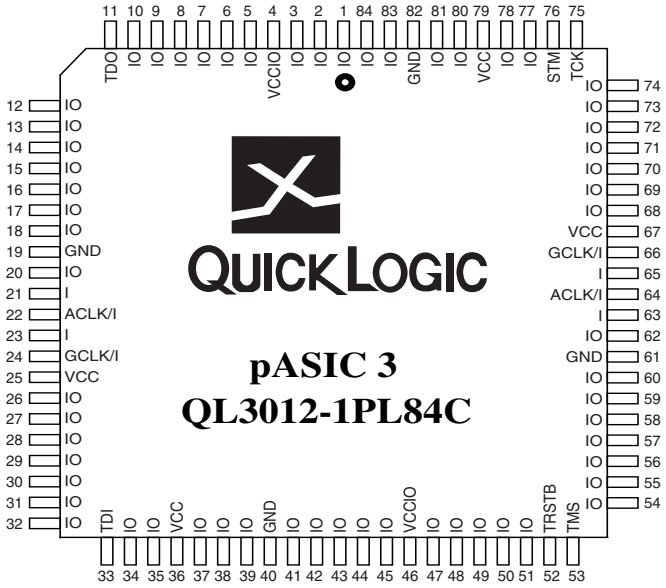
Pin Descriptions

Table 14: Pin Descriptions

Pin	Function	Description
TDI	Test data in for JTAG	Hold HIGH during normal operation. Connect to V_{CC} if not used for JTAG.
TRSTB	Active low reset for JTAG	Hold LOW during normal operation. Connect to ground if not used for JTAG.
TMS	Test mode select for JTAG	Hold HIGH during normal operation. Connect to V_{CC} if not used for JTAG.
TCK	Test clock for JTAG	Hold HIGH or LOW during normal operation. Connect to V_{CC} or ground if not used for JTAG.
TDO	Test data out for JTAG	Output that must be left unconnected if not used for JTAG.
STM	Special test mode	Must be grounded during normal operation.
I/ACLK	High-drive input and/or array network driver	Can be configured as either or both.
I/GCLK	High-drive input and/or global network driver	Can be configured as either or both.
I	High-drive input	Use for input signals with high fanout.
I/O	Input/output pin	Can be configured as an input and/or output.
V_{CC}	Power supply pin	Connect to 3.3 V supply.
V_{CCIO}	Input voltage tolerance pin	Connect to 5.0 V supply if 5.0 V input tolerance is required, otherwise connect to 3.3 V supply.
GND	Ground pin	Connect to ground.

QL3012 – 84 PLCC Pinout Diagram

Figure 7: QL3012 – 84 Pin PLCC (Top View)



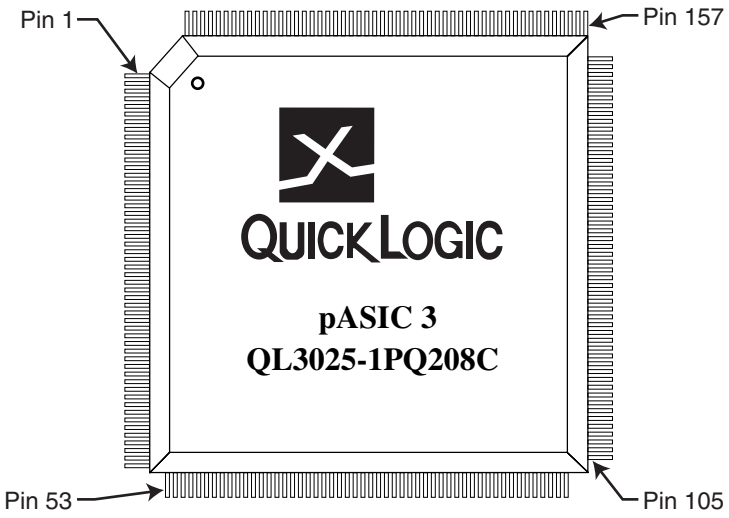
QL3012 – 84 PLCC Pinout Table

Table 15: QL3012 – 84 PLCC Pinout Table

84 PLCC	Function	84 PLCC	Function	84 PLCC	Function	84 PLCC	Function
1	I/O	22	ACLK/I	43	I/O	64	ACLK/I
2	I/O	23	I	44	I/O	65	I
3	I/O	24	GCLK/I	45	I/O	66	GCLK/I
4	VCCIO	25	VCC	46	VCCIO	67	VCC
5	I/O	26	I/O	47	I/O	68	I/O
6	I/O	27	I/O	48	I/O	69	I/O
7	I/O	28	I/O	49	I/O	70	I/O
8	I/O	29	I/O	50	I/O	71	I/O
9	I/O	30	I/O	51	I/O	72	I/O
10	I/O	31	I/O	52	TRSTB	73	I/O
11	TDO	32	I/O	53	TMS	74	I/O
12	I/O	33	TDI	54	I/O	75	TCK
13	I/O	34	I/O	55	I/O	76	STM
14	I/O	35	I/O	56	I/O	77	I/O
15	I/O	36	VCC	57	I/O	78	I/O
16	I/O	37	I/O	58	I/O	79	VCC
17	I/O	38	I/O	59	I/O	80	I/O
18	I/O	39	I/O	60	I/O	81	I/O
19	GND	40	GND	61	GND	82	GND
20	I/O	41	I/O	62	I/O	83	I/O
21	I	42	I/O	63	I	84	I/O

QL3025 – 208 PQFP Pinout Diagram

Figure 8: QL3025 – 208 Pin PQFP (Top View)



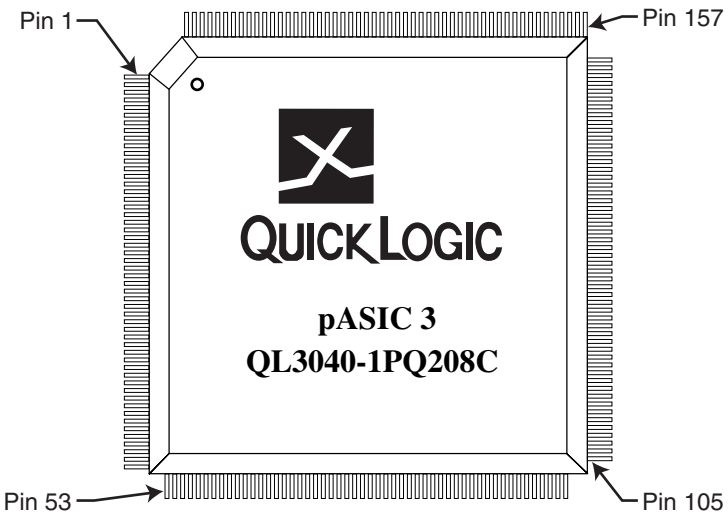
QL3025 – 208 PQFP Pinout Table

Table 16: QL3025 – 208 PQFP Pinout Table

208 PQFP	Function	208 PQFP	Function	208 PQFP	Function	208 PQFP	Function	208 PQFP	Function
1	I/O	43	GND	85	I/O	127	GND	169	I/O
2	I/O	44	I/O	86	I/O	128	I/O	170	I/O
3	I/O	45	I/O	87	I/O	129	I	171	I/O
4	I/O	46	I/O	88	I/O	130	ACLK/I	172	I/O
5	I/O	47	I/O	89	I/O	131	VCC	173	I/O
6	I/O	48	I/O	90	I/O	132	I	174	I/O
7	I/O	49	I/O	91	I/O	133	GCLK/I	175	I/O
8	I/O	50	I/O	92	I/O	134	VCC	176	I/O
9	I/O	51	I/O	93	I/O	135	I/O	177	GND
10	VCC	52	I/O	94	I/O	136	I/O	178	I/O
11	I/O	53	I/O	95	GND	137	I/O	179	I/O
12	GND	54	TDI	96	I/O	138	I/O	180	I/O
13	I/O	55	I/O	97	VCC	139	I/O	181	I/O
14	I/O	56	I/O	98	I/O	140	I/O	182	GND
15	I/O	57	I/O	99	I/O	141	I/O	183	I/O
16	I/O	58	I/O	100	I/O	142	I/O	184	I/O
17	I/O	59	GND	101	I/O	143	I/O	185	I/O
18	I/O	60	I/O	102	I/O	144	I/O	186	I/O
19	I/O	61	VCC	103	TRSTB	145	VCC	187	VCCIO
20	I/O	62	I/O	104	TMS	146	I/O	188	I/O
21	I/O	63	I/O	105	I/O	147	GND	189	I/O
22	I/O	64	I/O	106	I/O	148	I/O	190	I/O
23	GND	65	I/O	107	I/O	149	I/O	191	I/O
24	I/O	66	I/O	108	I/O	150	I/O	192	I/O
25	I	67	I/O	109	I/O	151	I/O	193	I/O
26	ACLK/I	68	I/O	110	I/O	152	I/O	194	I/O
27	VCC	69	I/O	111	I/O	153	I/O	195	I/O
28	I	70	I/O	112	I/O	154	I/O	196	I/O
29	GCLK/I	71	I/O	113	I/O	155	I/O	197	I/O
30	VCC	72	I/O	114	VCC	156	I/O	198	I/O
31	I/O	73	GND	115	I/O	157	TCK	199	GND
32	I/O	74	I/O	116	GND	158	STM	200	I/O
33	I/O	75	I/O	117	I/O	159	I/O	201	VCC
34	I/O	76	I/O	118	I/O	160	I/O	202	I/O
35	I/O	77	I/O	119	I/O	161	I/O	203	I/O
36	I/O	78	GND	120	I/O	162	I/O	204	I/O
37	I/O	79	I/O	121	I/O	163	GND	205	I/O
38	I/O	80	I/O	122	I/O	164	I/O	206	I/O
39	I/O	81	I/O	123	I/O	165	VCC	207	TDO
40	I/O	82	I/O	124	I/O	166	I/O	208	I/O
41	VCC	83	VCCIO	125	I/O	167	I/O		
42	I/O	84	I/O	126	I/O	168	I/O		

QL3040 – 208 PQFP Pinout Diagram

Figure 9: QL3040 – 208 Pin PQFP (Top View)



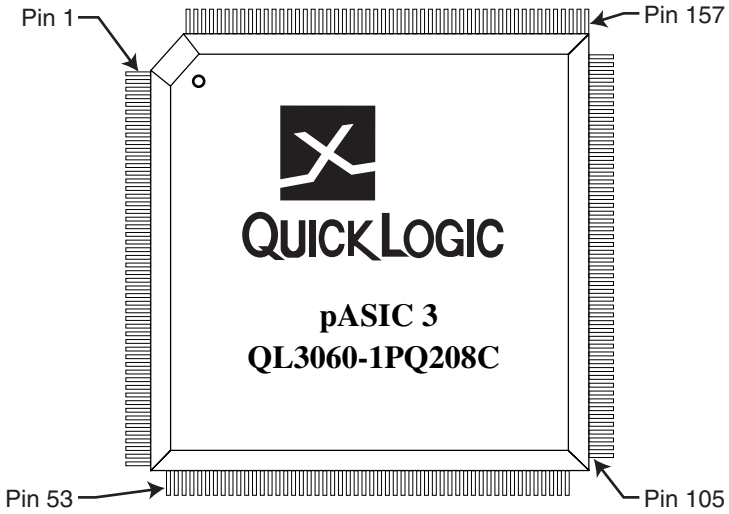
QL3040 – 208 PQFP Pinout Table

Table 17: QL3040 – 208 PQFP Pinout Table

208 PQFP	Function	208 PQFP	Function	208 PQFP	Function	208 PQFP	Function	208 PQFP	Function
1	I/O	43	GND	85	I/O	127	GND	169	I/O
2	I/O	44	I/O	86	I/O	128	I/O	170	I/O
3	I/O	45	I/O	87	I/O	129	GCLK/I	171	I/O
4	I/O	46	I/O	88	I/O	130	ACLK/I	172	I/O
5	I/O	47	I/O	89	I/O	131	VCC	173	I/O
6	I/O	48	I/O	90	I/O	132	GCLK/I	174	I/O
7	I/O	49	I/O	91	I/O	133	GCLK/I	175	I/O
8	I/O	50	I/O	92	I/O	134	VCC	176	I/O
9	I/O	51	I/O	93	I/O	135	I/O	177	GND
10	VCC	52	I/O	94	I/O	136	I/O	178	I/O
11	I/O	53	I/O	95	GND	137	I/O	179	I/O
12	GND	54	TDI	96	I/O	138	I/O	180	I/O
13	I/O	55	I/O	97	VCC	139	I/O	181	I/O
14	I/O	56	I/O	98	I/O	140	I/O	182	GND
15	I/O	57	I/O	99	I/O	141	I/O	183	I/O
16	I/O	58	I/O	100	I/O	142	I/O	184	I/O
17	I/O	59	GND	101	I/O	143	I/O	185	I/O
18	I/O	60	I/O	102	I/O	144	I/O	186	I/O
19	I/O	61	VCC	103	TRSTB	145	VCC	187	VCCIO
20	I/O	62	I/O	104	TMS	146	I/O	188	I/O
21	I/O	63	I/O	105	I/O	147	GND	189	I/O
22	I/O	64	I/O	106	I/O	148	I/O	190	I/O
23	GND	65	I/O	107	I/O	149	I/O	191	I/O
24	I/O	66	I/O	108	I/O	150	I/O	192	I/O
25	GCLK/I	67	I/O	109	I/O	151	I/O	193	I/O
26	ACLK/I	68	I/O	110	I/O	152	I/O	194	I/O
27	VCC	69	I/O	111	I/O	153	I/O	195	I/O
28	GCLK/I	70	I/O	112	I/O	154	I/O	196	I/O
29	GCLK/I	71	I/O	113	I/O	155	I/O	197	I/O
30	VCC	72	I/O	114	VCC	156	I/O	198	I/O
31	I/O	73	GND	115	I/O	157	TCK	199	GND
32	I/O	74	I/O	116	GND	158	STM	200	I/O
33	I/O	75	I/O	117	I/O	159	I/O	201	VCC
34	I/O	76	I/O	118	I/O	160	I/O	202	I/O
35	I/O	77	I/O	119	I/O	161	I/O	203	I/O
36	I/O	78	GND	120	I/O	162	I/O	204	I/O
37	I/O	79	I/O	121	I/O	163	GND	205	I/O
38	I/O	80	I/O	122	I/O	164	I/O	206	I/O
39	I/O	81	I/O	123	I/O	165	VCC	207	TDO
40	I/O	82	I/O	124	I/O	166	I/O	208	I/O
41	VCC	83	VCCIO	125	I/O	167	I/O		
42	I/O	84	I/O	126	I/O	168	I/O		

QL3060 – 208 PQFP Pinout Diagram

Figure 10: QL3060 – 208 Pin PQFP (Top View)



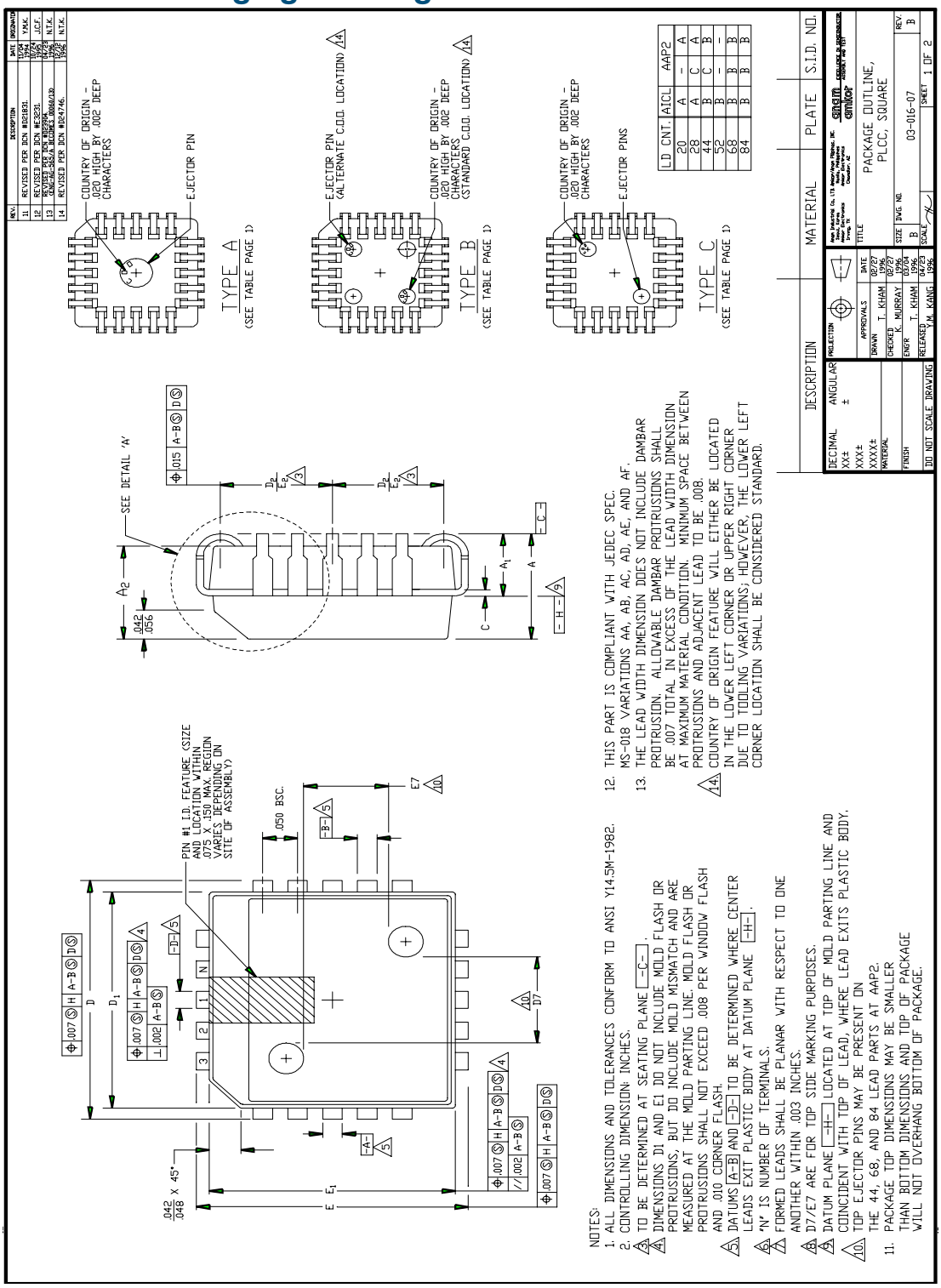
QL3060 – 208 PQFP Pinout Table

Table 18: QL3060 – 208 PQFP Pinout Table

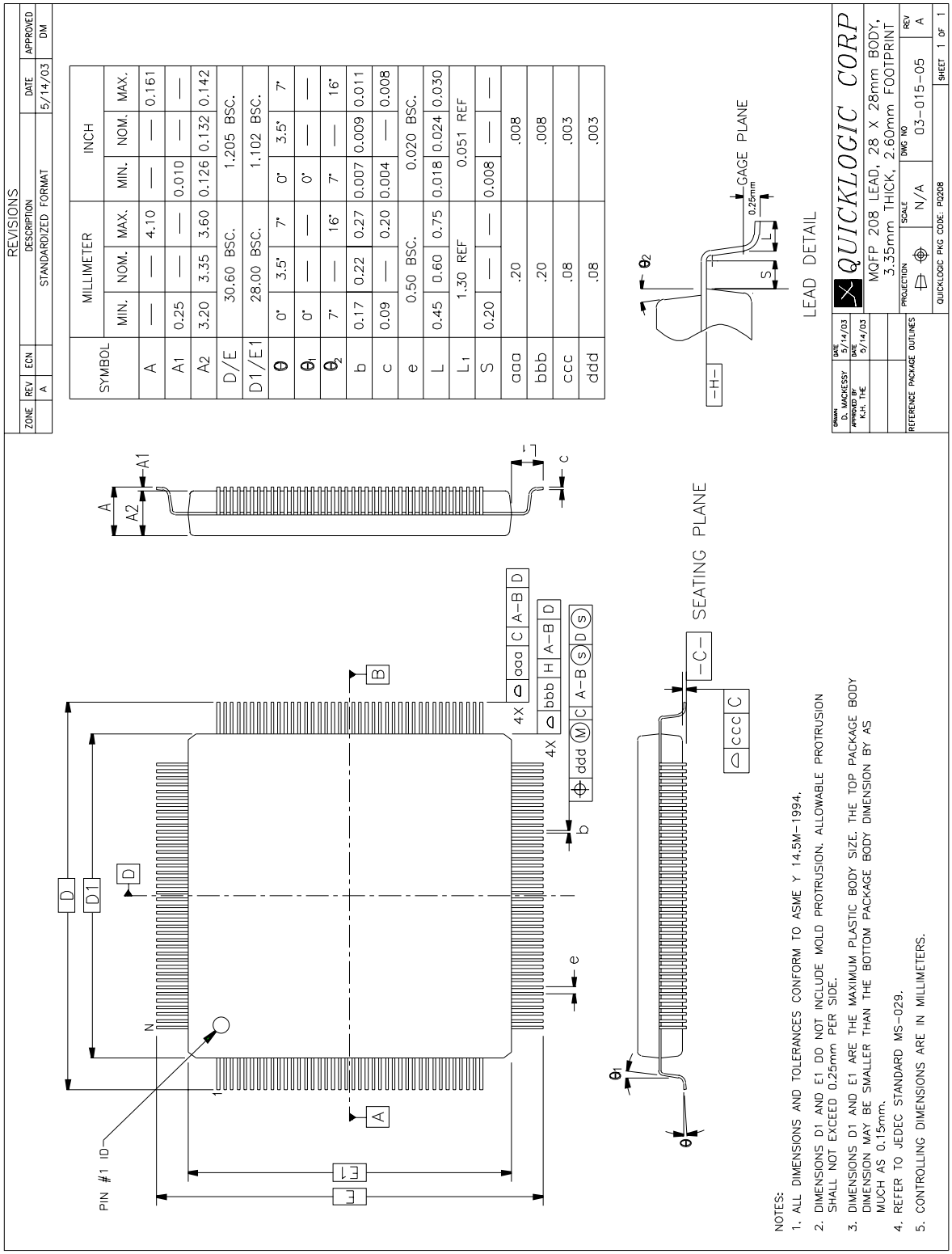
208 PQFP	Function	208 PQFP	Function	208 PQFP	Function	208 PQFP	Function	208 PQFP	Function
1	I/O	43	GND	85	I/O	127	GND	169	I/O
2	I/O	44	I/O	86	I/O	128	I/O	170	I/O
3	I/O	45	I/O	87	I/O	129	GCLK/I	171	I/O
4	I/O	46	I/O	88	I/O	130	ACLK/I	172	I/O
5	I/O	47	I/O	89	I/O	131	VCC	173	I/O
6	I/O	48	I/O	90	I/O	132	GCLK/I	174	I/O
7	I/O	49	I/O	91	I/O	133	GCLK/I	175	I/O
8	I/O	50	I/O	92	I/O	134	VCC	176	I/O
9	I/O	51	I/O	93	I/O	135	I/O	177	GND
10	VCC	52	I/O	94	I/O	136	I/O	178	I/O
11	I/O	53	I/O	95	GND	137	I/O	179	I/O
12	GND	54	TDI	96	I/O	138	I/O	180	I/O
13	I/O	55	I/O	97	V_{CC}	139	I/O	181	I/O
14	I/O	56	I/O	98	I/O	140	I/O	182	GND
15	I/O	57	I/O	99	I/O	141	I/O	183	I/O
16	I/O	58	I/O	100	I/O	142	I/O	184	I/O
17	I/O	59	GND	101	I/O	143	I/O	185	I/O
18	I/O	60	I/O	102	I/O	144	I/O	186	I/O
19	I/O	61	VCC	103	TRSTB	145	VCC	187	VCCIO
20	I/O	62	I/O	104	TMS	146	I/O	188	I/O
21	I/O	63	I/O	105	I/O	147	GND	189	I/O
22	I/O	64	I/O	106	I/O	148	I/O	190	I/O
23	GND	65	I/O	107	I/O	149	I/O	191	I/O
24	I/O	66	I/O	108	I/O	150	I/O	192	I/O
25	GCLK/I	67	I/O	109	I/O	151	I/O	193	I/O
26	ACLK/I	68	I/O	110	I/O	152	I/O	194	I/O
27	VCC	69	I/O	111	I/O	153	I/O	195	I/O
28	GCLK/I	70	I/O	112	I/O	154	I/O	196	I/O
29	GCLK/I	71	I/O	113	I/O	155	I/O	197	I/O
30	VCC	72	I/O	114	VCC	156	I/O	198	I/O
31	I/O	73	GND	115	I/O	157	TCK	199	GND
32	I/O	74	I/O	116	GND	158	STM	200	I/O
33	I/O	75	I/O	117	I/O	159	I/O	201	VCC
34	I/O	76	I/O	118	I/O	160	I/O	202	I/O
35	I/O	77	I/O	119	I/O	161	I/O	203	I/O
36	I/O	78	GND	120	I/O	162	I/O	204	I/O
37	I/O	79	I/O	121	I/O	163	GND	205	I/O
38	I/O	80	I/O	122	I/O	164	I/O	206	I/O
39	I/O	81	I/O	123	I/O	165	VCC	207	TDO
40	I/O	82	I/O	124	I/O	166	I/O	208	I/O
41	VCC	83	VCCIO	125	I/O	167	I/O		
42	I/O	84	I/O	126	I/O	168	I/O		

Package Mechanical Drawings

84 PLCC Packaging Drawing



208 PQFP Packaging Drawing



Packaging Information

The Military pASIC 3 product family packaging information is presented in **Table 19**.

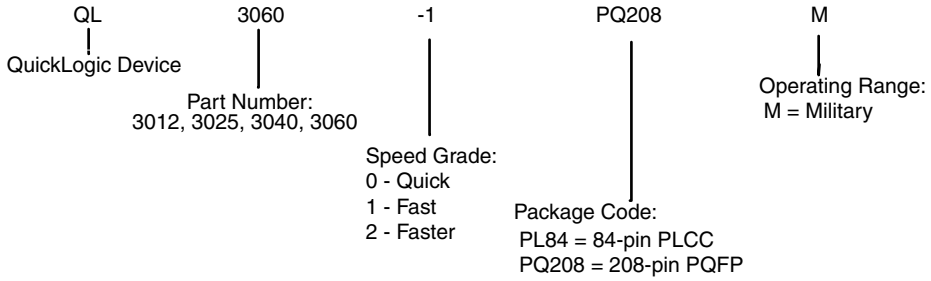
NOTE: Military temperature range plastic packages will be added as follows on products to the commercial and industrial products.

Table 19: Military Packaging Options

Device Information	Device							
	QL3012		QL3025		QL3040		QL3060	
	Pin	Pitch	Pin	Pin	Pitch	Pin	Pitch	Pitch
Package Definitions[a]	84 PLCC	0.05 in.	208 PQFP	0.5 mm	208 PQFP	0.5 mm	208 PQFP	0.5 mm

a. PLCC = Plastic Leaded Chip Carrier
PQFP = Plastic Quad Flat Pack

Ordering Information



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Revision History

Revision	Date	Originator and Comments
A	October 1999	Not available
B	December 2000	Not available
C	April 2005	Mehul Kochar and Kathleen Murchek Update format and content.

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