YAMAHA

YTD436

ISTC

ISDN BRI controller with S/T ref. pt. analog D/R

YTD436 is a high-performance communication LSI for the ISDN BRI user-network interface function (digital four-wire time-division full-duplex operation), supporting D channel layer 1 and layer 2 functions in one 100-pin SQFP chip.

YTD436 supports layer 1 (physical layer) control function conforming to ITU-T Recommendation I.430 and fully supports layer 2 (LAPD protocol) function conforming to ITU-T Recommendations Q.920 and Q.921. ETSI (European Telecommunication Standards Institute) and North American standard operating modes are also supported.

In addition, YTD436 includes layer 3 processor interface function which operate in DMA transfer mode or I/O transfer mode. This gives a great advantage for mounting and functional designing of both “active” (CPU on board) terminal equipment and “passive” (no CPU on board) PC cards.

The layer 1 function has a built-in S/T reference point analog driver/receiver to support the S/T reference point interface. In order to support the U interface, YTD436 also has a I.430 TTL interface (no built-in analog driver/receiver) suitable for connecting to an NT1 chip or a DSU module.

YAMAHA CORPORATION

YTD436 CATALOG
CATALOG No.:4TD436A41
2005.1

Features

1. Layer 1 function

- Conforms to ITU-T Recommendation I.430 (1992 edition) and TTC Standard JT-I430 (1997 edition) (default)
  - 192 kbps transmission rate
  - Interface structure : 2B + D (B = 64 kbps, D = 16 kbps)
  - Frame assembling and disassembling function
  - Collision control (built-in random number (Ri) reset), priority control (built-in retransmission control), and state transition control
  - Programmable T3 and T4 timers
- Supports ETSI ETS 300 012 (April 1992) and ANSI T1.605 operating modes
- Leased line capability (JT-I430-a)
- Built-in driver and receiver
  - I.430 TTL interface (when the driver / receiver is disconnected)
  - No external relay or common-mode choke needed
  - Supports 1-to-2 pulse transformer
- Abundant Test functions (for testing and maintenance)
  - Demo mode in which no switch simulator is needed.
  - Three kinds of loop-back modes (Loop-back 1 to 3)
  - INFO signals output for testing
  - Test pulse output for pulse shape check
- Multiframing capability
- INFO1 transmission and INFO4 reception monitor pins
- Power down monitor pin
- I.430 transmission frame phase adjustment function

2. Layer 2 function

- Conforms to ITU-T Recommendation Q.920 (1992 edition) and Q.921 (1997 edition) and TTC Standard JT-Q920 (1993 edition) and JT-Q921 (1998 edition)
  - HDLC frame control (Flag control, FCS generation/checking, Automatic zero insertion/deletion, Abort pattern transmission/detection, etc.)
  - LAPD status control (Sequence control, Flow control, SAPI control)
  - Built-in timer for time-out check
- Supports ETSI ETS 300 125 (September 1991), National ISDN-1/2, AT&T 5ESS 5E9 and Nortel DMS-100 S208-6 operating modes
- Multilink capability (circuit switching × 2 links, packet switching/teleaction communications × 2 links)
- Automatic assigned TEI/non-automatic assigned TEI (VC/PVC)
- Leased line mode (disable layer 2 function)

3. Layer 3 interface function

- Connects to 8-bit or 16-bit microprocessor
  (8086 family, 80186 family, 6800 family, 68000 family)
- Operates in one of two data transfer modes :
  - DMA transfer mode (with the built-in 16-bit address DMA controller)
  - I/O transfer mode (with the built-in FIFO)
- Primitive logical interface

4. B channel interface

- Data rate setting : 64 k, 56 k and 32 kbps
- Serial mode
  - B channel I/O clock selection function
    - Internal clock mode
      Inputs/outputs the B channel data with 64 k, 56 k or 32 kHz internal clock
    - External clock mode (PCM Highway mode)
      Inputs/outputs the B channel data with a 128 k to 2048 kHz external clock
  - B channel selection function
    - Internal clock mode
      Selects/switches B channel I/O pins
    - External clock mode (PCM Highway mode)
      Selects/switches B channel time slots
- Parallel mode
  - LSB/MSB switching function
  - Bit shift function
  - Data transfer mode
    - DMA transfer mode with the DMA request function
    - I/O transfer mode with the built-in FIFO

5. Low-power operation

(Host processor clock control function, Powerdown mode)

6. High-performance CMOS technology

7. 100-pin SQFP

8. DigitalSupply Voltage (+5V or +3.3V), Analog +5V supply

Applications

- ISDN telephone
- Video telephone
- Telemeter
- PBX
- Terminal adapter (TA)
- Other ISDN terminals

Functional Comparison of YAMAHA ISDN S/T Interface LSIs

FUNCTION			YTD410	YM7405B	YTD418	YTD423	YTD436
Layer 1	ITU-T Recommendation	I.430	1992 edition	1992 edition	1992 edition	1992 edition	1992 edition
	TTC Standard	JT-I430	1993 edition	1993 edition	1993 edition	1993 edition	1997 edition
Layer 2 (LAPD)	ITU-T Recommendation	Q.920 Q.921	1992 edition	1992 edition	1992 edition	1992 edition	1992 edition 1997 edition
	TTC Standard	JT-Q920 JT-Q921	1993 edition	1993 edition	1993 edition	1993 edition	1993 edition 1998 edition
ETSI ETS 300 012, ETS 300 125				√	√	√	√
North American Switches National ISDN-1/2, AT&T 5ESS, Nortel DMS-100						√	√
S/T Reference Point Analog Driver/Receiver			Internal	Internal	External [YTD421B]	External [YTD421B]	Internal
Maximum D Channel Links	Circuit Switching		1	2	2	2	2
	Dch Packet Switching (Teleaction Communication)		1	2	2	2	2 (2)
D Channel Layer 3 Data Transfer Method			DMA Transfer	DMA Transfer	DMA Transfer	DMA Transfer or I/O Transfer	DMA Transfer or I/O Transfer
HDLC Controller and DMA Controller for B Channel Data			External	External	External	Internal	Internal
B Channel Data Transfer Method			–	–	–	DMA Transfer or I/O Transfer	DMA Transfer or I/O Transfer **(Note 1)**
B Channel Internal Clock Mode (kHz)			56, 64	64	64	32, 56, 64	32, 56, 64
B Channel External Clock Mode				√	√	√	√
Clock Output Function for MPU			√			√	√
Signal Output Function for Testing			√			√	√
Supply Voltage (V)			+5	+5	+5	+5	+5 or +3.3 **(Note 2)**
Power Consumption during Operation [typ.] (mW)			65	125	75	85	75 (@+5V) 40 (@+3.3V)
Power Consumption during Sleep [typ.] (mW)			2	30	21	1	less than 0.5 **(Note 3)**
Package			80 pin QFP 100 pin TQFP	80 pin QFP 100 pin TQFP	80 Pin QFP	100 pin SQFP	100 pin SQFP

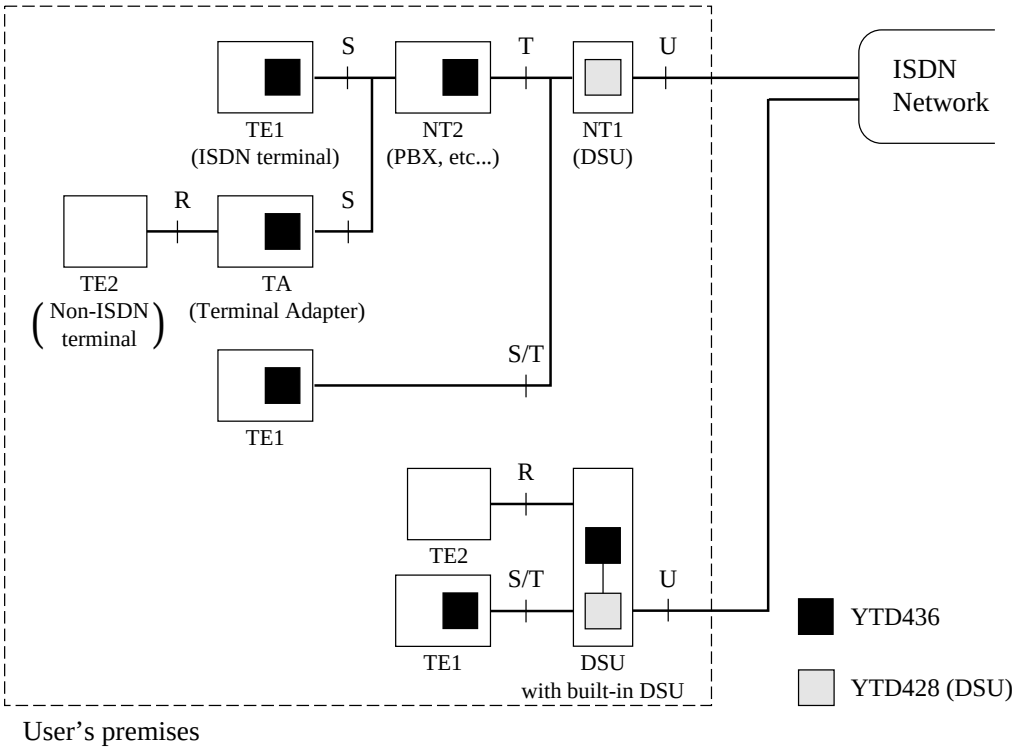
Note 1: DMA Transfer: Request function only
I/O transfer: 4 byte FIFO
Note 2: With respect to Digital Supply Voltage
Note 3: State at Line interface disconnection + Power down (SLEEP state)

BLOCK DIAGRAM

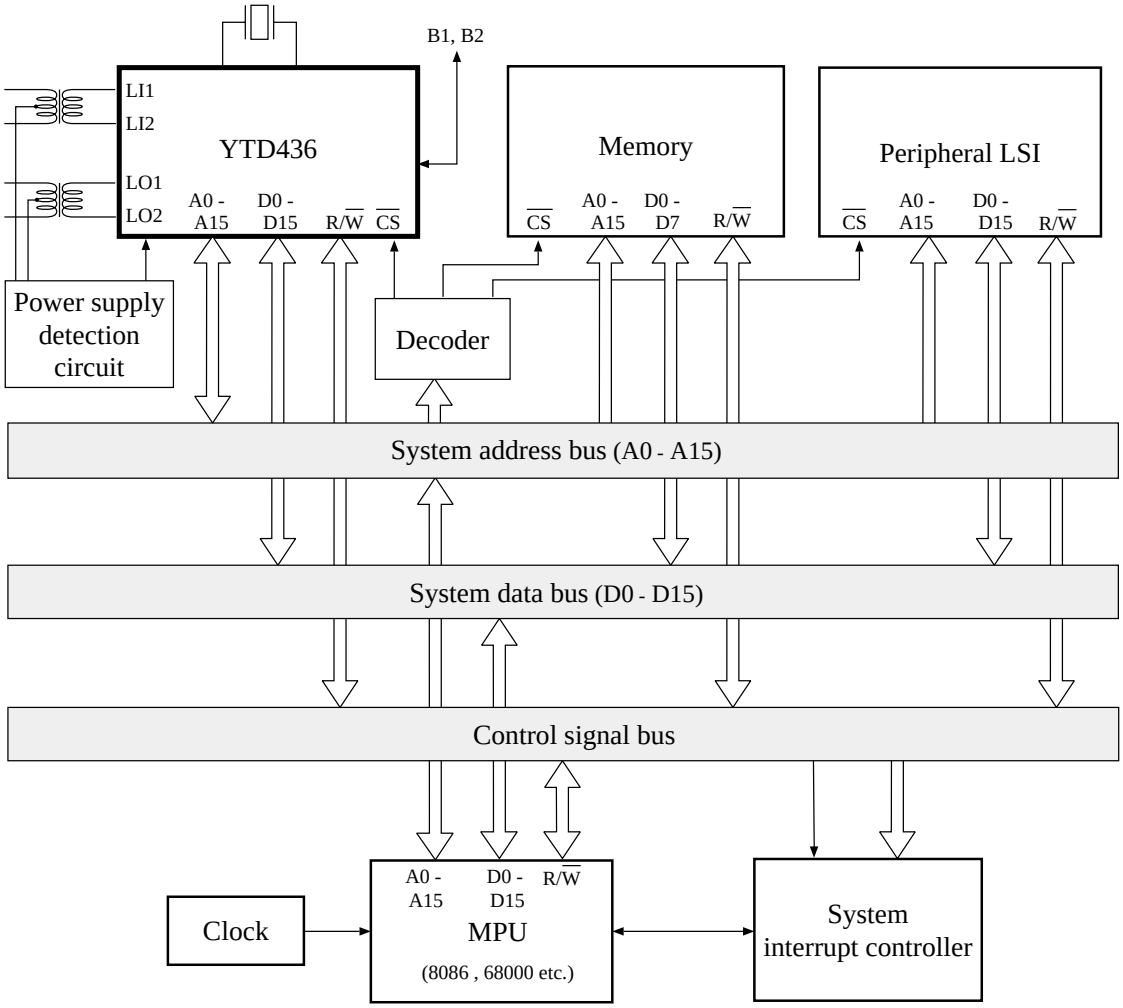
User Network Interface Block Diagram

YTD436 is the most-suited LSI for terminal equipment such as ISDN telephones and video telephones and for PHS base stations.

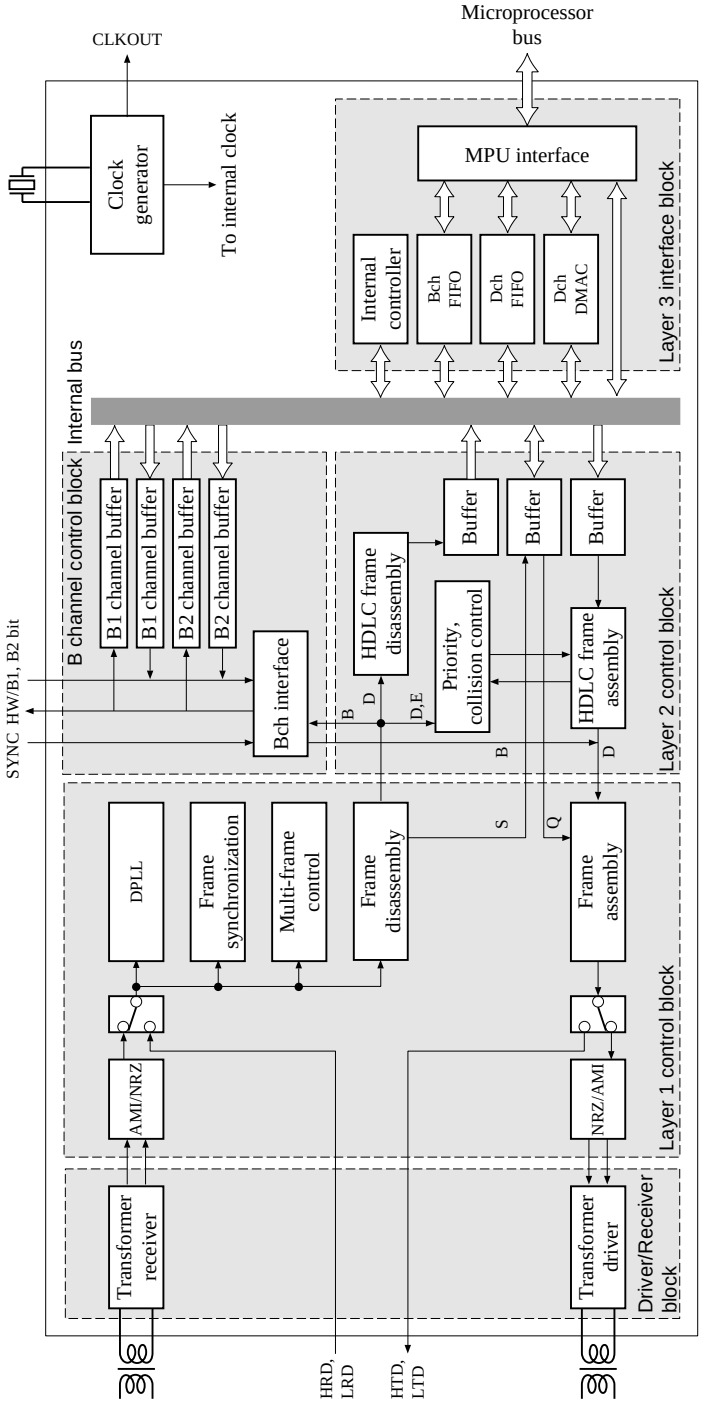
YTD436 contains layer 1 and layer 2 functions, analog driver/receiver for the S/T reference point, DMA request function for B channel data transfer, and DMA controller for D channel data transfer. Because of this, terminal equipment can be optimally configured by adding few circuits such as the layer 3 control processor.



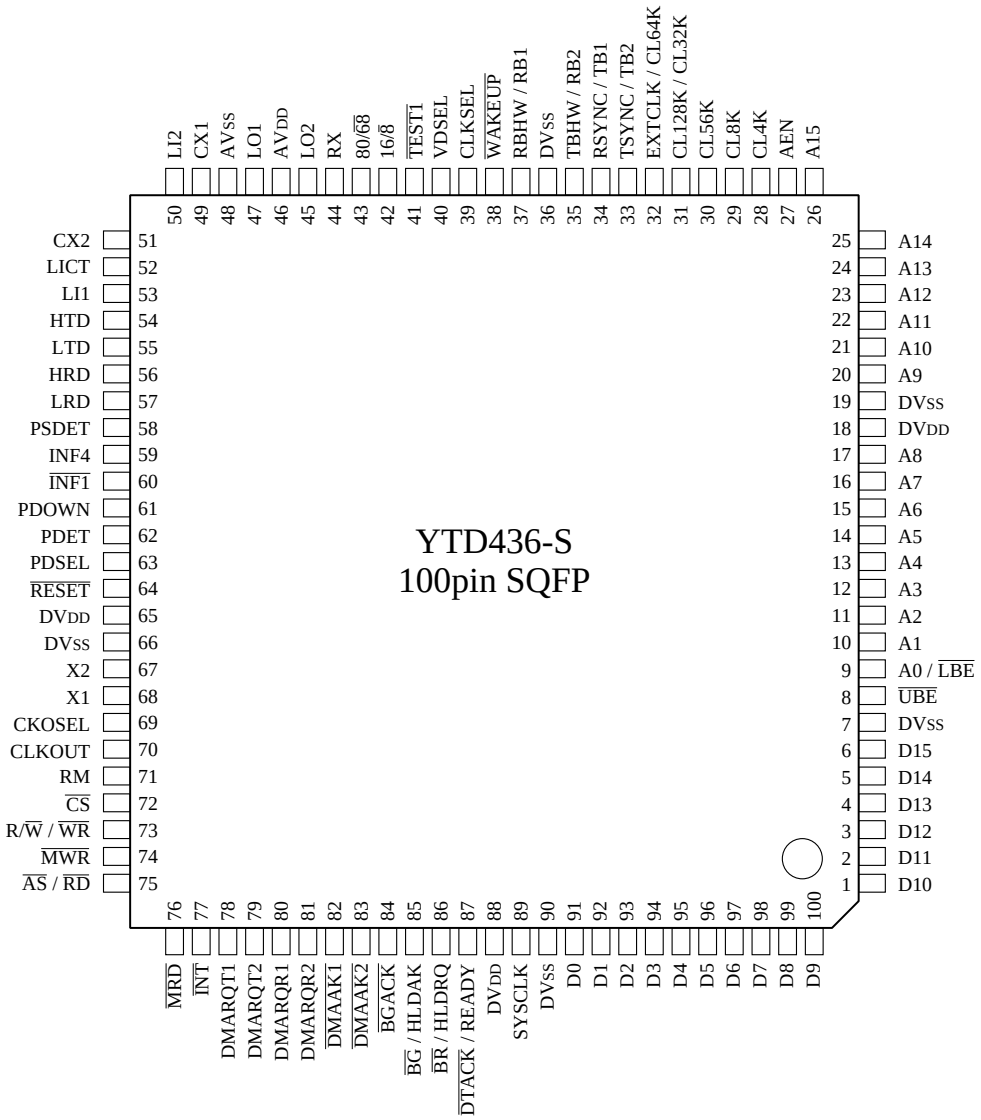
YTD436 Peripheral LSI Interface Block Diagram



YTD436 Internal Block Diagram



Pin Assignments



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{DD}	- 0.3	+ 7.0	V
Input Voltage	DV_I	- 0.3	DV_{DD} + 0.3	V
	AV_I	- 0.3	AV_{DD} + 0.3	V
Storage Temperature	T_{stg}	- 50	+ 125	ºC

(Based on DV_{SS} = AV_{SS} = 0.0 V)

Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Max.	Unit
Supply Voltage	DV_{DD}	VDSEL="H"	4.75	5.25	V
		VDSEL="L"	3.0	3.6	V
	AV_{DD}		4.75	5.25	V
Operating Temperature	T_{op}		- 30	85	ºC

(Based on DV_{SS}= AV_{SS} = 0.0 V)

DC Characteristics

When DVDD = 5 V ± 5 %, AVDD = 5 V ± 5 % (VDSEL="H", Top = - 30 to + 85 ºC)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
High-Level Input Voltage (CMOS)	V_{DIH}	(**Note 1**)	0.8DV_{DD}			V
Low-Level Input Voltage (CMOS)	V_{DIL}	(**Note 1**)			0.2DV_{DD}	V
High-Level Input Voltage (TTL)	V_{DIH}	(**Note 2**)	2.2			V
Low-Level Input Voltage (TTL)	V_{DIL}	(**Note 2**)			0.8	V
High-Level Output Voltage (CMOS)	V_{DOH}	$\|I_{DOH}\| < 10$ µA	DV_{DD} - 0.4			V
Low-Level Output Voltage (CMOS)	V_{DOL}	$\|I_{DOL}\| < 10$ µA			DV_{SS} + 0.4	V
High-Level Output Voltage (TTL)	V_{DOH}	(**Note 3**)	2.7			V
Low-Level Output Voltage (TTL)	V_{DOL}	(**Note 3**)			0.4	V
Low-Level Output Voltage (Open-D)	V_{DOL}	(**Note 4**)			0.4	V
Leakage Current	I_L		-10		10	µA
Off-State Leakage Current	I_{LZ}	(**Note 5**)	-10		10	µA
Power Supply Current (Digital block)	DI_{DD}	(**Note 6**)		10.2		mA
		(**Note 7**, **9**)		0.1		mA
Power Supply Current (Analog block)	AI_{DD}	(**Note 6**, **10**)		4.8		mA
		(**Note 7**, **10**)		0.4		mA
		(**Note 8**, **10**)		0.1		mA

Note 1: With respect to X1, PSDET, PDET, PDSEL, $\overline{\text{WAKEUP}}$, $\overline{\text{RESET}}$, CLKSEL, $\overline{\text{TEST1}}$, VDSEL pins (except for the analog pins).

Note 2: With respect to other pins (except for the analog pins).

Note 3: CLKOUT pin Test condition: I_{DOH} = - 1.0 mA, I_{DOL} = 2.0 mA

other output pins Test condition: I_{DOH} = - 0.4 mA, I_{DOL} = 1.2 mA

Note 4: HTD, LTD, $\overline{\text{INT}}$ pin Test condition : I_{DOL} = 1.2 mA

$\overline{\text{INF1}}$ pin Test condition : I_{DOL} = 3 mA

RBHW pin Test condition : R_L = 500 Ω

Note 5: With respect to cases in which D0 - D15, and A0 - A15 pins are in the input state and $\overline{\text{MWR}}$ and $\overline{\text{MRD}}$ pins are in Hi-Z state.

Note 6: RUN state (connecting with a B channel, transferring all "0", SYSCLK = 8 MHz, using internal driver/receiver, assuming as V_{DIH} = DV_{DD}, V_{DIL} = DV_{SS})

Note 7: SLEEP state

Note 8: SLEEP state + Line interface disconnection

Note 9: When SYSCLK is stopped.

Note 10: When using internal driver/receiver

When DVDD = 3.3 V ± 0.3 V, AVDD = 5 V ± 5 % (VDSEL="L", Top = - 30 to + 85 ºC)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
High-Level Input Voltage	V_{DIH}		0.8DV_{DD}			V
Low-Level Input Voltage	V_{DIL}				0.2DV_{DD}	V
High-Level Output Voltage	V_{DOH}	$\|I_{DOH}\|$ < 0.4 mA	DV_{DD} - 0.4			V
Low-Level Output Voltage	V_{DOL}	$\|I_{DOL}\|$ < 1.2 mA			DV_{SS} + 0.4	V
Low-Level Output Voltage (Open-D)	V_{DOL}	(**Note 1**)			0.4	V
Leakage Current	I_L		-10		10	µA
Off-State Leakage Current	I_{LZ}	(**Note 2**)	-10		10	µA
Power Supply Current (Digital block)	DI_{DD}	(**Note 3**)		4.9		mA
		(**Note 4**, **6**)		0.1		mA
Power Supply Current (Analog block)	AI_{DD}	(**Note 3**, **7**)		4.8		mA
		(**Note 4**, **7**)		0.4		mA
		(**Note 5**, **7**)		0.1		mA

Note 1: HTD, LTD, $\overline{INT}$, $\overline{INF1}$ pin Test condition : I_{DOL} = 1.2 mA

RBHW pin Test condition : R_L = 500 Ω

Note 2: With respect to cases in which D0 - D15, and A0 - A15 pins are in the input state and $\overline{MWR}$ and $\overline{MRD}$ pins are in Hi-Z state.

Note 3: RUN state (connecting with a B channel, transferring all "0", SYSCLK = 8 MHz, using internal driver/receiver, assuming as V_{DIH} = DV_{DD}, V_{DIL} = DV_{SS})

Note 4: SLEEP state

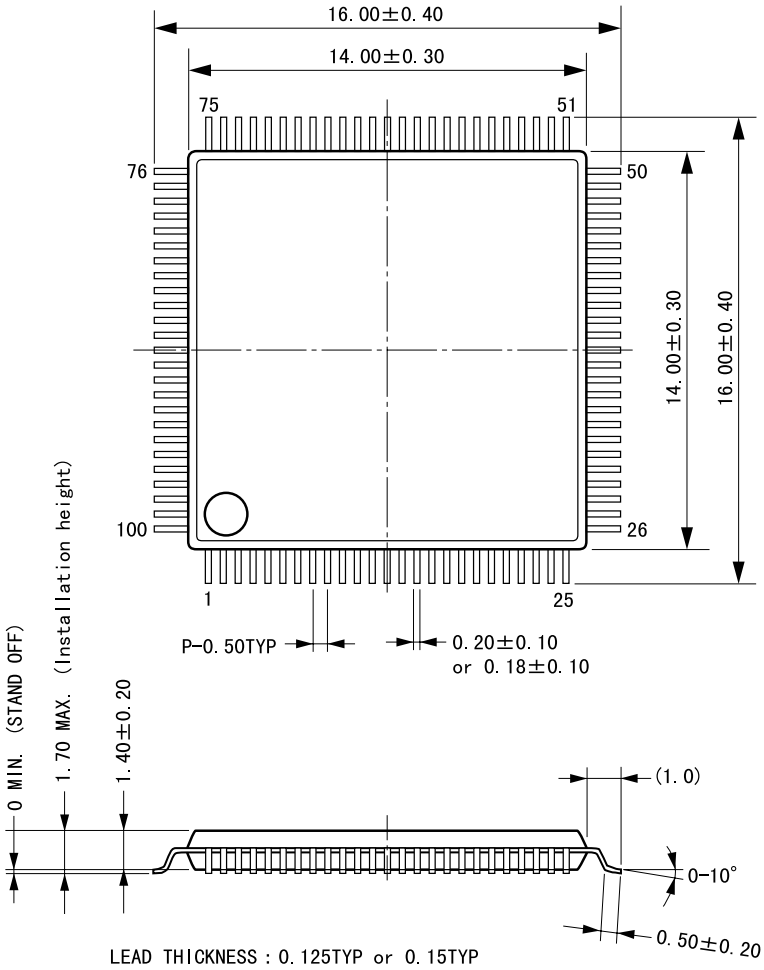
Note 5: SLEEP state + Line interface disconnection

Note 6: When SYSCLK is stopped.

Note 7: When using internal driver/receiver

PACKAGE OUTLINE

C-PK100SP-1



(UNIT) : mm (millimeters)

The shape of the molded corner may slightly different from the shape in this diagram.

The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

IMPORTANT NOTICE

1. YAMAHA RESERVES THE RIGHT TO MAKE CHANGES TO ITS PRODUCTS AND TO THIS DOCUMENT WITHOUT NOTICE. THE INFORMATION CONTAINED IN THIS DOCUMENT HAS BEEN CAREFULLY CHECKED AND IS BELIEVED. HOWEVER, YAMAHA SHALL ASSUME NO RESPONSIBILITIES FOR INACCURACIES AND MAKE NO COMMITMENT TO UPDATE OR TO KEEP CURRENT THE INFORMATION CONTAINED IN THIS DOCUMENT.

2. THESE YAMAHA PRODUCTS ARE DESIGNED ONLY FOR COMMERCIAL AND NORMAL INDUSTRIAL APPLICATIONS, AND ARE NOT SUITABLE FOR OTHER USES, SUCH AS MEDICAL LIFE SUPPORT EQUIPMENT, NUCLEAR FACILITIES, CRITICAL CARE EQUIPMENT OR ANY OTHER APPLICATION THE FAILURE OF WHICH COULD LEAD TO DEATH, PERSONAL INJURY OR ENVIRONMENTAL OR PROPERTY DAMAGE. USE OF THE PRODUCTS IN ANY SUCH APPLICATION IS AT THE CUSTOMER'S OWN RISK AND EXPENSE.

3. YAMAHA SHALL ASSUME NO LIABILITY FOR INCIDENTAL, CONSEQUENTIAL OR SPECIAL DAMAGES OR INJURY THAT MAY RESULT FROM MISAPPLICATION OR IMPROPER USE OR OPERATION OF THE PRODUCT.

4. YAMAHA MAKES NO WARRANTY OR REPRESENTATION THAT THE PRODUCTS ARE SUBJECT TO INTELLECTUAL PROPERTY LICENSE FROM YAMAHA OR ANY THIRD PARTY, AND YAMAHA MAKES NO WARRANTY OR REPRESENTATION OF NON-INFRINGEMENT WITH RESPECT TO THE PRODUCTS. YAMAHA SPECIFICALLY EXCLUDES ANY LIABILITY TO THE CUSTOMER OR ANY THIRD PARTY ARISING FROM OR RELATED TO THE PRODUCTS INFRINGEMENT OF ANY THIRD PARTY'S INTELLECTUAL PROPERTY RIGHTS, INCLUDING THE PATENT, COPYRIGHT, TRADEMARK OR TRADE SECRET RIGHTS OF ANY THIRD PARTY.

5. EXAMPLES OF USE DESCRIBED HEREIN ARE MERELY TO INDICATE THE CHARACTERISTICS AND PERFORMANCE OF PRODUCTS. YAMAHA SHALL ASSUME NO RESPONSIBILITY FOR ANY INTELLECTUAL PROPERTY CLAIMES OR OTHER PROBLEMS THAT MAY RESULT FROM APPLICATIONS BASED ON THE EXAMPLES DESCRIBED HEREIN. YAMAHA MAKES NO WARRANTY WITH RESPECT TO THE PRODUCTS, EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR USE AND TITLE.

6. YAMAHA MAKES EVERY EFFORT TO IMPROVE THE QUALITY AND RELIABILITY OF ITS PRODUCTS. HOWEVER, ALL SEMICONDUCTOR PRODUCTS FAIL WITH SOME PROBABILITY. THEREFORE, YAMAHA REQUIRES THAT SUFFICIENT CARE BE GIVEN TO ENSURING SAFE DESIGN IN CUSTOMER PRODUCTS SUCH AS REDUNDANT DESIGN, ANTI-CONFLAGRATION DESIGN, AND DESIGN FOR PREVENTING MALFUNCTION IN ORDER TO PREVENT ACCIDENTS RESULTING IN INJURY OR DEATH, FIRE OR OTHER SOCIAL DAMAGE FROM OCCURRING AS A RESULT OF PRODUCT FAILURE.

7. INFORMATION DESCRIBED IN THIS DOCUMENT: APPLICATION CIRCUITS AND ITS CONSTANTS AND CALCULATION FORMULAS, PROGRAMS AND CONTROL PROCEDURES ARE PROVIDED FOR THE PURPOSE OF EXPLAINING TYPICAL OPERATION AND USAGE. THEREFORE, PLEASE EVALUATE THE DESIGN SUFFICIENTLY AS WHOLE SYSTEM UNDER THE CONSIDERATION OF VARIOUS EXTERNAL OR ENVIRONMENTAL CONDITIONS AND DETERMINE THEIR APPLICATION AT THE CUSTOMER'S OWN RISK. YAMAHA SHALL ASSUME NO RESPONSIBILITY FOR CLAIMS, DAMAGES, COSTS AND EXPENSES CAUSED BY THE CUSTOMER OR ANY THIRD PARTY, OWING TO THE USE OF THE ABOVE INFORMATION.

Notice The specifications of this product are subject to improvement changes without prior notice.

AGENT

YAMAHA CORPORATION

Address inquiries to:
Semiconductor Sales & Marketing Department

■ Head Office 203, Matsunokijima, Toyooka-mura
Iwata-gun, Shizuoka-ken, 438-0192, Japan
Tel. +81-539-62-4918 Fax. +81-539-62-5054

■ Tokyo Office 2-17-11, Takanawa, Minato-ku,
Tokyo, 108-8568, Japan
Tel. +81-3-5488-5431 Fax. +81-3-5488-5088

■ Osaka Office 3-12-12, Minami Senba, Chuo-ku,
Osaka City, Osaka, 542-0081, Japan
Tel. +81-6-6252-6221 Fax. +81-6-6252-6229

Printed in Japan