HD61104,HD61104A

(Dot Matrix Liquid Crystal Graphic Display Column Driver)

T-52-13-07

Description

HD61104, HD61104A is a column (segment) driver for large-area dot matrix liquid crystal graphic display systems.

Features

- Display duty cycle: 1/64–1/200
- Internal liquid crystal display driver: 80 drivers
- 4-bit bus, bidirectional shift data transfer
- Cascade connection with enable format
- Data transfer rate: 3.5 MHz
- Power supply for logic circuit: 5 V ±10%
- Power supply for LCD drive circuits :
  10 to 26 V (HD61104)
  10 to 28 V (HD61104A)
- Standby function
- CMOS process
- 100-pin flat plastic package

Ordering Information

Type No.	LCD Driving Level (V)	Package
HD61104	+10 to +26	100 pin plastic QFP (FP-100)
HD61104A	+10 to +28V	
HD61104TF	+10 to +28V	100 pin plastic T-QFP (TFP-100)

Absolute Maximum Ratings

Item		Symbol	Value	Unit	Note
Supply voltage (1)		V_{CC}	–0.3 to +7.0	V	2
Supply voltage (2)	HD61104	V_{EE}	V_{CC} – 28.0 to V_{CC} + 0.3	V	
	HD61104A	V_{EE}	V_{CC} – 28.5 to V_{CC} + 0.3		
Terminal voltage (1)		V_{T1}	–0.3 to V_{CC} + 0.3	V	2, 3
Terminal voltage (2)		V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	4
Operating temperature		T_{opr}	–20 to +75	°C	
Storage temperature		T_{stg}	–55 to +125	°C	

Notes: 1. LSIs may be permanently destroyed if used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the limits of electrical characteristics, because using them beyond these conditions may cause malfunction and poor reliability.
2. All voltage values are referenced to GND = 0 V.
3. Applies to input terminals, SHL, CL1, CL2, D_0–D_3, $\overline{E}$, and M.
4. Applies to V_1, V_2, V_3, and V_4. Must maintain
$V_{CC} \geq V_1 \geq V_3 \geq V_4 \geq V_2 \geq V_{EE}$
Connect a protection resister of 15 Ω ± 10% to each terminal in series.

Pin Arrangement

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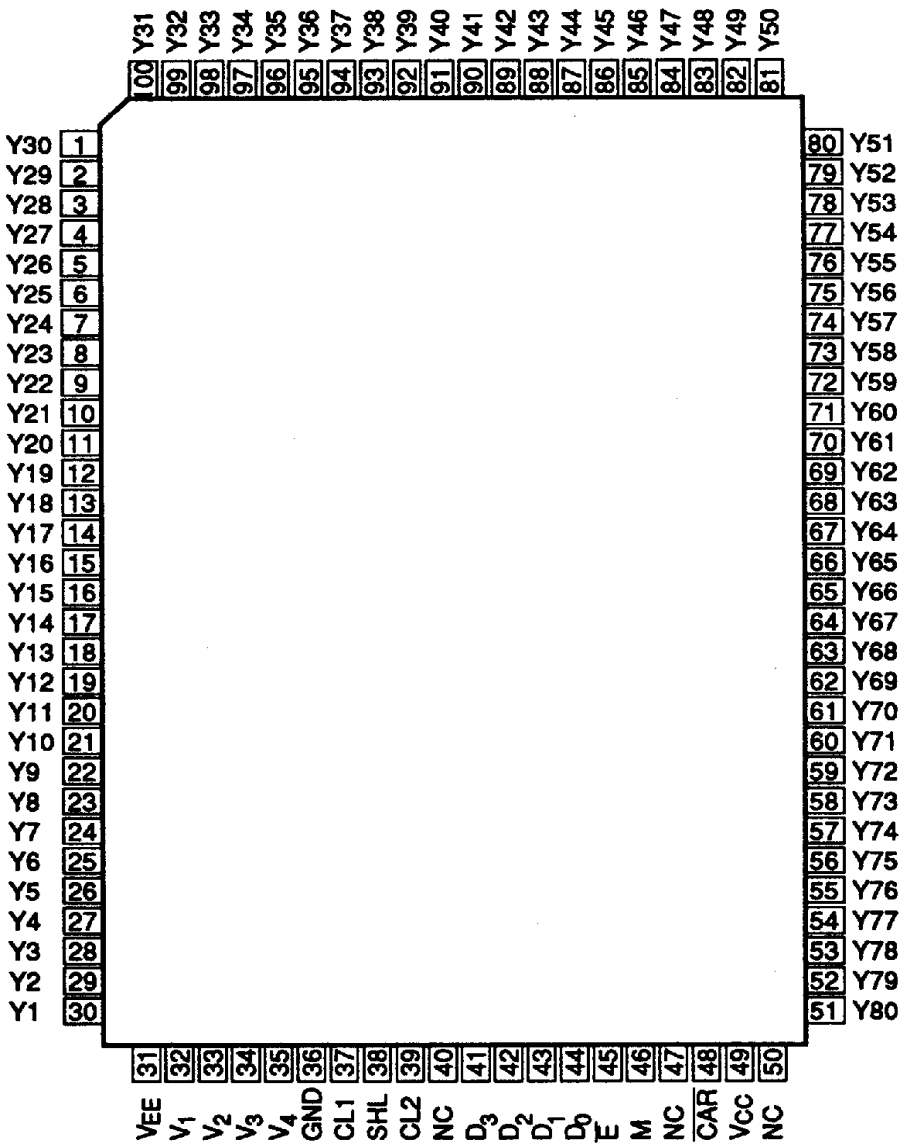

(Top View)

(FP–100/TFP–100)

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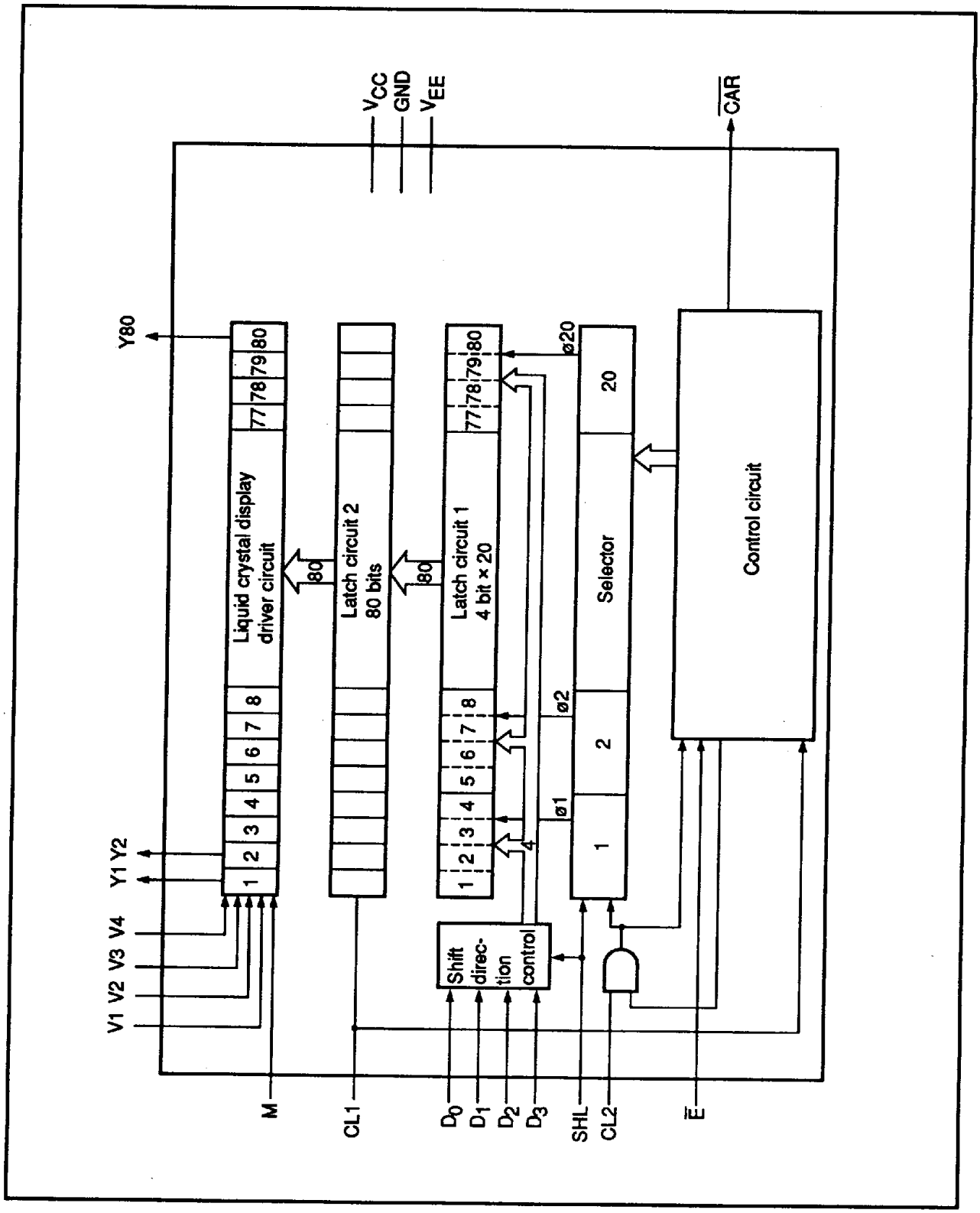
Block Diagram



Electrical Characteristics

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DC Characteristics

(V_{CC} = 5 V ± 10%, GND = 0 V, V_{CC} – V_{EE} = 10 to 26 V (HD61104), V_{CC} – V_{EE} = 10 to 28 V (HD61104A), Ta = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	0.7 × V_{CC}		V_{CC}	V		1
Input low voltage	V_{IL}	0		0.3 × V_{CC}	V		1
Output high voltage	V_{OH}	V_{CC} – 0.4			V	I_{OH} = – 400 µA	2
Output low voltage	V_{OL}			0.4	V	I_{OL} = 400 µA	2
Driver on resistance	R_{ON}			7.5	kΩ	V_{EE} = –1 0V,Load current =100 µA	5
Input leakage current	I_{IL1}	–1		1	µA	V_{IN} = 0 to V_{CC}	1
Input leakage current	I_{IL2}	–25		25	µA	V_{IN} = V_{EE} to V_{CC}	3
Dissipation current (1)	I_{GND}			2.0	mA		4
Dissipation current (2)	I_{EE}			0.2	mA	HD61104	4
				0.4		HD61104A	
Dissipation current (3)	I_{ST}			100	µA		4 5

Notes:
1. Applies to CL1, CL2, SHL, E, M, and D_0-D_3.
2. Applies to $\overline{CAR}$.
3. Applies to V_1, V_2, V_3, and V_4.
4. Specified when display data is transferred under following conditions:
   - CL2 frequency fcp2 = 2.5 MHz (data transfer rate)
   - CL1 frequency fcp1 = 14.0 kHz (data latch frequency)
   - M frequency f_M = 35 Hz (frame frequency/2)
   - Display duty ratio 1/200

   Specified when V_{IH} = V_{CC}, V_{IL} = GND and no load on outputs.
   - I_{GND}: currents between V_{CC} and GND
   - I_{EE}: currents between V_{CC} and V_{EE}
5. Currents between V_{CC} and GND at standby ($\overline{E}$ input = high).
6. Resistance between terminal Y (one of Y1 to Y80) and terminal V (one of V_1, V_2, V_3, and V_4) when load current flows through one of the terminals Y1 to Y80. This value is specified under the following conditions:

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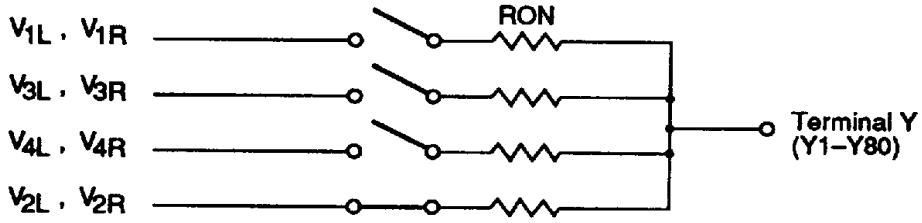
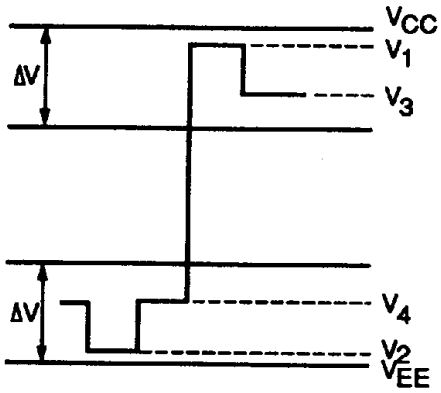
$V_{CC} - V_{EE} = 26$ V

$V_1, V_3 = V_{CC} - 2/10\ (V_{CC} - V_{EE})$

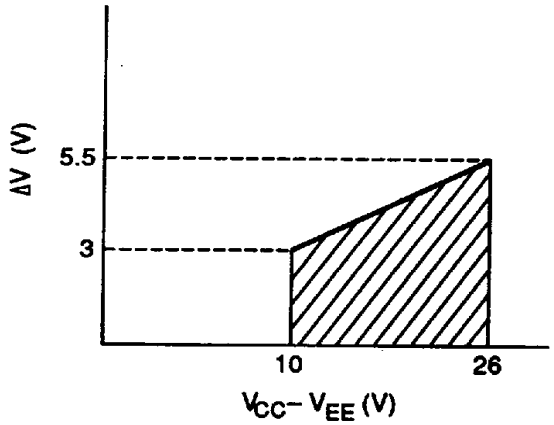
$V_2, V_4 = V_{EE} + 2/10\ (V_{CC} - V_{EE})$



The following is a description of the range of power supply voltage for liquid crystal display drives. Apply positive voltage to V_1 and V_3, and negative voltage to V_2 and V_4, within the ΔV range. This range allows stable impedance on driver output (R_{ON}). Notice that ΔV depends on power supply voltage $V_{CC} - V_{EE}$.



Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive



Correlation between Power Supply Voltage $V_{CC} - V_{EE}$ and ΔV

Terminal Configuration

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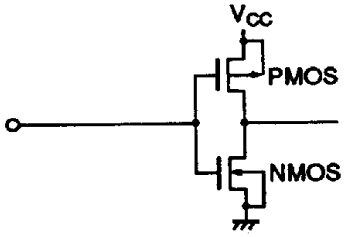
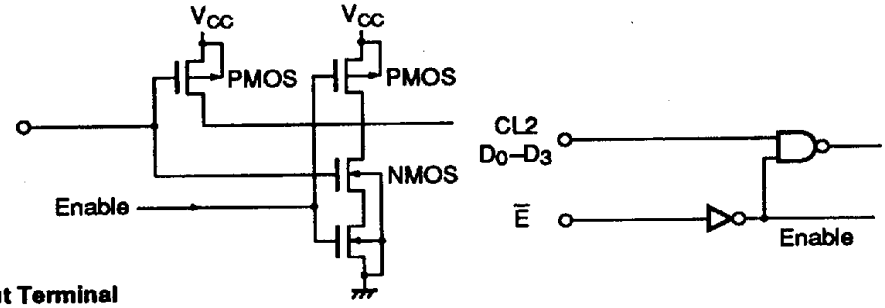
Input Terminal

Applicable Terminals : CL1, SHL, $\overline{E}$, M



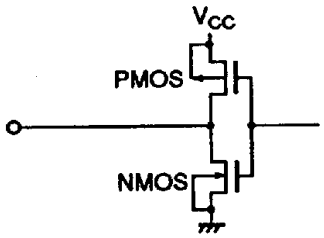
Input Terminal (controlled by Enable signal)

Applicable Terminals : CL2, D_0–D_3



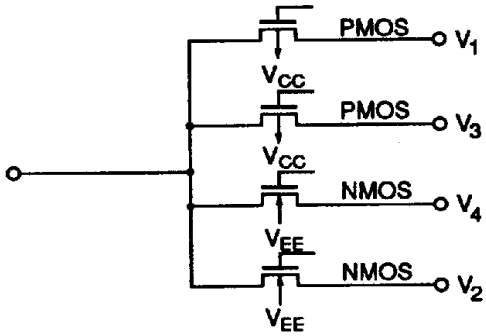
Output Terminal

Applicable Terminal : $\overline{CAR}$



Output Terminal

Applicable Terminals : Y1–Y80



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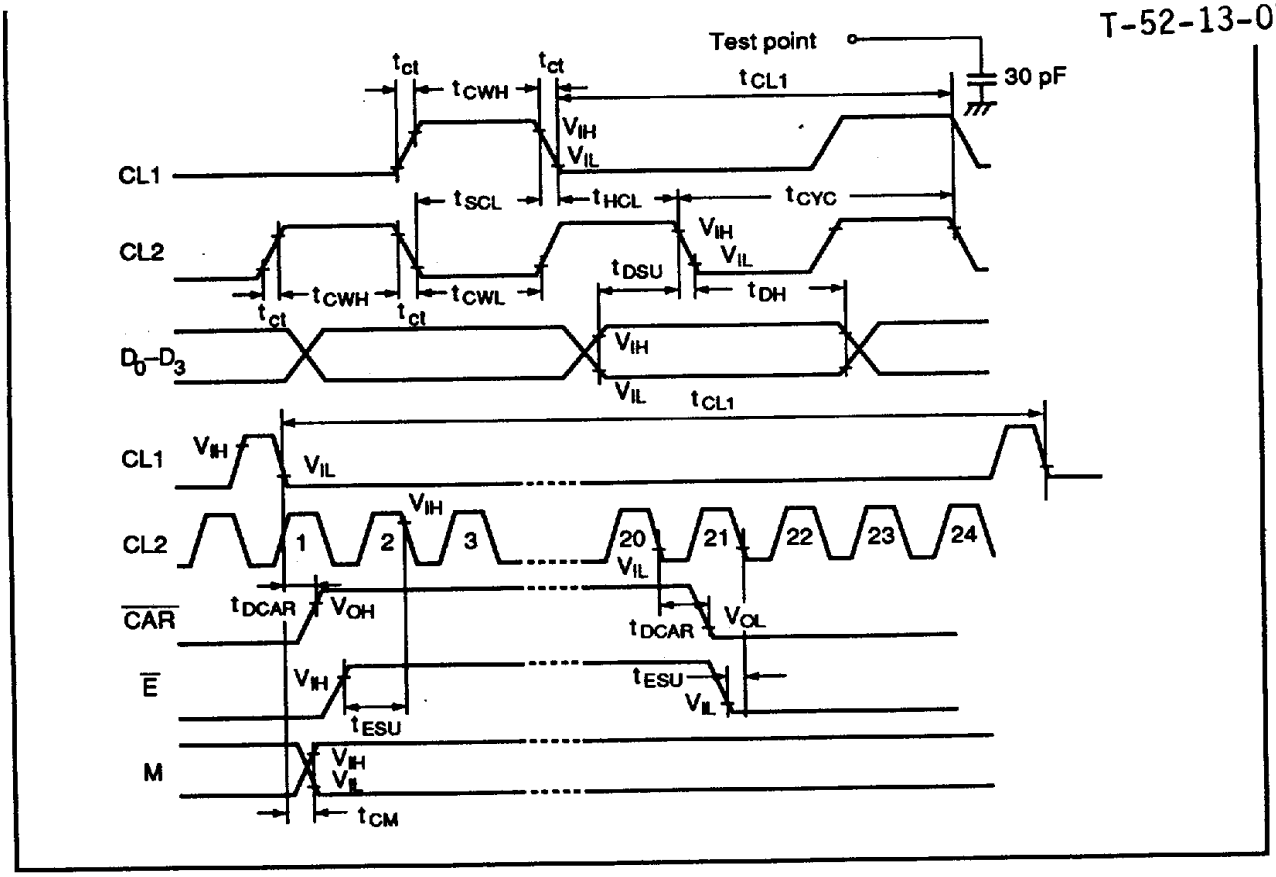
AC Characteristics
(V_{CC} = 5 V ± 10%, GND = 0 V, Ta = -20 to ±75°C)

Item	Symbol	Min	Typ	Max	Unit	Note
Clock cycle time	t_{CYC}	285	—	—	ns	
Clock high level width	t_{CWH}	110	—	—	ns	
Clock low level width	t_{CWL}	110	—	—	ns	
Clock setup time	t_{SCL}	80	—	—	ns	
Clock hold time	t_{HCL}	80	—	—	ns	
Clock rise/fall time	t_{CT}	—	—	30	ns	
Data setup time	t_{DSU}	80	—	—	ns	
Data hold time	t_{DH}	80	—	—	ns	
E setup time	t_{ESU}	75	—	—	ns	
Output delay time	t_{DCAR}	—	—	180	ns	1
M phase difference time	t_{CM}	—	—	300	ns	
CL1 cycle time	t_{CL1}	$t_{CYC} \times 10$	—	—	ns	

Note: 1. The following load circuit is connected for specification:



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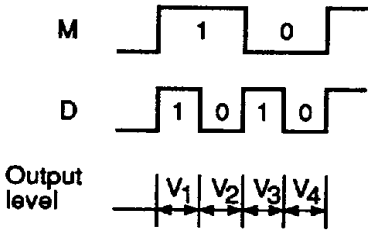
Terminal Name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND V_{EE}	1 1 1		Power supply	V_{CC} – GND: Power supply for internal logic V_{CC} – V_{EE}: Power supply for LCD drive circuit
V_1 V_2 V_3 V_4	4		Power supply	Power supply for liquid crystal drive. V_1, V_2: selection level V_3, V_4: non-selection level
Y1–Y80	80	O	LCD	Liquid crystal driver outputs. Selects one of the 4 levels, V_1, V_2, V_3, and V_4. Relation among output level, M, and display data (D) is as follows: 
M	1	I	Controller	Switch signal to convert liquid crystal drive waveform into AC.
CL1	1	I	Controller	Latch clock of display data (falling edge triggered). Synchronized with the fall of CL1, liquid crystal driver signals corresponding to the display data are output.
CL2	1	I	Controller	Shift clock of display data (D). Falling edge triggered.
D_0–D_3	4	I	Controller	Input of 4-bit display data (D)

D	Liquid Crystal Driver Output	Liquid Crystal Display
1 (High level)	Selection level	On
0 (Low level)	Non-selection level	Off

Truth table (Positive logic)

SHL	Input data and latch circuit 1
0	$D_3 \rightarrow 1 \rightarrow 5 \rightarrow 9 \cdots \rightarrow 73 \rightarrow 77$
	$D_2 \rightarrow 2 \rightarrow 6 \rightarrow 10 \cdots \rightarrow 74 \rightarrow 78$
	$D_1 \rightarrow 3 \rightarrow 7 \rightarrow 11 \cdots \rightarrow 75 \rightarrow 79$
	$D_0 \rightarrow 4 \rightarrow 8 \rightarrow 12 \cdots \rightarrow 76 \rightarrow 80$

Terminal Name	Number of Terminals	I/O	Connected to	Functions
				Truth table (Positive logic) (cont) SHL: 1 — Input data and latch circuit 1 $D_3 \rightarrow 80 \rightarrow 76 \rightarrow 72 \cdots \rightarrow 8 \rightarrow 4$ $D_2 \rightarrow 79 \rightarrow 75 \rightarrow 71 \cdots \rightarrow 7 \rightarrow 3$ $D_1 \rightarrow 78 \rightarrow 74 \rightarrow 70 \cdots \rightarrow 6 \rightarrow 2$ $D_0 \rightarrow 77 \rightarrow 73 \rightarrow 69 \cdots \rightarrow 5 \rightarrow 1$ ex: When SHL = 0, the data that is input to D_3 is latched to each bit of the latch circuit 1 in order of $1 \rightarrow 5 \rightarrow 9 \cdots \rightarrow 77$.
SHL	1	I	V_{CC} or GND	Selects a shift direction of display data.
$\overline{E}$	1	I	GND or the terminal $\overline{CAR}$ of the HD61104	Enable input. The operation stops at high level, and is enabled at low level.
$\overline{CAR}$	1	O	Input terminal $\overline{E}$ of the HD61104	Enable output. Used for cascade connection.
NC	3			Unused. No wire should be connected.

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Typical Application

Figure 1 is an LCD panel with 200 × 640 dots on which characters are displayed with 1/200 duty cycle dynamic drive.

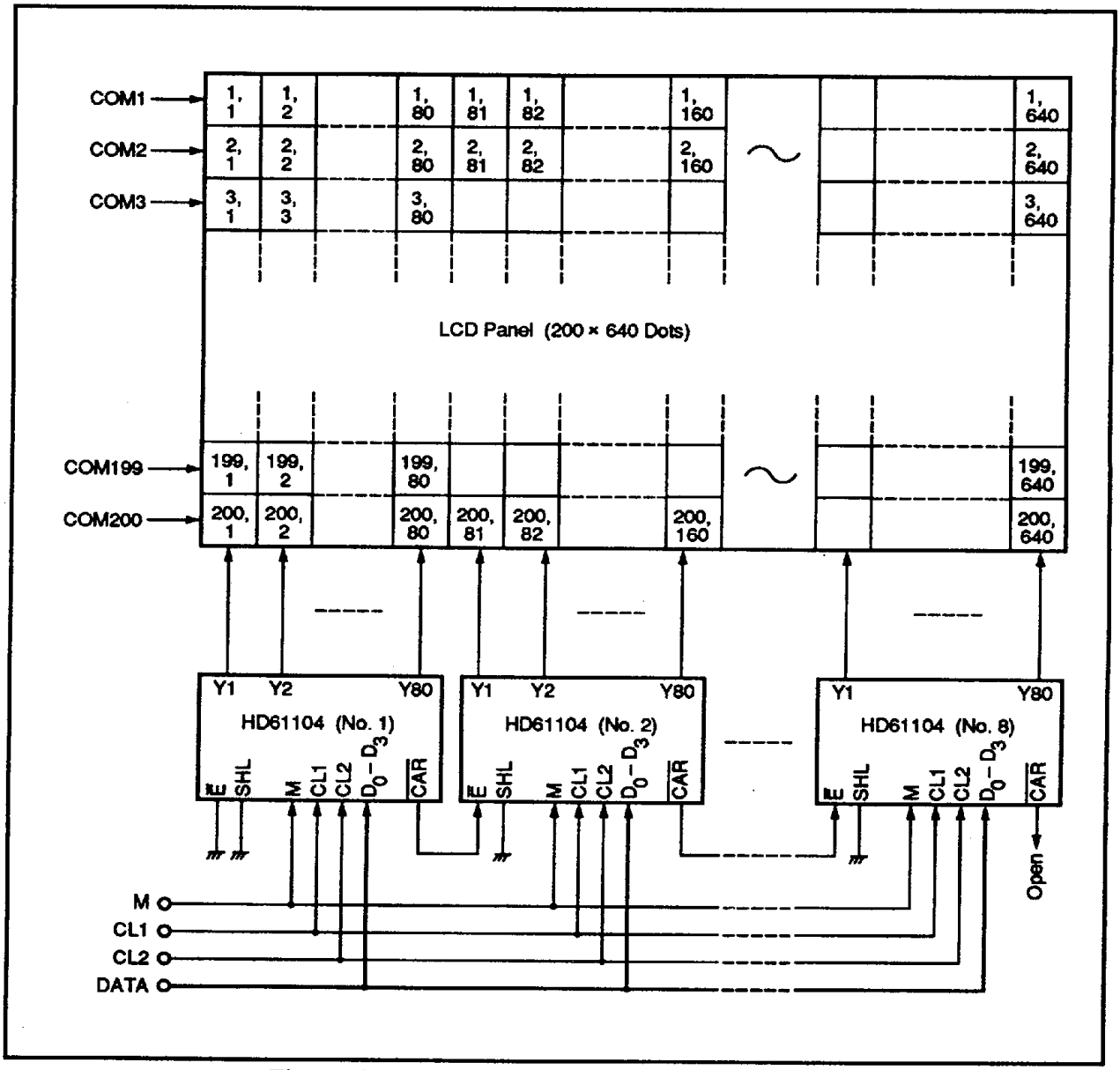

Figure 1 200 × 640 Dot LCD Panel Example

Cascade eight HD61104s. Input data to the D_0—D_3 terminals of Nos. 1–8. Connect $\overline{E}$ of No. 1 to GND. Connect no lines to $\overline{CAR}$ of No. 8 . Connect common signal terminals (COM1–COM200) to the common driver HD61105. (m,n) of LCD panel is the address corresponding to each dot. Figure 2 shows timing.

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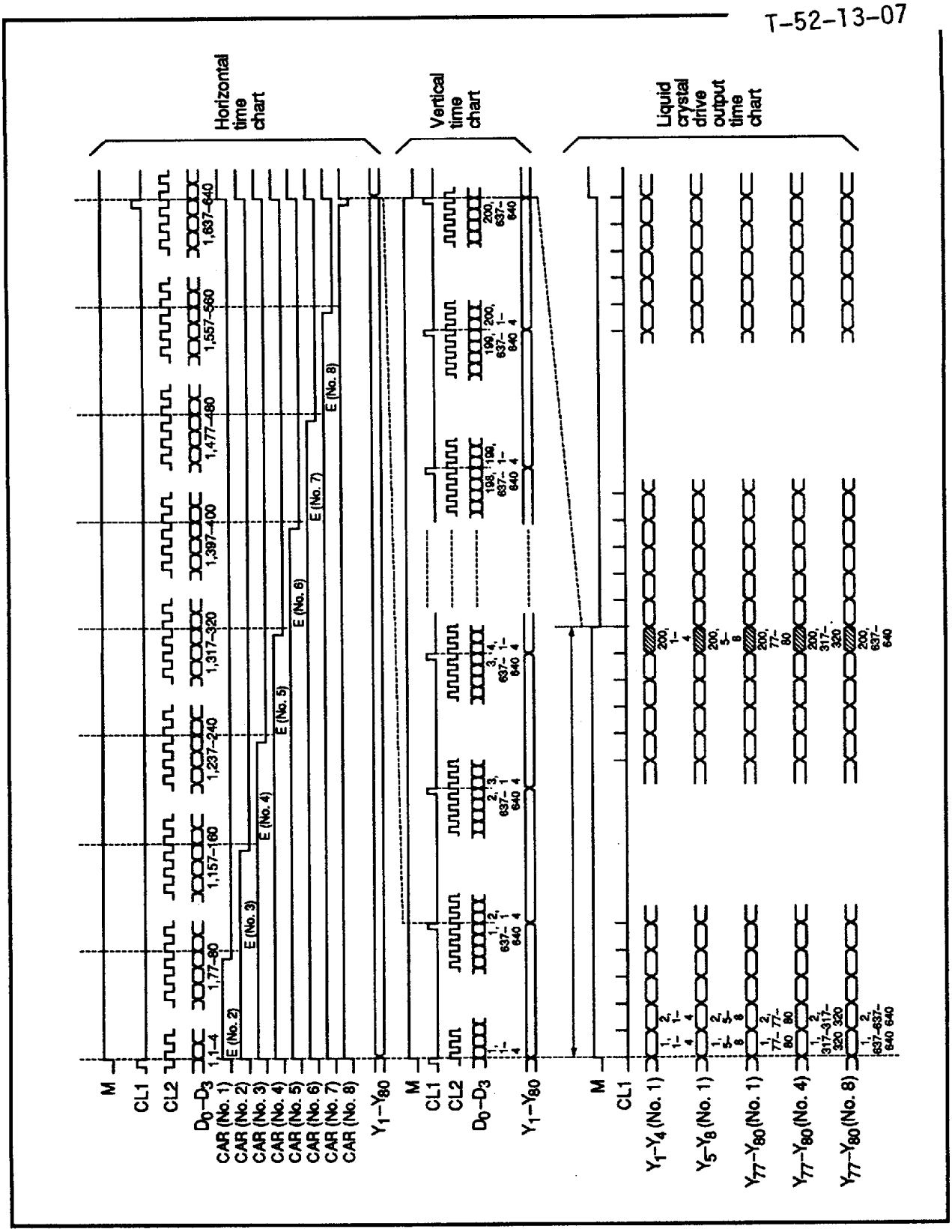

Figure 2 Waveform Example

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HD61105, HD61105A

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(Dot Matrix Liquid Crystal Graphic Display Common Driver)

Description

The HD61105, HD61105A is a common signal driver for dot matrix liquid crystal graphic display systems. It provides 80 driver output lines and the impedance is low enough to drive a large screen.

As the HD61105, HD61105A is produced in a CMOS process, it is fit for use in portable battery drive equipments utilizing the liquid crystal display's low power consumption.

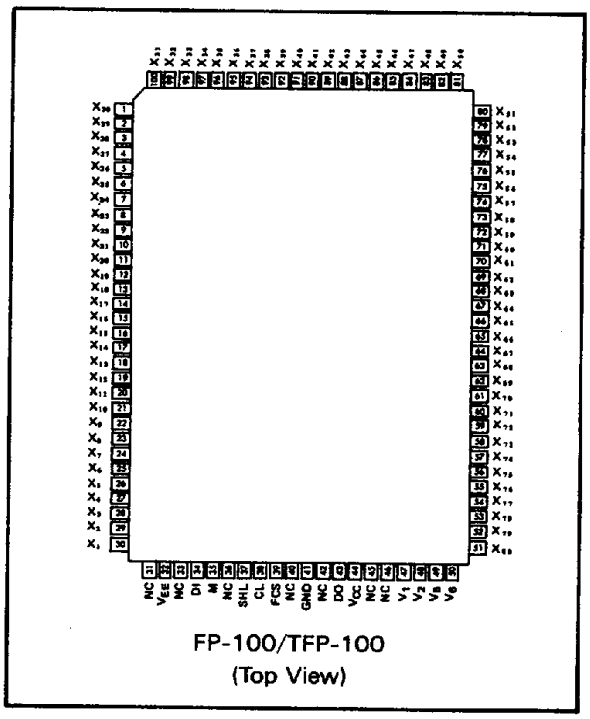
Features

- Dot matrix liquid crystal graphic display common driver with low impedance
- Internal liquid crystal display driver circuit: 80 circuits
- Display duty ratio factor: 1/64—1/200
- Internal 80-bit shift register
- Power supply for logic circuit: 5 ± 10%
- Power supply for LCD drive circuits:
  —10 to 26 V (HD61105)
  —10 to 28 V (HD61105A)
- CMOS process
- 100-pin plastic QFP (FP-100)

Ordering Information

Type No.	LCD Driving Level (V)	Package
HD61105	10 to 26	100 pin plastic QFP (FP-100)
HD61105A	10 to 28	
HD61105TF	10 to 28	100 pin plastic T-QFP (TFP-100)

Pin Arrangement



FP-100/TFP-100
(Top View)

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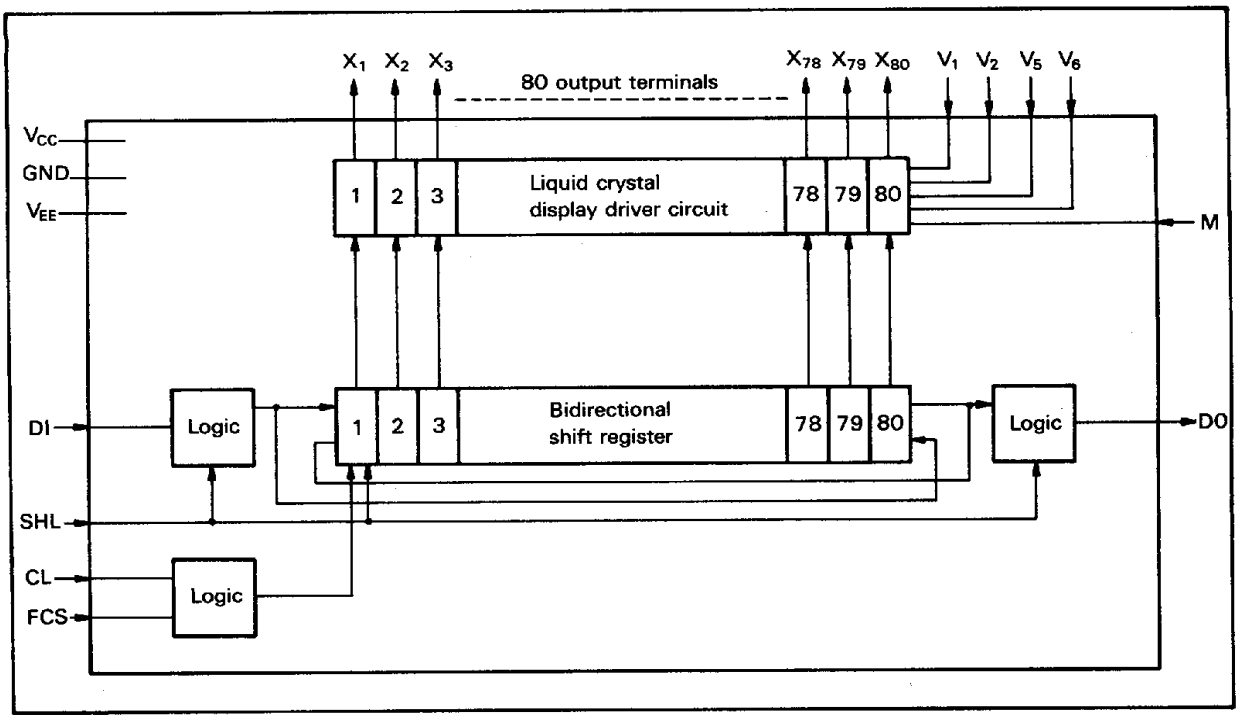
Block Diagram



Absolute maximum ratings

Item		Symbol	Value	Unit	Note
Supply voltage (1)		V_{CC}	− 0.3 to + 7.0	V	2
Supply voltage (2)	HD61105	V_{EE}	V_{CC} − 28.0 to V_{CC} + 0.3	V	5
	HD61105A		V_{CC} − 28.5 to V_{CC} + 0.3		
Terminal voltage (1)		V_{T1}	− 0.3 to V_{CC} +0.3	V	2, 3
Terminal voltage (2)		V_{T2}	V_{EE} − 0.3 to V_{CC} +0.3	V	4, 5
Operating temperature		Topr	− 20 to + 75	°C	
Storage temperature		Tstg	− 55 to + 125	°C	

Notes: 1. LSIs may be permanently destroyed if used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the limits of electrical characteristics, because using them beyond these conditions may cause malfunction and poor reliability.
2. All voltage values are referred to GND = 0 V.
3. Applies to input terminals except V_1, V_2, V_5, and V_6.
4. Applies to V_1, V_2, V_5, and V_6.
5. $V_{CC} \geqq V_1 \geqq V_6 \geqq V_5 \geqq V_2 \geqq V_{EE}$ must be maintained.

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Electrical Characteristics

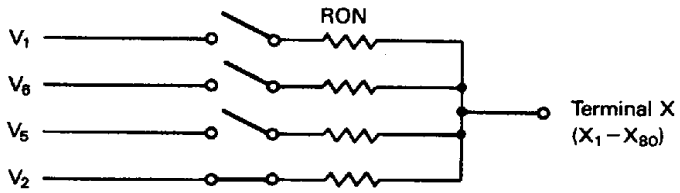
DC Characteristics

(V_{CC} = 5 V ± 10%, GND = 0 V, V_{CC} − V_{EE} = 10 to 26 V (HD61105), V_{CC} − V_{EE} = 10 to 28 V (HD61105A), T_a = − 20 to + 75°C)

		Specifications					
Test Item	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Condition**	**Note**
Input high voltage	V_{IH}	0.7 × V_{CC}	—	V_{CC}	V		1
Input low voltage	V_{IL}	GND	—	0.3 × V_{CC}	V		1
Output high voltage	V_{OH}	V_{CC} − 0.4	—	—	V	I_{OH} = − 0.4mA	2
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 0.4mA	2
Vi—Xj on resistance	R_{ON}	—	—	2.0	kΩ	V_{CC} − V_{EE} = 10 V Load current ± 150 μA	5
Input leakage current	I_{IL1}	− 1.0	—	1.0	μA	V_{IN} = 0 to V_{CC}	3
Input leakage current	I_{IL2}	− 25	—	25	μA	V_{IN} = V_{EE} to V_{CC}	4
Clock frequency	f_{CL}	—	—	100	kHz	Transfer clock CL	
Dissipation current (1)	I_{GG1}	—	—	200	μA	at 1/200 duty cycle operation	6
Dissipation current (2)	I_{EE}	—	—	100	μA	at 1/200 duty cycle operation	7

Notes:
1. Applies to input terminals FCS, SHL, DI, M, and CL.
2. Applies to output terminal of DO.
3. Applies to the terminals NC, and the input terminals FCS, SHL, DI, M, and CL.
4. Applies to V_1, V_2, V_5, and V_6. No wire should be connected to X_1—X_{80}.
5. Resistance value between terminal X (one of X_1 to X_{80}) and terminal V (one of V_1, V_2, V_5, and V_6) when load current is applied to one of terminals X_1 to X_{80}. This value is specified under the following conditions:

$V_{CC}-V_{EE}=26V$
V_1, $V_6=V_{CC}-1/10\ (V_{CC}-V_{EE})$
V_2, $V_5=V_{EE}+1/10\ (V_{CC}-V_{EE})$



The following is a description of the range of power supply voltage for liquid crystal display drives. Apply positive voltage to V_1 and V_6, and negative voltage to V_2 and V_5, within the △V range. This range allows stable impedance on driver output (R_{ON}). Notice that △V depends on power supply voltage V_{CC}—V_{EE}.

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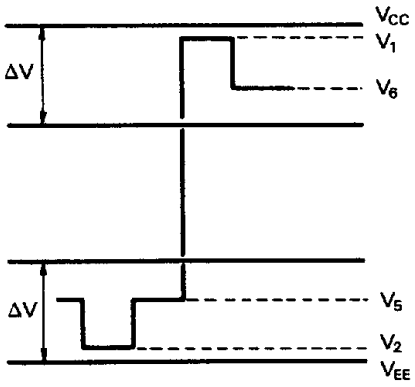
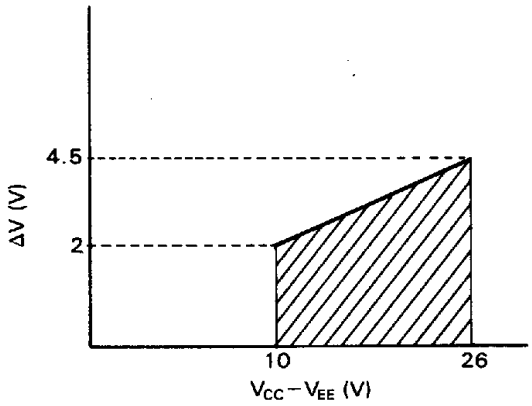


Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive



Correlation between Power Supply Voltage V_{CC}—V_{EE} and △V

6. The currents flowing through the GND terminal. Specified when display data is transferred under following conditions:
   CL frequency f_{CL} = 14kHz (data transfer rate)
   M frequency fM = 35 Hz (frame frequency/2) 1/200
   Display duty ratio
   $V_{IH} = V_{CC}$, V_{IL} = GND
   No load on outputs
7. The currents flowing through the V_{EE} terminal in the conditions of note 6. No line should be connected to the V terminal.

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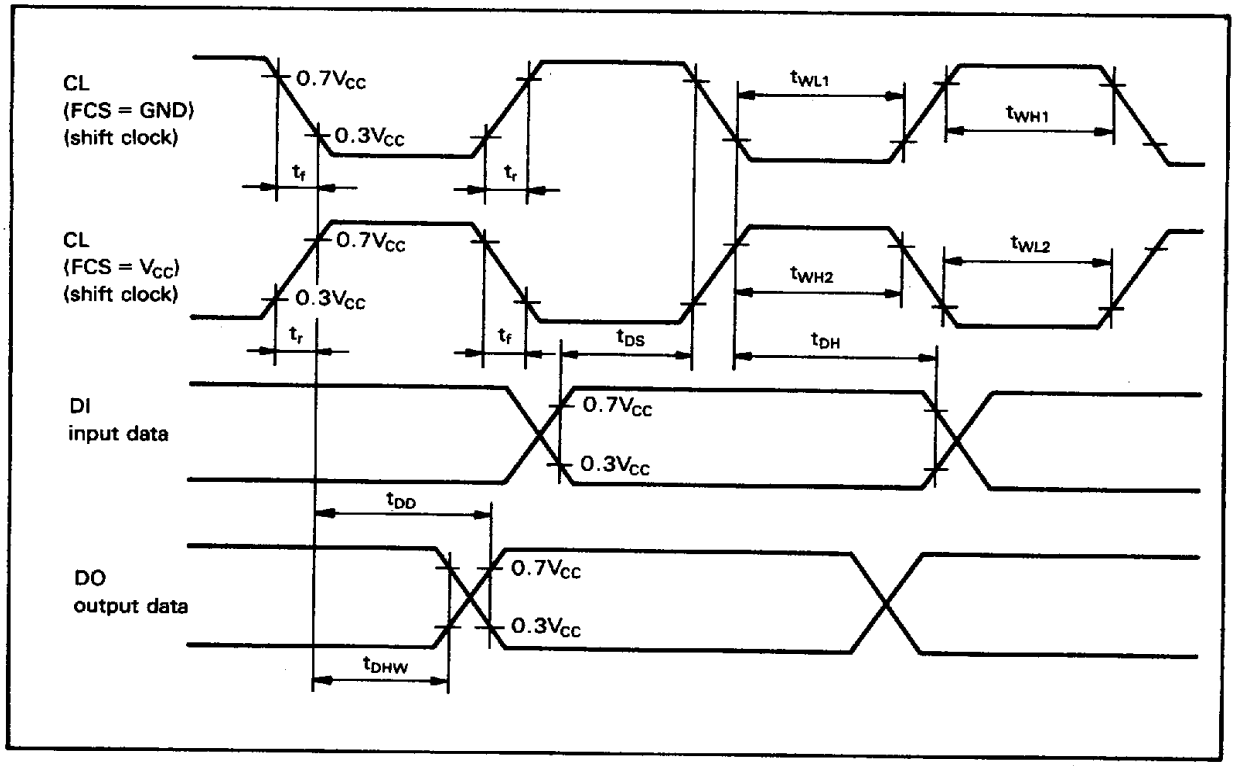
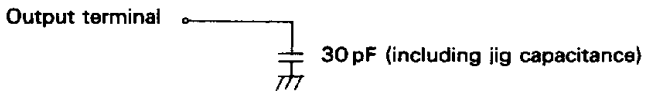
AC Characteristics (V_{CC} = 5 V ± 10%, GND = 0 V, T_a = − 20 to + 75°C)



Item	Symbol	Min	Typ	Max	Unit	Note
Clock low level width (FCS = GND)	t_{WL1}	5.0			µs	
Clock high level width (FCS = GND)	t_{WH1}	125			ns	
Clock low level width (FCS = V_{CC})	t_{WL2}	125			ns	
Clock high level width (FCS = V_{CC})	t_{WH2}	5.0			µs	
Data setup time	t_{DS}	100			ns	
Data hold time	t_{DH}	100			ns	
Output delay time	t_{DD}			3.0	µs	1
Output hold time	t_{DHW}	100			ns	
Clock rise time	t_r			30	ns	
Clock fall time	t_f			30	ns	

Note: 1. The following load circuits are connected for specification:



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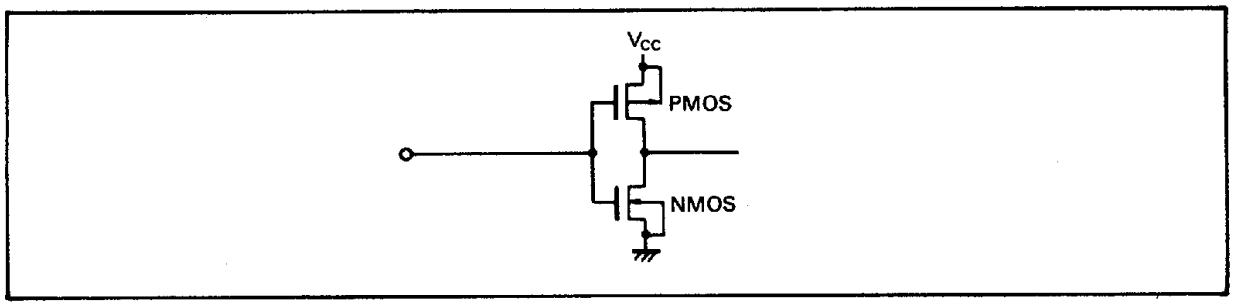
Terminal Configuration

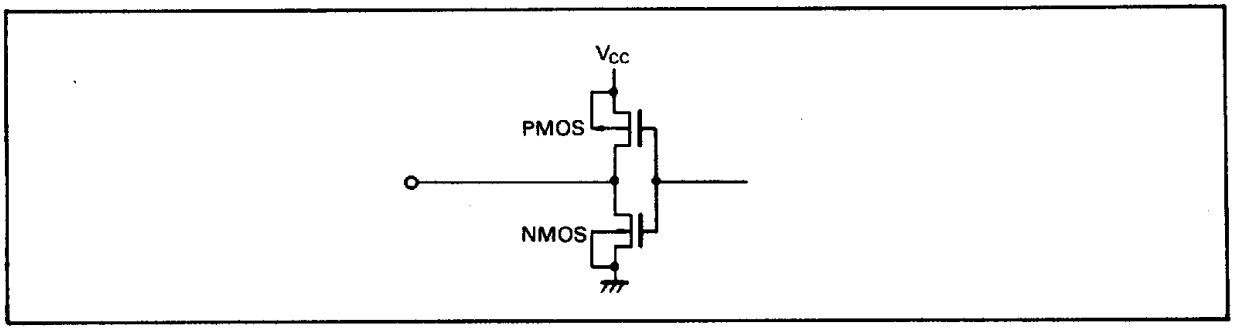
Input Terminal

Applicable Terminals: DI, CL, SHL, FCS, M



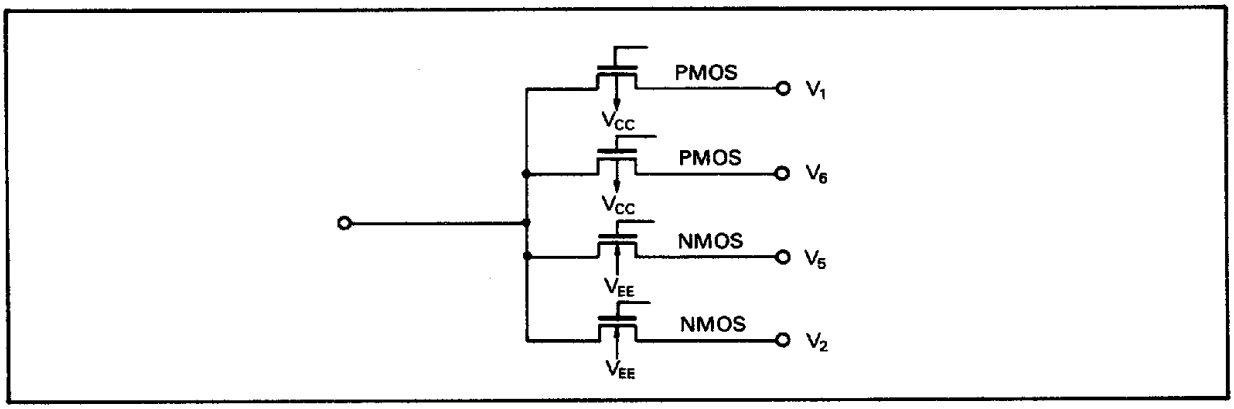
Output Terminal

Applicable Terminal: DO



Output Terminal

Applicable Terminals: X_1—X_{80}



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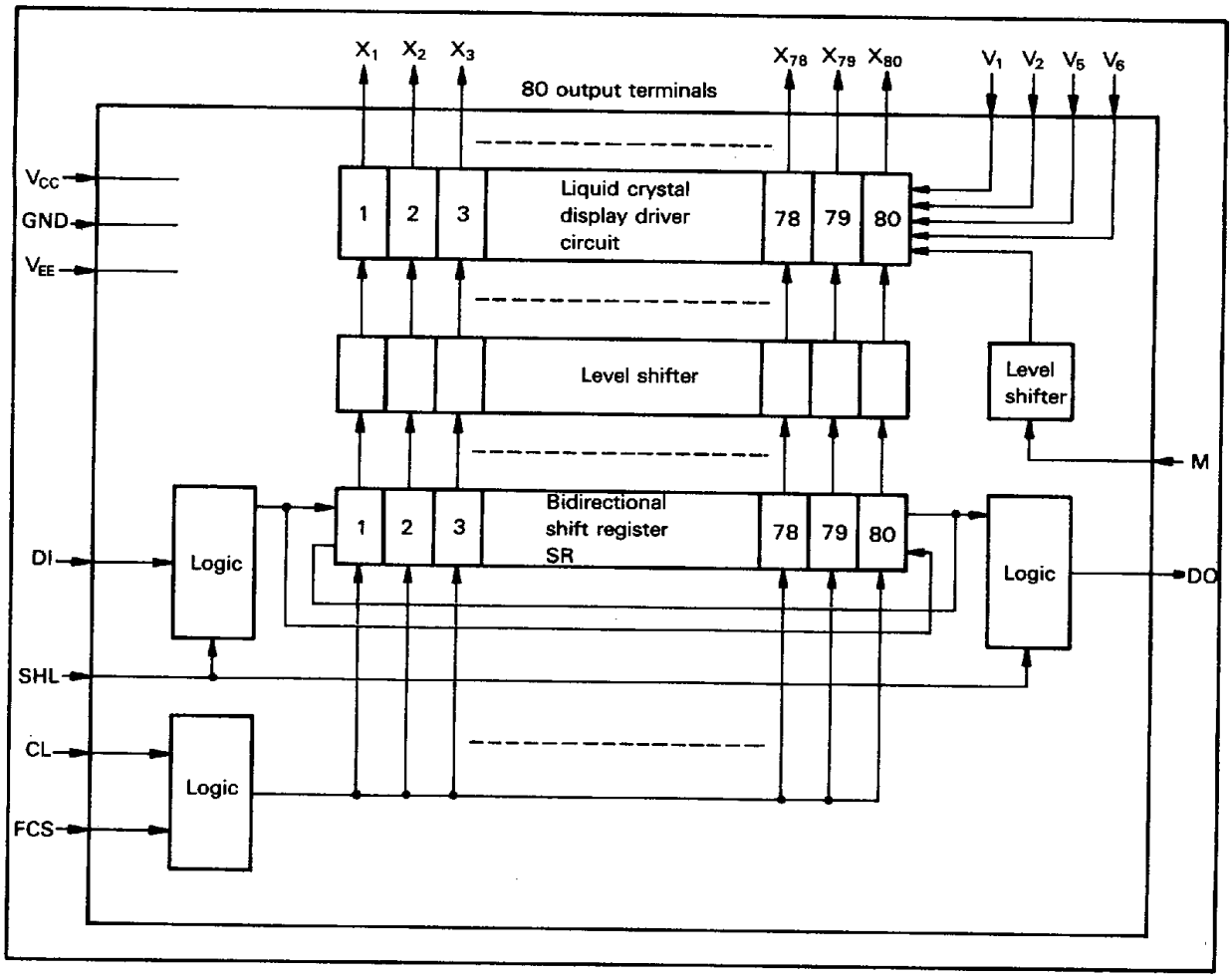
Block Diagram



Block Functions

Bidirectional Shift Register

This is a 80-bit bidirectional register. The data from the DI terminal is shifted by the shift clock CL. The output terminal DO outputs the last shifted data. In case of serial cascade connection, terminal DO functions as the data input to the next LSI. Terminal SHL selects the data shift direction (table 1), and the terminal FCS selects the shift clock phase (table 2).

Liquid Crystal Display Driver Circuit

The combination of the data from the shift register with M signal allows one of the four liquid crystal display driver levels V1, V2, V5, and V6 to be transferred to the output terminals (table 3).

Table 1 SHL Truth Table

(Positive Logic)

SHL	Data Shift Direction
1	DI → SR1 → SR2 → SR3 ····· SR79 → SR80 → DO
0	DI → SR80 → SR79 → SR78 ····· SR2 → SR1 → DO

Table 2 FCS Truth Table

FCS	Shift Clock Phase
0	Shifted at the falling edge of CL
1	Shifted at the rising edge of CL

Table 3 M Truth Table

(Positive Logic)

Data from the Shift Register	M	Output level
0	0	V_5
1	0	V_1
0	1	V_6
1	1	V_2

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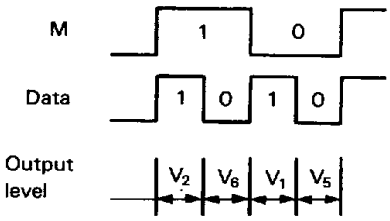
HD61105 Terminal Functions

Terminal Name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND V_{EE}	1 1 1		Power supply	V_{CC} — GND: Power supply for internal logic V_{CC} — V_{EE}: Power supply for LCD drive circuit
V_1 V_2 V_5 V_6	4		Liquid crystal drive level power supply	Power supply for liquid crystal drive V_1, V_2: selection level V_5, V_6: non-selection level
FCS	1	I	V_{CC} or GND	Selects shift clock phase. FCS = V_{CC} Shift register operates at the rise of CL FCS = GND Shift register operates at the fall of CL
M	1	I	Controller	Signal to convert LCD driver signal into AC
CL	1	I	Controller	Shift clock FCS = V_{CC} Shift register operates at the rise of CL FCS = GND Shift register operates at the fall of CL
DI	1	I	Controller or terminal DO of HD61105	Shift register data input In case of cascade connection, the terminal DI is connected to the terminal DO of the preceding LSI.
DO	1	O	Open or terminal DI of HD61105	Shift register data output In case of cascade connection, the terminal DO is connected to the terminal DI of the next LSI.
SHL	1	I	V_{CC} or GND	Selects shift direction of bidirectional shift register.
X_1—X_{80}	80	O	Liquid crystal display	Liquid crystal display driver output Outputs one of the four liquid crystal display driver levels V_1, V_2, V_5, and V_6 with the combination of the data from the shift register and M signal.
NC	7		Open	Unused. No line should be connected.

SHL	Shift Direction	Common Scanning Direction
V_{CC}	DI → SR1 → SR2 → SR80	$X_1 \rightarrow X_{80}$
GND	DI → SR80 → SR79 → SR1	$X_{80} \rightarrow X_1$

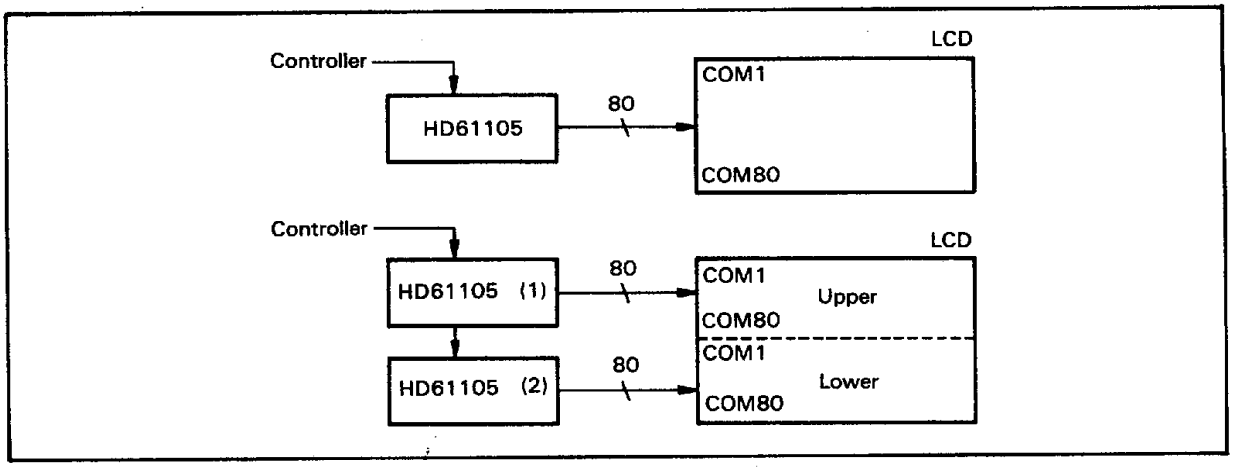


Data 1: Selection level
Data 0: Non-selection level

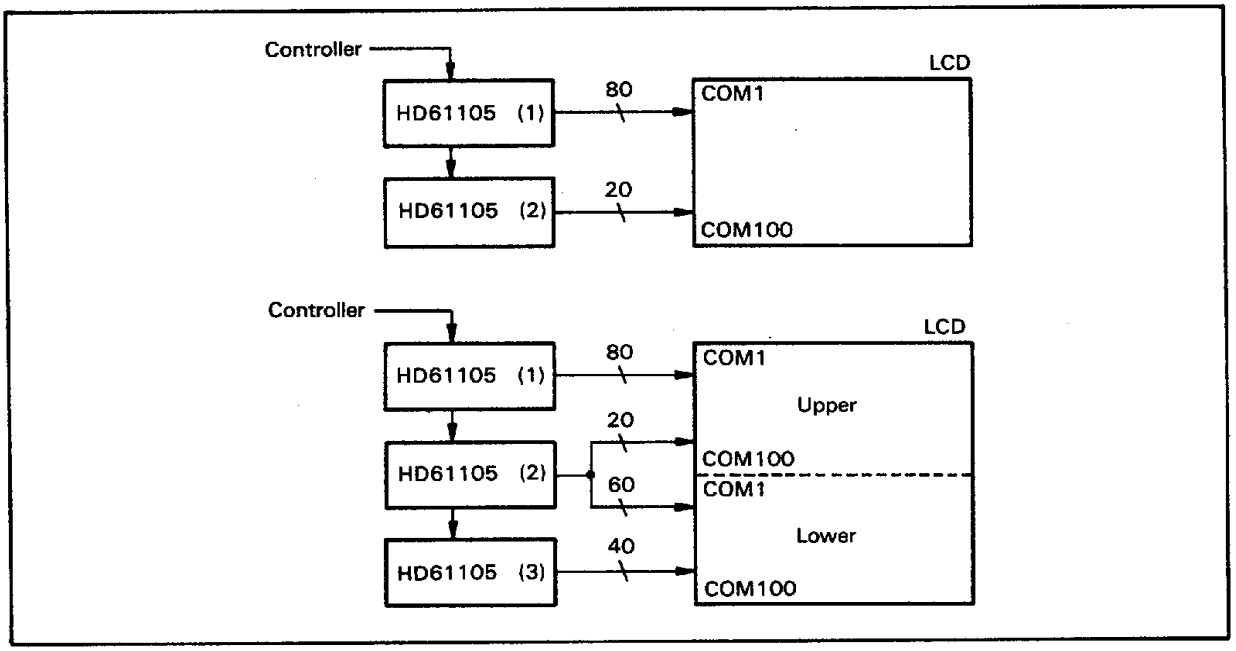
When SHL is V_{CC}, X_1 corresponds to COM1 and X_{80} corresponds to COM80.
When SHL is GND, X_{80} corresponds to COM1 and X_1 corresponds to COM80.

Outline of HD61105 System Configuration

When display duty ratio of LCD is 1/80



When display duty ratio of LCD is 1/100



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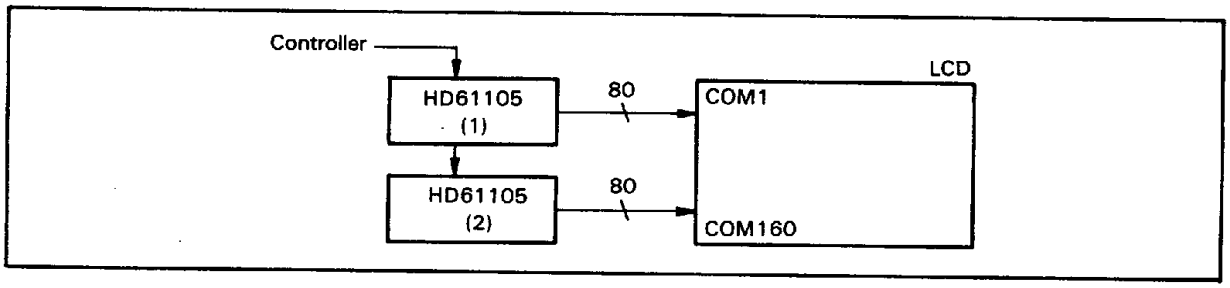
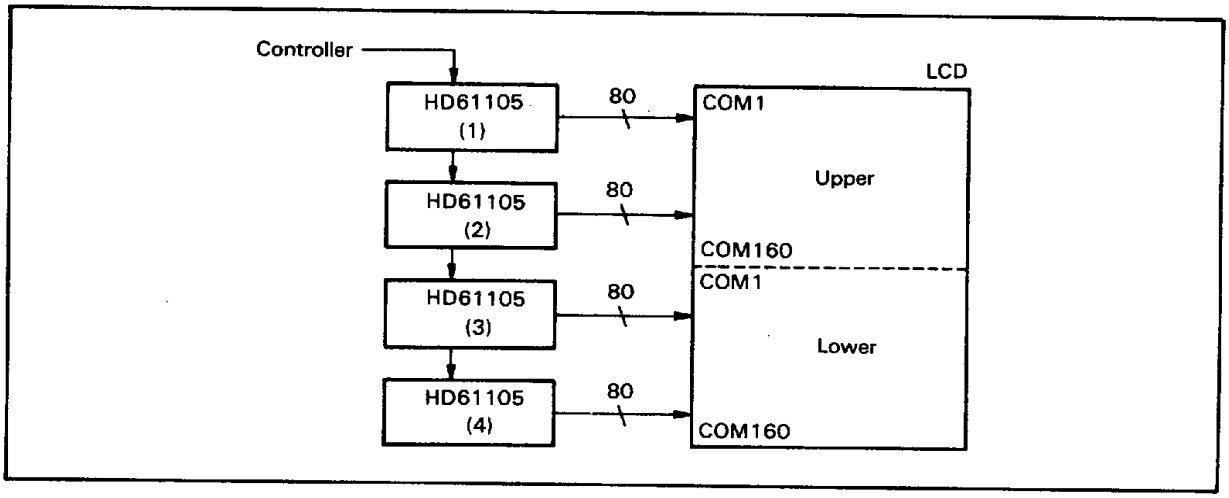
When display duty ratio of LCD is 1/160



When display duty ratio of LCD is 1/160



When display duty ratio of LCD is 1/200

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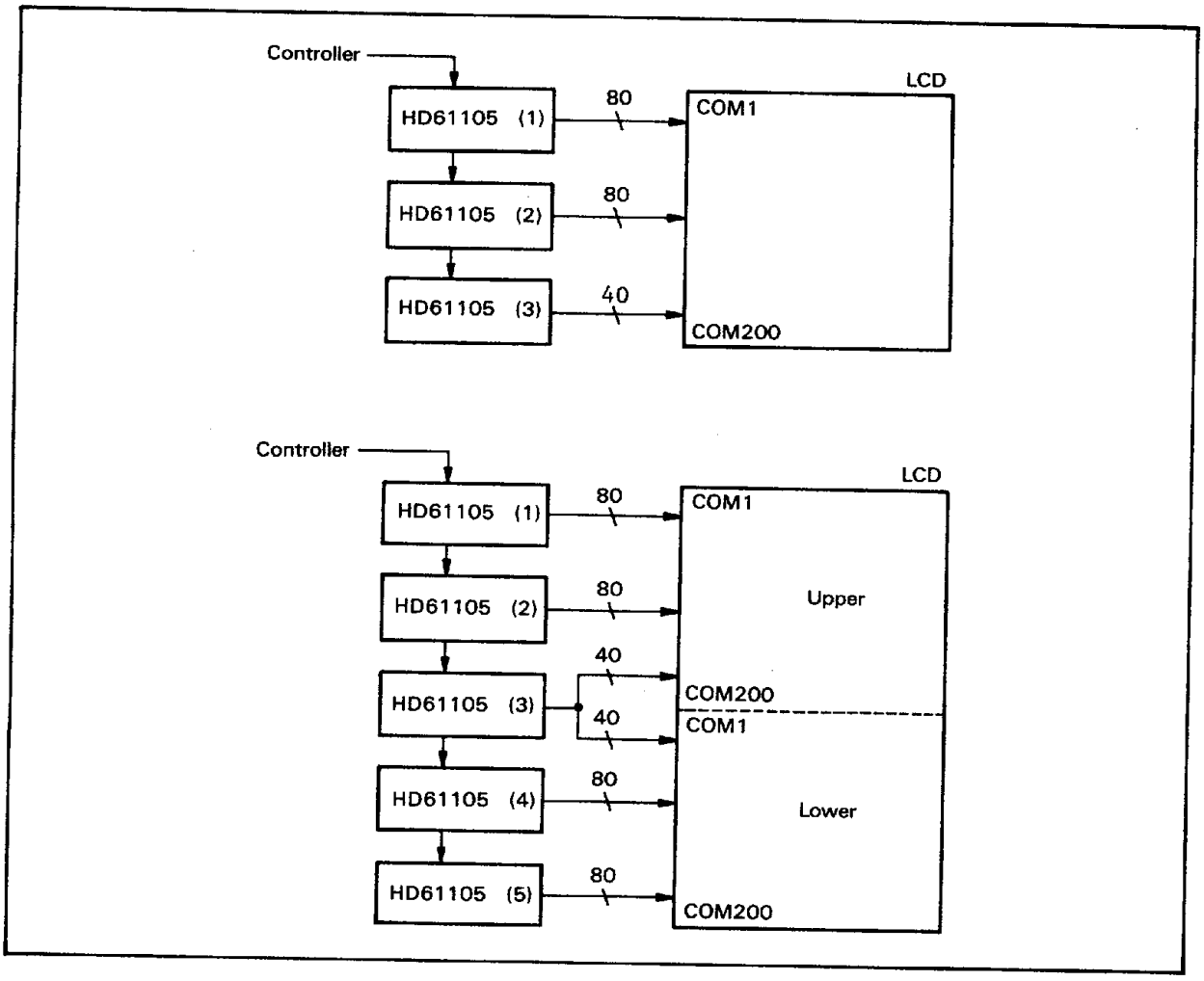

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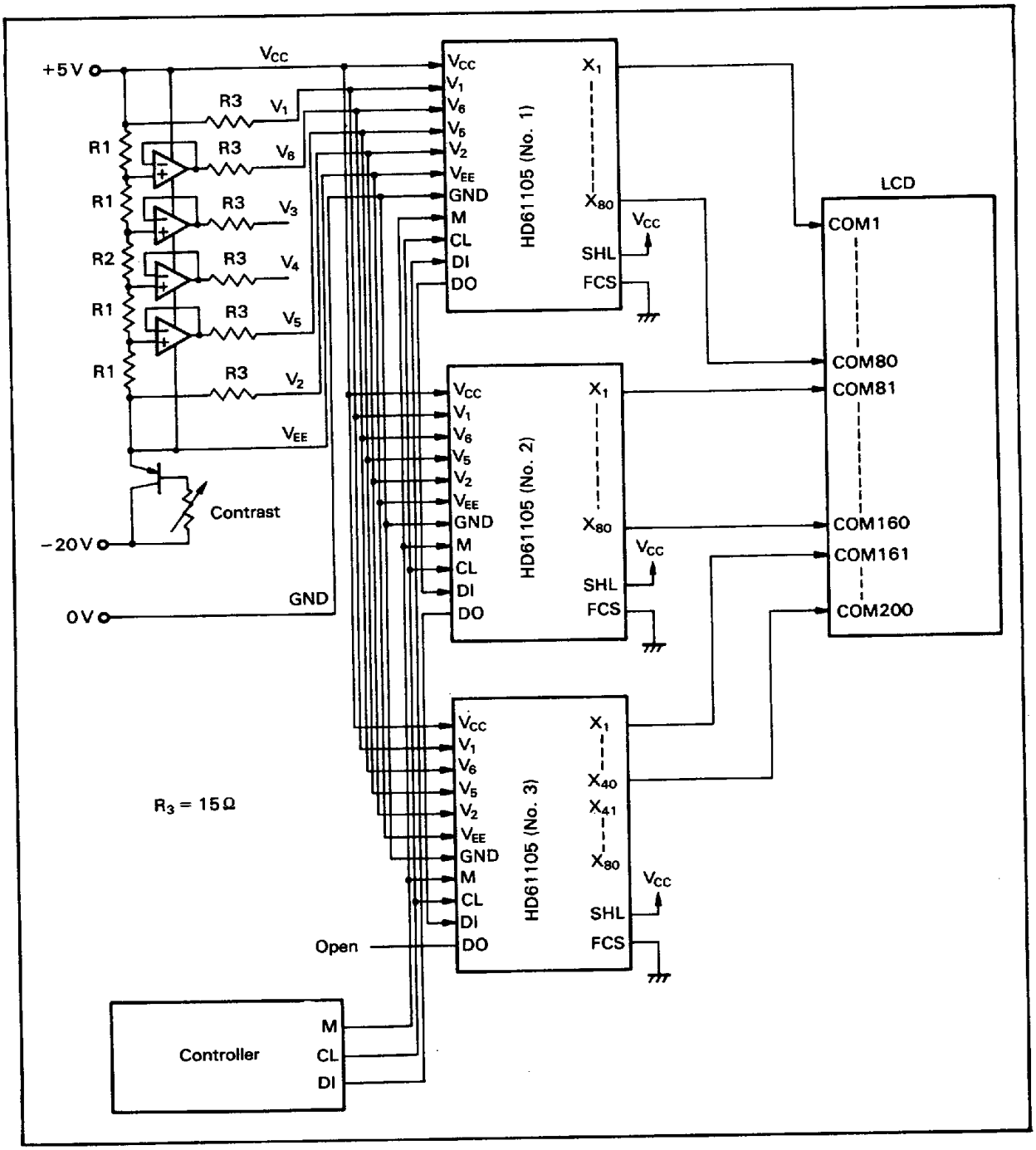
Example of Connection

1/200 duty ratio



Note: 1. The values of R1 and R2 vary with the LCD panel used. When bias factor is 1/15, the values of R1 and R2 should satisfy $\frac{R1}{4R1+R2}=\frac{1}{15}$

For example, R1 = 3 KΩ, R2 = 33 KΩ

Figure 1 Example of Connection (SHL = V_{CC}, FCS = GND)

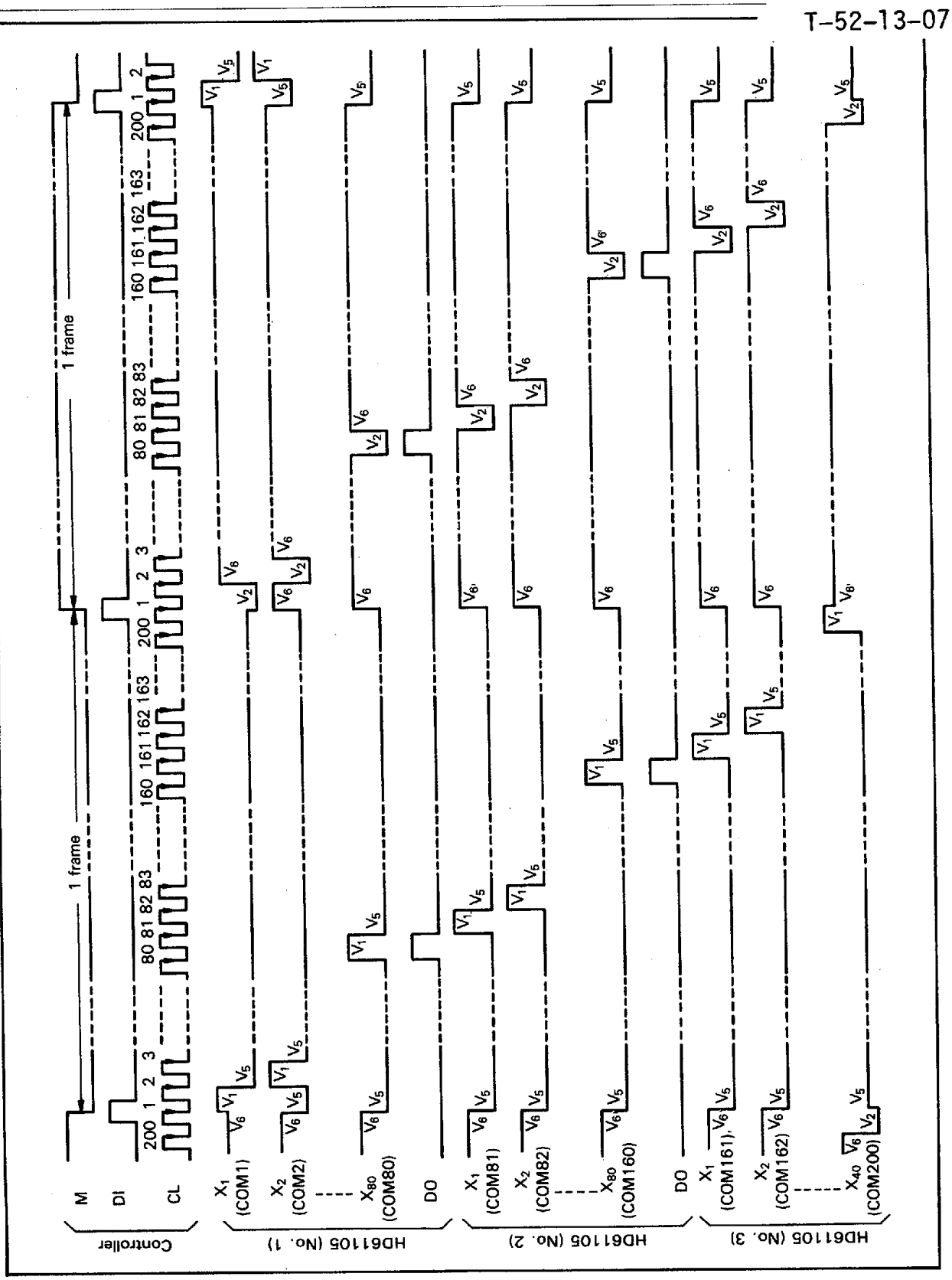


Figure 2 Waveform Example

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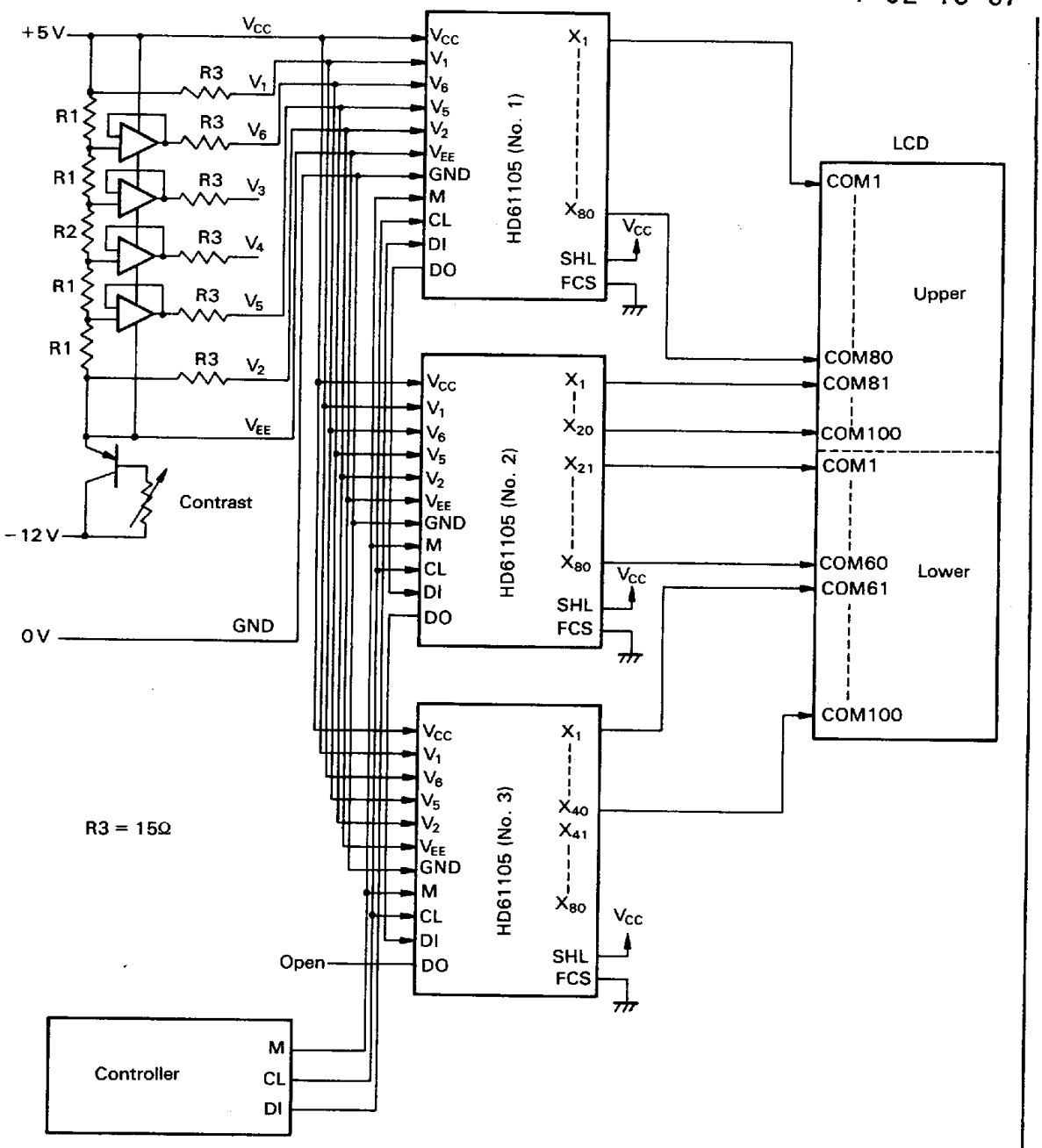

Note: 1. The values of R1 and R2 vary with the LCD panel used.
When bias factor is 1/11, the values of R1 and R2 should satisfy

$$\frac{R1}{4R1+R2}=\frac{1}{11}$$

For example, R1 = 3 KΩ, R2 = 21 KΩ

Figure 3 Example of Connection 1 (SHL = V_{CC}, FCS = GND)

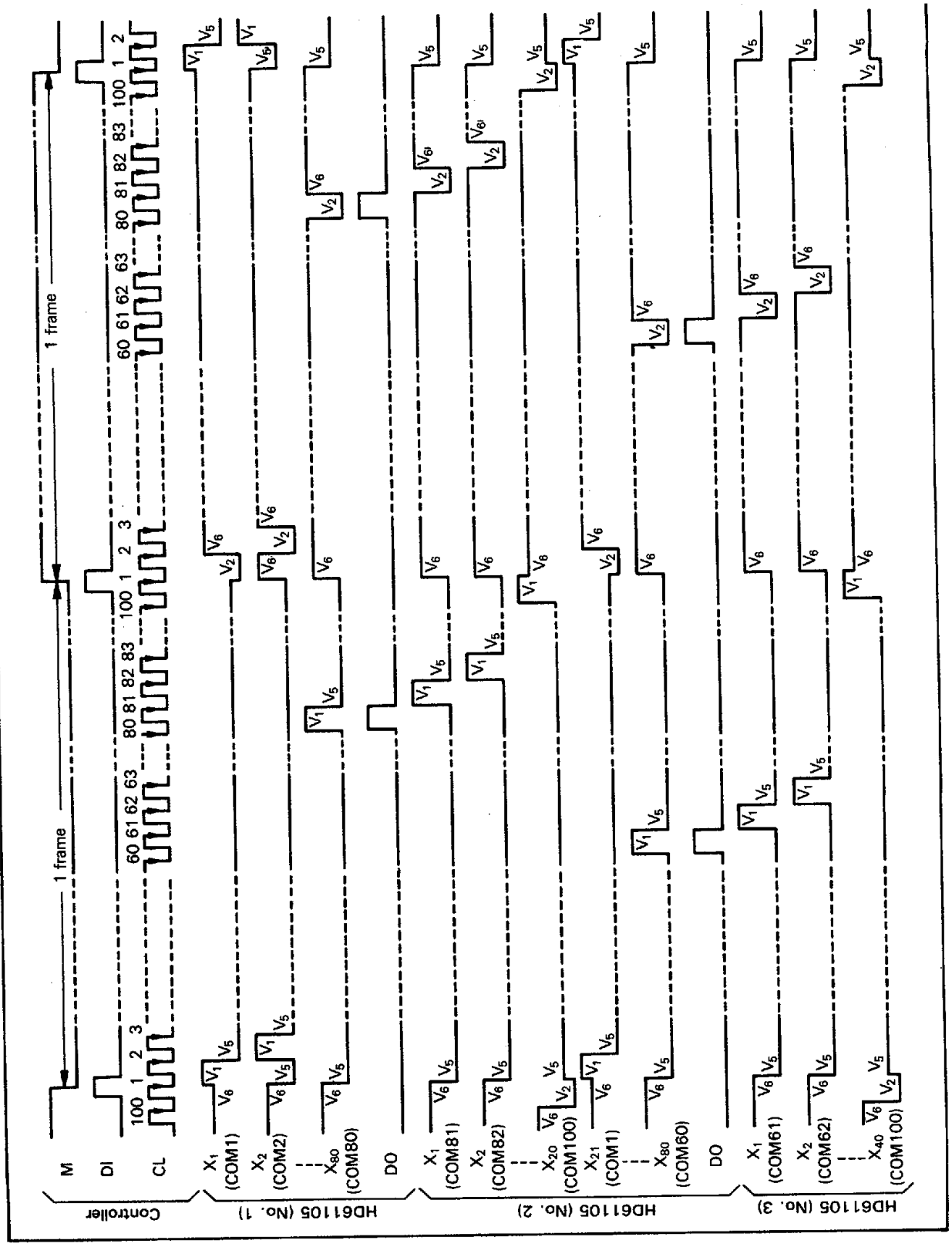

Figure 4 Waveform Example

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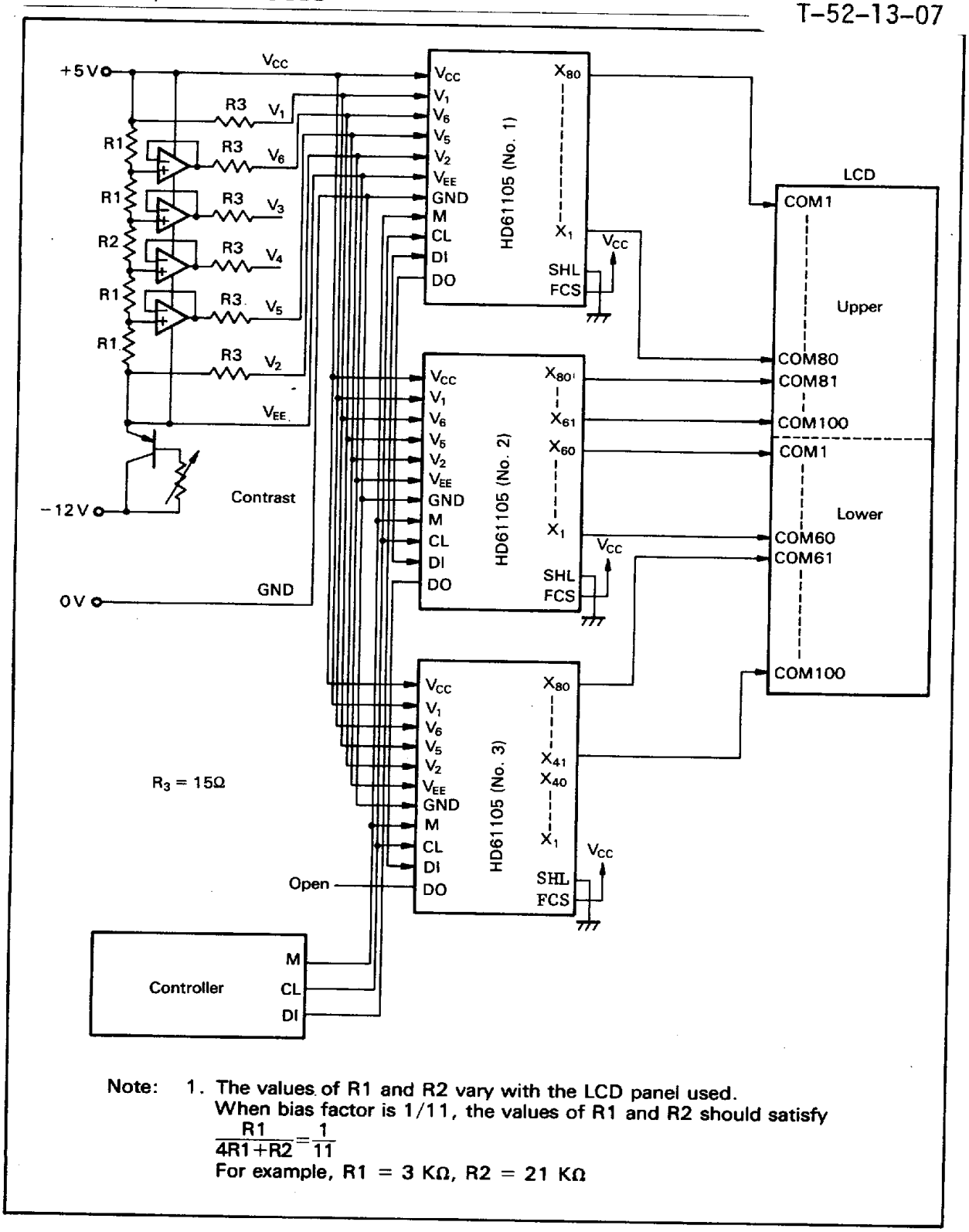

Note: 1. The values of R1 and R2 vary with the LCD panel used.
When bias factor is 1/11, the values of R1 and R2 should satisfy
$\frac{R1}{4R1+R2}=\frac{1}{11}$
For example, R1 = 3 KΩ, R2 = 21 KΩ

Figure 5 Example of Connection 2 (SHL = GND, FCS = V_{CC})

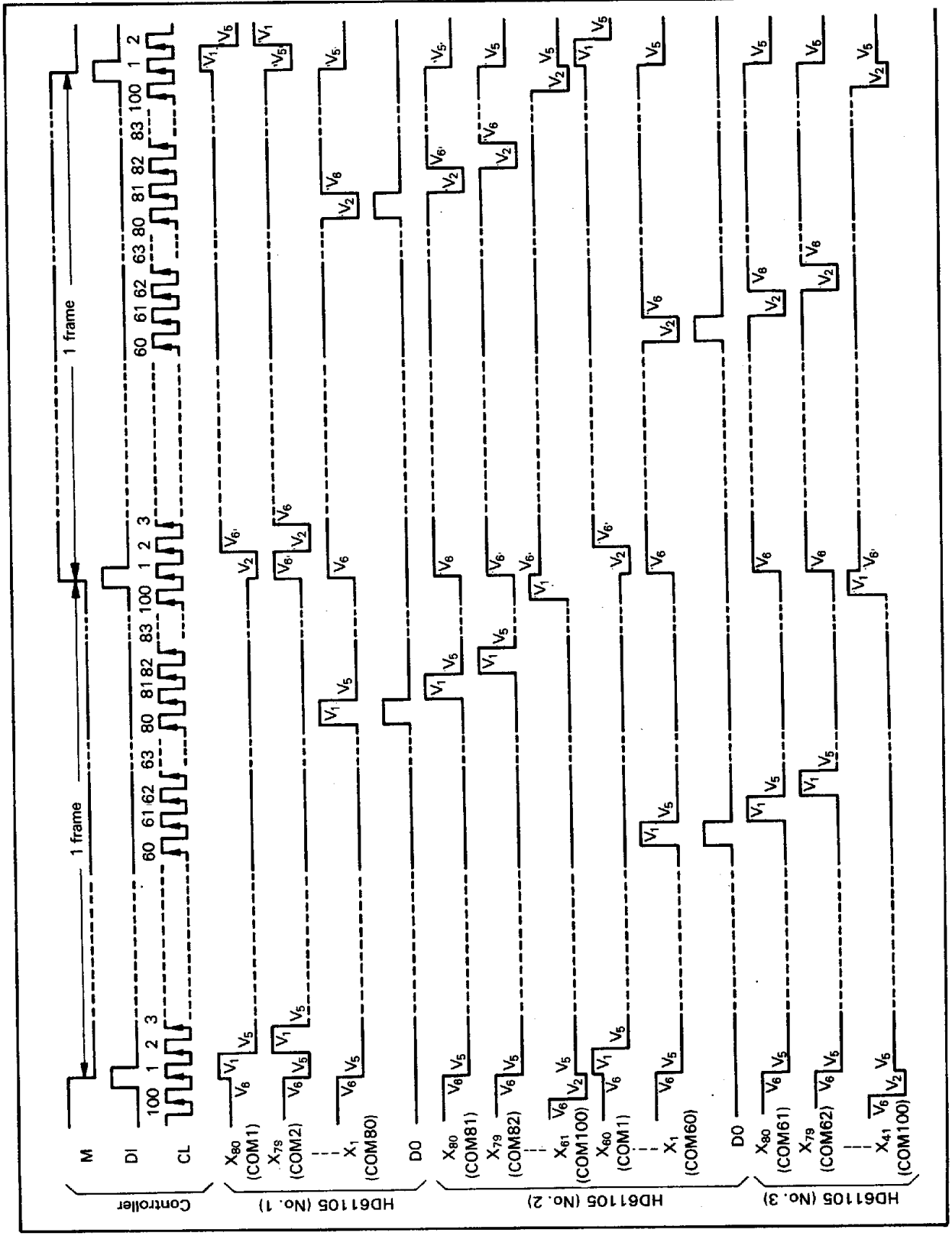

Figure 6 Waveform Example

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