DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD78P214

8-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD78P214 is an 8-bit single-chip microcomputer with the on-chip mask ROM of the μPD78214 replaced with an EPROM or one-time PROM. Since the μPD78P214 is a user-programmable microcomputer, it is suitable for system development evaluation and small production.

Use this manual together with μPD78214 manuals.

Furthermore, for details of the internal functions, be sure to see the separate **"78K/II Series User's Manual Instruction Volume"** and **"μPD78214 Series User's Manual Hardware Volume"**

In this document, "PROM" is used in parts common to one-time PROM products and EPROM products.

FEATURES

- μPD78214 compatible
- On-chip EPROM
  - μPD78P214DW : Reprogrammable (suitable for system development)
  - μPD78P214CW/GC/GJ/GQ/L : One-time programmable (suitable for small production)
- QTOP™ microcomputer compatibility

Remarks "QTOP microcomputer" is the generic name for NEC single-chip microcomputers with on-chip one-time PROM which are totally supported from program writing through printing, screening and verification.

ORDERING INFORMATION

Ordering Code	Package	On-chip ROM
μPD78P214CW	64-pin plastic shrink DIP (750 mil)	one-time PROM
μPD78P214GC-AB8	64-pin plastic QFP (□ 14 mm)	one-time PROM
μPD78P214GJ-5BJ	74-pin plastic QFP (□ 20 mm)	one-time PROM
μPD78P214GQ-36	64-pin plastic QUIP	one-time PROM
μPD78P214L	64-pin plastic QFJ (□ 950 mil)	one-time PROM
μPD78P214DW	64-pin ceramic shrink DIP (CERDIP) (with window) (750mil)	EPROM

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

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(O. D. No. IC-7732E)
Date Published December 1993 P
Printed in Japan

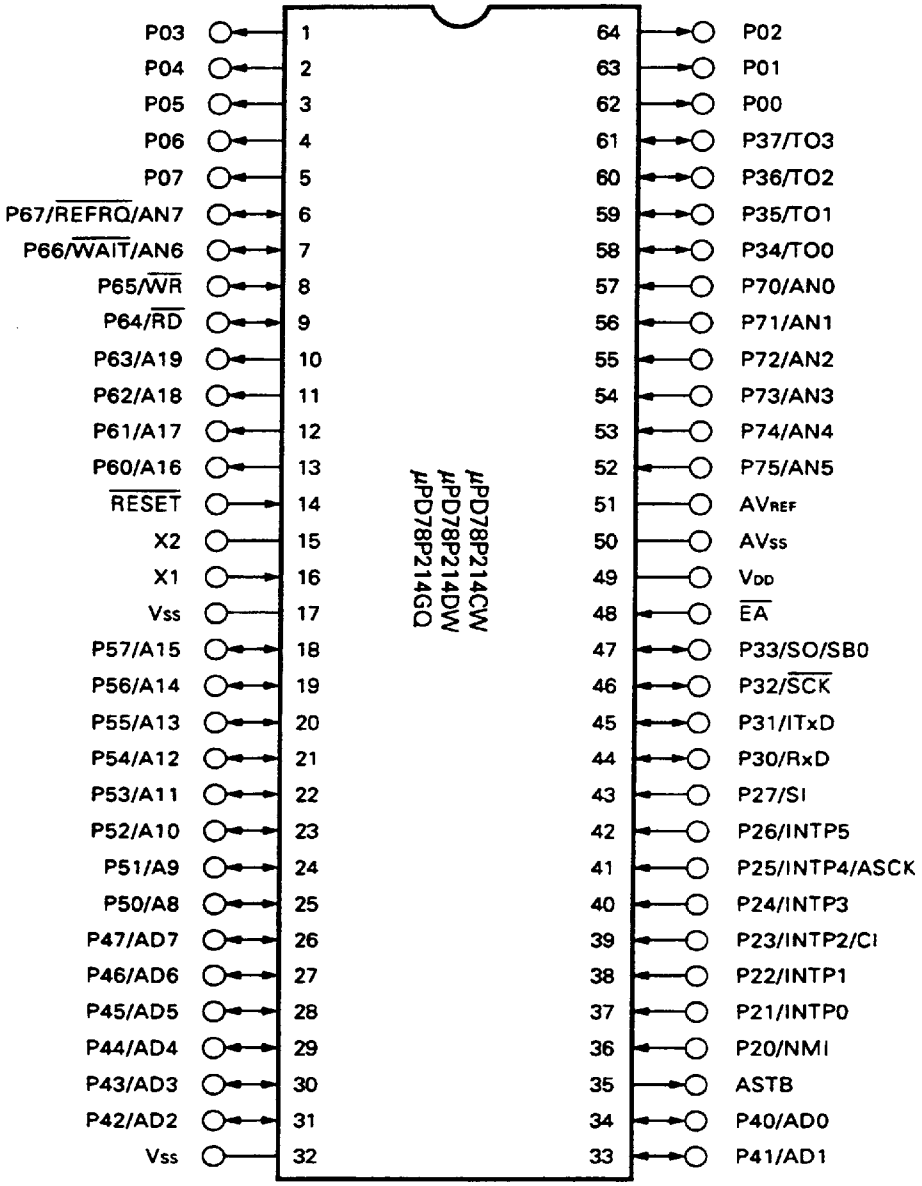
The mark ★ shows major revised points.

6427525 0085905 80T

PIN CONFIGURATION (TOP VIEW)

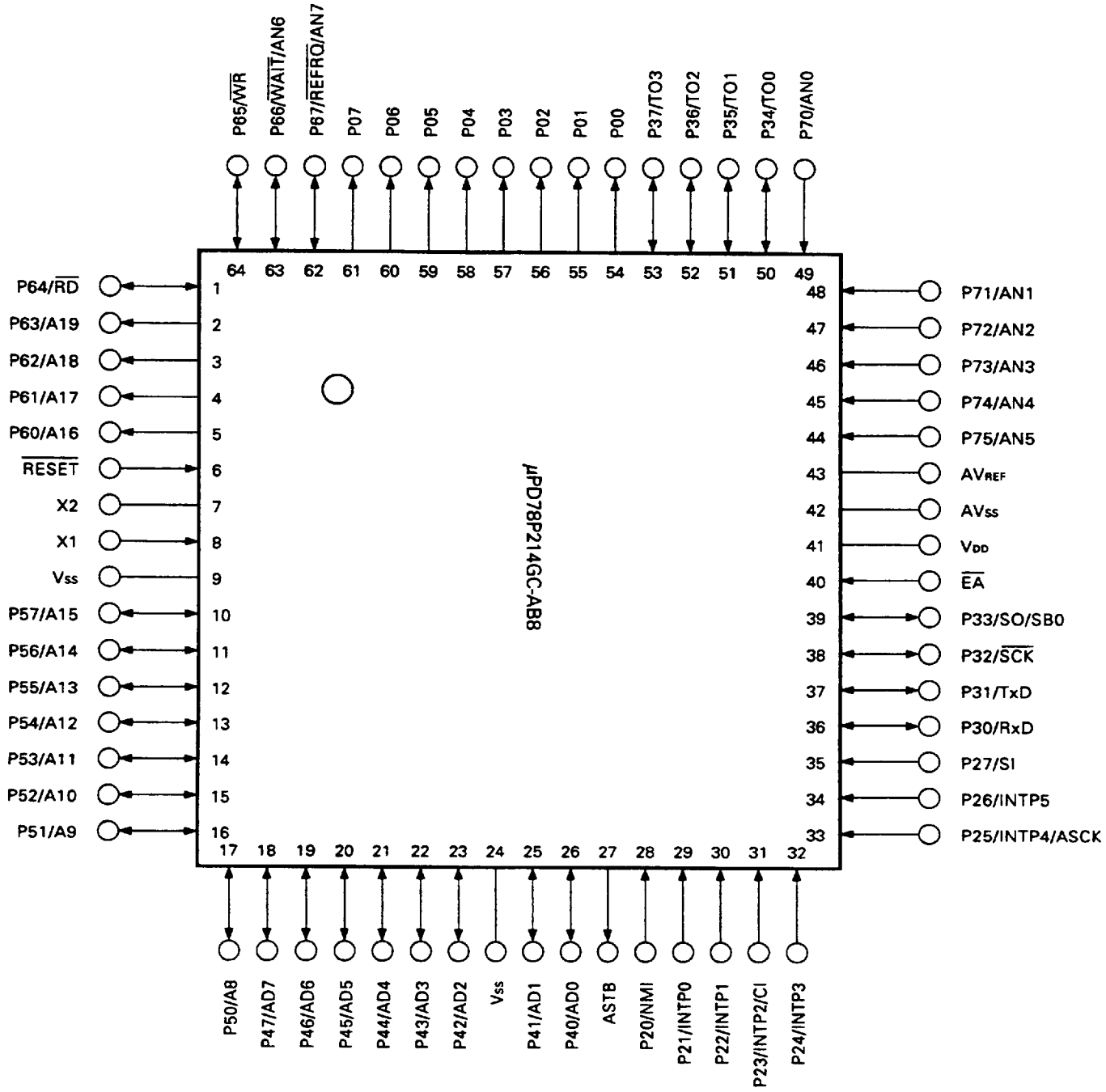
(1) Normal Operating Mode

(a) 64-pin plastic shrink DIP, 64-pin plastic QUIP, and 64-pin ceramic shrink DIP (CERDIP) (with window)

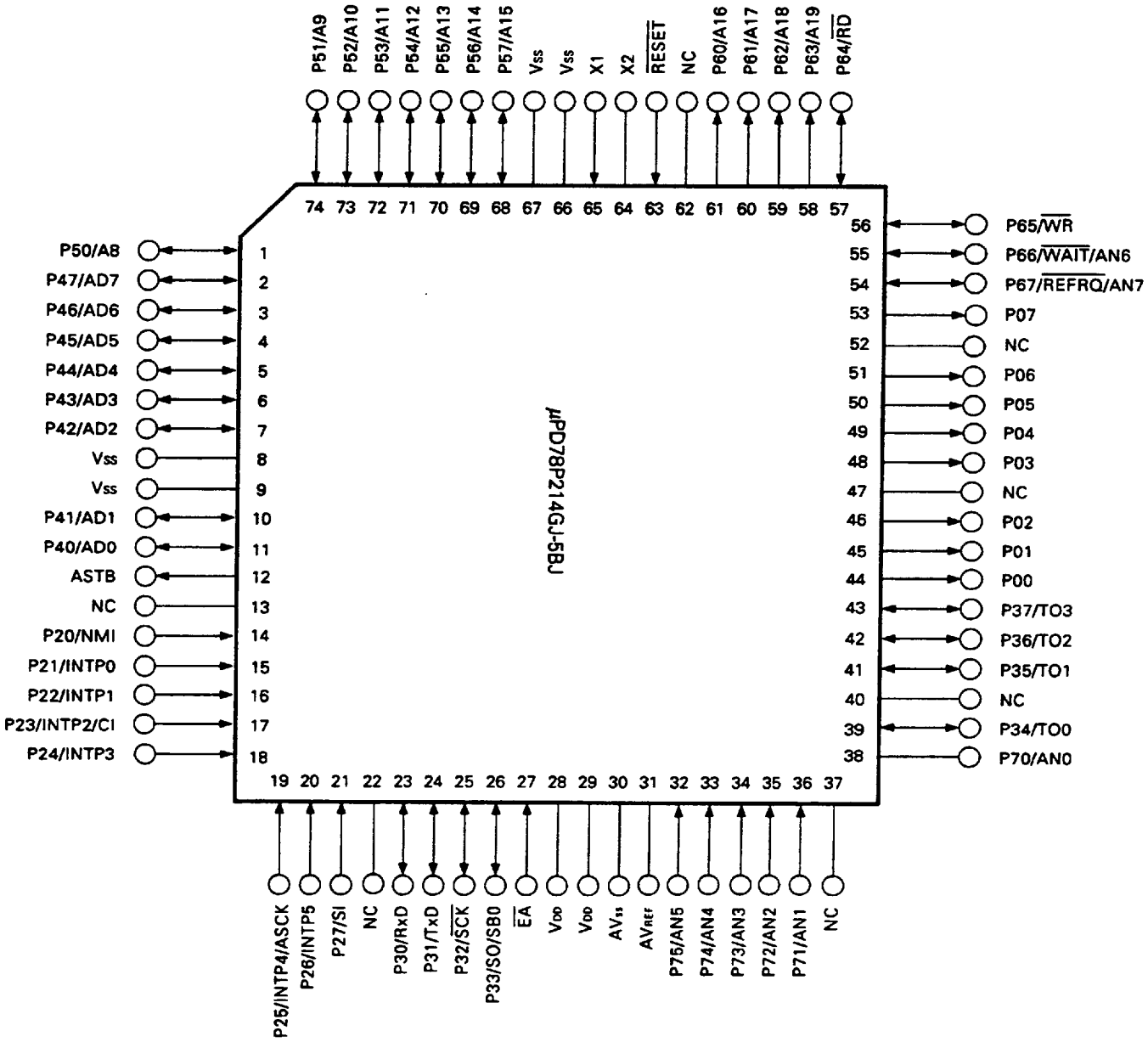


Remarks Pin compatible with μPD78210CW/GQ.

(b) 64-pin plastic QFP

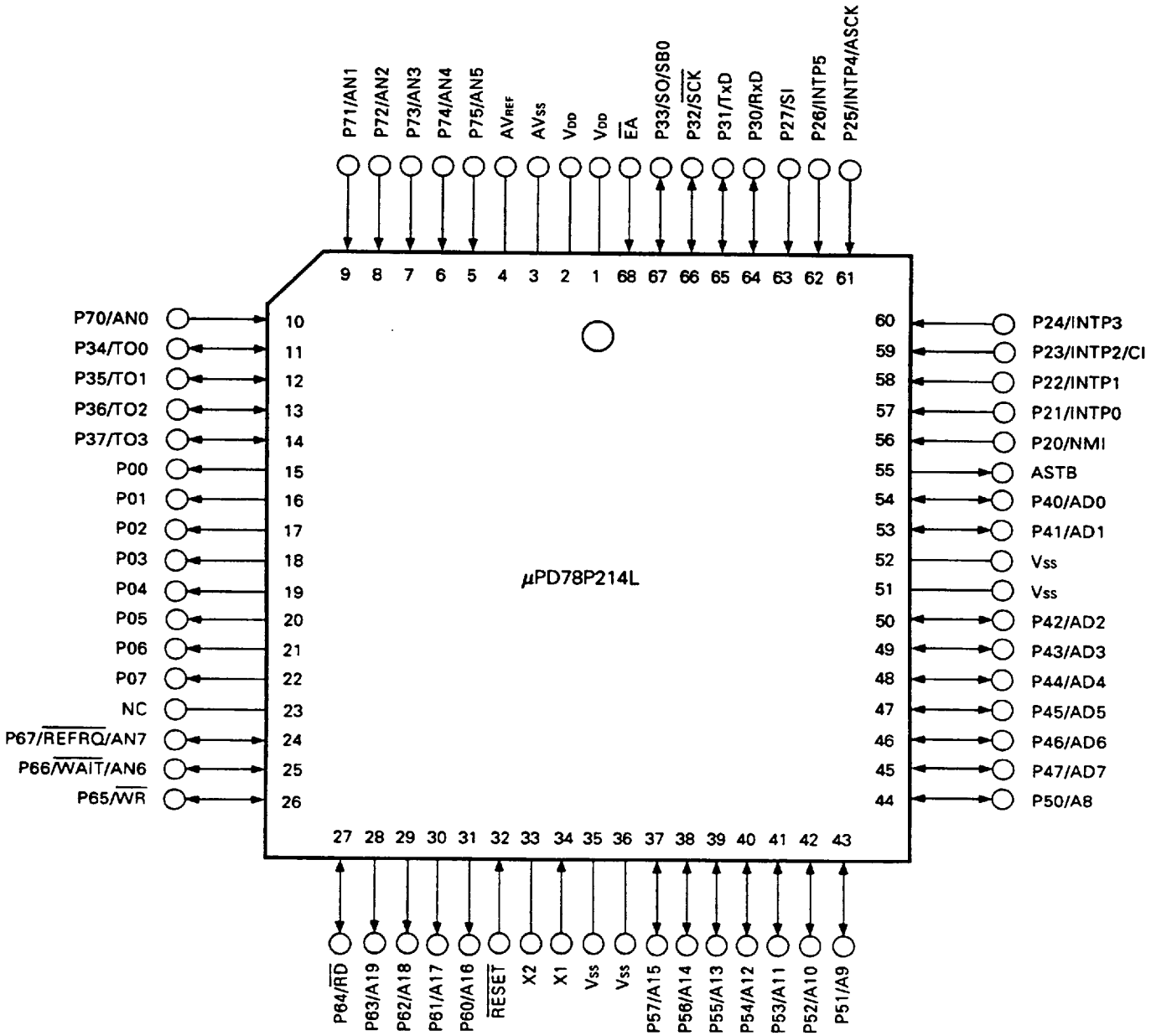


(c) 74-pin plastic QFP



Remarks 1. Pin compatible with μPD78210GJ.
2. NC : not connected internally.

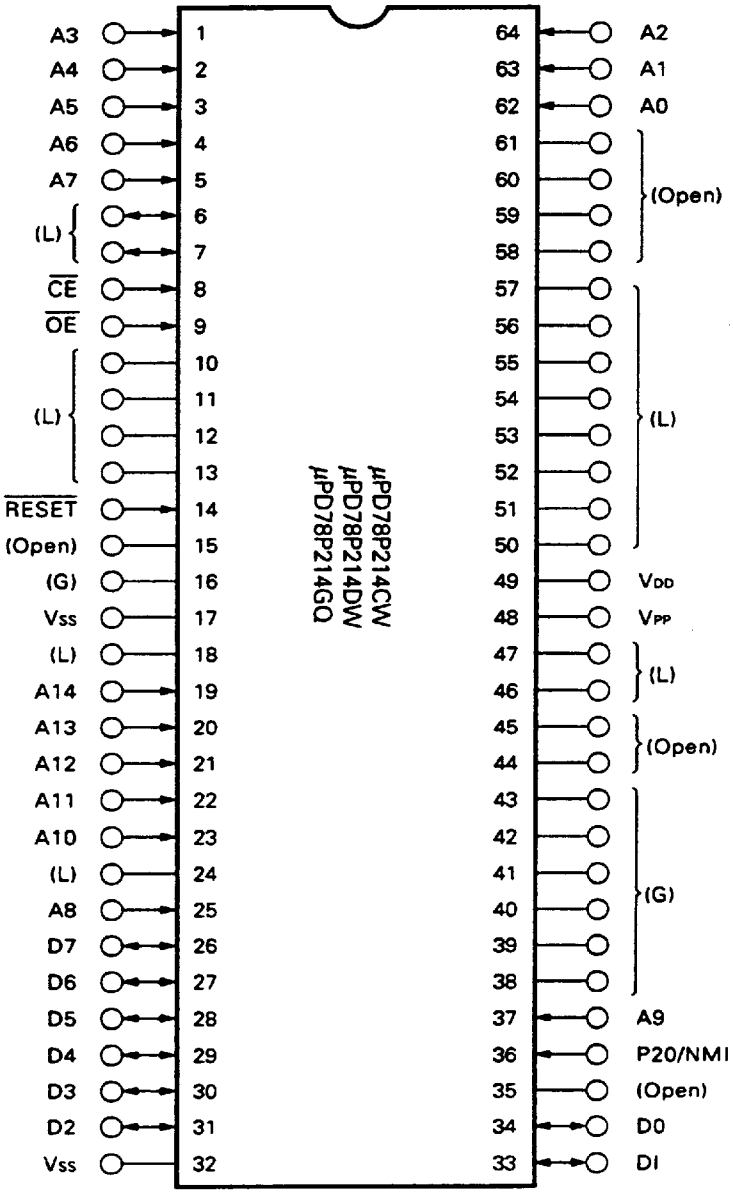
(d) 68-pin plastic QFJ



Remarks 1. Pin compatible with μPD78210L.
2. NC : not connected internally.

(2) PROM Programming Mode (P20/NMI = 12.5 V, $\overline{\text{RESET}}$ = L)

(a) 64-pin plastic shrink DIP, 64-pin plastic QUIP, and 64-pin ceramic shrink DIP (CERDIP) (with window)



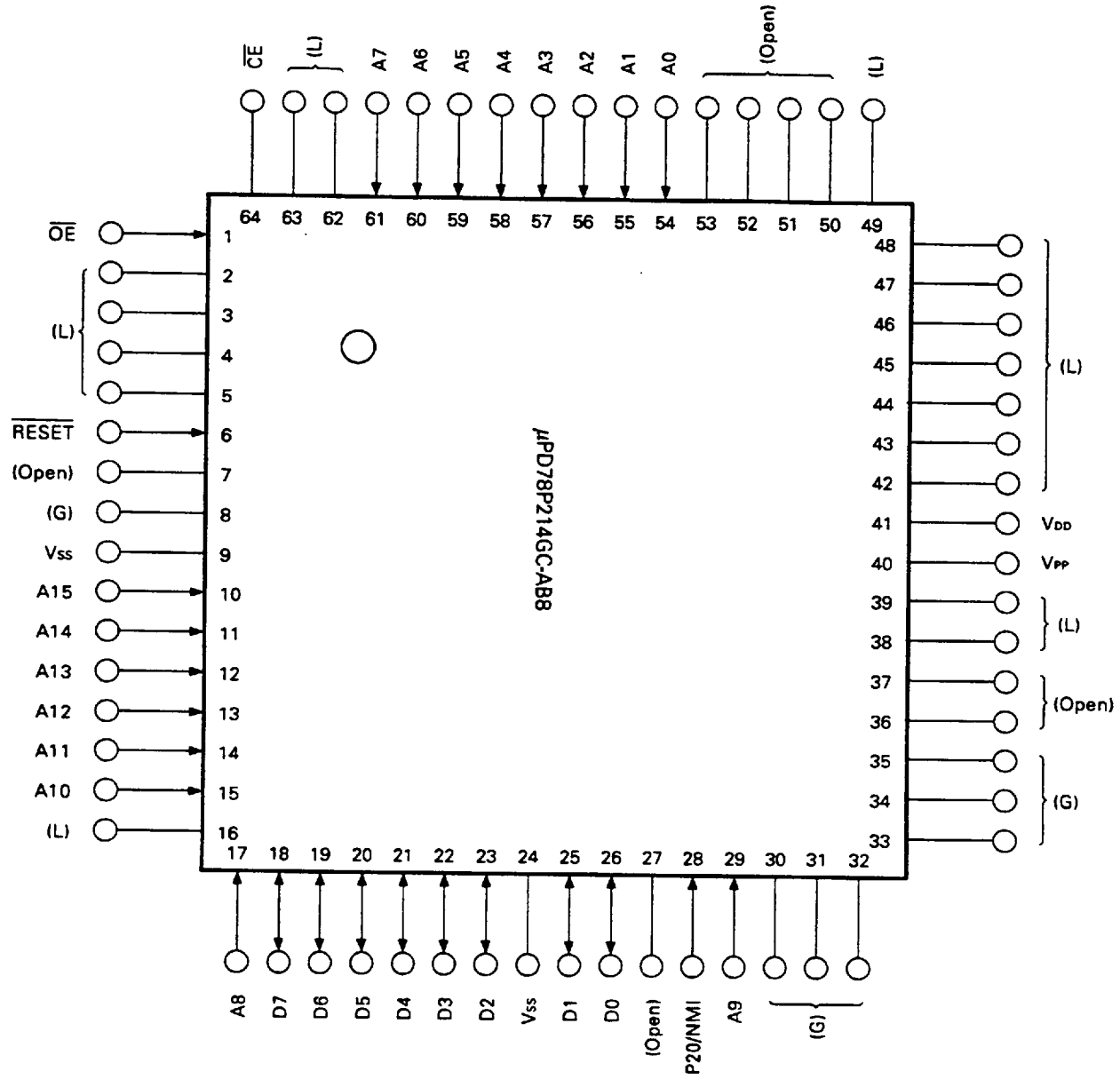
Note **Processing for pins which are not used in the PROM programming mode is indicated in parentheses.**

L : Connect these pins independently to VSS via a resistor.

G : Connect these pins to VSS.

Open : No connection required.

(b) 64-pin plastic QFP



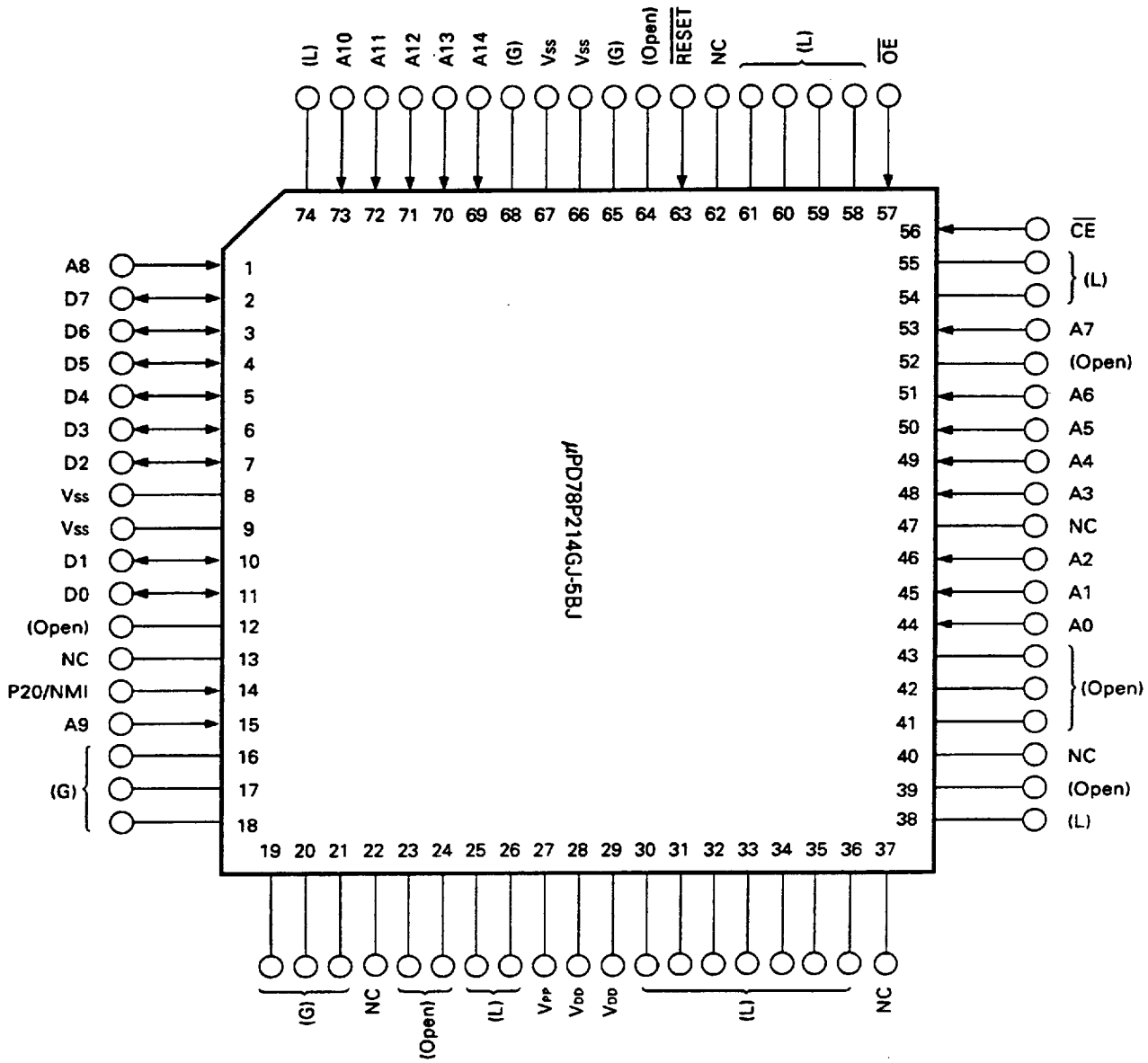
Note **Processing for pins which are not used in the PROM programming mode is indicated in parentheses.**

L : Connect these pins independently to Vss via a resistor.

G : Connect these pins to Vss.

Open : No connection required.

(c) 74-pin plastic QFP



Note **Processing for pins which are not used in the PROM programming mode is indicated in parentheses.**

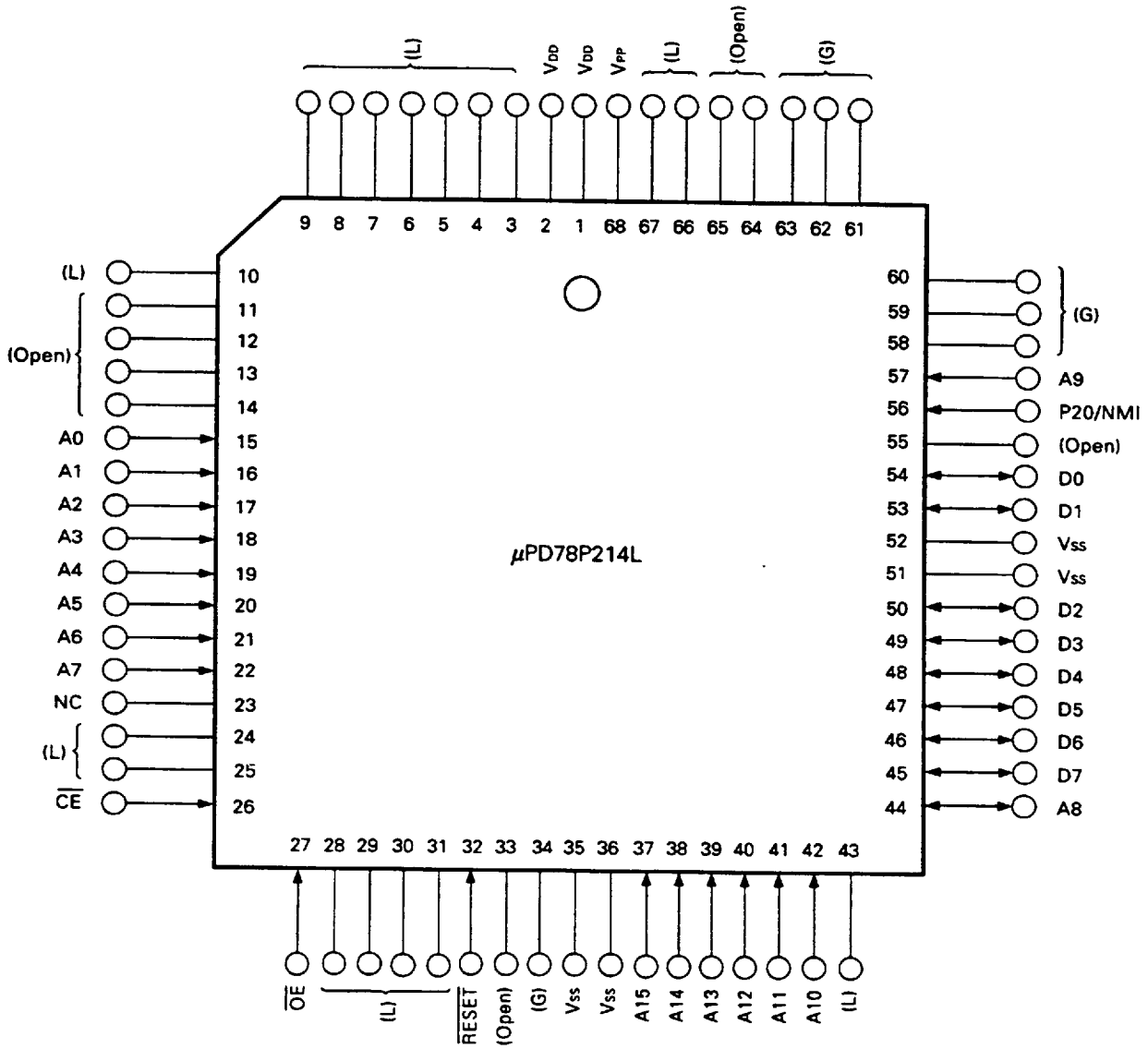
L : Connect these pins independently to Vss via a resistor.

G : Connect these pins to Vss.

Open : No connection required.

Remarks NC : not connected internally.

(d) 68-pin plastic QFJ



Note **Processing for pins which are not used in the PROM programming mode is indicated in parentheses.**

L : Connect these pins independently to Vss via a resistor.

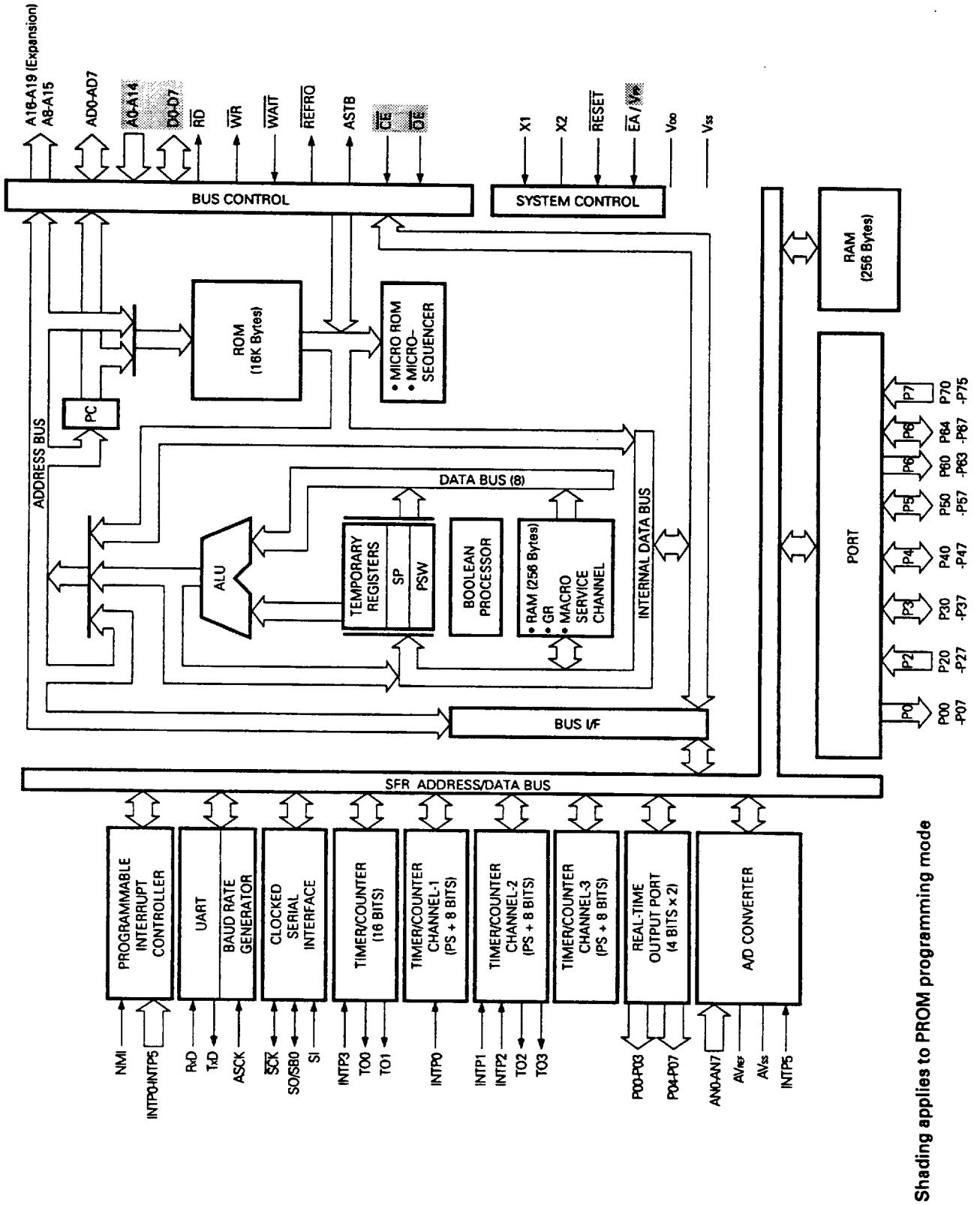
G : Connect these pins to Vss.

Open : No connection required.

Remarks NC : not connected internally.

P00 to P07	:	Port 0
P20 to P27	:	Port 2
P30 to P37	:	Port 3
P40 to P47	:	Port 4
P50 to P57	:	Port 5
P60 to P67	:	Port 6
P70 to P75	:	Port 7
TO0 to TO3	:	Timer Output
CI	:	Clock Input
RxD	:	Receive Data
TxD	:	Transmit Data
$\overline{SCK}$	:	Serial Clock
ASCK	:	Asynchronous Serial Clock
SB0	:	Serial Bus
SI	:	Serial Input
SO	:	Serial Output
NMI	:	Non-Maskable Interrupt
INTP0 to INTP5	:	Interrupt From Peripherals
AD0 to AD7	:	Address/Data Bus
A8 to A19	:	Address Bus
$\overline{RD}$	:	Read Strobe
$\overline{WR}$	:	Write Strobe
$\overline{WAIT}$	:	Wait
ASTB	:	Address Strobe
$\overline{REFRQ}$	:	Refresh Request
$\overline{RESET}$	:	Reset
X1, X2	:	Crystal
$\overline{EA}$	:	External Access
AN0 to AN7	:	Analog Input
AV_{REF}	:	Reference Voltage
AV_{SS}	:	Analog Ground
V_{DD}	:	Power Supply
V_{SS}	:	Ground
NC	:	Non-Connection
$\overline{CE}$	:	Chip Enable
$\overline{OE}$	:	Output Enable
V_{PP}	:	Programming Power Supply

INTERNAL BLOCK DIAGRAM



Shading applies to PROM programming mode

CONTENTS

1. PIN FUNCTIONS

1.1 NORMAL OPERATING MODE

(1) Ports

Pin Name	Input/Output	Dual Function Pin	Function
P00 to P07	Output	——	Port 0 (P0): Use enabled as a real-time output port (4 bits × 2). Transistor direct drive capability.
P20	Input	NMI	Port 2 (P2): P20 is abled for use as a general-purpose port (non-maskable interrupt). However, input level can be checked in the interrupt routine. P22 to P27 are specifiable for on-chip resistor connection in 6-bit batch by software.
P21		INTP0	
P22		INTP1	
P23		INTP2/CI	
P24		INTP3	
P25		INTP/ASCK	
P26		INTP5	
P27		SI	
P30	Input/output	RxD	Port 3 (P3): Input/output specifiable as a bit-wise. Input mode pins specifiable for on-chip pull-up resistor connection as a batch by software.
P31		TxD	
P32		$\overline{SCK}$	
P33		SO/SB0	
P34 to P37		TO0 to TO3	
P40 to P47	Input/output	AD0 to AD7	Port 4 (P4): Input/output specifiable for eight bits at one time. Specifiable for on-chip pull-up resistor connection in 8- bit batch by software.
P50 to P57	Input/output	A8 to A15	Port 5 (P5): Input/output specifiable as a bit-wise. Input mode pins specifiable for on-chip pull-up resistor connection as a batch by software. LED direct drive capability.
P60 to P63	Output	A16 to A19	Port 6 (P6): Input/output specifiable as a bit-wise for P64 to P67. The connection of the on-chip pull-up resistor can be specified as a batch for input mode pins P64 to P67 in a software.
P64	Input/output	$\overline{RD}$	
P65		$\overline{WR}$	
P66		$\overline{WAIT}$/AN6	
P67		$\overline{REFRQ}$/AN7	
P70 to P75	Input	AN0 to AN5	Port 7 (P7)

(2) Other than ports

Pin Name	Input/Output	Function	Dual Function Pin
TO0 to TO3	Output	Timer output	P34 to P37
CI	Input	Count clock input to 8-bit timer/counter 2	P23/INTP2
RxD	Input	Serial data input (UART)	P30
TxD	Output	Serial data output (UART)	P31
ASCK	Input	Baud rate clock input (UART)	P25/INTP4
SB0	Input/output	Serial data input/output (SBI)	P33/SO
SI	Input	Serial data input (3-wire serial I/O)	P27
SO	Output	Serial data output (3-wire serial I/O)	P33/SB0
$\overline{SLK}$	Input/output	Serial clock input/output (SBI, 3-wire serial I/O)	P32
NMI	Input	External interrupt request	P20
INTP0			P21
INTP1			P22
INTP2			P23/CI
INTP3			P24
INTP4			P25/ASCK
INTP5			P26
AD0 to AD7	Input/output	Time-multiplexing address/data bus (external memory connection)	P40 to P47
A8 to A15	Output	Higher address bus (external memory connection)	P50 to P57
A16 to A19	Output	Expanded higher address (external memory connection)	P60 to P63
$\overline{RD}$	Output	Read strobe for external memory	P64
$\overline{WR}$	Output	Write strobe for external memory	P65
$\overline{WAIT}$	Input	Wait insert	P66/AN6
ASTB	Output	Latch timing output of time-multiplexing addresses (A0 to A7) (in external memory access)	—
$\overline{REFRQ}$	Output	Refresh pulse output to external pseudo static memory	P67/AN7
$\overline{RESET}$	Input	Chip reset	—
X1	Input	Crystal connection for system clock oscillation (clock to X1 enabled)	—
X2	—		
$\overline{EA}$	Input	ROM-less operation specification (external access in the same space as internal ROM)	—
AN0 to AN5	Input	Analog voltage input for A/D converter	P70 to P75
AN6, AN7			P66/$\overline{WAIT}$, P67/$\overline{REFRQ}$
AV_{REF}	—	Reference voltage application for A/D converter	—
AV_{SS}		GND for A/D converter	
V_{DD}		Positive power supply	
V_{SS}		GND	
NC		—	

1.2 PROM PROGRAMMING MODE (P20/NMI = +12.5 V, $\overline{\text{RESET}}$ = L)

Pin Name	Input/Output	Function
P20/NMI	Input	PROM programming mode set
$\overline{\text{RESET}}$		
A0 to A14		Address bus
D0 to D7	Input/output	Data bus
$\overline{\text{CE}}$	Input	PROM enable input
$\overline{\text{OE}}$		Read strobe for PROM
V_{PP}	—	Write power supply
V_{DD}		Positive power supply
V_{SS}		GND
NC		—

2. DIFFERENCES BETWEEN μPD78P214 AND μPD78214

Since the μPD78P214 is a product with the μPD78214 on-chip mask ROM replaced with a rewritable EPROM, functions other than those related to EPROM, such as write/verify, are the same as those of the μPD78214. Table 2-1 shows the differences between μPD78P214 and μPD78214.

For details regarding the CPU functions and on-chip hardware, refer to the **μPD78214 Series User's Manual** and relevant manuals.

Table 2-1 Differences between μPD78P214 and μPD78214

Item	μPD78P214	μPD78214
On-chip program memory	EPROM	Mask ROM
EPROM programming pin	Yes	No
Package	• 64-pin plastic shrink DIP • 64-pin plastic QUIP • 64-pin plastic QFJ • 64-pin plastic QFP • 74-pin plastic QFP	
	• 64-pin ceramic shrink DIP (with window)*	—

* Reprogrammable.

3. PROGRAMMING

The on-chip program memory of the μPD78P214 is a 16384 × 8-bit electrically programmable PROM. For PROM programming, the PROM programming mode is set using the NMI and $\overline{\text{RESET}}$ pins.

The programming characteristics are compatible with the μPD27C256A*. However, no write is performed to addresses 4000H to 7FFFH. In a data read or verify operation, FFH is read from addresses 4000H to 7FFFH. ★

* Not applicable to a mode with a program pulse of 100μs.

Note In PROM programming, the address range of 000H to 3FFFH should be programmed. For a programmer with which address specification is impossible, be sure to write FFH to address 4000H. If data guaranteed for the μPD78P214.
The use of address 4000H is reserved by NEC for the future function expansion.

3.1 OPERATING MODE

When +6 V and +12.5 V are applied to V_{DD} pin and V_{PP} pin, respectively, the μPD78P214 is set to the program-write/ verify mode. This mode can be reset to the operating mode described in Table 3-1 by setting $\overline{\text{CE}}$ and $\overline{\text{OE}}$ pins.

In the read mode, the μPD78P214 can read the PROM contents.

Table 3-1 PROM Programming Operating Mode

Mode \ Pin	NMI	$\overline{\text{RESET}}$	$\overline{\text{CE}}$	$\overline{\text{OE}}$	V_{PP}	V_{DD}	D0 to D7
Program write	+12.5 V	L	L	H	+12.5 V	+6 V	Data input
Program verify			H	L			Data output
Program inhibit			H	H			High impedance
Read			L	L	+5 V	+5 V	Data output
Output disable			L	H			High impedance
Standby			H	L/H			High impedance

Note When V_{PP} is set to +12.5 V and V_{DD} is set to +6 V, it is inhibited to set both $\overline{\text{CE}}$ and $\overline{\text{OE}}$ to L.

3.2 PROM WRITE PROCEDURE

PROM write can be executed at high speeds using the following procedure:

(1) Fix the $\overline{\text{RESET}}$ pin to the low level. Apply +12.5 V to the NMI pin. Treat all other unused pins as shown in the pin configuration.
(2) Apply +6 V to the V_{DD} pin and +12.5 V to the V_{PP} pin.
(3) Supply the initial address.
(4) Supply write data.
(5) Supply a 1 ms program pulse (active low) to the $\overline{\text{CE}}$ pin.
(6) Set the verify mode. If data has been written, procedure to step (8). If data has not been written, repeat steps (4) to (6). If data cannot yet be written after repeating the three steps 25 times, proceed to step (7).
(7) Stop carrying out the write operation assuming that the device is defective.
(8) Supply write data and then supply (number of repetitions of steps (4) to (6): X) × 3 ms program pulses (additional write).
(9) Increment the address.
(10) Repeat steps (4) to (9) up to the final address.

The timings in steps (2) to (8) are shown in Fig. 3-1.

Fig. 3-1 PROM Write/Verify Timings

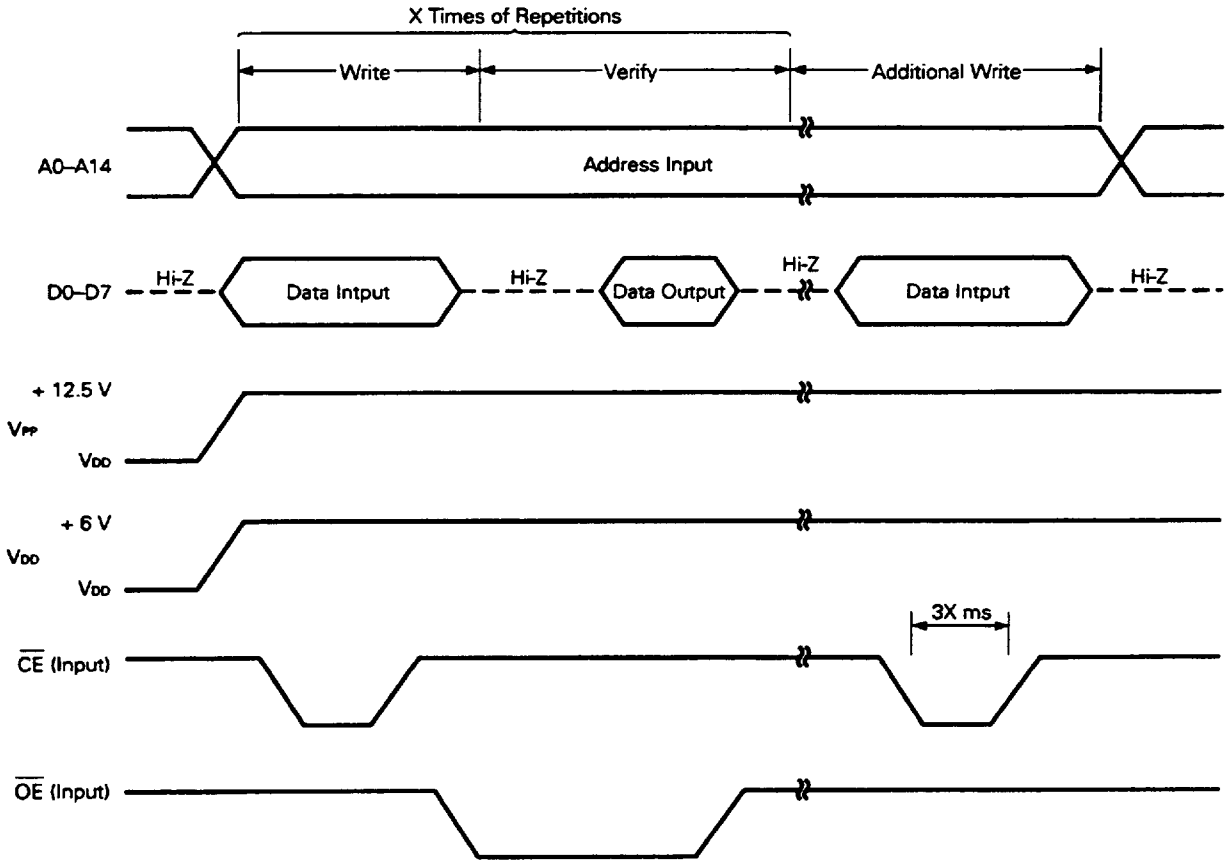
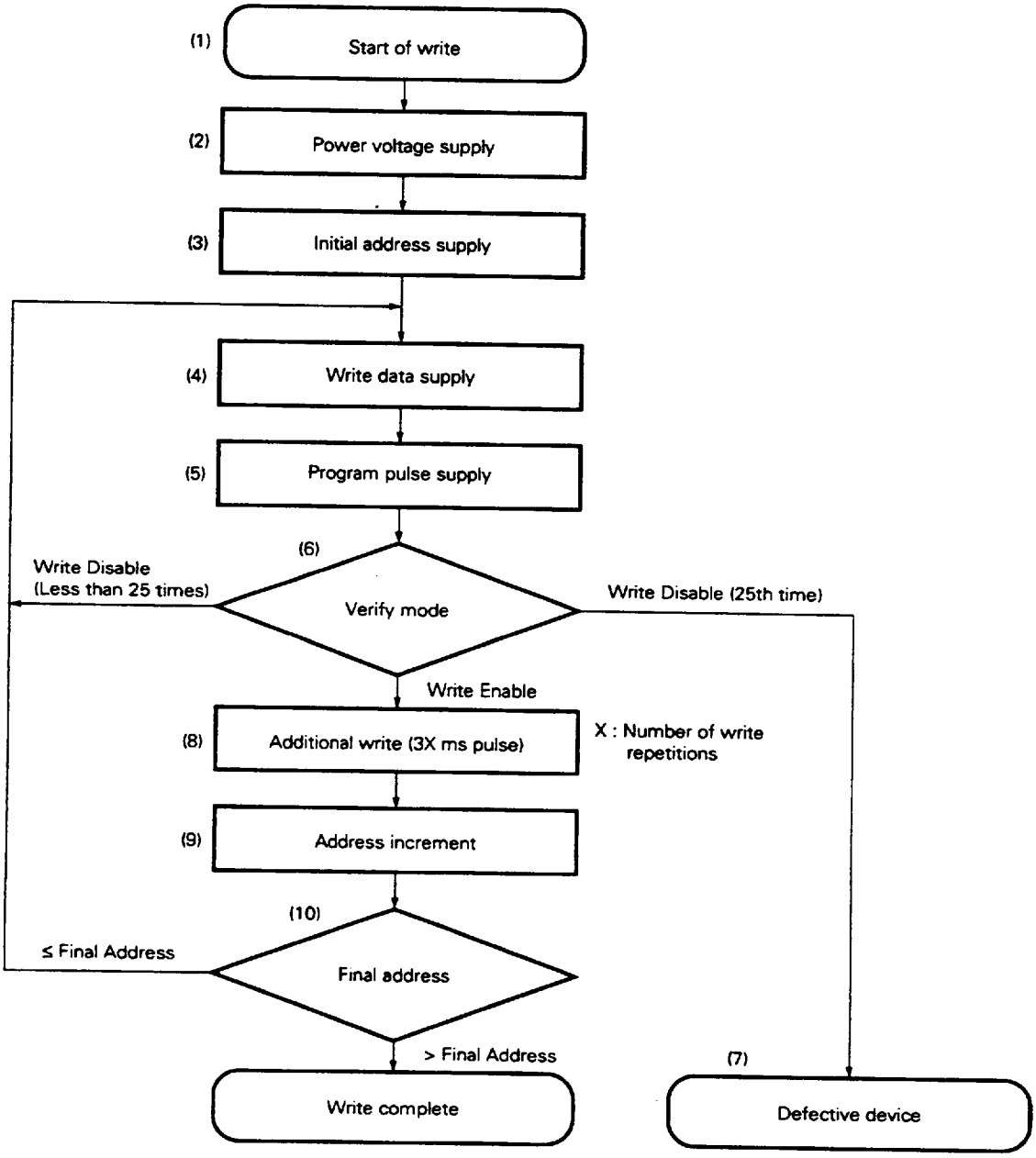


Fig. 3-2 Write Operation Flowchart



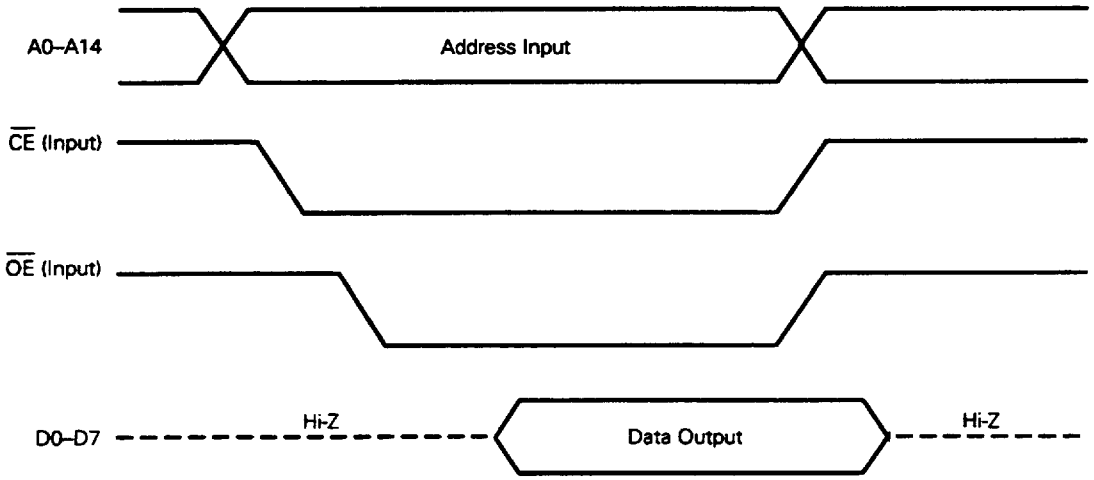
3.3 PROM READ PROCEDURE

PROM contents can be read into the external data bus (D0 to D7) using the following procedure:

(1) Fix the $\overline{\text{RESET}}$ pin to the low level. Apply +12.5 V to the NMI pin. Treat all other unused pins as shown in the pin configuration.
(2) Apply +5 V to the V_{DD} and V_{PP} pins.
(3) Input the address of the data to be read to the A0 to A14 pins.
(4) Set the read mode.
(5) Output data to the D0 to D7 pins.

The timings in steps (2) to (5) are shown in Fig. 3-3.

Fig. 3-3 PROM Read Timings



4. ERASE CHARACTERISTICS (μPD78P214DW ONLY)

The μPD78P214DW can erase the programmed data content (FFH) by applying light having wavelengths of less than about 400 nm.

To erase the μPD78P214DW program memory contents, normally apply ultraviolet rays having a wavelength of 254 nm. The total radiation required to erase the μPD78P214DW contents completely is a minimum of 15 W·s/cm² (ultraviolet strength × erase time). The erase time is approximately 15 to 20 minutes (when a 12000 μW/cm² ultraviolet lamp is used). The erase time may possible become longer due to deterioration in the performance of the ultraviolet lamp or fouling of the package window. For the erase operation, place the μPD78P214DW within 2.5 cm from the ultraviolet lamp. Use the ultraviolet lamp with the filter removed.

5. ERASE WINDOW SEALING (μPD78P214DW ONLY)

Except when erasing EPROM contents, apply a protective seal to the erase window. This is important to prevent the EPROM contents from being inadvertently erased due to light other than the erase lamp or the internal circuits other than the EPROM from malfunctioning due to light.

6. SCREENING OF ONE-TIME PROM PRODUCTS

By reason of their structure, one-time PROM products (μPD78P214CW, μPD78P214GC-AB8, μPD78P214GJ-5BJ, μPD78P214GQ-36, and μPD78P214L) cannot be fully tested by NEC prior to shipment. After the necessary data has been written, it is recommended that screening be performed for PROM verification after high-temperature storage under the following conditions.

Storage Temperature	Storage Period
125 °C	24 hrs.

Under the generic name "QTOP microcomputer", NEC offers a charged service covering one-time PROM writing, printing, screening and verification. Please consult our sales representative for details.

7. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Ta = +25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATING	UNIT
Supply voltage	V_{DD}		−0.5 to +7.0	V
	AV_{REF}		−0.5 to V_{DD} +0.5	V
	AV_{SS}		−0.5 to +0.5	V
Input voltage	V_{I1}		−0.5 to V_{DD} +0.5	V
	V_{I2}	*1	−0.5 to AV_{REF} +0.5	V
	V_{I3}	*2	−0.5 to +13.5	V
Output voltage	V_O		−0.5 to V_{DD} +0.5	V
Output current low	I_{OL}	1 pin	15	mA
		All output pins total	100	mA
Output current high	I_{OH}	1 pin	−10	mA
		All output pins total	−50	mA
Operating temperature	T_{opt}		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

* 1. 70/AN0 to P75/AN5, P66/WAIT/AN6, and P67/REFRQ/AN7 pins except for those used as A/D converter input pins and those selected by ANI0 to ANI2 bits of the ADM register when the A/D converter is not in operation. However, it is required that the V_{I1} absolute maximum rating is satisfied.

2. P20/NMI, EA/V_{PP} and P21/INTP0/A9 pins in the PROM programming mode

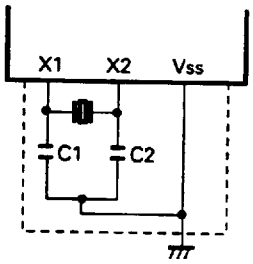
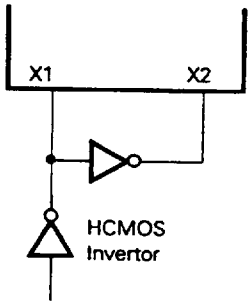
OPERATING CONDITIONS

CLOCK FREQUENCY	OPERATING TEMPERATURE (T_{opt})	SUPPLY VOLTAGE (V_{DD})
4 MHz ≤ fxx ≤ 12 MHz	−40 to +85 °C	+5.0 V ±10 %

CAPACITANCE (Ta = +25 °C, V_{DD} = V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_I	f = 1 MHz unmeasured pins returned to 0 V.			20	pF
Output capacitance	C_O				20	pF
I/O capacitance	C_{IO}				20	pF

OSCILLATOR CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	MIN.	MAX.	Unit
Ceramic resonator or crystal resonator		Oscillator frequency (f_{XX})	4	12	MHz
External clock		X1 input frequency (f_X)	4	12	MHz
		X1 input rising/falling time (t_{XR}, t_{XF})	0	30	ns
		X1 input high/low level width (t_{WXH}, t_{WXL})	30	130	ns

Note When using the clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- Wiring should be as short as possible.
- Wiring should not cross other signal lines.
- Wiring should be placed close to a varying high current.
- The potential of the oscillator capacitor ground should be the same as Vss. Do not ground pattern in which a high current flows.
- Do not fetch a signal from the oscillator.

RECOMMENDED OSCILLATION CIRCUIT CONSTANTS

CERAMIC RESONATOR

MANUFACTURER	FREQUENCY [MHz]	PRODUCT NAME	RECOMMENDED CONSTANTS	
			C1 [pF]	C2 [pF]
Murata Mfg. Co., Ltd.	12	CSA12.0MT	30	30
		CST12.0MT	Capacitor on-chip type	
	4	CSA4.00MG040	100	100
		CST4.00MG040	Capacitor on-chip type	
Kyocera Corporation	12	KBR12.0M	33	33

CRYSTAL RESONATOR

MANUFACTURER	FREQUENCY [MHz]	PRODUCT NAME	RECOMMENDED CONSTANTS	
			C1 [pF]	C2 [pF]
Kinseki, Ltd.	12	HC-49/U	18	18

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input voltage low	V_{IL}		0		0.8	V
Input voltage high	V_{IH1}	Pins except for *1 and *2	2.2		V_{DD}	V
	V_{IH2}	Pin of *1	2.2		AV_{REF}	V
	V_{IH3}	Pin of *2	0.8V_{DD}		V_{DD}	V
Output voltage low	V_{OL1}	I_{OL} = 2.0 mA			0.45	V
	V_{OL2}	I_{OL} = 8.0 mA *3			1.0	V
Output voltage high	V_{OH1}	I_{OH} = –1.0 mA	V_{DD}–1.0			V
	V_{OH2}	I_{OH} = –100 μA	V_{DD}–0.5			V
	V_{OH3}	I_{OH} = –5.0 mA *4	2.0			V
X1 input current low	I_{IL}	0 V ≤ V_I ≤ V_{IL}			–100	μA
X1 input current high	I_{IH}	V_{IH3} ≤ V_I ≤ V_{DD}			100	μA
Input leakage current	I_{LI}	0 V ≤ V_I ≤ V_{DD}			±10	μA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}			±10	μA
AV_{REF} current	AI_{REF}	Operating mode f_{XX} = 12 MHz		1.5	5.0	mA
V_{DD} supply current	I_{DD1}	Operating mode f_{XX} = 12 MHz		20	40	mA
	I_{DD2}	HALT mode f_{XX} = 12 MHz		7	20	mA
Data retention voltage	V_{DDDR}	STOP mode	2.5		5.5	V
Data retention current	I_{DDDR}	STOP mode V_{DDDR} = 2.5 V		2	20	μA
		STOP mode V_{DDDR} = 5 V ±10 %		5	50	μA
Pull-up resistor	R_L	V_I = 0 V	15	40	80	kΩ

* 1. P70/AN0 to P75/AN5, P66/$\overline{WAIT}$/AN6, and P67/$\overline{REFRQ}$/AN7 pins except for those used as A/D converter input pins and those selected by ANI0 to ANI2 bits of the ADM register when the A/D converter is not in operation.

2. X1, X2, $\overline{RESET}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK, P26/INTP5, P27/SI, P32/$\overline{SCK}$, P33/SO/SB0, $\overline{EA}$ pins
3. P40/AD0 to P47/AD7, P50/A8 to P57/A15 pins
4. P00 to P07 pins

AC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

READ/WRITE OPERATION (1/2)

	PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
	X1 input clock cycle time	t_{CYX}		82	250	ns
	Address set-up time (to ASTB↓)	t_{SAST} •		52		ns
	Address hold time (from ASTB↓) *	t_{HSTA}		25		ns
	Address hold time (from $\overline{RD}$↑)	t_{HRA}		30		ns
	Address hold time (from $\overline{WR}$↑)	t_{HWA}		30		ns
	$\overline{RD}$↓ delay time from address	t_{DAR} •		129		ns
	Address float time (from $\overline{RD}$↓)	t_{FAR} •		11		ns
	Data input time from address	t_{DAID} •	Number of waits = 0		228	ns
	Data input time from ASTB↓	t_{DSTID} •	Number of waits = 0		181	ns
	Data input time from $\overline{RD}$↓	t_{DRID} •	Number of waits = 0		100	ns
	$\overline{RD}$↓ delay time from ASTB↓	t_{DSTR} •		52		ns
	Data hold time (from $\overline{RD}$↑)	t_{HRID}		0		ns
	Address active time from $\overline{RD}$↑	t_{DRA} •		124		ns
	ASTB↑ delay time from $\overline{RD}$↑	t_{DRST} •		124		ns
	$\overline{RD}$ low-level width	t_{WRL} •	Number of waits = 0	124		ns
	ASTB high-level width	t_{WSTH} •		52		ns
	$\overline{WR}$↓ delay time from address	t_{DAW} •		129		ns
	Data output time from ASTB↓	t_{DSTOD} •			142	ns
	Data output time from $\overline{WR}$↓	t_{DWOD}			60	ns
★	$\overline{WR}$↓ delay time from ASTB↓	t_{DSTW1} •	With refreshing desabled	52		ns
		t_{DSTW2} •	With refreshing enabled	129		ns
	Data set-up time (to $\overline{WR}$↑)	t_{SODWR} •	Number of waits = 0	146		ns
	Data set-up time (to $\overline{WR}$↓)	t_{SODWF} •	With refreshing enabled	22		ns
	Data hold time (from $\overline{WR}$↑) *	t_{HWOD}		20		ns
	ASTB↑ delay time from $\overline{WR}$↑	t_{DWST} •		42		ns
★	$\overline{WR}$ low-level width	t_{WWL1} •	With refreshing desabled Number of waits = 0	196		ns
		t_{WWL2} •	With refreshing enabled Number of waits = 0	114		ns
	$\overline{WAIT}$↓ input time from address	t_{DAWT} •			146	ns
	$\overline{WAIT}$↓ input time from ASTB↓	t_{DSTWT} •			84	ns

* The hold time includes the time to hold the V_{OH} and V_{OL} under the load conditions of C_L = 100 pF and R_L = 2 kΩ.

Remarks 1. The values in the above table are based on "f_{XX} = 12 MHz and C_L = 100 pF".
2. For a parameter with a dot(•) in the SYMBOL column, refer to "t_{CYX} **DEPENDENT BUS TIMING DEFINITION**" as well.

READ/WRITE OPERATION (2/2)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
$\overline{WAIT}$ hold time from ASTB↓		t_{HSTWT} •	No. of external waits = 1	174		ns
$\overline{WAIT}$↑ delay time from ASTB↓		t_{DSTWTH} •	No. of external waits = 1		273	ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓		t_{DRWTL} •			22	ns
$\overline{WAIT}$ hold time from $\overline{RD}$↓		t_{HRWT} •	No. of external waits = 1	87		ns
$\overline{WAIT}$↑ delay time from $\overline{RD}$↓		t_{DRWTH} •	No. of external waits = 1		186	ns
Data input time from $\overline{WAIT}$↑		t_{DWTID} •			62	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑		t_{DWTW} •		154		ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑		t_{DWTR} •		72		ns
$\overline{WAIT}$ input time from $\overline{WR}$↓ (At refresh disabled)		t_{DWWTL} •			22	ns
$\overline{WAIT}$ hold time from $\overline{WR}$↓	Refresh disabled	t_{HWWT1} •	No. of external waits = 1	87		ns
	Refresh enabled	t_{HWWT2} •	No. of external waits = 1	5		ns
$\overline{WAIT}$↑ delay time from $\overline{WR}$↓	Refresh disabled	t_{DWWTH1} •	No. of external waits = 1		186	ns
	Refresh enabled	t_{DWWTH2} •	No. of external waits = 1		104	ns
$\overline{REFRQ}$↓ delay time from $\overline{RD}$↑		t_{DRRFQ} •		154		ns
$\overline{REFRQ}$↓ delay time from $\overline{WR}$↑		t_{DWRFQ} •		72		ns
$\overline{REFRQ}$ low-level width		t_{WRFQL} •		120		ns
ASTB↑ delay time from $\overline{REFRQ}$↑		t_{DRFQST} •		280		ns

Remarks 1. The values in the above table are based on "fxx = 12 MHz and C_L = 100 pF".

2. For a parameter with a dot(•) in the SYMBOL column, refer to "t_{CYX} **DEPENDENT BUS TIMING DEFINITION** " as well.

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	MAX.	UNIT
Serial clock cycle time	t_{CYSK}	Input	External clock	1.0		μs
		Output	Internal divided by 16	1.3		μs
			Internal divided by 64	5.3		μs
Serial clock low-level width	t_{WSKL}	Input	External clock	420		ns
		Output	Internal divided by 16	556		ns
			Internal divided by 64	2.5		μs
Serial clock high-level width	t_{WSKH}	Input	External clock	420		ns
		Output	Internal divided by 16	556		ns
			Internal divided by 64	2.5		μs
SI, SB0 set-up time (to $\overline{SCK}\uparrow$)	t_{SSSK}			150		ns
SI, SB0 hold time (from $\overline{SCK}\uparrow$)	t_{HSSK}			400		ns
SO/SB0 output delay time (from $\overline{SCK}\downarrow$)	t_{DSSSK1}	CMOS push-pull output (3-wire serial I/O mode)		0	300	ns
	t_{DSSSK2}	Open-drain output (SBI mode), R_L = 1 kΩ		0	800	ns
SB0 high hold time (from $\overline{SCK}\uparrow$)	t_{HSSSK}	SBI mode		4		t_{CYX}
SB0 low set-up time (to $\overline{SCK}\downarrow$)	t_{SSSSK}			4		t_{CYX}
SB0 low-level width	t_{WSSL}			4		t_{CYX}
SB0 high-level width	t_{WSSH}			4		t_{CYX}

Remarks The values in the above table are based on "f_{XX} = 12 MHz and C_L = 100 pF".

OTHER OPERATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
NMI low-level width	t_{WNIL}		10		μs
NMI high-level width	t_{WNIH}		10		μs
INTP0 to INTP5 low-level width	t_{WITL}		24		t_{CYX}
INTP0 to INTP5 high-level width	t_{WITH}		24		t_{CYX}
$\overline{\text{RESET}}$ low-level width	t_{WRSL}		10		μs
$\overline{\text{RESET}}$ high-level width	t_{WRSH}		10		μs

EXTERNAL CLOCK TIMING

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
X1 input low-level width	t_{WXL}		30	130	ns
X1 input high-level width	t_{WXH}		30	130	ns
X1 input rise time	t_{XR}		0	30	ns
X1 input fall time	t_{XF}		0	30	ns
X1 input clock cycle time	t_{CYX}		82	250	ns

A/D CONVERTER CHARACTERISTICS (Ta = −40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = AV_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Resolution			8			bit
Overall error*		4.0 V ≤ AV_{REF} ≤ V_{DD} Ta = −10 to +70 °C			0.4	%
		3.4 V ≤ AV_{REF} ≤ V_{DD} Ta = −10 to +70 °C			0.8	%
		4.0 V ≤ AV_{REF} ≤ V_{DD}			0.8	%
Quantization error					±1/2	LSB
Conversion time	t_{CONV}	82 ns ≤ t_{CYX} < 125 ns (The FR bit of ADM is to be "0")	360			t_{CYX}
		125 ns ≤ t_{CYX} ≤ 250 ns (The FR bit of ADM is to be "1")	240			t_{CYX}
Sampling time	t_{SAMP}	82 ns ≤ t_{CYX} < 125 ns (The FR bit of ADM is to be "0")	72			t_{CYX}
		125 ns ≤ t_{CYX} ≤ 250 ns (The FR bit of ADM is to be "1")	48			t_{CYX}
Analog input voltage	V_{IAN}		−0.3		AV_{REF} +0.3	V
Analog input impedance	R_{AN}			1000		MΩ
Reference voltage	AV_{REF}		3.4		V_{DD}	V
AV_{REF} current	AI_{REF}	f_{XX} = 12 MHz		1.5	5.0	mA
		STOP mode		0.2	1.5	mA

* Quantization error is not included. Represented by the ratio to full-scale value.

t_{CYX} DEPENDENT BUS TIMING DEFINITION (1/2)

	PARAMETER	SYMBOL	CALCULATION FORMULA	MIN./MAX.	12 MHZ	UNIT
	X1 input clock cycle time	t_{CYX}		MIN.	82	ns
	Address set-up time (to ASTB↓)	t_{SAST}	t_{CYX} – 30	MIN.	52	ns
	$\overline{RD}$↓ delay time from address	t_{DAR}	2t_{CYX} – 35	MIN.	129	ns
	Address float time (from $\overline{RD}$↓)	t_{FAR}	t_{CYX}/2 – 30	MIN.	11	ns
	Data input time from address	t_{DAID}	(4 + 2n) t_{CYX} – 100	MAX.	228*	ns
	Data input time from ASTB↓	t_{DSTID}	(3 + 2n) t_{CYX} – 65	MAX.	181*	ns
	Data input time from $\overline{RD}$↓	t_{DRID}	(2 + 2n) t_{CYX} – 64	MAX.	100*	ns
	$\overline{RD}$↓ delay time from ASTB↓	t_{DSTR}	t_{CYX} – 30	MIN.	52	ns
	Address active time from $\overline{RD}$↑	t_{DRA}	2t_{CYX} – 40	MIN.	124	ns
	ASTB↑ delay time from $\overline{RD}$↑	t_{DRST}	2t_{CYX} – 40	MIN.	124	ns
	$\overline{RD}$ low-level width	t_{WRL}	(2 + 2n) t_{CYX} – 40	MIN.	124*	ns
	ASTB high-level width	t_{WSTH}	t_{CYX} – 30	MIN.	52	ns
	$\overline{WR}$↓ delay time from address	t_{DAW}	2t_{CYX} – 35	MIN.	129	ns
	Data output time from ASTB↓	t_{DSTOD}	t_{CYX} + 60	MAX.	142	ns
★	$\overline{WR}$↓ delay time from ASTB↓	t_{DSTW1}	t_{CYX} – 30 (With refreshing disabled)	MIN.	52	ns
		t_{DSTW2}	2t_{CYX} – 35 (With refreshing enabled)	MIN.	129	ns
	Data set-up time (to $\overline{WR}$↑)	t_{SODWR}	(3 + 2n) t_{CYX} – 100	MIN.	146*	ns
	Data set-up time (to $\overline{WR}$↓)	t_{SODWF}	t_{CYX} – 60 (With refreshing enabled)	MIN.	22	ns
	ASTB↑ delay time from $\overline{WR}$↑	t_{DWST}	t_{CYX} – 40	MIN.	42	ns
★	$\overline{WR}$ low-level width	t_{WWL1}	(3 + 2n) t_{CYX} – 50 (With refreshing disabled)	MIN.	196*	ns
		t_{WWL2}	(2 + 2n) t_{CYX} – 50 (With refreshing enabled)	MIN.	114*	ns
	$\overline{WAIT}$↓ input time from address	t_{DAWT}	3t_{CYX} – 100	MAX.	146	ns
	$\overline{WAIT}$↓ input time from ASTB↓	t_{DSTWT}	2t_{CYX} – 80	MAX.	84	ns

Remarks "n" indicates the number of waits.

* When n = 0

t_{CYX} DEPENDENT BUS TIMING DEFINITION (2/2)

PARAMETER		SYMBOL	CALCULATION FORMULA	MIN./MAX.	12 MHZ	UNIT
$\overline{WAIT}$ hold time from ASTB↓		t_{HSTWT}	2Xt_{CYX} + 10	MIN.	174*	ns
$\overline{WAIT}$↑ delay time from ASTB↓		t_{DSTWTH}	2(1 + X)t_{CYX} – 55	MAX.	273*	ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓		t_{DRWTL}	t_{CYX} – 60	MAX.	22	ns
$\overline{WAIT}$ hold time from $\overline{RD}$↓		t_{HRWT}	(2X – 1)t_{CYX} + 5	MIN.	87*	ns
$\overline{WAIT}$↑ delay time from $\overline{RD}$↓		t_{DRWTH}	(2X + 1)t_{CYX} – 60	MAX.	186*	ns
Data input time from $\overline{WAIT}$↑		t_{DWTID}	t_{CYX} – 20	MAX.	62	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑		t_{DWTW}	2t_{CYX} – 10	MIN.	154	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑		t_{DWTR}	t_{CYX} – 10	MIN.	72	ns
$\overline{WAIT}$ input time from $\overline{WR}$↓ (At refresh disabled)		t_{DWWTL}	t_{CYX} – 60	MAX.	22	ns
$\overline{WAIT}$ hold time from $\overline{WR}$↓	Refresh disabled	t_{HWWT1}	(2X – 1)t_{CYX} + 5	MIN.	87*	ns
	Refresh enabled	t_{HWWT2}	2(X – 1)t_{CYX} + 5	MIN.	5*	ns
$\overline{WAIT}$↑ delay time from $\overline{WR}$↓	Refresh disabled	t_{DWWTH1}	(2X + 1)t_{CYX} – 60	MAX.	186*	ns
	Refresh enabled	t_{DWWTH2}	2Xt_{CYX} – 60	MAX.	104*	ns
$\overline{REFRQ}$↓ delay time from $\overline{RD}$↑		t_{DRRFQ}	2t_{CYX} – 10	MIN.	154	ns
$\overline{REFRQ}$↓ delay time from $\overline{WR}$↑		t_{DWRFQ}	t_{CYX} – 10	MIN.	72	ns
$\overline{REFRQ}$ low-level width		t_{WRFQL}	2t_{CYX} – 44	MIN.	120	ns
ASTB↑ delay time from $\overline{REFRQ}$↑		t_{DRFQST}	4t_{CYX} – 48	MIN.	280	ns

Remarks 1. X : The number of the external wait. (1, 2, ...)
2. $t_{CYX} \equiv 82$ ns (f_{XX} = 12 MHz)

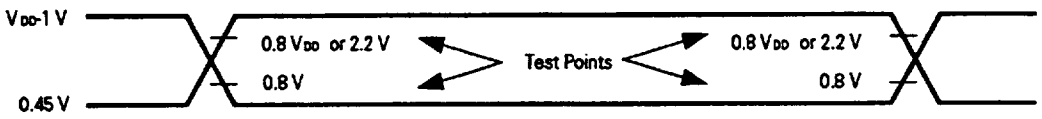
* When X = 1

DATA RETENTION CHARACTERISTICS (Ta = –40 to +85 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention voltage	V_{DDDR}	STOP mode	2.5		5.5	V
Data retention current	I_{DDDR}	V_{DDDR} = 2.5 V		2	20	μA
		V_{DDDR} = 5 V ±10 %		5	50	μA
V_{DD} rise time	t_{RVD}		200			μs
V_{DD} fall time	t_{FVD}		200			μs
V_{DD} hold time (from STOP mode setting)	t_{HVD}		0			ms
STOP release signal input time	t_{DREL}		0			ms
Oscillation stabilization wait time	t_{WAIT}	Crystal resonator	30			ms
		Ceramic resonator	5			ms
Low-level input voltage	V_{IL}	Specified pin*	0		0.1 V_{DDDR}	V
High-level input voltage	V_{IH}		0.9 V_{DDDR}		V_{DDDR}	V

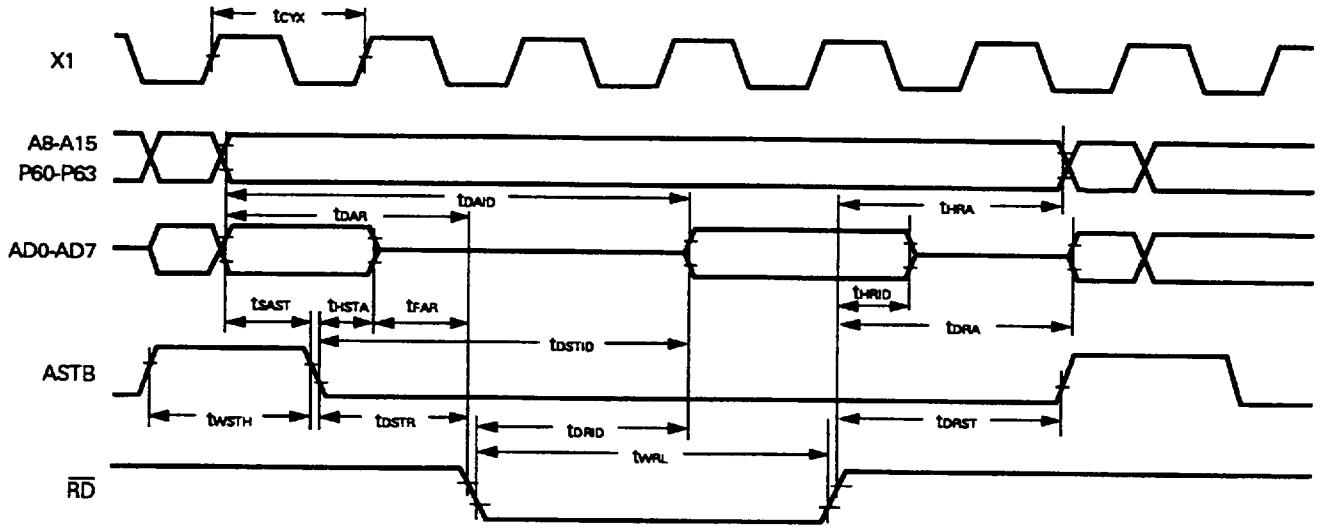
* $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK, P26/INTP5, P27/SI, $\overline{\text{P32}}$/SCK, P33/SO/$\overline{\text{SB0}}$ EA pins

AC Timing Test Point

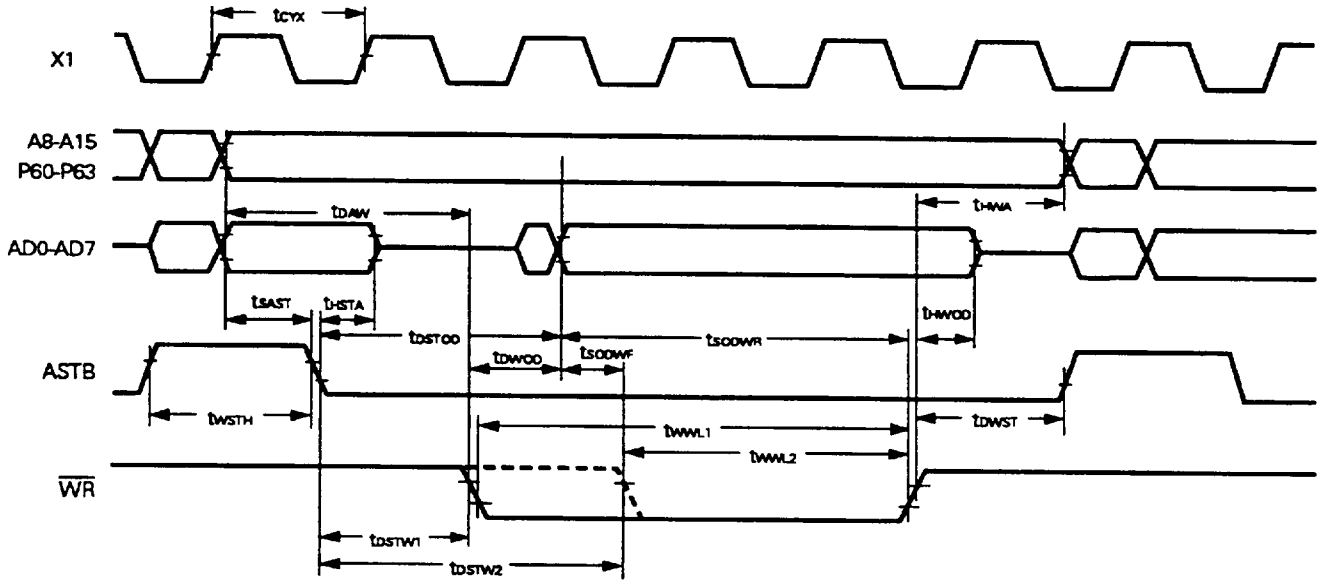


Timing Waveform ★

Read operation

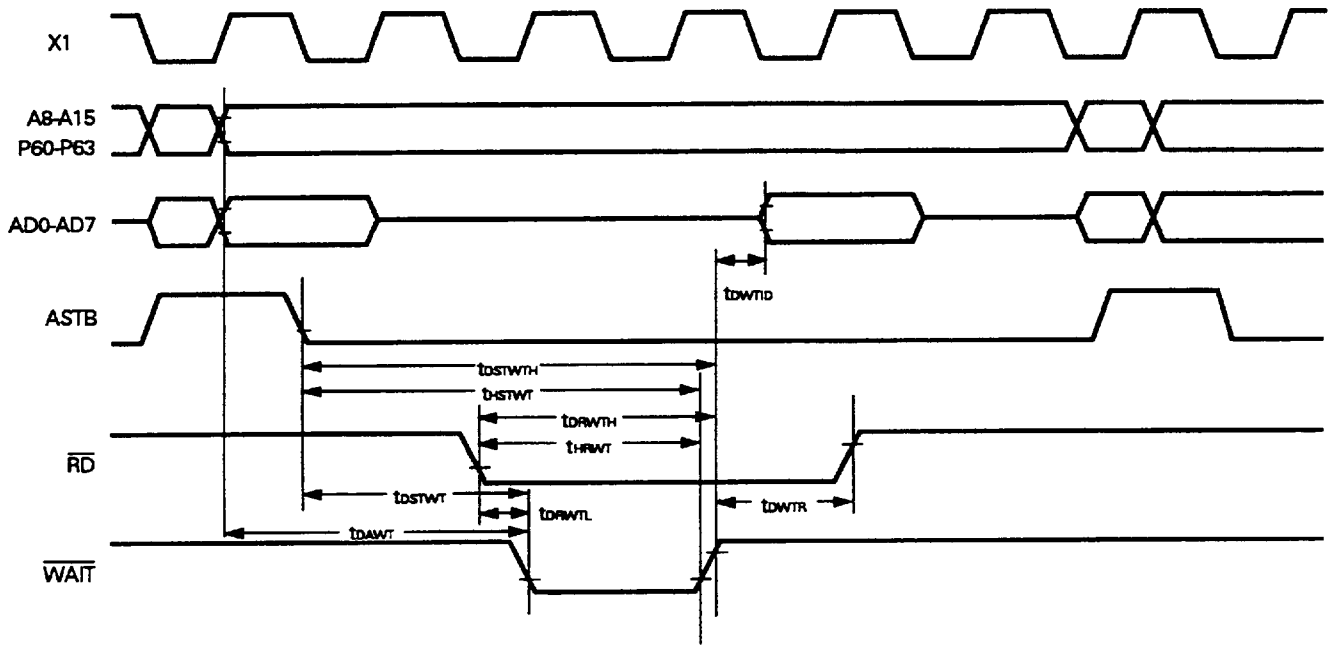


Write operation

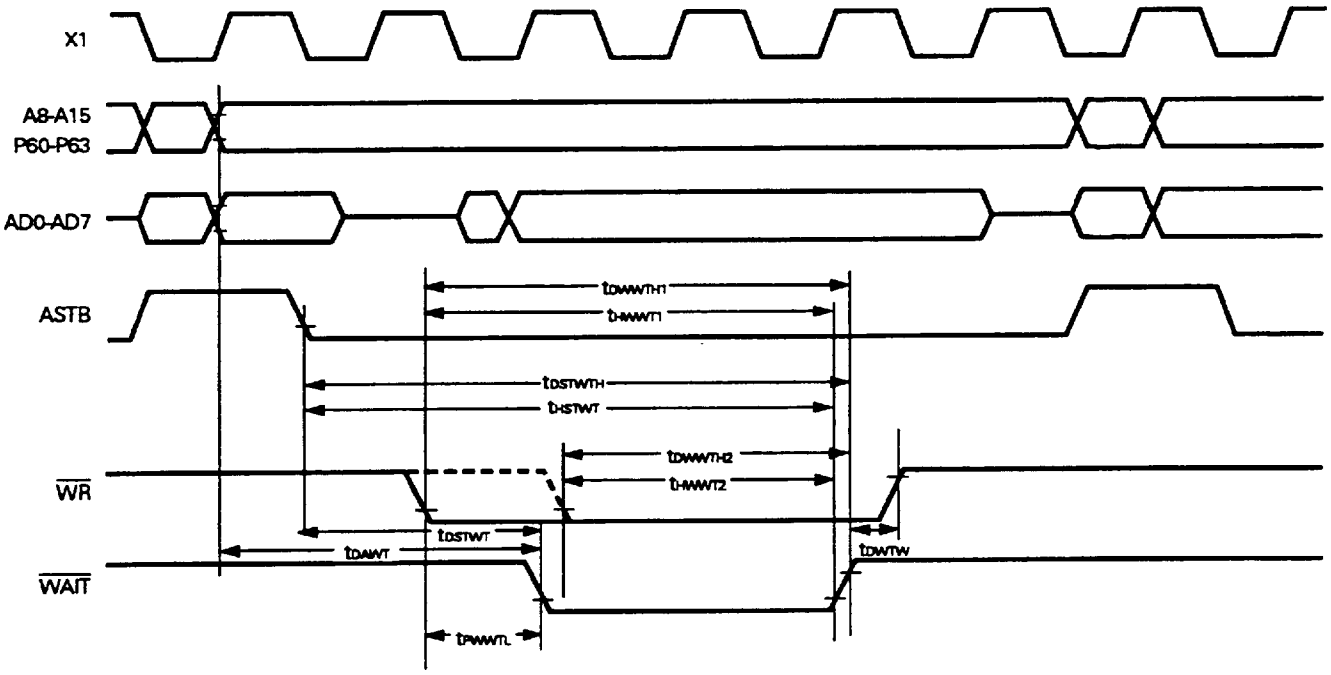


External WAIT Signal Input Timing

Read operation

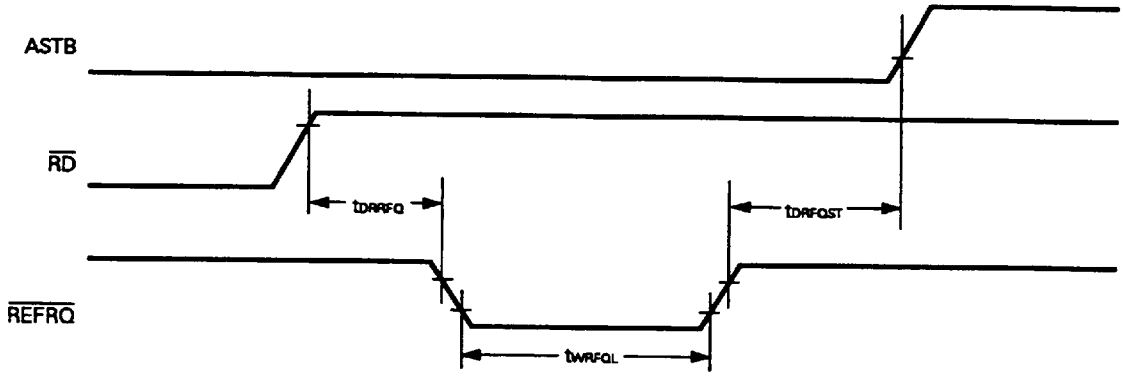


Write operation

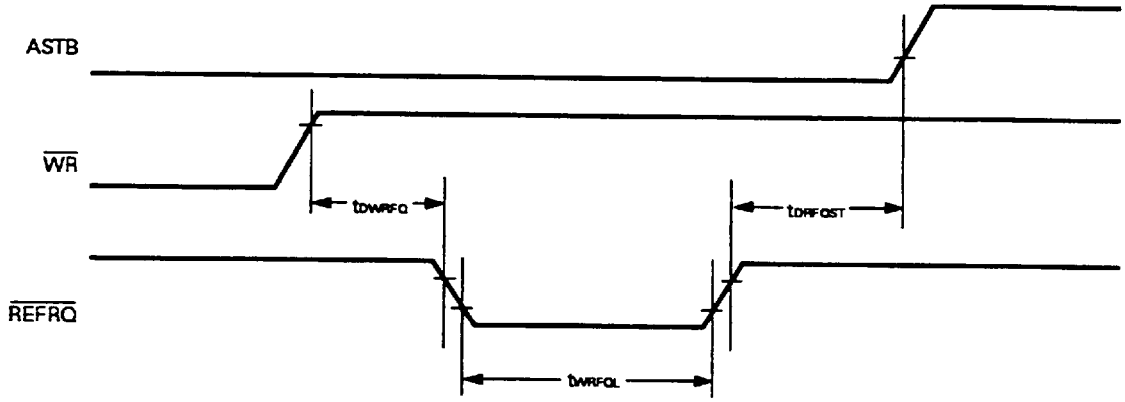


Refresh Timing Waveform

Refresh after read

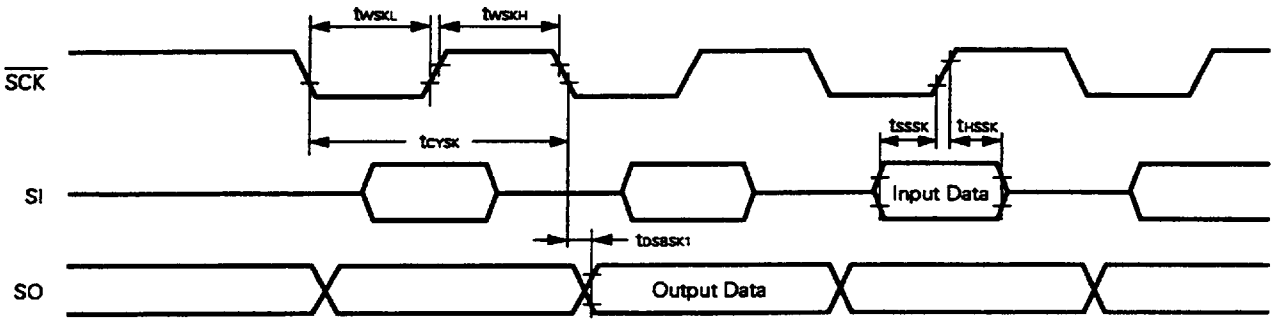


Refresh after write



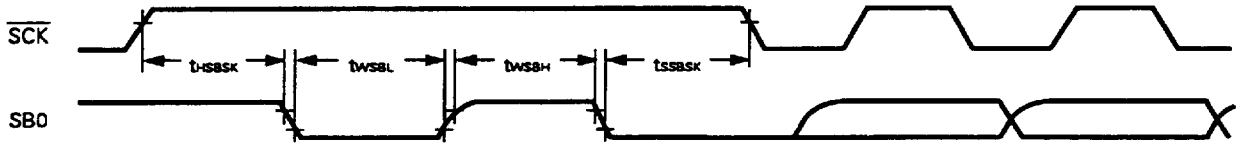
Serial Operation

3-wire serial I/O mode

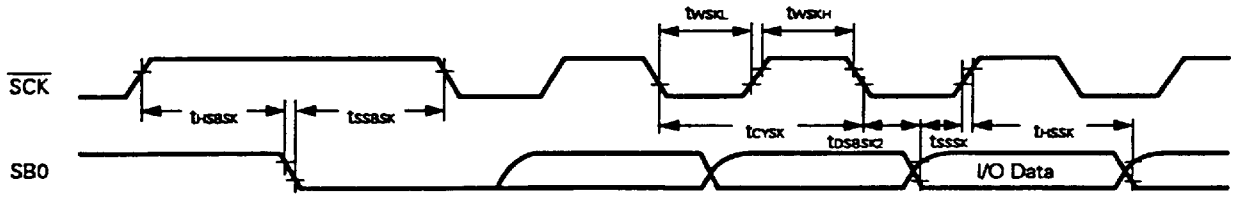


SBI Mode

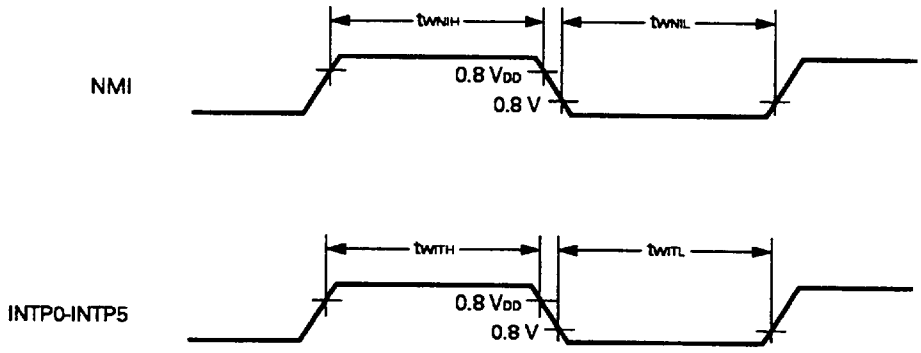
Bus release signal transfer



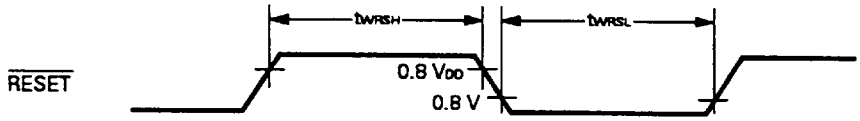
Command signal transfer



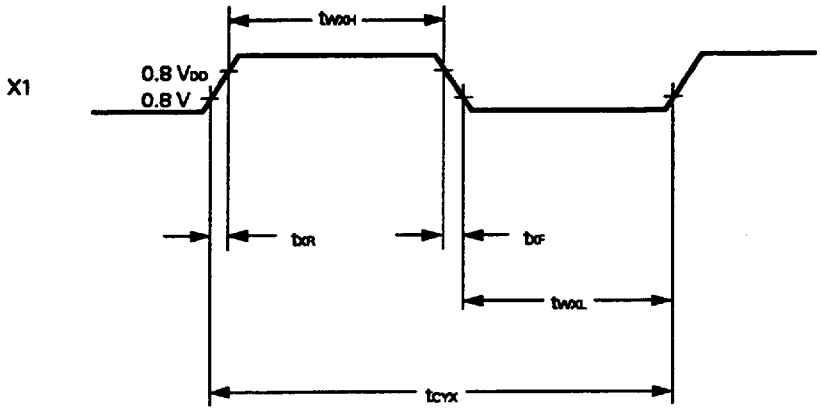
Interrupt Input Timing



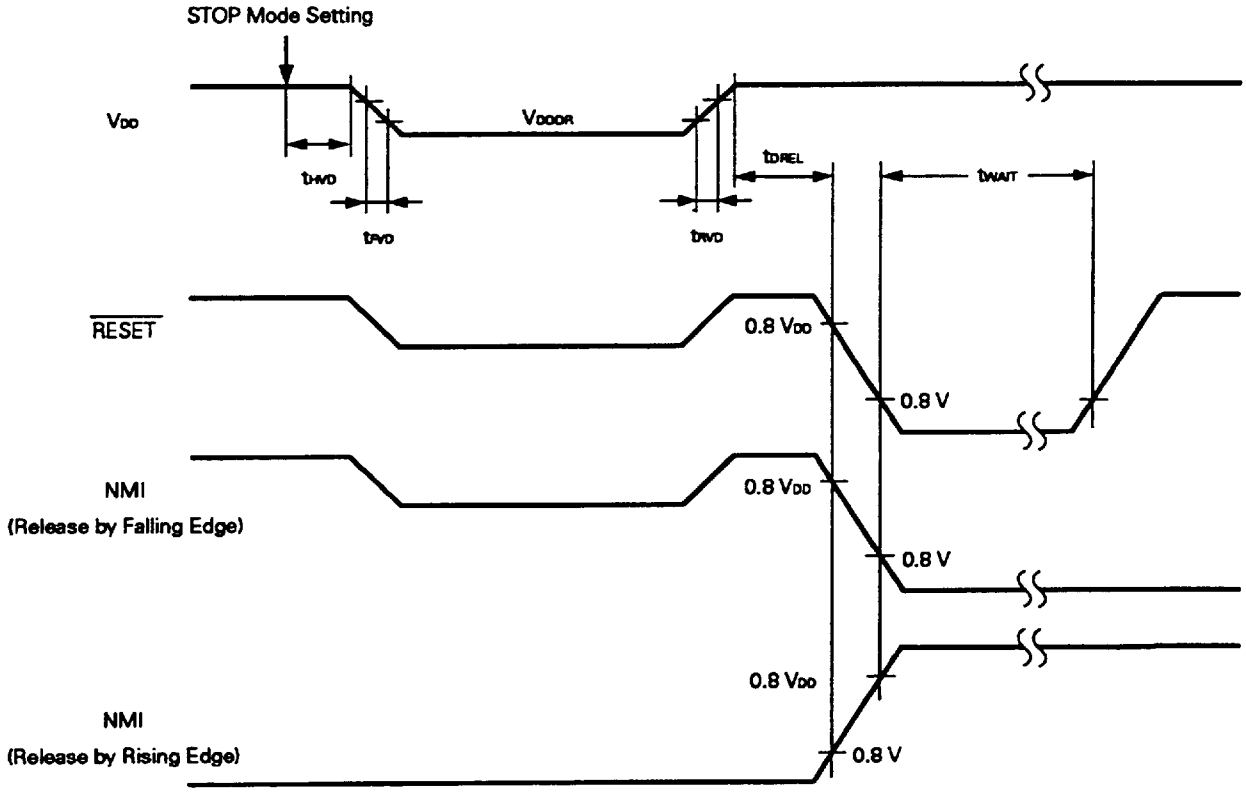
Reset Input Timing



External Clock Timing



Data Retention Characteristics



DC PROGRAMMING CHARACTERISTICS (T_a = 25 ±5 °C, V_{PP} *1= 12.5 ±0.5 V, V_{SS} = 0 V)

PARAMETER	SYMBOL	SYMBOL*2	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input voltage high	V_{IH}	V_{IH}		2.4		V_{DDP}+0.3	V
Input voltage low	V_{IL}	V_{IL}		−0.3		0.8	V
Input leakage current	I_{LIP}	I_{LI}	$0 \le V_I \le V_{DDP}$			10	μA
Output voltage high	V_{OH1}	V_{OH1}	I_{OH} = −400 μA	2.4			V
	V_{OH2}	V_{OH2}	I_{OH} = −100 μA	V_{DD}−0.7			V
Output voltage low	V_{OL}	V_{OL}	I_{OH} = 2.1 mA			0.45	V
Output leakage current	I_{LO}		$0 \le V_O \le V_{DDP}$, $\overline{OE}$ = V_{IH}			10	μA
NMI pin high-voltage input current	I_{IP}					±10	μA
V_{DDP} power supply voltage	V_{DDP}	V_{CC}	Program memory write mode	5.75	6.0	6.25	V
			Program memory read mode	4.5	5.0	5.5	V
V_{PP} power supply voltage	V_{PP}	V_{PP}	Program memory write mode	12.2	12.5	12.8	V
			Program memory read mode	V_{PP} = V_{DDP}			V
V_{DDP} power supply current	I_{DD}	I_{CC}	Program memory write mode		5	30	mA
			Program memory read mode $\overline{CE}$ = V_{IL}, V_I = V_{IH}		5	30	mA
V_{PP} power supply current	I_{PP}	I_{PP}	Program memory write mode $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		5	30	mA
			Program memory read mode		1	100	μA

* 1. Voltage applied to P20/NMI pin
2. Symbol of the corresponding μPD27C256A

PROGRAM OPERATION

AC CHARACTERISTICS (T_a = 25 ±5 °C, V_{IP} *1 = 12.5 ±0.5 V, V_{DD} = 6 ±0.25 V, V_{PP} = 12.5 ±0.3 V, V_{SS} = 0 V)

PARAMETER	SYMBOL	SYMBOL*2	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Address set-up time (to $\overline{CE}\downarrow$)	t_{SAC}	t_{AS}		2			μs
$\overline{OE}$ hold time (from input data disable)	t_{DDOO}	t_{OES}		2			μs
Input data set-up time (to $\overline{CE}\downarrow$)	t_{SIDC}	t_{DS}		2			μs
Address hold time (from $\overline{CE}\uparrow$)	t_{HCA}	t_{AH}		2			μs
Input data hold time (from $\overline{CE}\uparrow$)	t_{HCID}	t_{DH}		2			μs
Output data hold time (from $\overline{OE}\uparrow$)	t_{HOOD}	t_{DF}		0		130	ns
V_{PP} set-up time (to $\overline{CE}\downarrow$)	t_{SVPC}	t_{VPS}		1			ms
V_{DDP} se-tup time (to $\overline{CE}\downarrow$)	t_{SVDC}	t_{VCS}		1			ms
Initial program puls width	t_{WL1}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{WL2}	t_{OPW}		2.85		78.75	ms
NMI high-voltage input set-up time (to $\overline{CE}\downarrow$)	t_{SPC}			2			μs
Data output time from $\overline{OE}\downarrow$	t_{DOOD}	t_{OE}				150	ns

* 1. Voltage applied to P20/NMI pin
2. Symbol of the corresponding μPD27C256A

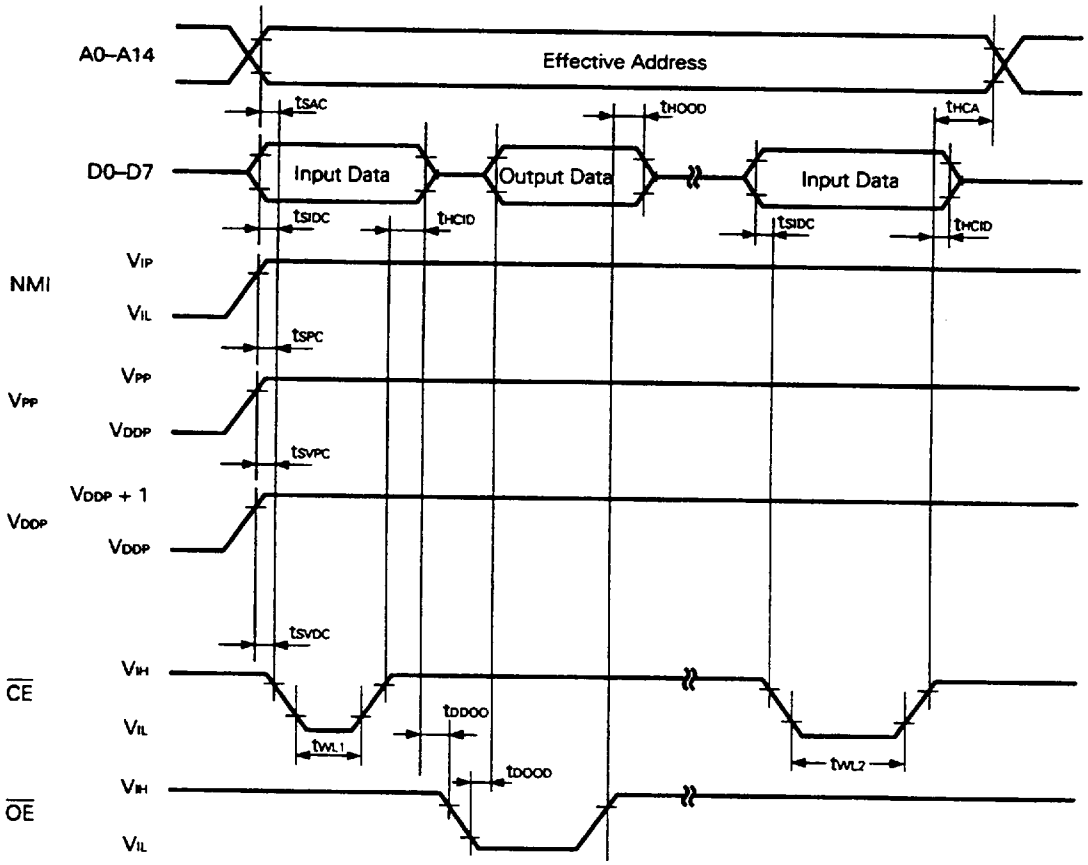
READ OPERATION

AC CHARACTERISTICS (T_a = 25 ±5 °C, V_{IP} *1 = 12.5 V, V_{DD} = 5 ±0.5 V, V_{PP} = V_{DDP}, V_{SS} = 0 V)

PARAMETER	SYMBOL	SYMBOL*2	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Address data output time	t_{DAOD}	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			200	ns
Data output time from $\overline{CE}\downarrow$	t_{DCOD}	t_{CE}	$\overline{OE}$ = V_{IL}			200	ns
Data output time from $\overline{OE}\downarrow$	t_{DOOD}	t_{OE}	$\overline{CE}$ = V_{IL}			75	ns
★ Data hold time (from $\overline{OE}\uparrow$,$\overline{CE}\uparrow$)*3	t_{HCOD}	t_{DF}	$\overline{CE}$ = V_{IL} or $\overline{OE}$ = V_{IL}	0		60	ns
Data hold time (from address)	t_{HAOD}	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0			ns

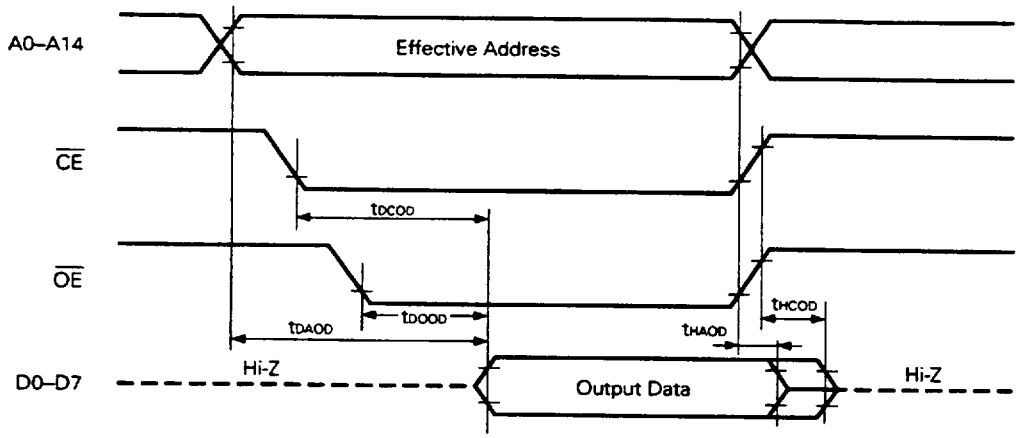
* 1. Voltage applied to P20/NMI pin
2. Symbol of the corresponding μPD27C256A
3. t_{HCOD} is the time counted from when either $\overline{OE}$ or $\overline{CE}$ becomes V_{IH}.

PROM Write Mode Timing



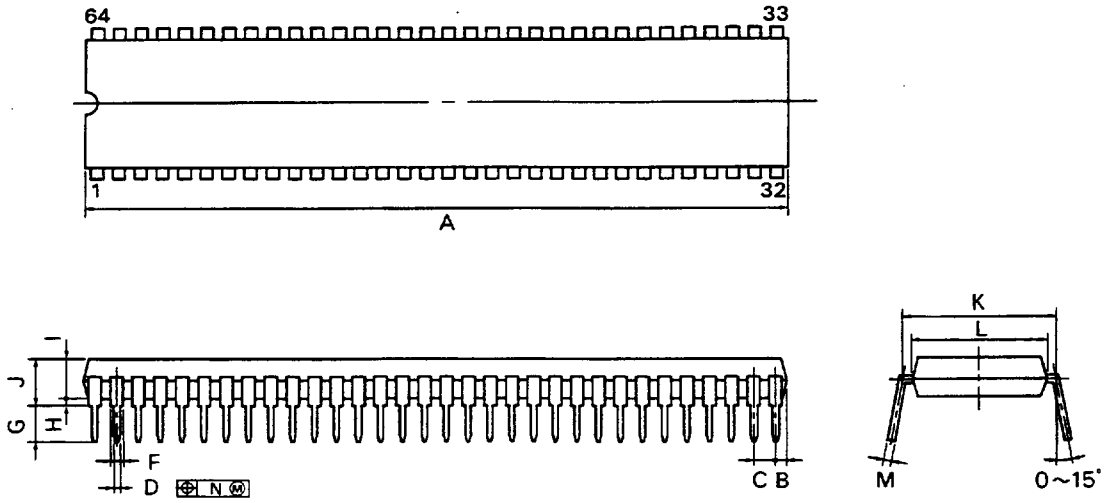
Note 1. **Apply V_{DDP} before V_{PP} and shut it off after V_{PP}.**
2. **Do not allow V_{PP} to become +13 V or more including an overshoot.**

PROM Read Mode Timing



8. PACKAGE INFORMATION

64PIN PLASTIC SHRINK DIP (750 mil)



P64C-70-750A,C

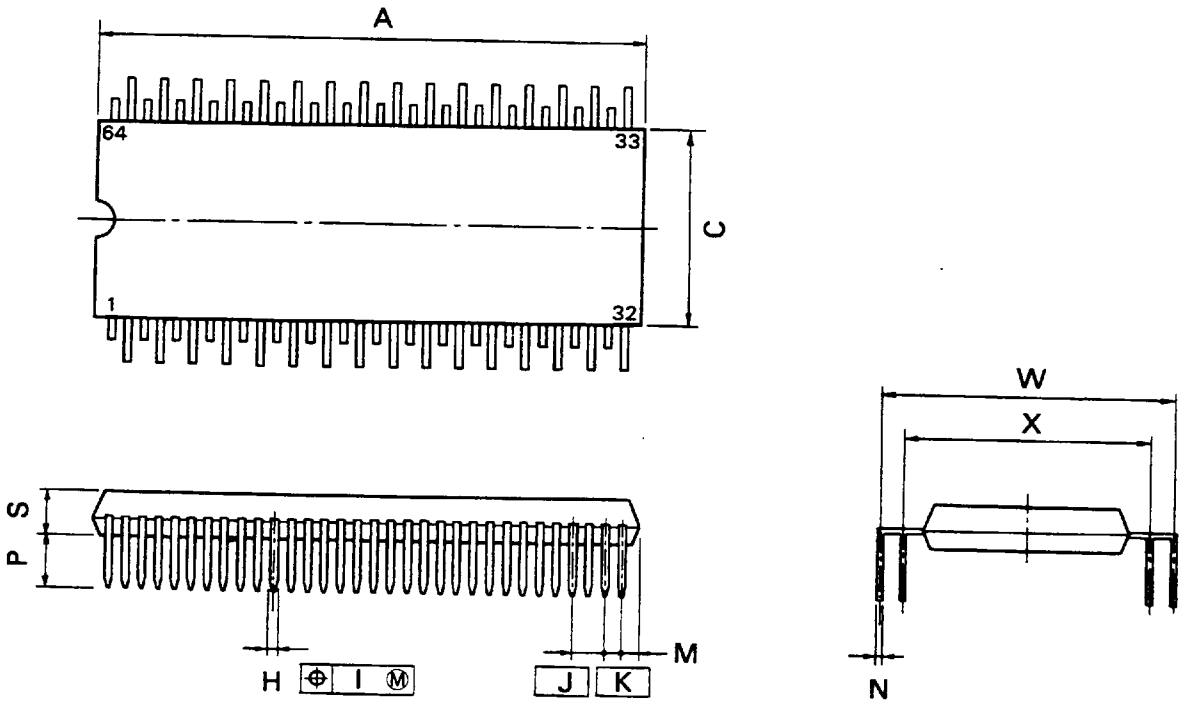
NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

64 PIN PLASTIC QUIP



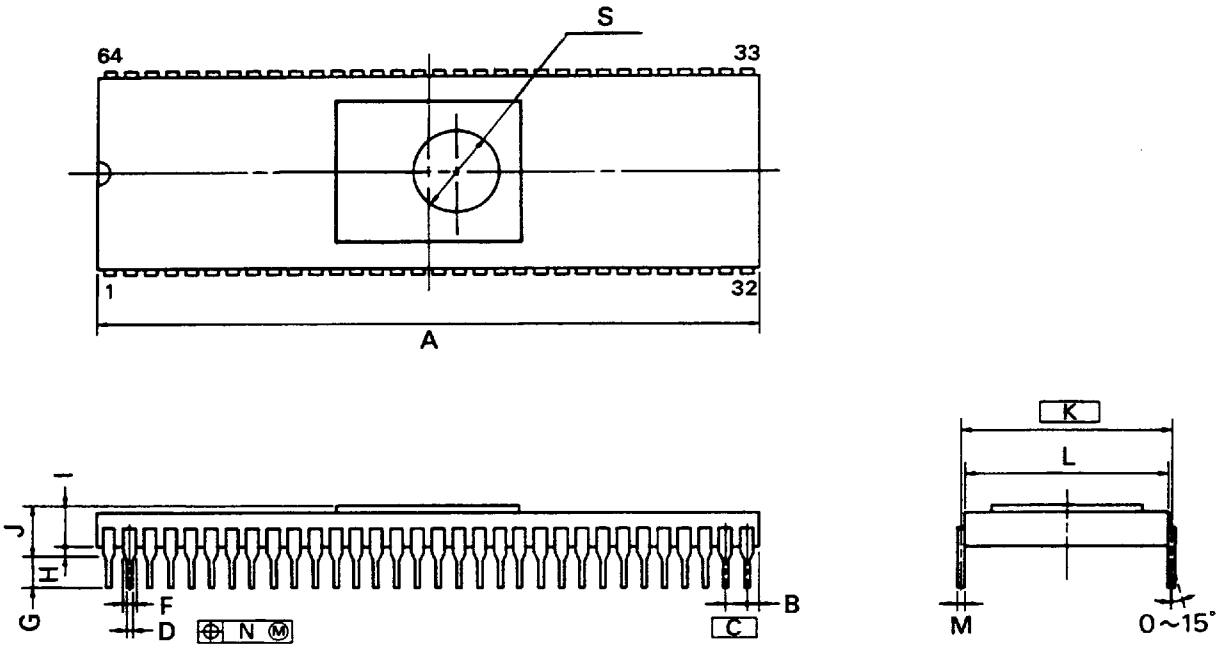
P64GQ-100-36

NOTE

Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$41.5^{+0.3}_{-0.2}$	$1.634^{+0.012}_{-0.008}$
C	16.5	0.650
H	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
I	0.25	0.010
J	2.54 (T.P.)	0.100 (T.P.)
K	1.27 (T.P.)	0.050 (T.P.)
M	$1.1^{+0.25}_{-0.15}$	$0.043^{+0.011}_{-0.006}$
N	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
P	$4.0^{\pm 0.3}$	$0.157^{+0.013}_{-0.012}$
S	$3.6^{\pm 0.1}$	$0.142^{+0.004}_{-0.005}$
W	$24.13^{\pm 1.05}$	$0.950^{\pm 0.042}$
X	$19.05^{\pm 1.05}$	$0.750^{\pm 0.042}$

64PIN CERAMIC SHRINK DIP (CERDIP) (WINDOW) (750 mil)



P64DW-70-750A1

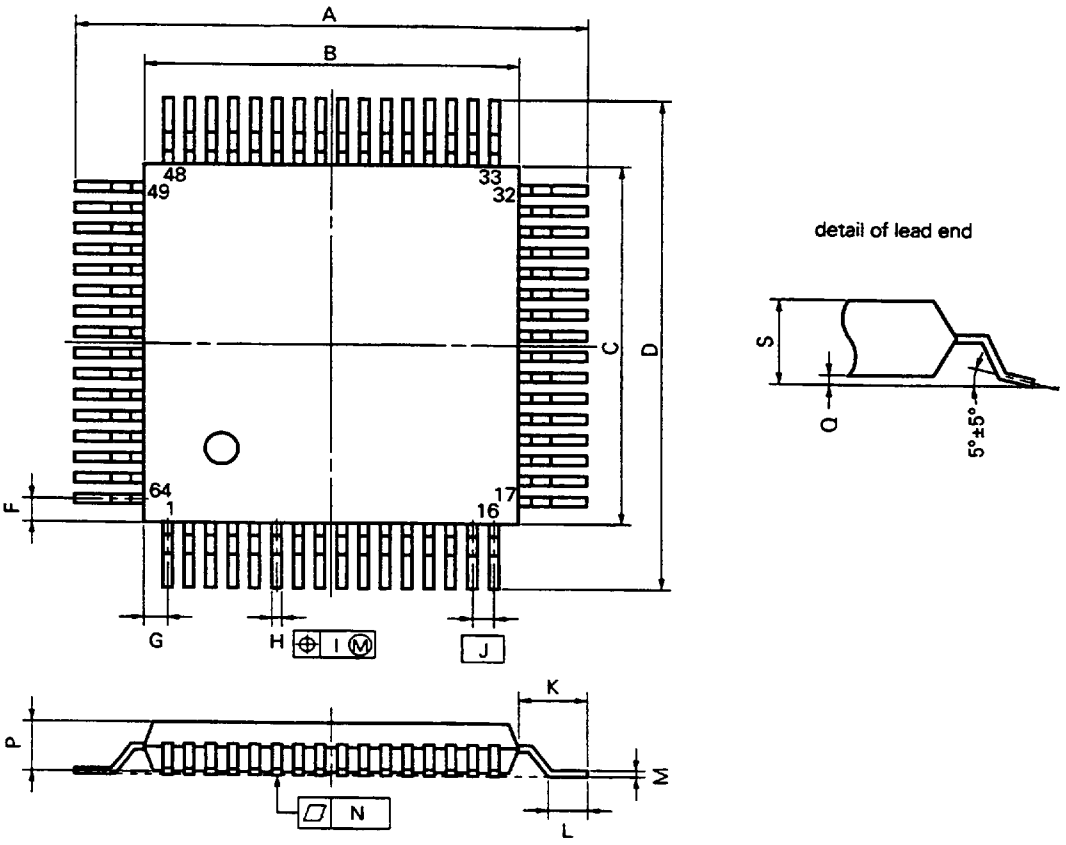
NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.310 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.46^{\pm 0.05}$	$0.018^{\pm 0.002}$
F	0.8 MIN.	0.031 MIN.
G	$3.5^{\pm 0.3}$	$0.138^{\pm 0.012}$
H	1.0 MIN.	0.039 MIN.
I	3.0	0.118
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	18.8	0.740
M	$0.25^{\pm 0.05}$	$0.010^{+0.002}_{-0.003}$
N	0.25	0.01
S	φ7.62	φ0.300

64 PIN PLASTIC QFP (□14)



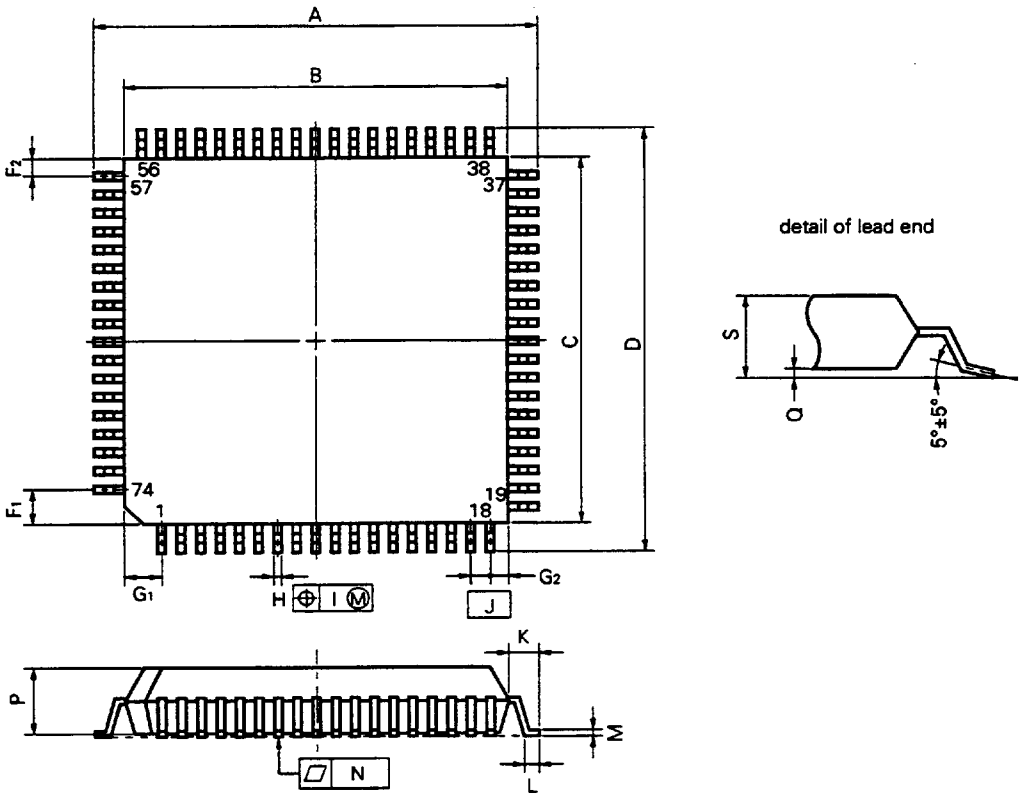
P64GC-80-AB8-3

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

74 PIN PLASTIC QFP (□20)



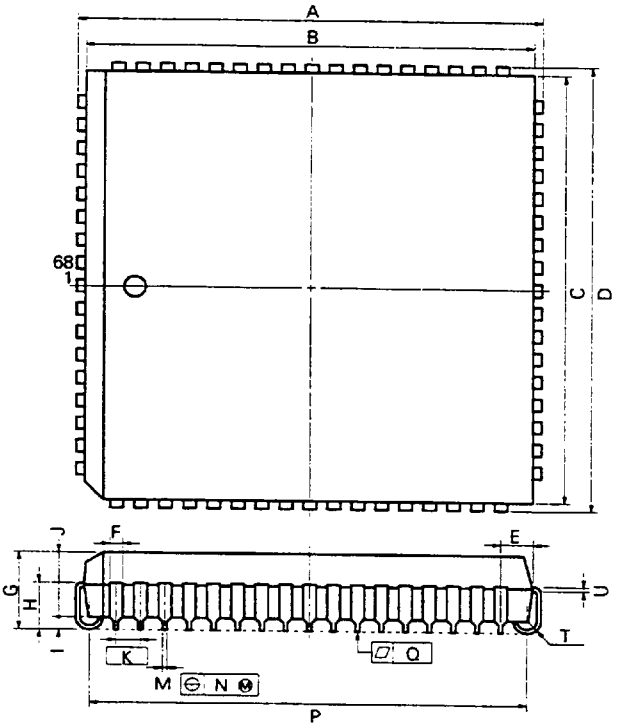
S74GJ-100-5BJ-2

NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.2±0.4	$0.913^{+0.017}_{-0.016}$
B	20.0±0.2	$0.787^{+0.009}_{-0.008}$
C	20.0±0.2	$0.787^{+0.009}_{-0.008}$
D	23.2±0.4	$0.913^{+0.017}_{-0.016}$
F_1	2.0	0.079
F_2	1.0	0.039
G_1	2.0	0.079
G_2	1.0	0.039
H	0.40±0.10	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.12	0.005
P	3.7	0.146
Q	0.1±0.1	0.004±0.004
S	4.0 MAX.	0.158 MAX.

68 PIN PLASTIC QFJ (□950 mil)



P68L-50A1-2

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	25.2±0.2	0.992±0.008
B	24.20	0.953
C	24.20	0.953
D	25.2±0.2	0.992±0.008
E	1.94±0.15	$0.076^{+0.007}_{-0.006}$
F	0.6	0.024
G	4.4±0.2	$0.173^{+0.009}_{-0.008}$
H	2.8±0.2	$0.110^{+0.009}_{-0.008}$
I	0.9 MIN.	0.035 MIN.
J	3.4	0.134
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±1.0	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	23.12±0.20	$0.910^{+0.009}_{-0.008}$
Q	0.15	0.006
T	R 0.8	R 0.031
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

9. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended in the table below.

For details of recommended soldering conditions for the surface mounting type, refer to the information document "Surface Mount Technology Manual" (IEI-1207).

For soldering methods and conditions other than those recommended below, contact our salesman.

Table 9-1 Surface Mounting Type Soldering Conditions

(1) μPD78P214GC-AB8 : 64-pin plastic QFP (□ 14mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230 °C, Duration: 30 sec. max. (at 210 °C or above) Number of times: Once Time limit: 2 days*1 (thereafter 16 hours prebaking required at 125°C)	IR30-162-1*2
VPS	Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above) Number of times: Once Time limit: 2 days*1 (thereafter 16 hours prebaking required at 125 °C)	VP15-162-1*2
Pin part heating	Pin part temperature: 300 °C max., Duration: 3 sec. max. (per device side)	———

(2) μPD78P214GJ-5BJ : 74-pin plastic QFP (□ 20mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230 °C, Duration: 30 sec. max. (at 210 °C or above) Number of times: Once Time limit: 7 days*1 (thereafter 10 hours prebaking required at 125 °C)	IR30-107-1
VPS	Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above) Number of times: Once Time limit: 7 days*1 (thereafter 10 hours prebaking required at 125 °C)	VP15-107-1
Pin part heating	Pin part temperature: 300°C max. Duration: 3 sec. max. (per device side)	———

(3) μPD78P214L : 68-pin plastic QFJ (□ 950mil)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
VPS	Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above) Number of times: Once Time limit: 7 days*1 (thereafter 10 hours prebaking required at 125 °C)	VP15-107-1
Pin part heating	Pin part temperature: 300 °C max. Duration: 3 sec. max. (per device side)	———

* 1. For the storage period after dry-pack decapsulation, storage conditions are max. 25 °C, 65% RH.

2. This condition is not applicable to the "K" specification product.

Note Use of more than one soldering method should be avoided (except in the case of pin part heating).

Table 9-2 Insert Type Soldering Conditions

μPD78P214CW : 64-pin plastic shrink DIP(750mil)
μPD78P214DW : 64-pin ceramic shrink DIP (CERDIP)(with wundow)(750mil)
μPD78P214GQ-36 : 64-pin plastic QUIP

Soldering Method	Soldering Conditions
Wave soldering (lead part only)	Solder bath temperature: 260 °C max., Duration: 10 sec. max.
Pin part heating	Pin part temperature: 260 °C max., Duration: 10 sec. max.

Note **Ensure that the application of wave soldering is limited to the lead part and no solder touches the main unit directly.**

Notification

A version of this product with improved recommended soldering conditions is available. For details (improvements such as infrared reflow peak temperature extension (235°C), number of times : twice, relaxation of time limit), contact NEC sales personnel.

APPENDIX. DEVELOPMENT TOOLS

The following development tools are available for system development using μPD78P214.

For development tools manufactured by a third party, see the **"78K/II Series Development Tools Selection Guide (EF-2)"**.

Hardware (1/2)

IE-78240-R-A	The IE-78240-R-A is a functionally enhanced version of the IE-78210-R and IE-78240-R, and is an in-circuit emulator for use with the entire μPD78214 series. It can be used when a PC-9800 series or IBM PC/AT™model is used as the host machine. The separately available screen debugger and device file are required, and in combination with these it is possible to perform debugging at the C language or structured assembly language source program level. More efficient debugging and program testing is possible through simultaneous data access and program fetch trace and C0 coverage functions, etc. If the user already has an IE-78210-R or IE-78240-R, this can be used in the same way as the IE-78240-R-A by purchasing a separately available board (IE-78200-R-BK).
IE-78240-R IE-78210-R*	IE-78210-R and IE-78240-R are in-circuit emulators which can be used in common with the μPD78214 series. Debugging is performed by connecting a host machine or a console. Connecting it to a host machine permits a symbolic debugging, object file transfer to a host machine, and efficient debugging. This tool incorporates RS-232-C serial interface for 2 channels, which enables connection to the PG-1500 PROM programmer. The IE-78240-R also executes the high-speed down loading of an object file and symbol file via Centronics I/F.
IE-78240-R-EM IE-78210-R-EM* IE-78200-R-EM IE-78200-R-BK	This board upgrades an in-circuit emulator for the 75X series and 78K series to the IE-78210-R, IE-78240-R or IE-78240-R-A. For details, refer to **"System upgrade"** described later.
EP-78210CW* EP-78240CW-R	This is an emulation probe for μPD78P214CW. EP-78240CW-R is the same product as EP-78210CW except its longer cable length.
EP-78210GC* EP-78240GC-R	This is an emulation probe for μPD78P214GC-AB8. It should be used together with EV-9200GC-64. EP-78240GC-R is the same product as EP-78210GC except its longer cable length.
EP-78210GJ*	This is an emulation probe for μPD78P214GJ-5BJ. It should be used together with either EP-78210L, EP-78240LP-R or EV-9200G-74.
EP-78240GJ-R	This is an emulation probe for μPD78P214GJ-5BJ. It should be used together with EV-9200G-74. Unlike the EP-78210GJ, this is an integral probe, allowing easy operation.
EP-78210GQ* EP-78240GQ-R	This is an emulation probe for μPD78P214GQ-36. EP-78240GC-R is the same product as EP-78210GQ except its longer cable length.
EP-78210L* EP-78240LP-R	This is an emulation probe for μPD78P214L. EP-78240LP-R is the same product as EP-78210L except its longer cable length.

★

* No longer manufactured.

Remarks The cables EP-78210GJ, EP-78210GC, EP-78240GC-R, EP-78240GJ-R are respectively provided with one piece of the socket EV-9200GC-74 or EV-9200GC-64.

Hardware (2/2)

EV-9200G-74	This is a socket mounted on the board of user system which is made for μPD78P214GJ-5BJ. It should be used together with either EP-78210GJ or EP-78240GJ-R.
EV-9200GC-64	This is a socket mounted on the board of user system which is made for μPD78P214GC-AB8. It should be used together with either EP-78210GC or EP-78240GC-R.
PG-1500	PROM programmer which enables a single-chip microcomputer with on-chip PROM to be programmed in stand-alone mode or by operations from a host machine by connection of the supplied board and separately available programmer adapter. Typical PROMs from 256K bits to 4M bits can also be programmed.
PA-78P214CW	This is a PROM programmer adapter for μPD78P214CW/78P214DW, and should be used in combination with PG-1500, etc.
PA-78P214GC	This is a PROM programmer adapter for μPD78P214GC-AB8 and should be used in combination with PG-1500, etc.
PA-78P214GJ	This is a PROM programmer adapter for μPD78P214GJ-5BJ and should be used in combination with PG-1500, etc.
PA-78P214GQ	This is a PROM programmer adapter for μPD78P214GQ-36 and should be used in combination with PG-1500, etc.
PA-78P214L	This is a PROM programmer adapter for μPD78P214L and should be used in combination with PG-1500, etc.

★

* No longer manufactured.

Remarks EV-9200GC-74 or EV-9200GC-64 is available by the 5- piece set (ordered in units of a set).

Software

① Language Processing Software (1/2)

78K/II series relocatable assembler (RA78K/II)

A relocatable assembler package which can be used by the entire 78K/II series. Because it is a relocatable assembler with a macro function, development efficiency can be improved.
A structured assembler which can describe explicitly the program control structure is also provided. Thus program productivity and maintainability can be improved.

Host Machine	OS	Supply Medium	Ordering Code	
PC-9800 series	MS-DOS™ (Ver.3.30 to Ver.5.00A*3)	8-inch 2D *1	μS5A1RA78K2	
		5-inch 2HD	μS5A10RA78K2	
		3.5-inch 2HD	μS5A13RA78K2	
IBM PC / AT	PC DOS™ (Ver.3.1)	5-inch 2D *2	μS7B11RA78K2	
		5-inch 2HC	μS7B10RA78K2	
HP9000 series 300™	HP-UX™ (rel.7.05B)	Cartridge tape (QIC-24)	μS3H15RA78K2	★
SPARKstation™	Sun OS™ (rel.4.1.1)		μS3K15RA78K2	★
EWS-4800 series™ (RISC)	EWS-UX/V™ (rel.4.0)		S3M15RA78K2	★

78K/II series C compiler (CC78K/II)

A C compiler which can be used by the entire 78K/II series.
Its language specification is compliant with ANSI, thus programs can be converted into ROM. It is provided with such functions as special function register manipulation, bit manipulation, variables using short direct addressing, interrupt control functions. Use of these function allows efficient programming and higher object efficiency to be achieved.
It is also provided with start-up routine sample programs and standard function object libraries.
Use of this compiler requires 78K/II series relocatable assembler (RA78K/II).

Host Machine	OS	Supply Medium	Ordering Code	
PC-9800 series	MS-DOS (Ver.3.30 to Ver.5.00A*3)	5-inch 2HD	μS5A10CC78K2	
		3.5-inch 2HD	μS5A13CC78K2	
IBM PC / AT	PC DOS (Ver.3.1)	5-inch 2D *2	μS7B11CC78K2	
		5-inch 2HC	μS7B10CC78K2	
HP9000 series 300	HP-UX (rel.7.05B)	Cartridge tape (QIC-24)	μS3H15CC78K2	★
SPARKstation	Sun OS (rel.4.1.1)		μS3K15CC78K2	★
EWS-4800 series (RISC)	EWS-UX/V (rel.4.0)		S3M15CC78K2	★

* 1. No longer available for purchase with 8-inch 2D. 5-inch 2HD or 3.5-inch 2HD should be selected instead. If it has been purchased with 8-inch 2D, the 5-inch 2HD will be sent in the next version upgrade.
2. The 5-inch 2D version is no longer sold. Please note that users who have previously purchased software in 5-inch 2D format will be sent future version upgrades in 5-inch 2HC format.
3. The task swap function, which is provided with Ver.5.00/5.00A, is not available with this software.

① Language Processing Software (2/2)

78K/II series C compiler library source file (CC78K/II-L)	A source program of a library which belongs to the CC78K/II. Required to improve (to adapt more to the user specifications.) the library.			
	Host Machine	OS	Supply Medium	Ordering Code
	PC-9800 series	MS-DOS (Ver.3.30 to Ver.5.00A*)	5-inch 2HD	μS5A10CC78K2-L
			3.5-inch 2HD	μS5A13CC78K2-L
	IBM PC / AT	PC DOS (Ver.3.1)	5-inch 2HC	μS7B10CC78K2-L
★	HP9000 series 300	HP-UX (rel.7.05B)	Cartridge tape (QIC-24)	μS3H15CC78K2-L
★	SPARKstation	Sun OS (rel.4.1.1)		μS3K15CC78K2-L
★	EWS-4800 series (RISC)	EWS-UX/V (rel.4.0)		μS3M15CC78K2-L

* The task swap function, which is provided with Ver.5.00/5.00A, is not available with this software.

② In-Circuit Emulator Software

Screen debugger (SD78K/II)

Program which controls the 78K/II series in-circuit emulator. Used in conjunction with the device file (DF78210).
Using the IE-78240-R-A or an in-circuit emulator system-upgraded to equivalence with the IE-78240-R-A , can be used with a PC-9800 series or IBM PC/AT host machine. ★
This software enables highly efficient debugging to be performed through functions for source program level debugging of programs written in C language, structured assembly language or assembly language, and host machine screen splitting for the simultaneous display of various kinds of information.

Host Machine	OS	Supply Medium	Ordering Code	
PC-9800 series	MS-DOS (Ver.3.30 to Ver.5.00A*1)	5-inch 2HD	μS5A10SD78K2	
		3.5-inch 2HD	μS5A13SD78K2	
IBM PC / AT	PC DOS (Ver.3.1)	5-inch 2HC	μS7B10SD78K2*2	★

Device file (DF78210)

Required to perform μPD78214 series debugging in conjunction with the screen debugger (SD78K/II).

Host Machine	OS	Supply Medium	Ordering Code	
PC-9800 series	MS-DOS (Ver.3.30 to Ver.5.00A*1)	5-inch 2HD	μS5A10DF78210	
		3.5-inch 2HD	μS5A13DF78210	
IBM PC / AT	PC DOS (Ver.3.1)	5-inch 2HC	μS7B10DF78210*2	★

IE-78210-R IE-78210-R-EM control program (IE78210)

A program which controls the IE-78210 from the host machine. Its automatic command execution capability allows more efficient debugging.

Host Machine	OS	Supply Medium	Ordering Code
PC-9800 series	MS-DOS (Ver.3.30 to Ver.5.00A*1)	8-inch 2D *3	μS5A1IE78210-P01
		5-inch 2HD	μS5A10IE78210-P01
		3.5-inch 2HD	μS5A13IE78210
IBM PC / AT	PC DOS (Ver.3.1)	5-inch 2D *4	μS7B11IE78210-P02
		5-inch 2HC	μS7B10IE78210

IE-78240-R IE-78240-R-EM control program (IE78240)

A program which controls the IE-78240 from the host machine.
Its automatic command execution capability allows more efficient debugging.

Host Machine	OS	Supply Medium	Ordering Code
PC-9800 series	MS-DOS (Ver.3.30 to Ver.5.00A*1)	8-inch 2D *3	μS5A1IE78240
		5-inch 2HD	μS5A10IE78240
		3.5-inch 2HD	μS5A13IE78240
IBM PC / AT	PC DOS (Ver.3.1)	5-inch 2D *4	μS7B11IE78240
		5-inch 2HC	μS7B10IE78240

* 1. The task swap function, which is provided with Ver.5.00/5.00A, is not available with this software.
  2. Under development.
  3. No longer available for purchase with 8-inch 2D. 5-inch 2HD or 3.5-inch 2HD should be selected instead. If it has been purchased with 8-inch 2D, the 5-inch 2HD will be sent in the next version upgrade.
  4. The 5-inch 2D version is no longer sold. Please note that users who have previously purchased software in 5-inch 2D format will be sent future version upgrades in 5-inch 2HC format.

③ PROM Programmer Software

PG-1500 controller	Controls the PG-1500 on the host machine, with the PG-1500 and host machine connected via a serial or parallel interface.			
	Host Machine	OS	Supply Medium	Ordering Code
	PC-9800 series	MS-DOS (Ver.3.30 to Ver.5.00A*1)	5-inch 2HD	μS5A10PG1500
			3.5-inch 2HD	μS5A13PG1500
	IBM PC / AT	PC DOS (Ver.3.1)	5-inch 2D *2	μS7B11PG1500
			5-inch 2HC	μS7B10PG1500

* 1. The task swap function, which is provided with Ver.5.00/5.00A, is not available with this software.
  2. The 5-inch 2D version is no longer sold. Please note that users who have previously purchased software in 5-inch 2D format will be sent future version upgrades in 5-inch 2HC format.

System Upgrade from Another In-Circuit Emulator

① System upgrade to IE-78240-R-A

Current Emulator	IE-Group No.	Boards to be Purchased	Remarks
IE-78230-R-A IE-78140-R	1	IE-78240-R-EM	—
IE-78240-R	2	IE-78200-R-BK	—
IE-78112-R*1 IE-78220-R*1 IE-78310-R*1 IE-78310A-R	3	IE-78200-R-BK IE-78240-R-EM*2	The high-speed download function cannot be used. If you also have an IE Group 1/2/4 in-circuit emulator, a system upgrading based on the IE Group 1/2/4 in-circuit emulator is recommended. If you also have an IE Group 1 in-circuit emulator, the IE-78200-R-BK is not required (the IE Group 1 in-circuit emulator contains an IE-78200-R-BK and therefore this board can be used).
IE-75000-R IE-78000-R IE-78130-R IE-78230-R IE-78320-R*1 IE-78327-R IE-78330-R IE-78350-R IE-78600-R	4	IE-78200-R-BK IE-78240-R-EM	If you also have an IE Group 1, in-circuit emulator, the IE-78200-R-BK is not required (the IE Group 1 in-circuit emulator contains an IE78200-R-BK, and therefore this board can be used).
IE-78210-R*1	5	IE-78200-R-BK	The high-speed download function cannot be used.

* 1. No longer manufactured and not available for purchase.
2. When performing emulation of the μPD78214 series, if you have already the IE-78210-R-EM*1, the IE-78240-R-EM is not required.

② **System upgrade to IE-78240-R**

Current Emulator	IE-Group No.	Boards to be Purchased	Remarks
IE-78112-R*1 IE-78210-R*1 IE-78220-R*1	1	IE-78240-R-EM*2	The high-speed download function cannot be used. If you also have an IE of Group 4, use of IE cabinet of Group 4 is recommended.
IE-78130-R IE-78230-R	2	IE-78240-R-EM	—
IE-78310-R*1 IE-78310A-R	3	IE-78200-R-EM IE-78240-R-EM*2	The high-speed download function cannot be used. If you have an IE of Group 1, the IE-7800-R-EM is not required (the IE of Group 1 contains an IE-78200-R-EM and therefore this board can be used).
IE-75000-R IE-78000-R IE-78320-R*1 IE-78327-R IE-78330-R IE-78350-R IE-78600-R	4	IE-78200-R-EM IE-78240-R-EM	If you have an IE of Group 1, the IE-78200-R-EM is not required (the IE of Group 1 contains an IE-78200-R-EM, and therefore this board can be used).
IE-78140-R IE-78230-R-A	5	IE-78200-R-EM IE-78240-R-EM	A system upgrading to IE-78240-R-A equivalence is recommended.

* 1. No longer manufactured and not available for purchase.
2. When performing emulation of the μPD78214 series, if you have already the IE-78210-R-EM*1, the IE-78240-R-EM is not required.

★ ③ **System upgrade to IE-78210-R*1**

Current Emulator	IE-Group No.	Boards to be Purchased	Remarks
IE-78112-R*1 IE-78220-R*1	1	IE-78210-R-EM*2	—
IE-78310-R*1 IE-78310A-R	2	IE-78200-R-EM IE-78210-R-EM*1	If you have an IE of Group 1, the IE-7800-R-EM is not required (the IE of Group 1 contains an IE-78200-R-EM and therefore this board can be used).
IE-75000-R IE-78000-R IE-78130-R IE-78140-R IE-78230-R IE-78230-R-A IE-78320-R*1 IE-78327-R IE-78330-R IE-78350-R IE-78600-R	3	—	A system upgrading to IE-78210-R is not possible. A system upgrading to IE-78240-R is recommended.

* 1. No longer manufactured and not available for purchase.
2. IE-78210-R-EM no longer manufactured and not available for purchase. Therefore, if you do not have the IE-78210-R-EM, a system upgrade to IE-78240-R or IE-78240-R-A is recommended.

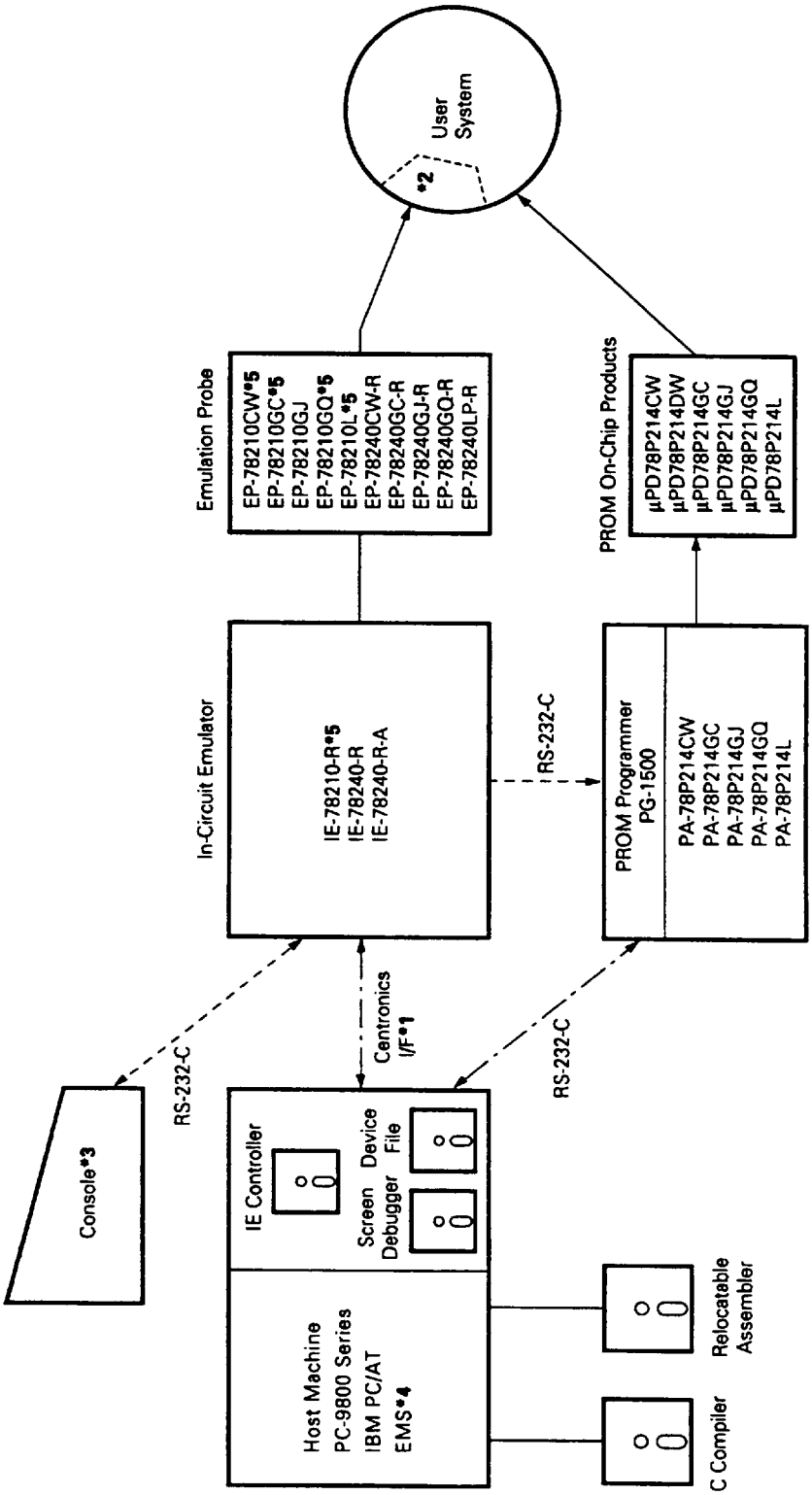
Built-In Software ★

① **Fuzzy Inference Development Support System**

Fuzzy knowledge data creation tool (FE9000)	A program to support fuzzy knowledge data (fuzzy rules and membership function) input/editing and evaluation (simulation).			
	Host Machine	OS	Supply Medium	Ordering Code
	PC-9800 series	MS-DOS (Ver.3.10 to Ver.3.30C)	5-inch 2HD	μS5A10FE9000
			3.5-inch 2HD	μS5A13FE9000
	IBM PC / AT	PC DOS (Ver.3.1)	5-inch 2HC	μS7B10FE9000
Translator (FT9080)	A program to convert the fuzzy knowledge data obtained by the fuzzy knowledge data creation tool to an RA78K/II assembler source program.			
	Host Machine	OS	Supply Medium	Ordering Code
	PC-9800 series	MS-DOS (Ver.3.10 to Ver.3.30C)	5-inch 2HD	μS5A10FT9080
			3.5-inch 2HD	μS5A13FT9080
	IBM PC / AT	PC DOS (Ver.3.1)	5-inch 2HC	μS7B10FT9080
Fuzzy inference module (FI78k/II)	A program to execute fuzzy inference. Executes fuzzy inference by linking with the fuzzy knowledge data converted by the translator.			
	Host Machine	OS	Supply Medium	Ordering Code
	PC-9800 series	MS-DOS (Ver.3.10 to Ver.3.30C)	5-inch 2HD	μS5A10FI78K2
			3.5-inch 2HD	μS5A13FI78K2
	IBM PC / AT	PC DOS (Ver.3.1)	5-inch 2HC	μS7B10FI78K2
Fuzzy debugger (FD78K/II)*	A support software to evaluate and adjust the fuzzy knowledge data at the hardware level using an in-circuit emulator.			
	Host Machine	OS	Supply Medium	Ordering Code
	PC-9800 series	MS-DOS (Ver.3.10 to Ver.3.30C)	5-inch 2HD	μS5A10FD78K2
			3.5-inch 2HD	μS5A13FD78K2
	IBM PC / AT	PC DOS (Ver.3.1)	5-inch 2HC	μS7B10FD78K2

* Under development

Development Tool Configuration ★



* 1. It is used when a file is transferred at high speed (down-loading). —·—·— : When using by connecting with a host machine
2. EV-9200GC-64, EV-9200G-74 - - - - - : Using the IE as stand-alone by connecting with a console
3. Only when the IE-78240-R is used
4. The EWS used are HP9000 series 300, SUN4/3900 and EWS-4800/200 series. The EWS cannot be connected to an in-circuit emulator.
5. Not available for purchase