Document Title

256K X 8 Bit CMOS 5.0 Volt-only, Boot Sector Flash Memory

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	May 8, 2000	Preliminary
0.1	Add A290021 part data	May 31, 2000	
0.2	Add Top/Bottom ordering information	June 26, 2000	
0.3	Change I_{LIT} from 50μA to 100μA	January 3, 2001	
	Change typical byte programming time from 7μs to 35μs		
0.4	Erase VCC supply voltage for ± 5% devices in Operation Ranges	February 6, 2001	
	Add the time limit t_{WPH} max. = 50μs of command cycle sequence		
0.5	Correct the Continuation ID command to hexadecimal	August 21, 2001	
1.0	Final version release	February 6, 2002	Final
1.1	Error Correction:		
	P.8: Autoselect Command Sequence (line 15), XX11 → XX03h	December 24, 2002	
1.2	Add 32L Pb-free PLCC package type	July 5, 2004	
1.3	Add Pb-Free package type for all parts	August 6, 2004	

A29002/A290021 Series

256K X 8 Bit CMOS 5.0 Volt-only, Boot Sector Flash Memory

Features

- 5.0V ± 10% for read and write operations
- Access times:
  - 55/70/90/120/150 (max.)
- Current:
  - 20 mA typical active read current
  - 30 mA typical program/erase current
  - 1 μA typical CMOS standby
- Flexible sector architecture
  - 16 Kbyte/ 8 KbyteX2/ 32 Kbyte/ 64 KbyteX3 sectors
  - Any combination of sectors can be erased
  - Supports full chip erase
  - Sector protection:
    A hardware method of protecting sectors to prevent any inadvertent program or erase operations within that sector
- Top or bottom boot block configurations available
- Embedded Erase Algorithms
  - Embedded Erase algorithm will automatically erase the entire chip or any combination of designated sectors and verify the erased sectors
  - Embedded Program algorithm automatically writes and verifies bytes at specified addresses
- Typical 100,000 program/erase cycles per sector
- 20-year data retention at 125°C
  - Reliable operation for the life of the system
- Compatible with JEDEC-standards
  - Pinout and software compatible with single-power-supply Flash memory standard
  - Superior inadvertent write protection
- $\overline{\text{Data}}$ Polling and toggle bits
  - Provides a software method of detecting completion of program or erase operations
- Erase Suspend/Erase Resume
  - Suspends a sector erase operation to read data from, or program data to, a non-erasing sector, then resumes the erase operation
- Hardware reset pin ($\overline{\text{RESET}}$)
  - Hardware method to reset the device to reading array data (not available on A290021)
- Package options
  - 32-pin P-DIP, PLCC, or TSOP (Forward type)

General Description

The A29002 is a 5.0 volt-only Flash memory organized as 262,144 bytes of 8 bits each. The A29002 offers the $\overline{\text{RESET}}$ function, but it is not available on A290021. The 256 Kbytes of data are further divided into seven sectors for flexible sector erase capability. The 8 bits of data appear on I/O_0 - I/O_7 while the addresses are input on A0 to A17. The A29002 is offered in 32-pin PLCC, TSOP, and PDIP packages. This device is designed to be programmed in-system with the standard system 5.0 volt VCC supply. Additional 12.0 volt VPP is not required for in-system write or erase operations. However, the A29002 can also be programmed in standard EPROM programmers.

The A29002 has the first toggle bit, I/O_6, which indicates whether an Embedded Program or Erase is in progress, or it is in the Erase Suspend. Besides the I/O_6 toggle bit, the A29002 has a second toggle bit, I/O_2, to indicate whether the addressed sector is being selected for erase. The A29002 also offers the ability to program in the Erase Suspend mode. The standard A29002 offers access times of 55, 70, 90, 120, and 150 ns, allowing high-speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable ($\overline{\text{CE}}$), write enable ($\overline{\text{WE}}$) and output enable ($\overline{\text{OE}}$) controls.

The device requires only a single 5.0 volt power supply for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The A29002 is entirely software command set compatible with the JEDEC single-power-supply Flash standard.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by writing the proper program command sequence. This initiates the Embedded Program algorithm - an internal algorithm that automatically times the program pulse widths and verifies proper program margin.

Device erasure occurs by executing the proper erase command sequence. This initiates the Embedded Erase algorithm - an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper erase margin.

The host system can detect whether a program or erase operation is complete by reading the I/O_7 ($\overline{\text{Data}}$ Polling) and I/O_6 (toggle) status bits. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The A29002 is fully erased when shipped from the factory.

The hardware sector protection feature disables operations for both program and erase in any combination of the sectors of memory. This can be achieved via programming equipment.

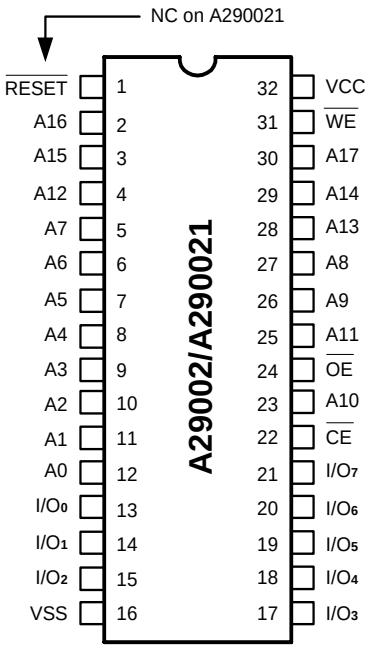
The Erase Suspend feature enables the user to put erase on hold for any period of time to read data from, or program data to, any other sector that is not selected for erasure. True background erase can thus be achieved.

Power consumption is greatly reduced when the device is placed in the standby mode.

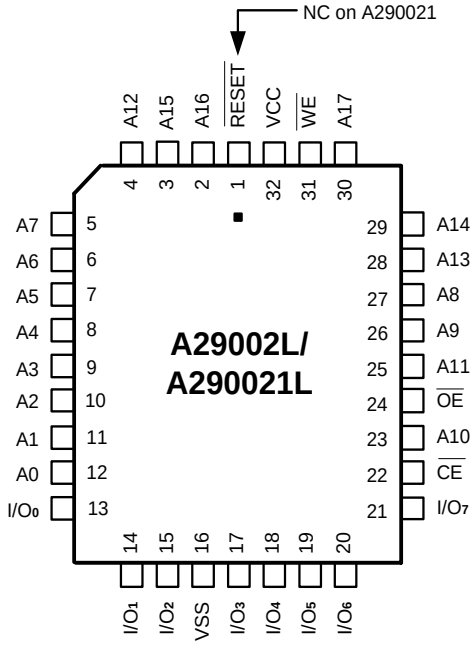
The hardware $\overline{\text{RESET}}$ pin terminates any operation in progress and resets the internal state machine to reading array data (This feature is not available on the A290021).

Pin Configurations

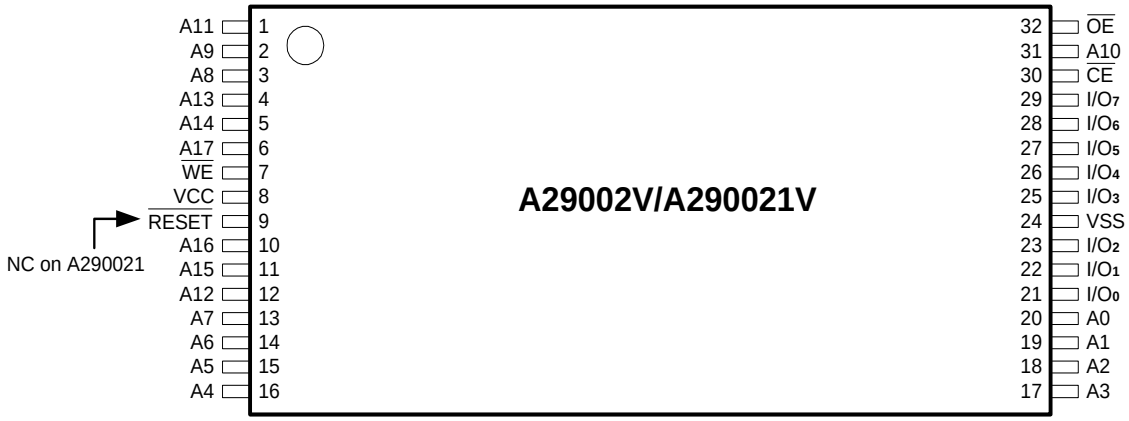
■ DIP



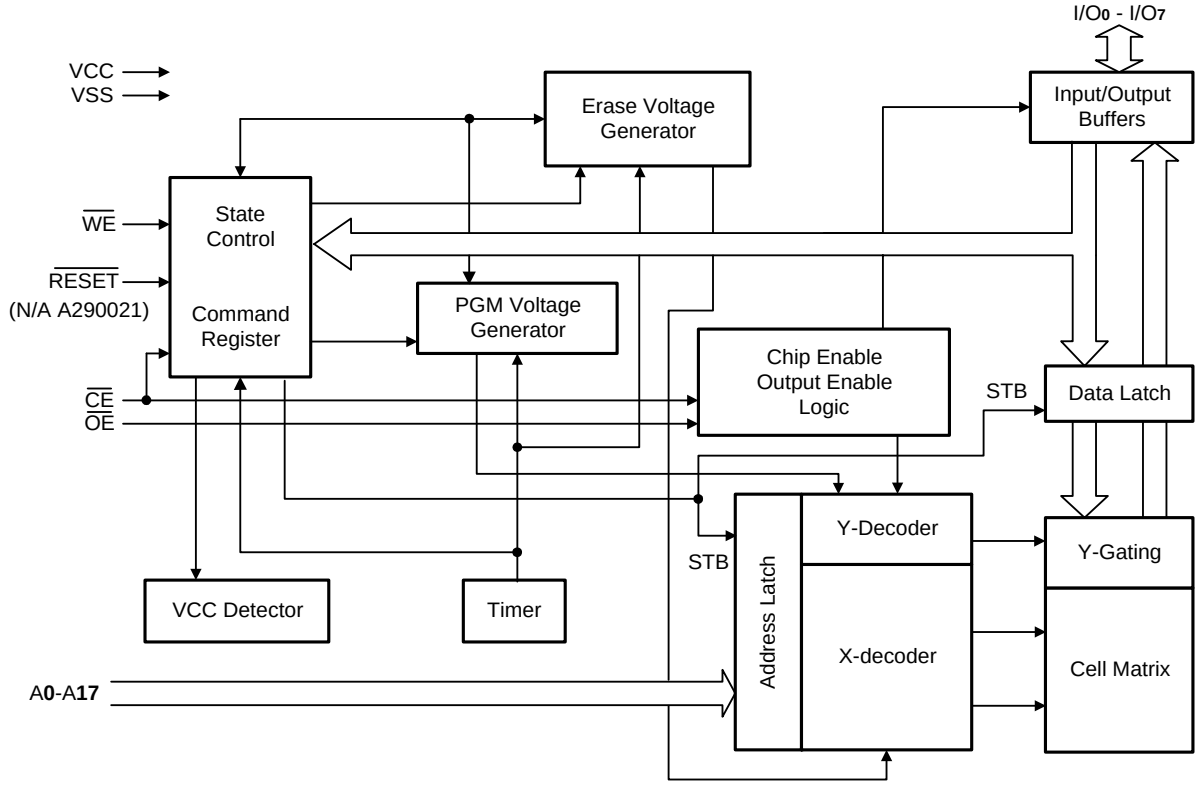
■ PLCC



■ TSOP (Forward type)



Block Diagram



Pin Descriptions

Pin No.	Description
A0 - A17	Address Inputs
I/O0 - I/O7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{RESET}$	Hardware Reset (N/A A290021)
VSS	Ground
VCC	Power Supply

Absolute Maximum Ratings*

Ambient Operating Temperature . . . .-55°C to + 125°C
Storage Temperature . . . . -65°C to + 125°C
Ground to VCC . . . .-2.0V to 7.0V
Output Voltage (Note 1) . . . .-2.0V to 7.0V
A9, $\overline{OE}$ & $\overline{RESET}$ (Note 2) .... -2.0V to 12.5V
All other pins (Note 1) . . . . -2.0V to 7.0V
Output Short Circuit Current (Note 3)..... . . . . . 200mA

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot VSS to -2.0V for periods of up to 20ns. Maximum DC voltage on output and I/O pins is VCC +0.5V. During voltage transitions, outputs may overshoot to VCC +2.0V for periods up to 20ns.
2. Minimum DC input voltage on A9 pins is -0.5V. During voltage transitions, A9, $\overline{OE}$ and $\overline{RESET}$ may overshoot VSS to -2.0V for periods of up to 20ns. Maximum DC input voltage on A9 and $\overline{OE}$ is +12.5V which may overshoot to 13.5V for periods up to 20ns. ($\overline{RESET}$ is N/A on A290021)
3. No more than one output is shorted at a time. Duration of the short circuit should not be greater than one second.

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of these specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Operating Ranges

Commercial (C) Devices
Ambient Temperature (T_A) . . .. 0°C to +70°C

VCC Supply Voltages
VCC for ± 10% devices .... +4.5V to +5.5V
Operating ranges define those limits between which the functionally of the device is guaranteed.

Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The appropriate device bus operations table lists the inputs and control levels required, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. A29002/A290021 Device Bus Operations

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$ (N/A A290021)	A0 – A17	I/O_0 - I/O_7
Read	L	L	H	H	A_{IN}	D_{OUT}
Write	L	H	L	H	A_{IN}	D_{IN}
CMOS Standby	VCC ± 0.5 V	X	X	VCC ± 0.5 V	X	High-Z
TTL Standby	H	X	X	VCC ± 0.5 V	X	High-Z
Output Disable	L	H	H	H	X	High-Z
Reset	X	X	X	L	X	High-Z
Temporary Sector Unprotect (Note)	X	X	X	V_{ID}	X	X

Legend:
L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 12.0 ± 0.5V, X = Don't Care, D_{IN} = Data In, D_{OUT} = Data Out, A_{IN} = Address In
Note: 1. See the "Sector Protection/Unprotection" section and Temporary Sector Unprotect for more information.
2. This function is not available on A290021.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the $\overline{CE}$ and $\overline{OE}$ pins to V_{IL}. $\overline{CE}$ is the power control and selects the device. $\overline{OE}$ is the output control and gates array data to the output pins. $\overline{WE}$ should remain at V_{IH} all the time during read operation. The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Reading Array Data" for more information. Refer to the AC Read Operations table for timing specifications and to the Read Operations Timings diagram for the timing waveforms, I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive $\overline{WE}$ and $\overline{CE}$ to V_{IL}, and $\overline{OE}$ to V_{IH}. An erase operation can erase one sector, multiple sectors, or the entire device. The Sector Address Tables indicate the address range that each sector occupies. A "sector address" consists of the address inputs required to uniquely select a sector. See the "Command Definitions" section for details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on I/O_7 - I/O_0. Standard read cycle timings apply in this mode. Refer to the "Autoselect Mode" and "Autoselect Command Sequence" sections for more information.

I_{CC2} in the Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification tables and timing diagrams for write operations.

Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on I/O_7 - I/O_0. Standard read cycle timings and I_{CC} read specifications apply. Refer to "Write Operation Status" for more information, and to each AC Characteristics section for timing diagrams.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the $\overline{OE}$ input.

The device enters the CMOS standby mode when the $\overline{CE}$ & $\overline{RESET}$ pins ($\overline{CE}$ only on A290021) are both held at $V_{CC} \pm 0.5V$. (Note that this is a more restricted voltage range than V_{IH}.) The device enters the TTL standby mode when $\overline{CE}$ is held at V_{IH}, while $\overline{RESET}$ (Not available on A290021) is held at VCC±0.5V. The device requires the standard access time (t_{CE}) before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the DC Characteristics tables represents the standby current specification.

Output Disable Mode

When the $\overline{OE}$ input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

$\overline{RESET}$: Hardware Reset Pin (N/A on A290021)

The $\overline{RESET}$ pin provides a hardware method of resetting the device to reading array data. When the system drives the $\overline{RESET}$ pin low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all data output pins, and ignores all read/write attempts for the duration of the $\overline{RESET}$ pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

The $\overline{RESET}$ pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

Refer to the AC Characteristics tables for $\overline{RESET}$ parameters and diagram.

Table 2. A29002/A290021 Top Boot Block Sector Address Table

Sector	A17	A16	A15	A14	A13	Sector Size (Kbytes)	Address Range
SA0	0	0	X	X	X	64	00000h - 0FFFFh
SA1	0	1	X	X	X	64	10000h - 1FFFFh
SA2	1	0	X	X	X	64	20000h - 2FFFFh
SA3	1	1	0	X	X	32	30000h - 37FFFh
SA4	1	1	1	0	0	8	38000h - 39FFFh
SA5	1	1	1	0	1	8	3A000h - 3BFFFh
SA6	1	1	1	1	X	16	3C000h - 3FFFFh

Table 3. A29002/A290021 Bottom Boot Block Sector Address Table

Sector	A17	A16	A15	A14	A13	Sector Size (Kbytes)	Address Range
SA0	0	0	0	0	X	16	00000h - 03FFFh
SA1	0	0	0	1	0	8	04000h - 05FFFh
SA2	0	0	0	1	1	8	06000h - 07FFFh
SA3	0	0	1	X	X	32	08000h - 0FFFFh
SA4	0	1	X	X	X	64	10000h - 1FFFFh
SA5	1	0	X	X	X	64	20000h - 2FFFFh
SA6	1	1	X	X	X	64	30000h - 3FFFFh

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on I/O_7 - I/O_0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.
When using programming equipment, the autoselect mode requires V_{ID} (11.5V to 12.5 V) on address pinA9. Address pins A6, A1, and AO must be as shown in Autoselect Codes (High Voltage Method) table. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. Refer to the corresponding Sector Address Tables. The Command Definitions table shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on I/O_7 - I/O_0.To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in the Command Definitions table. This method does not require V_{ID}. See "Command Definitions" for details on using the autoselect mode.

Table 4. A29002/A290021 Autoselect Codes (High Voltage Method)

Description	A17 - A13	A12 - A10	A9	A8 - A7	A6	A5 - A2	A1	AO	Identifier Code on I/O_7 - I/O_0
Manufacturer ID: AMIC	X	X	V_{ID}	X	V_{IL}	X	V_{IL}	V_{IL}	37h
Device ID: A29002/ A290021	X	X	V_{ID}	X	V_{IL}	X	V_{IL}	V_{IH}	Top Boot Block: 8Ch Bottom Boot Block: 0Dh
Sector Protection Verification	Sector Address	X	V_{ID}	X	V_{IL}	X	V_{IH}	V_{IL}	01h (protected)
									00h (unprotected)
Continuation ID	X	X	V_{ID}	X	V_{IL}	X	V_{IH}	V_{IH}	7Fh

Note: $\overline{CE}$ =V_{IL}, $\overline{OE}$ =V_{IL} and $\overline{WE}$ =V_{IH} when Autoselect Mode

Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.
Sector protection/unprotection must be implemented using programming equipment. The procedure requires a high voltage (V_{ID}) on address pin A9 and the control pins.
The device is shipped with all sectors unprotected.
It is possible to determine whether a sector is protected or unprotected. See "Autoselect Mode" for details.

Hardware Data Protection

The requirement of command unlocking sequence for programming or erasing provides data protection against inadvertent writes (refer to the Command Definitions table). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during Vcc power-up transitions, or from system noise. The device is powered up to read array data to avoid accidentally writing data to the array.

Write Pulse "Glitch" Protection

Noise pulses of less than 5ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ do not initiate a write cycle.

Logical Inhibit

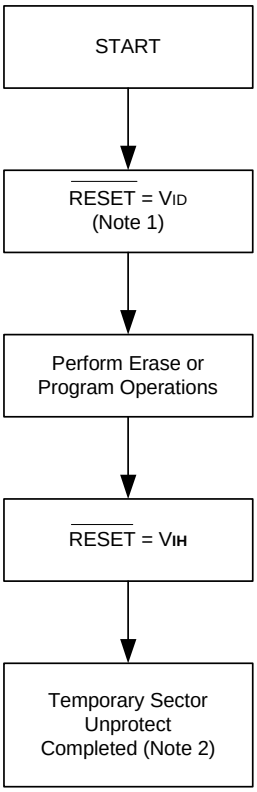
Write cycles are inhibited by holding any one of $\overline{OE}$ =V_{IL}, $\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IH}. To initiate a write cycle, $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

If $\overline{WE}$ = $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IH} during power up, the device does not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to reading array data on the initial power-up.

Temporary Sector Unprotect (N/A on A290021)

This feature allows temporary unprotection of previous protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the $\overline{RESET}$ pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the $\overline{RESET}$ pin, all the previously protected sectors are protected again. Figure 1 shows the algorithm, and the Temporary Sector Unprotect diagram shows the timing waveforms, for this feature.



Notes:
1. All protected sectors unprotected.
2. All previously protected sectors are protected once again.

Figure 1. Temporary Sector Unprotect Operation

Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. The Command Definitions table defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data.

All addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later. All data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Refer to the appropriate timing diagrams in the "AC Characteristics" section.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm. After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See "Erase Suspend/Erase Resume Commands" for more information on this mode.

The system must issue the reset command to re-enable the device for reading array data if I/O_5 goes high, or while in the autoselect mode. See the "Reset Command" section, next.

See also "Requirements for Reading Array Data" in the "Device Bus Operations" section for more information. The Read Operations table provides the read parameters, and Read Operation Timings diagram shows the timing diagram.

Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command. The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to reading array data (also applies to autoselect during Erase Suspend).

If I/O_5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. The Command Definitions table shows the address and data requirements. This method is an alternative to that shown in the Autoselect Codes (High Voltage Method) table, which is intended for PROM programmers and requires V_{ID} on address bit A9.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence.

A read cycle at address XX00h retrieves the manufacturer code and another read cycle at XX03h retrieves the continuation code. A read cycle at address XX01h returns the device code. A read cycle containing a sector address (SA) and the address 02h in returns 01h if that sector is protected, or 00h if it is unprotected. Refer to the Sector Address tables for valid sector addresses.

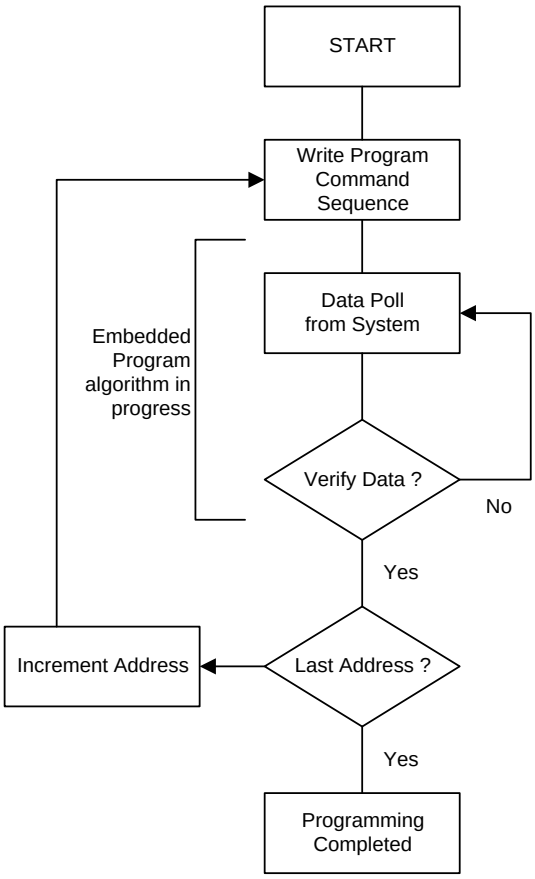
The system must write the reset command to exit the autoselect mode and return to reading array data.

Byte Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verify the programmed cell margin. The Command Definitions table shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using I/O_7 or I/O_6. See "Write Operation Status" for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Programming is allowed in any sequence and across sector boundaries. A bit cannot be programmed from a "0" back to a "1 ". Attempting to do so may halt the operation and set I/O_5 to "1", or cause the $\overline{Data}$ Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1".



Note : See the appropriate Command Definitions table for program command sequence.

Figure 2. Program Operation

Chip Erase Command Sequence

Chip erase is a six-bus-cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. The Command Definitions table shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored. The system can determine the status of the erase operation by using I/O_7, I/O_6, or I/O_2. See "Write Operation Status" for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 3 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in "AC Characteristics" for parameters, and to the Chip/Sector Erase Operation Timings for timing waveforms.

Sector Erase Command Sequence

Sector erase is a six-bus-cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. The Command Definitions table shows the address and data requirements for the sector erase command sequence.

The device does not require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50μs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50μs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50μs, the system need not monitor I/O_3. Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data. The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor I/O_3 to determine if the sector erase timer has timed out. (See the " I/O_3: Sector Erase Timer" section.) The time-out begins from the rising edge of the final $\overline{WE}$ pulse in the command sequence.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using I/O_7, I/O_6, or I/O_2. Refer to "Write Operation Status" for information on these status bits.

Figure 3 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the "AC Characteristics" section for parameters, and to the Sector Erase Operations Timing diagram for timing waveforms.

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50μs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase

operation. Addresses are "don't cares" when writing the Erase Suspend command.

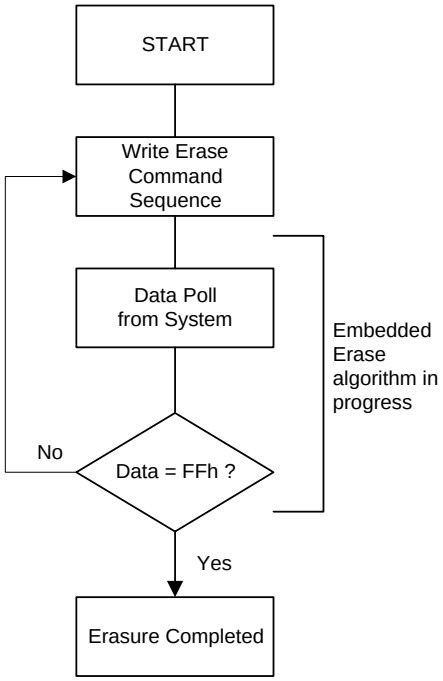
When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20μs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on I/O_7 - I/O_0. The system can use I/O_7, or I/O_6 and I/O_2 together, to determine if a sector is actively erasing or is erase-suspended. See "Write Operation Status" for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the I/O_7 or I/O_6 status bits, just as in the standard program operation. See "Write Operation Status" for more information.

The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See "Autoselect Command Sequence" for more information.

The system must write the Erase Resume command (address bits are "don't care") to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.



Note :
1. See the appropriate Command Definitions table for erase command sequences.
2. See "I/O_3 : Sector Erase Timer" for more information.

Figure 3. Erase Operation

Table 5. A29002/A290021 Command Definitions

Command Sequence (Note 1)			Cycles	Bus Cycles (Notes 2 - 4)											
				First		Second		Third		Fourth		Fifth		Sixth	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 5)			1	RA	RD										
Reset (Note 6)			1	XXX	F0										
Autoselect (Note 7)	Manufacturer ID		4	555	AA	2AA	55	555	90	X00	37				
	Device ID	Top	4	555	AA	2AA	55	555	90	X01	8C				
		Bottom									0D				
	Continuation ID		4	555	AA	2AA	55	555	90	X03	7F				
	Sector Protect Verify (Note 8)		4	555	AA	2AA	55	555	90	SA X02	00				
											01				
Program			4	555	AA	2AA	55	555	A0	PA	PD				
Chip Erase			6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase			6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend (Note 9)			1	XXX	B0										
Erase Resume (Note 10)			1	XXX	30										

Legend:
X = Don't care
RA = Address of the memory location to be read.
RD = Data read from location RA during read operation.
PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the $\overline{WE}$ or $\overline{CE}$ pulse, whichever happens later.
PD = Data to be programmed at location PA. Data latches on the rising edge of $\overline{WE}$ or $\overline{CE}$ pulse, whichever happens first.
SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A17 - A13 select a unique sector.

Note:
1. See Table 1 for description of bus operations.
2. All values are in hexadecimal.
3. Except when reading array or autoselect data, all bus cycles are write operation.
4. Address bits A17 - A12 are don't cares for unlock and command cycles, unless SA or PA required.
5. No unlock or command cycles required when reading array data.
6. The Reset command is required to return to reading array data when device is in the autoselect mode, or if I/O_5 goes high (while the device is providing status data).
7. The fourth cycle of the autoselect command sequence is a read cycle.
8. The data is 00h for an unprotected sector and 01h for a protected sector. See "Autoselect Command Sequence" for more information.
9. The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode.
10. The Erase Resume command is valid only during the Erase Suspend mode.
11. The time between each command cycle has to be less than 50μs.

Write Operation Status

Several bits, I/O_2, I/O_3, I/O_5, I/O_6, and I/O_7, are provided in the A29002/A290021 to determine the status of a write operation. Table 6 and the following subsections describe the functions of these status bits. I/O_7, I/O_6 and I/O_2 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

I/O_7: $\overline{\text{Data}}$ Polling

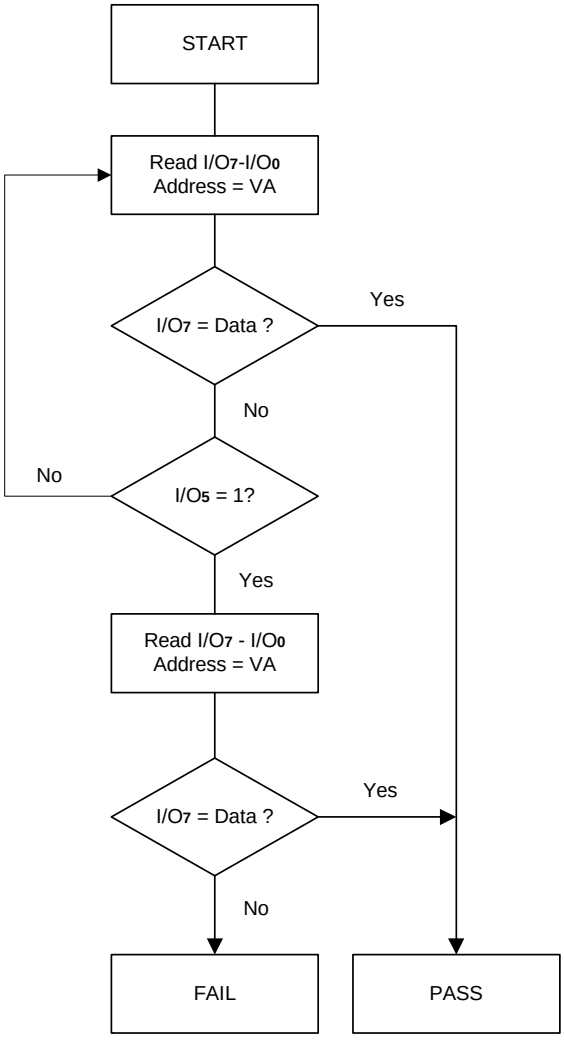
The $\overline{\text{Data}}$ Polling bit, I/O_7, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. $\overline{\text{Data}}$ Polling is valid after the rising edge of the final $\overline{\text{WE}}$ pulse in the program or erase command sequence.

During the Embedded Program algorithm, the device outputs on I/O_7 the complement of the datum programmed to I/O_7. This I/O_7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to I/O_7. The system must provide the program address to read valid status information on I/O_7. If a program address falls within a protected sector, $\overline{\text{Data}}$ Polling on I/O_7 is active for approximately 2μs, then the device returns to reading array data.

During the Embedded Erase algorithm, $\overline{\text{Data}}$ Polling produces a "0" on I/O_7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, $\overline{\text{Data}}$ Polling produces a "1" on I/O_7.This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to "1"; prior to this, the device outputs the "complement," or "0." The system must provide an address within any of the sectors selected for erasure to read valid status information on I/O_7.

After an erase command sequence is written, if all sectors selected for erasing are protected, $\overline{\text{Data}}$ Polling on I/O_7 is active for approximately 100μs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects I/O_7 has changed from the complement to true data, it can read valid data at I/O_7 - I/O_0 on the following read cycles. This is because I/O_7 may change asynchronously with I/O_0 - I/O_6 while Output Enable ($\overline{\text{OE}}$) is asserted low. The $\overline{\text{Data}}$ Polling Timings (During Embedded Algorithms) figure in the "AC Characteristics" section illustrates this. Table 6 shows the outputs for $\overline{\text{Data}}$ Polling on I/O_7. Figure 4 shows the $\overline{\text{Data}}$ Polling algorithm.



Note :
1. VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.
2. I/O_7 should be rechecked even if I/O_5 = "1" because I/O_7 may change simultaneously with I/O_5.

Figure 4. $\overline{\text{Data}}$ Polling Algorithm

I/O6: Toggle Bit I

Toggle Bit I on I/O6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause I/O6 to toggle. (The system may use either $\overline{OE}$ or $\overline{CE}$ to control the read cycles.) When the operation is complete, I/O6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, I/O6 toggles for approximately 100μs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use I/O6 and I/O2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), I/O6 toggles. When the device enters the Erase Suspend mode, I/O6 stops toggling. However, the system must also use I/O2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use I/O7 (see the subsection on " I/O7: $\overline{Data}$ Polling").

If a program address falls within a protected sector, I/O6 toggles for approximately 2μs after the program command sequence is written, then returns to reading array data.

I/O6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

The Write Operation Status table shows the outputs for Toggle Bit I on I/O6. Refer to Figure 5 for the toggle bit algorithm, and to the Toggle Bit Timings figure in the "AC Characteristics" section for the timing diagram. The I/O2 vs. I/O6 figure shows the differences between I/O2 and I/O6 in graphical form. See also the subsection on " I/O2: Toggle Bit II".

I/O2: Toggle Bit II

The "Toggle Bit II" on I/O2, when used with I/O6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence.

I/O2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either $\overline{OE}$ or $\overline{CE}$ to control the read cycles.) But I/O2 cannot distinguish whether the sector is actively erasing or is erase-suspended. I/O6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 6 to compare outputs for I/O2 and I/O6.

Figure 5 shows the toggle bit algorithm in flowchart form, and the section " I/O2: Toggle Bit II" explains the algorithm. See also the " I/O6: Toggle Bit I" subsection. Refer to the Toggle Bit Timings figure for the toggle bit timing diagram. The I/O2 vs. I/O6 figure shows the differences between I/O2 and I/O6 in graphical form.

Reading Toggle Bits I/O6, I/O2

Refer to Figure 5 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read I/O7 - I/O0 at least twice in a row to determine whether a toggle bit is toggling. Typically, a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on I/O7 - I/O0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of I/O5 is high (see the section on I/O5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as I/O5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and I/O5 has not gone high. The system may continue to monitor the toggle bit and I/O5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 5).

I/O5: Exceeded Timing Limits

I/O5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions I/O5 produces a "1." This is a failure condition that indicates the program or erase cycle was not successfully completed.

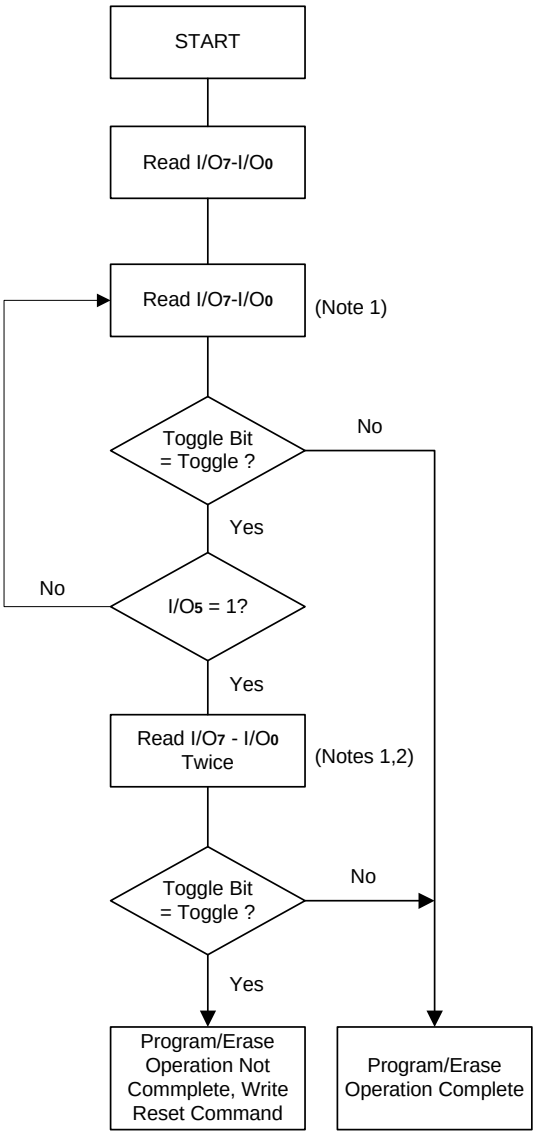
The I/O5 failure condition may appear if the system tries to program a "1 "to a location that is previously programmed to "0." Only an erase operation can change a "0" back to a "1." Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, I/O5 produces a "1."

Under both these conditions, the system must issue the reset command to return the device to reading array data.

I/O3: Sector Erase Timer

After writing a sector erase command sequence, the system may read I/O3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, I/O3 switches from "0" to "1." The system may ignore I/O3 if the system can guarantee that the time between additional sector erase commands will always be less than 50μs. See also the "Sector Erase Command Sequence" section.

After the sector erase command sequence is written, the system should read the status on I/O7 (Data Polling) or I/O6 (Toggle Bit 1) to ensure the device has accepted the command sequence, and then read I/O3. If I/O3 is "1", the internally controlled erase cycle has begun; all further commands (other than Erase Suspend) are ignored until the erase operation is complete. If I/O3 is "0", the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of I/O3 prior to and following each subsequent sector erase command. If I/O3 is high on the second status check, the last command might not have been accepted. Table 6 shows the outputs for I/O3.



Notes :
1. Read toggle bit twice to determine whether or not it is toggling. See text.
2. Recheck toggle bit because it may stop toggling as I/O5 changes to "1". See text.

Figure 5. Toggle Bit Algorithm

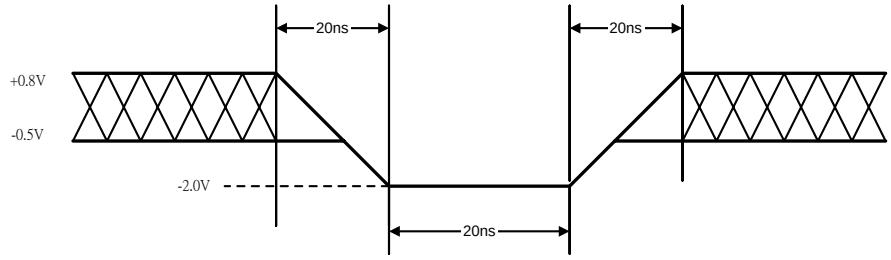
Table 6. Write Operation Status

Operation		I/O_7 (Note 1)	I/O_6	I/O_5 (Note 2)	I/O_3	I/O_2 (Note 1)
Standard Mode	Embedded Program Algorithm	$\overline{I/O_7}$	Toggle	0	N/A	No toggle
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No toggle	0	N/A	Toggle
	Reading within Non-Erase Suspend Sector	Data	Data	Data	Data	Data
	Erase-Suspend-Program	$\overline{I/O_7}$	Toggle	0	N/A	N/A

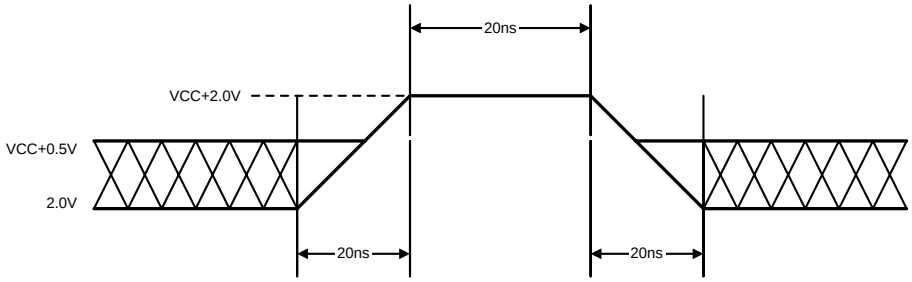
Notes:

1. I/O_7 and I/O_2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
2. I/O_5 switches to "1" when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See "I/O5: Exceeded Timing Limits" for more information.

Maximum Negative Input Overshoot



Maximum Positive Input Overshoot



DC Characteristics

TTL/NMOS Compatible

Parameter Symbol	Parameter Description	Test Description	Min.	Typ.	Max.	Unit
I_{LI}	Input Load Current	V_{IN} = VSS to VCC. VCC = VCC Max			±1.0	µA
I_{LIT}	A9, $\overline{OE}$ & $\overline{RESET}$ Input Load Current	VCC = VCC Max, A9, $\overline{OE}$ & $\overline{RESET}$=12.5V			100	µA
I_{LO}	Output Leakage Current	V_{OUT} = VSS to VCC. VCC = VCC Max			±1.0	µA
I_{CC1}	VCC Active Read Current (Notes 1, 2)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		20	30	mA
I_{CC2}	VCC Active Write (Program/Erase) Current (Notes 2, 3, 4)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ =V_{IH}		30	40	mA
I_{CC3}	VCC Standby Current (Note 2)	$\overline{CE}$ = V_{IH}, $\overline{RESET}$= VCC ± 0.5V		0.4	1.0	mA
V_{IL}	Input Low Level		-0.5		0.8	V
V_{IH}	Input High Level		2.0		VCC+0.5	V
V_{ID}	Voltage for Autoselect and Temporary Unprotect Sector	VCC = 5.25 V	10.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12mA, VCC = VCC Min			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -2.5 mA, VCC = VCC Min	2.4			V

CMOS Compatible

Parameter Symbol	Parameter Description	Test Description	Min.	Typ.	Max.	Unit
I_{LI}	Input Load Current	V_{IN} = VSS to VCC, VCC = VCC Max			±1.0	µA
I_{LIT}	A9, $\overline{OE}$ & $\overline{RESET}$ Input Load Current	VCC = VCC Max, A9, $\overline{OE}$ & $\overline{RESET}$= 12.5V			100	µA
I_{LO}	Output Leakage Current	V_{OUT} = VSS to VCC, VCC = VCC Max			±1.0	µA
I_{CC1}	VCC Active Read Current (Notes 1,2)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		20	30	mA
I_{CC2}	VCC Active Program/Erase Current (Notes 2,3,4)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		30	40	mA
I_{CC3}	VCC Standby Current (Notes 2, 5)	$\overline{CE}$ = $\overline{RESET}$ = VCC ± 0.5 V		1	5	µA
V_{IL}	Input Low Level		-0.5		0.8	V
V_{IH}	Input High Level		0.7 x VCC		VCC+0.3	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	VCC = 5.25 V	10.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12.0 mA, VCC = VCC Min			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -2.5 mA, VCC = VCC Min	0.85 x VCC			V
V_{OH2}		I_{OH} = -100 µA. VCC = VCC Min	VCC-0.4			V

Notes for DC characteristics (both tables):
1. The I_{CC} current listed includes both the DC operation current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.
2. Maximum I_{CC} specifications are tested with VCC = VCC max.
3. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
4. Not 100% tested.
5. For CMOS mode only, I_{CC3} = 20µA max at extended temperatures (> +85°C).
6. $\overline{RESET}$ is not available on A290021.

AC Characteristics

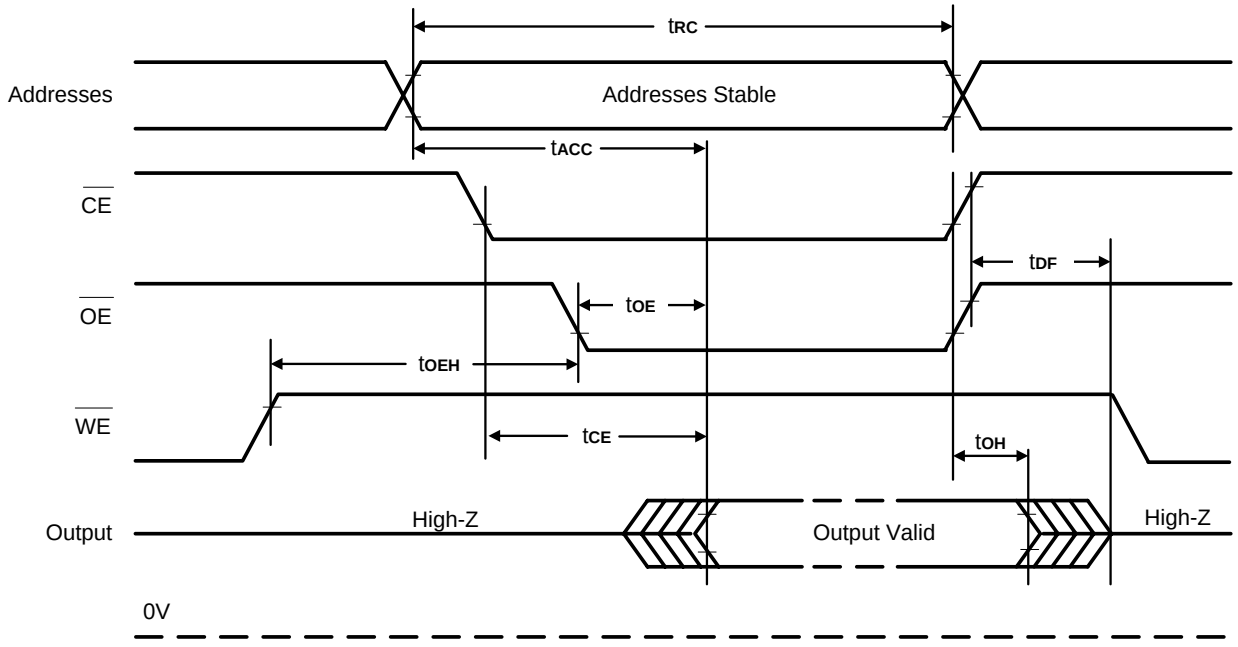
Read Only Operations

Parameter Symbols		Description		Test Setup		Speed					Unit
JEDEC	Std					-55	-70	-90	-120	-150	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 2)			Min.	55	70	90	120	150	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		$\overline{CE}$ = V_{IL} $\overline{OE}$ = V_{IL}	Max.	55	70	90	120	150	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		$\overline{OE}$ = V_{IL}	Max.	55	70	90	120	150	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max.	30	30	35	50	55	ns
	t_{OEH}	Output Enable Hold Time (Note 2)	Read		Min.	0	0	0	0	0	ns
			Toggle and $\overline{Data}$ Polling		Min.	10	10	10	10	10	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Notes 1,2)			Max.	18	20	20	30	35	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 1,2)				18	20	20	30	35	ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First			Min.	0	0	0	0	0	ns

Notes:

1. Output driver disable time.
2. Not 100% tested.

Timing Waveforms for Read Only Operation ($\overline{RESET}$ = V_{IH} on A29002)

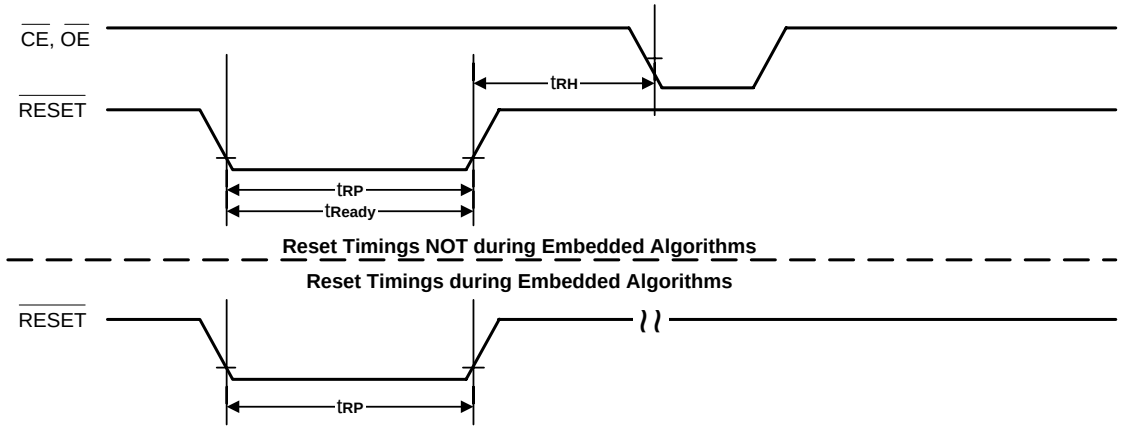


Hardware Reset ($\overline{RESET}$) (N/A on A290021)

Parameter		Description	Test Setup		All Speed Options	Unit
JEDEC	Std					
	t_{READY}	$\overline{RESET}$ Pin Low (During Embedded Algorithms) to Read or Write (See Note)		Max	20	µs
	t_{READY}	$\overline{RESET}$ Pin Low (Not During Embedded Algorithms) to Read or Write (See Note)		Max	500	ns
	t_{RP}	$\overline{RESET}$ Pulse Width		Min	500	ns
	t_{RH}	$\overline{RESET}$ High Time Before Read (See Note)		Min	50	ns

Note: Not 100% tested.

$\overline{RESET}$ Timings

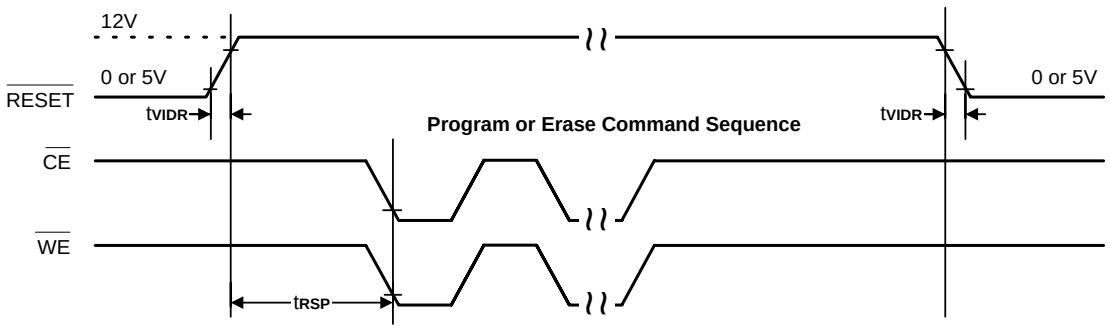


Temporary Sector Unprotect (N/A on A290021)

Parameter		Description			All Speed Options	Unit
JEDEC	Std					
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)		Min	500	ns
	t_{RSP}	$\overline{RESET}$ Setup Time for Temporary Sector Unprotect		Min	4	µs

Note: Not 100% tested.

Temporary Sector Unprotect Timing Diagram



AC Characteristics

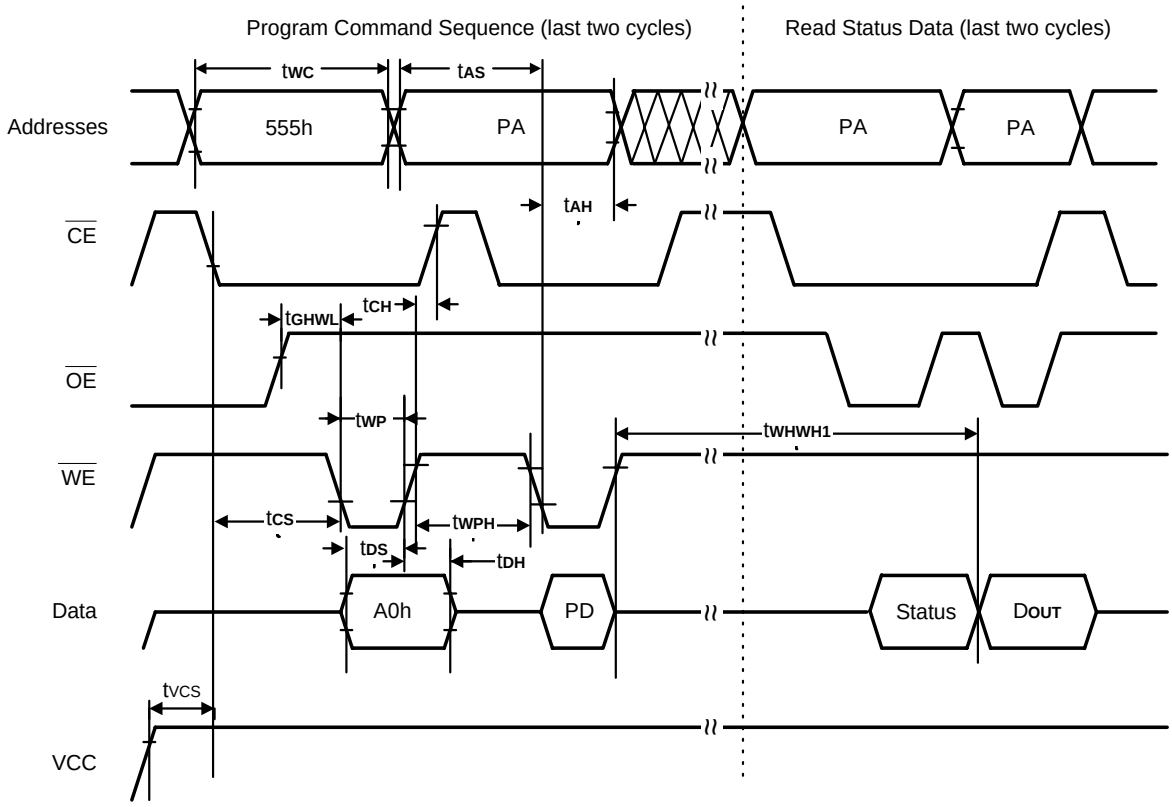
Erase and Program Operations

Parameter Symbols		Description		Speed					Unit
JEDEC	Std			-55	-70	-90	-120	-150	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min.	55	70	90	120	150	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min.	0					ns
t_{WLAX}	t_{AH}	Address Hold Time	Min.	40	45	45	50	50	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min.	25	30	45	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min.	0					ns
	t_{OES}	Output Enable Setup Time	Min.	0					ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write ($\overline{OE}$ high to $\overline{WE}$ low)	Min.	0					ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time	Min.	0					ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time	Min.	0					ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min.	30	35	45	50	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min.	20					ns
			Max.	50					µs
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation (Note 2)	Typ.	7					µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ.	1					sec
	t_{VCS}	VCC Set Up Time (Note 1)	Min.	50					µs

Notes:

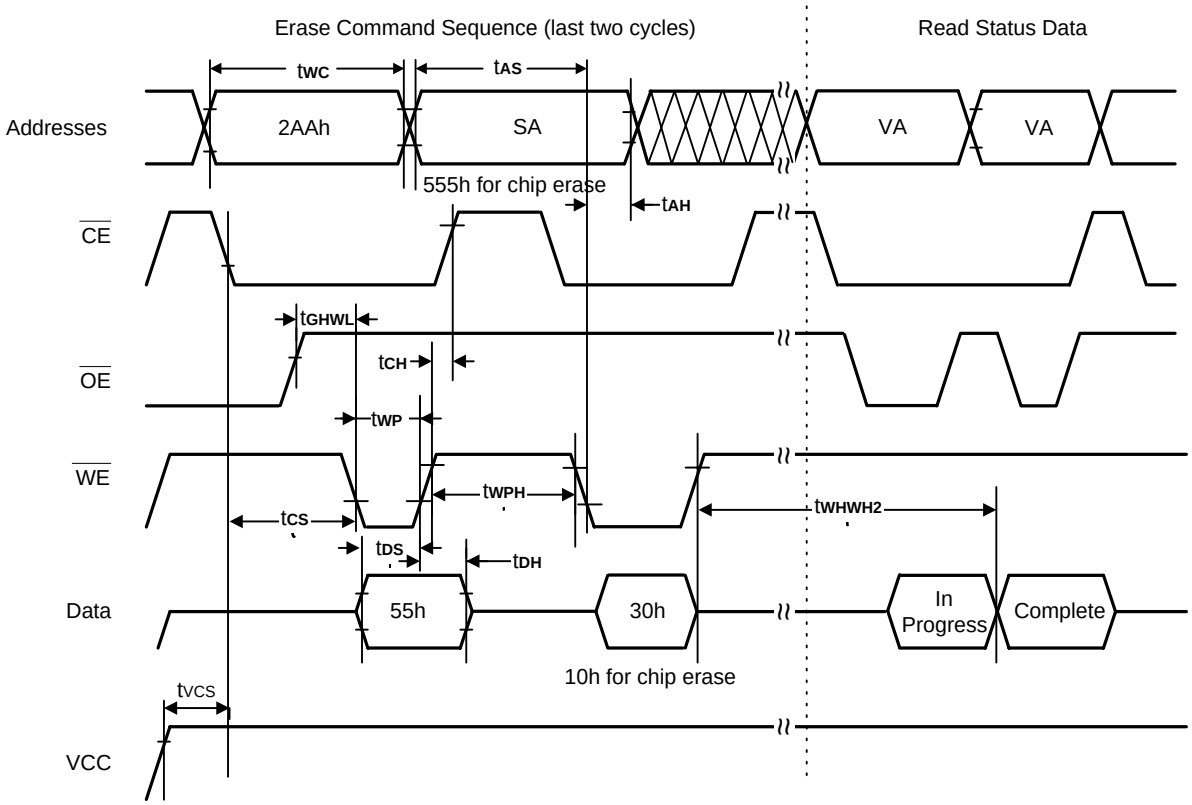
1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more information.

Timing Waveforms for Program Operation



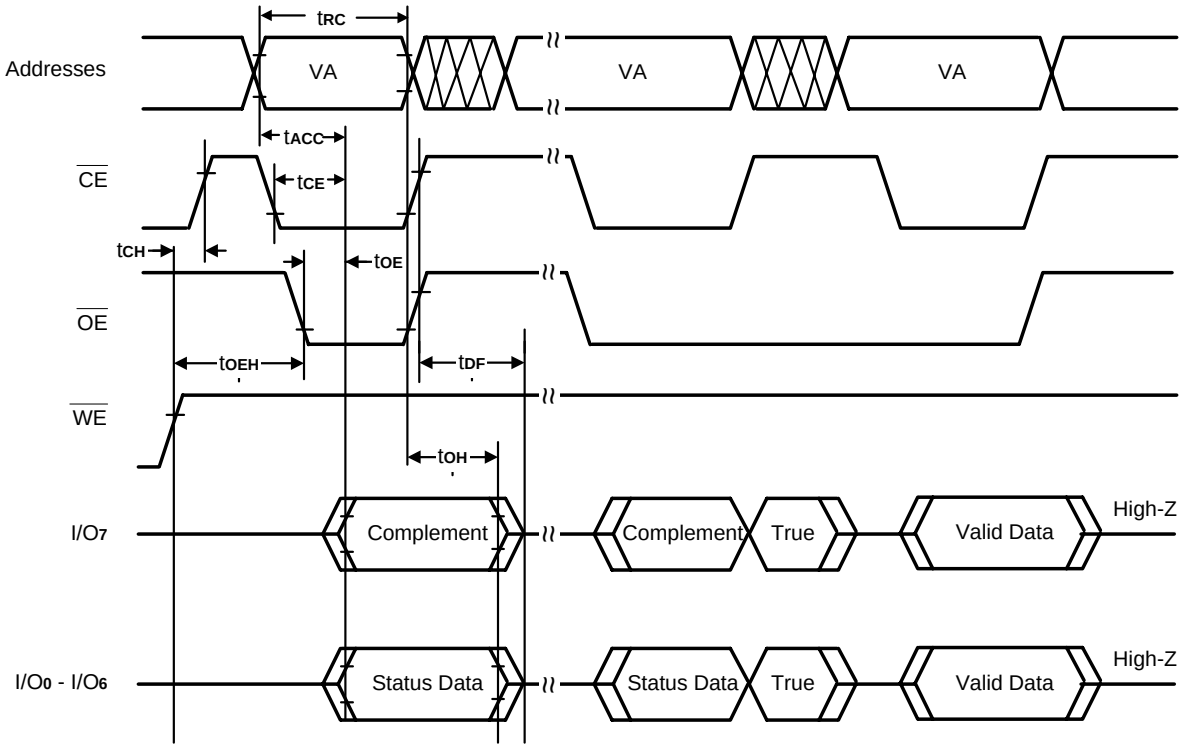
Note : PA = program addrss, PD = program data, Dout is the true data at the program address.

Timing Waveforms for Chip/Sector Erase Operation



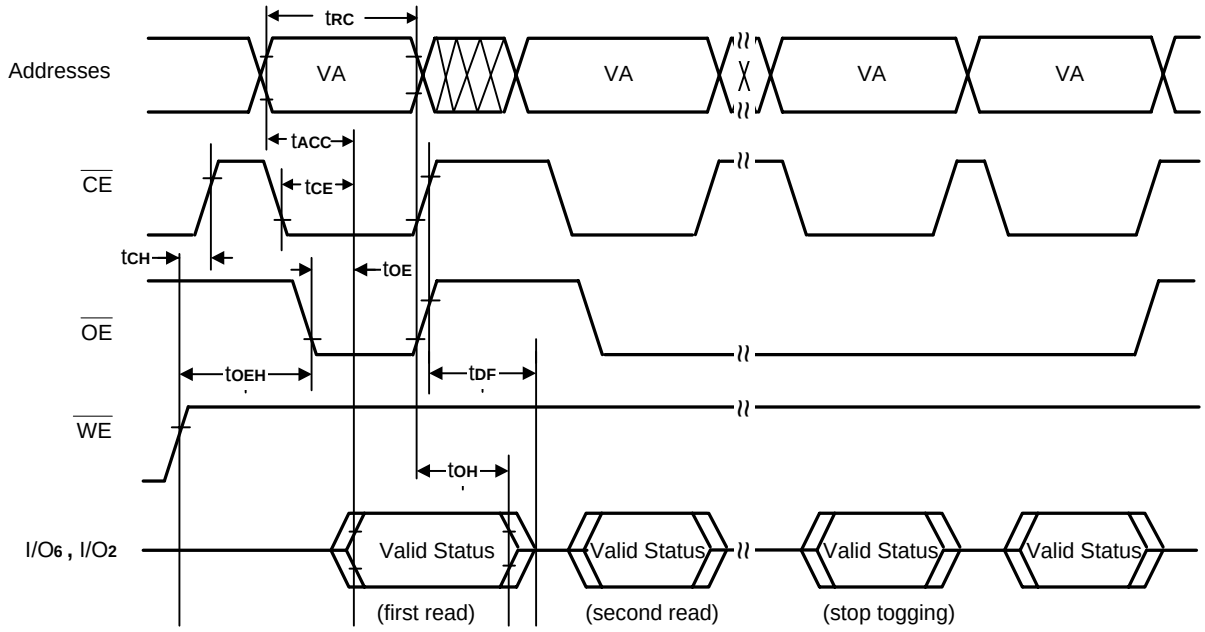
Note : SA = Sector Address. VA = Valid Address for reading status data.

Timing Waveforms for $\overline{\text{Data}}$ Polling (During Embedded Algorithms)



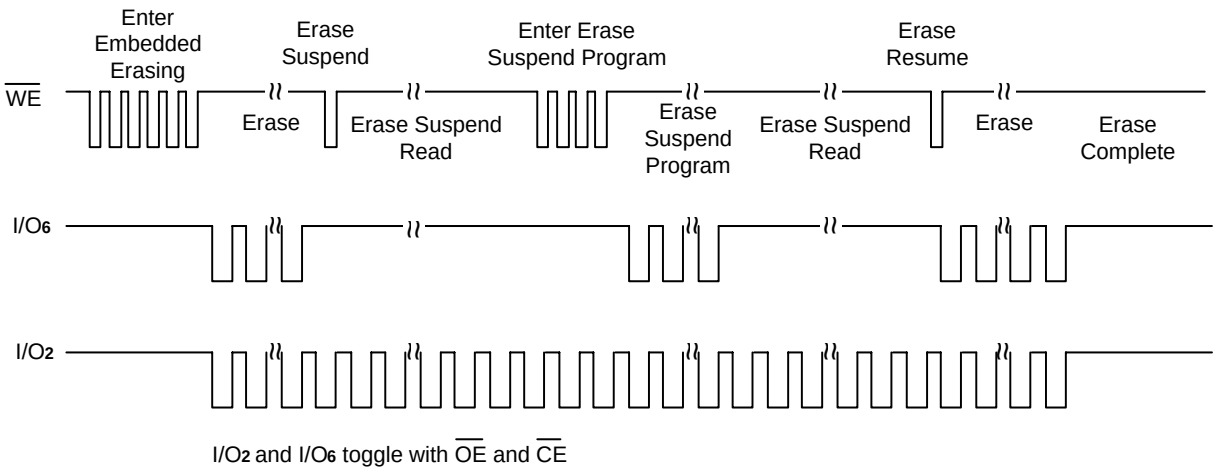
Note : VA = Valid Address. Illustation shows first status cycle after command sequence, last status read cycle, and array data read cycle.

Timing Waveforms for Toggle Bit (During Embedded Algorithms)



Note: VA = Valid Address; not required for I/O_6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

Timing Waveforms for I/O2 vs. I/O6



Note : Both I/O6 and I/O2 toggle with $\overline{OE}$ or $\overline{CE}$. See the text on I/O6 and I/O2 in the section "Write Operation Statue" for more information.

AC Characteristics

Erase and Program Operations

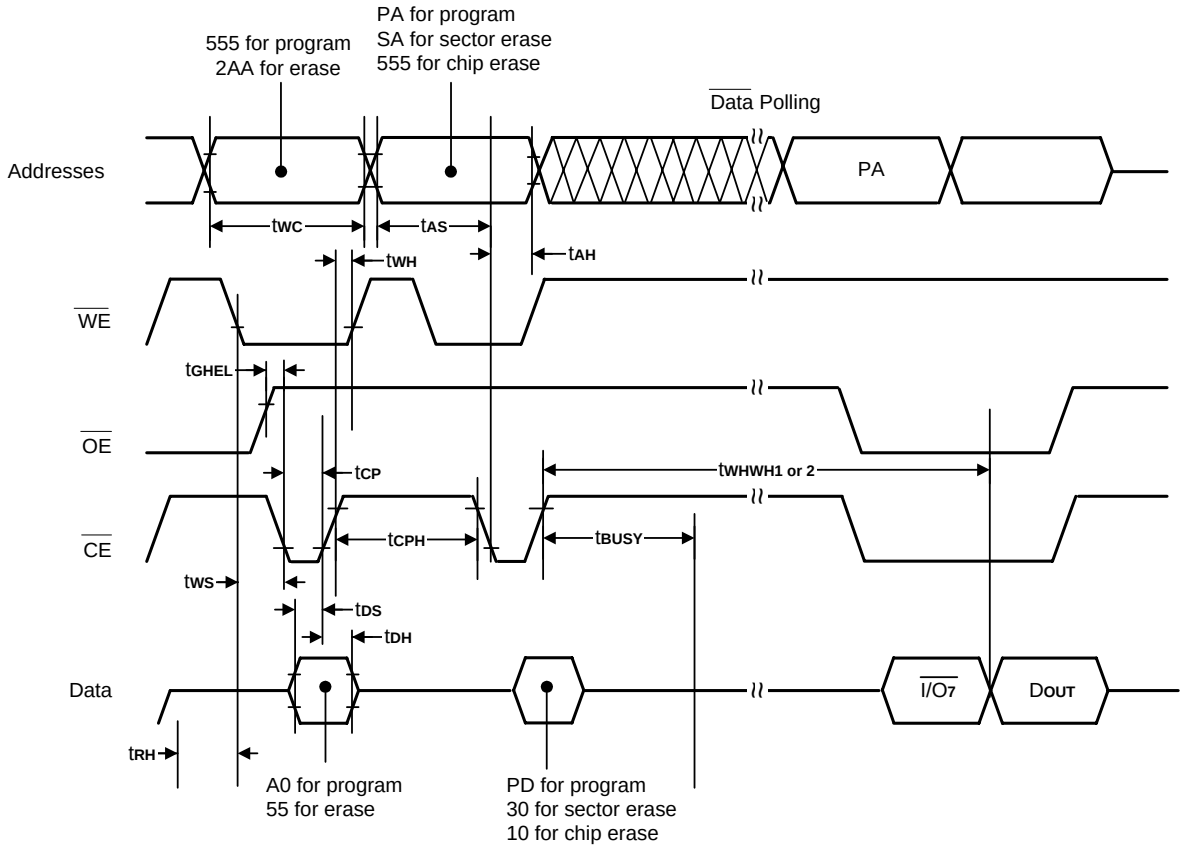
Alternate $\overline{CE}$ Controlled Writes

Parameter Symbols		Description		Speed					Unit
JEDEC	Std			-55	-70	-90	-120	-150	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min.	55	70	90	120	150	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min.	0					ns
t_{ELAX}	t_{AH}	Address Hold Time	Min.	40	45	45	50	50	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min.	25	30	45	50	50	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min.	0					ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write	Min.	0					ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time	Min.	0					ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time	Min.	0					ns
t_{ELEH}	t_{CP}	Write Pulse Width	Min.	30	35	45	50	50	ns
t_{EHEL}	t_{CPH}	Write Pulse Width High	Min.	20	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation (Note 2)	Typ.	7					µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ.	1					sec

Notes:

1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more information.

Timing Waveforms for Alternate $\overline{CE}$ Controlled Write Operation ($\overline{RESET}$ =V_{IH} on A29002)



Note :
1. PA = Program Address, PD = Program Data, SA = Sector Address, $\overline{I/O_7}$ = Complement of Data Input, D_{OUT} = Array Data.
2. Figure indicates the last two bus cycles of the command sequence.

Erase and Programming Performance

Parameter	Typ. (Note 1)	Max. (Note 2)	Unit	Comments
Sector Erase Time	1	8	sec	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time	8	64	sec	
Byte Programming Time	35	300	µs	Excludes system-level overhead (Note 5)
Chip Programming Time (Note 3)	3.6	10.8	sec	

Notes:
1. Typical program and erase times assume the following conditions: 25°C, 5.0V VCC, 100,000 cycles. Additionally, programming typically assumes checkerboard pattern.
2. Under worst case conditions of 90°C, VCC = 4.5V (4.75V for -55), 100,000 cycles.
3. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum byte program time listed. If the maximum byte program time given is exceeded, only then does the device set I/O_5 = 1. See the section on I/O_5 for further information.
4. In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.
5. System-level overhead is the time required to execute the four-bus-cycle command sequence for programming. See Table 4 for further information on command definitions.
6. The device has a guaranteed minimum erase and program cycle endurance of 100,000 cycles.

Latch-up Characteristics

Description	Min.	Max.
Input Voltage with respect to VSS on all I/O pins	-1.0V	VCC+1.0V
VCC Current	-100 mA	+100 mA
Input voltage with respect to VSS on all pins except I/O pins (including A9, $\overline{OE}$ and $\overline{RESET}$)	-1.0V	12.5V

Includes all pins except VCC. Test conditions: VCC = 5.0V, one pin at time. $\overline{RESET}$ N/A on A290021

TSOP Pin Capacitance

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN}=0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT}=0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN}=0	7.5	9	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0MHz

PLCC and P-DIP Pin Capacitance

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN}=0	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=0	8	12	pF
C_{IN2}	Control Pin Capacitance	V_{PP}=0	8	12	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0MHz

Data Retention

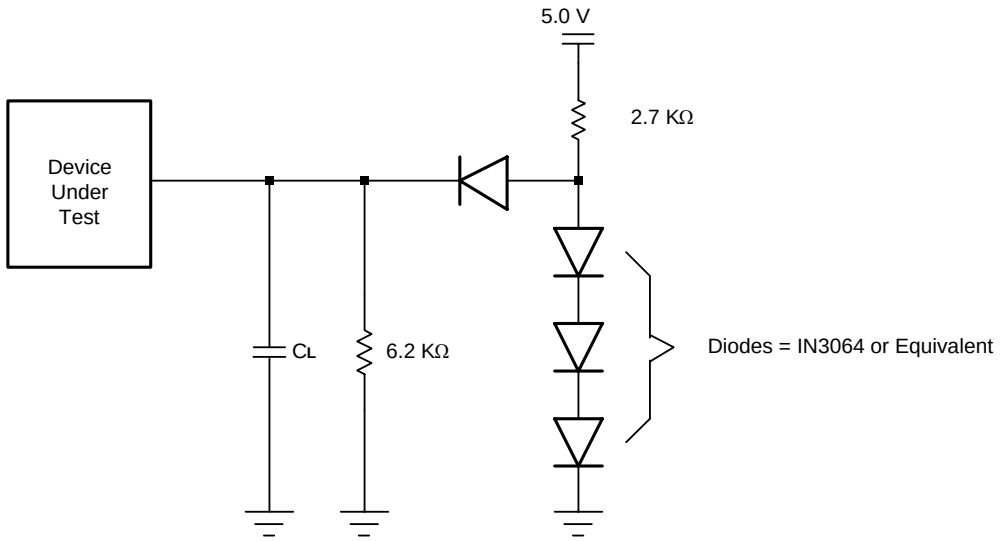
Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

Test Conditions

Test Specifications

Test Condition	-55	All others	Unit
Output Load	1 TTL gate		
Output Load Capacitance, C_L(including jig capacitance)	30	100	pF
Input Rise and Fall Times	5	20	ns
Input Pulse Levels	0.0 - 3.0	0.45 - 2.4	V
Input timing measurement reference levels	1.5	0.8, 2.0	V
Output timing measurement reference levels	1.5	0.8, 2.0	V

Test Setup



Ordering Information

Top Boot Sector Flash

Part No.	Access Time (ns)	Active Read Current Typ. (mA)	Program/Erase Current Typ. (mA)	Standby Current Typ. (μA)	Package
A29002T-55 A290021T-55	55	20	30	1	32Pin DIP
A29002T-55F A290021T-55F					32Pin Pb-Free DIP
A29002TL-55 A290021TL-55					32Pin PLCC
A29002TL-55F A290021TL-55F					32Pin Pb-Free PLCC
A29002TV-55 A290021TV-55					32Pin TSOP
A29002TV-55F A290021TV-55F					32Pin Pb-Free TSOP
A29002T-70 A290021T-70	70	20	30	1	32Pin DIP
A29002T-70F A290021T-70F					32Pin Pb-Free DIP
A29002TL-70 A290021TL-70					32Pin PLCC
A29002TL-70F A290021TL-70F					32Pin Pb-Free PLCC
A29002TV-70 A290021TV-70					32Pin TSOP
A29002TV-70F A290021TV-70F					32Pin Pb-Free TSOP
A29002T-90 A290021T-90	90	20	30	1	32Pin DIP
A29002T-90F A290021T-90F					32Pin Pb-Free DIP
A29002TL-90 A290021TL-90					32Pin PLCC
A29002TL-90F A290021TL-90F					32Pin Pb-Free PLCC
A29002TV-90 A290021TV-90					32Pin TSOP
A29002TV-90F A290021TV-90F					32Pin Pb-Free TSOP

Ordering Information (continued)

Top Boot Sector Flash

Part No.	Access Time (ns)	Active Read Current Typ. (mA)	Program/Erase Current Typ. (mA)	Standby Current Typ. (μA)	Package
A29002T-120 A290021T-120	120	20	30	1	32Pin DIP
A29002T-120F A290021T-120F					32Pin Pb-Free DIP
A29002TL-120 A290021TL-120					32Pin PLCC
A29002TL-120F A290021TL-120F					32Pin Pb-Free PLCC
A29002TV-120 A290021TV-120					32Pin TSOP
A29002TV-120F A290021TV-120F					32Pin Pb-Free TSOP
A29002T-150 A290021T-150	150	20	30	1	32Pin DIP
A29002T-150F A290021T-150F					32Pin Pb-Free DIP
A29002TL-150 A290021TL-150					32Pin PLCC
A29002TL-150F A290021TL-150F					32Pin Pb-Free PLCC
A29002TV-150 A290021TV-150					32Pin TSOP
A29002TV-150F A290021TV-150F					32Pin Pb-Free TSOP

Ordering Information (continued)

Bottom Boot Sector Flash

Part No.	Access Time (ns)	Active Read Current Typ. (mA)	Program/Erase Current Typ. (mA)	Standby Current Typ. (μA)	Package
A29002U-55 A290021U-55	55	20	30	1	32Pin DIP
A29002U-55F A290021U-55F					32Pin Pb-Free DIP
A29002UL-55 A290021UL-55					32Pin PLCC
A29002UL-55F A290021UL-55F					32Pin Pb-Free PLCC
A29002UV-55 A290021UV-55					32Pin TSOP
A29002UV-55F A290021UV-55F					32Pin Pb-Free TSOP
A29002U-70 A290021U-70	70	20	30	1	32Pin DIP
A29002U-70F A290021U-70F					32Pin Pb-Free DIP
A29002UL-70 A290021UL-70					32Pin PLCC
A29002UL-70F A290021UL-70F					32Pin Pb-Free PLCC
A29002UV-70 A290021UV-70					32Pin TSOP
A29002UV-70F A290021UV-70F					32Pin Pb-Free TSOP
A29002U-90 A290021U-90	90	20	30	1	32Pin DIP
A29002U-90F A290021U-90F					32Pin Pb-Free DIP
A29002UL-90 A290021UL-90					32Pin PLCC
A29002UL-90F A290021UL-90F					32Pin Pb-Free PLCC
A29002UV-90 A290021UV-90					32Pin TSOP
A29002UV-90F A290021UV-90F					32Pin Pb-Free TSOP

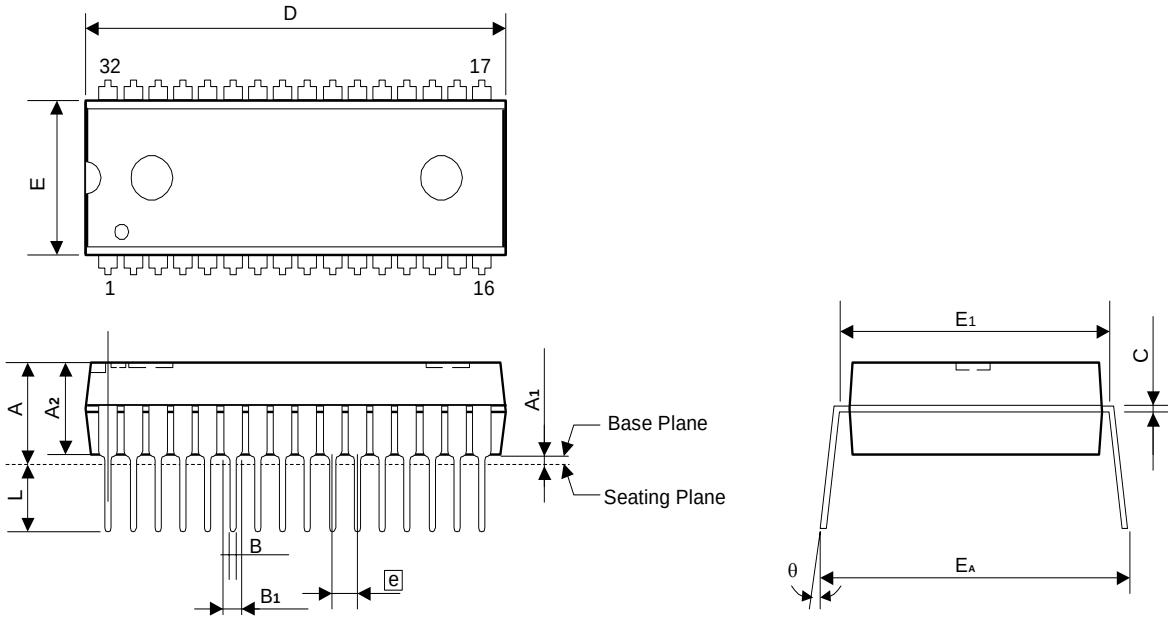
Ordering Information (continued)

Bottom Boot Sector Flash

Part No.	Access Time (ns)	Active Read Current Typ. (mA)	Program/Erase Current Typ. (mA)	Standby Current Typ. (μA)	Package
A29002U-120 A290021U-120	120	20	30	1	32Pin DIP
A29002U-120F A290021U-120F					32Pin Pb-Free DIP
A29002UL-120 A290021UL-120					32Pin PLCC
A29002UL-120F A290021UL-120F					32Pin Pb-Free PLCC
A29002UV-120 A290021UV-120					32Pin TSOP
A29002UV-120F A290021UV-120F					32Pin Pb-Free TSOP
A29002U-150 A290021U-150	150	20	30	1	32Pin DIP
A29002U-150F A290021U-150F					32Pin Pb-Free DIP
A29002UL-150 A290021UL-150					32Pin PLCC
A29002UL-150F A290021UL-150F					32Pin Pb-Free PLCC
A29002UV-150 A290021UV-150					32Pin TSOP
A29002UV-150F A290021UV-150F					32Pin Pb-Free TSOP

Package Information

P-DIP 32L Outline Dimensions unit: inches/mm



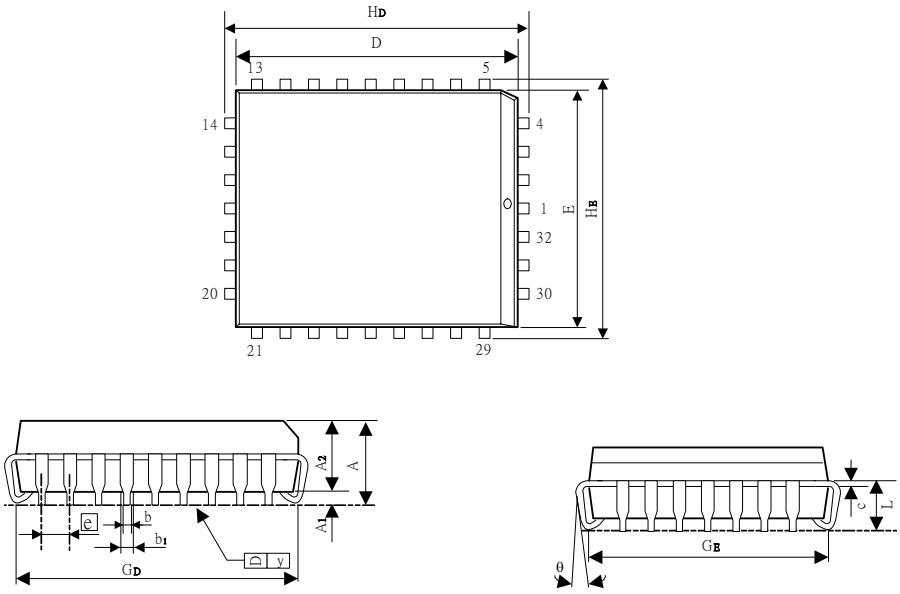
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.210	-	-	5.334
A_1	0.015	-	-	0.381	-	-
A_2	0.149	0.154	0.159	3.785	3.912	4.039
B	-	0.018	-	-	0.457	-
B_1	-	0.050	-	-	1.270	-
C	-	0.010	-	-	0.254	-
D	1.645	1.650	1.655	41.783	41.91	42.037
E	0.537	0.542	0.547	13.64	13.767	13.894
E_1	0.590	0.600	0.610	14.986	15.240	15.494
E_A	0.630	0.650	0.670	16.002	16.510	17.018
e	-	0.100	-	-	2.540	-
L	0.120	0.130	0.140	3.048	3.302	3.556
θ	0°	-	15°	0°	-	15°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.

Package Information

PLCC 32L Outline Dimension

unit: inches/mm



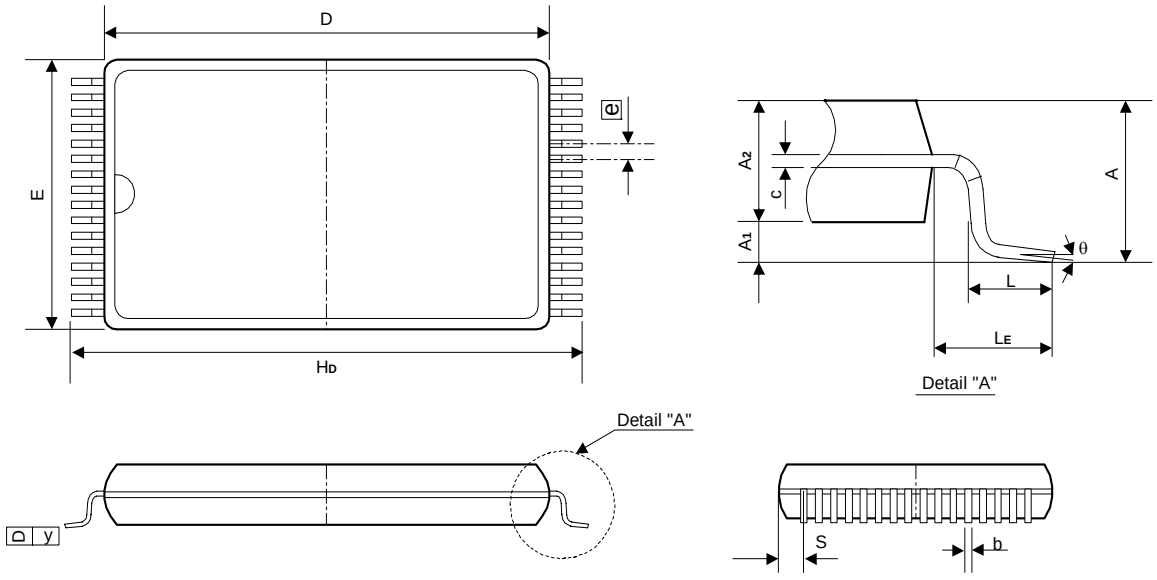
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.134	-	-	3.40
A_1	0.0185	-	-	0.47	-	-
A_2	0.105	0.110	0.115	2.67	2.80	2.93
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.021	0.41	0.46	0.54
C	0.008	0.010	0.014	0.20	0.254	0.35
D	0.547	0.550	0.553	13.89	13.97	14.05
E	0.447	0.450	0.453	11.35	11.43	11.51
e	0.044	0.050	0.056	1.12	1.27	1.42
G_D	0.490	0.510	0.530	12.45	12.95	13.46
G_E	0.390	0.410	0.430	9.91	10.41	10.92
H_D	0.585	0.590	0.595	14.86	14.99	15.11
H_E	0.485	0.490	0.495	12.32	12.45	12.57
L	0.075	0.090	0.095	1.91	2.29	2.41
y	-	-	0.003	-	-	0.075
θ	0°	-	10°	0°	-	10°

Notes:
1. Dimensions D and E do not include resin fins.
2. Dimensions G_D & G_E are for PC Board surface mount pad pitch design reference only.

Package Information

TSOP 32L TYPE I (8 X 20mm) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.009	0.011	0.18	0.22	0.27
c	0.004	-	0.008	0.11	-	0.20
D	0.720	0.724	0.728	18.30	18.40	18.50
E	-	0.315	0.319	-	8.00	8.10
e	0.020 BSC			0.50 BSC		
HD	0.779	0.787	0.795	19.80	20.00	20.20
L	0.016	0.020	0.024	0.40	0.50	0.60
LE	-	0.032	-	-	0.80	-
S	-	-	0.020	-	-	0.50
y	-	-	0.003	-	-	0.08
θ	0°	-	5°	0°	-	5°

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.