Integrated Circuit Systems, Inc.

ICS9158-07

Frequency Generator and Integrated Buffer

General Description

The **ICS9158-07** is a low-cost frequency generator designed specifically for desktop and notebook PC applications. Four copies of the CPU clock are available and four copies of the BUS clock are available, elimating the need for an external buffer.

Each high drive (25mA) output is capable of driving a 30pF load and has a typical duty cycle of 50/50. The clock outputs are skew-controlled to within ±250ps.

The **ICS9158-07** makes a gradual transition between frequencies, so that it meets the Intel cycle-to-cycle timing specification for 486 and Pentium systems.

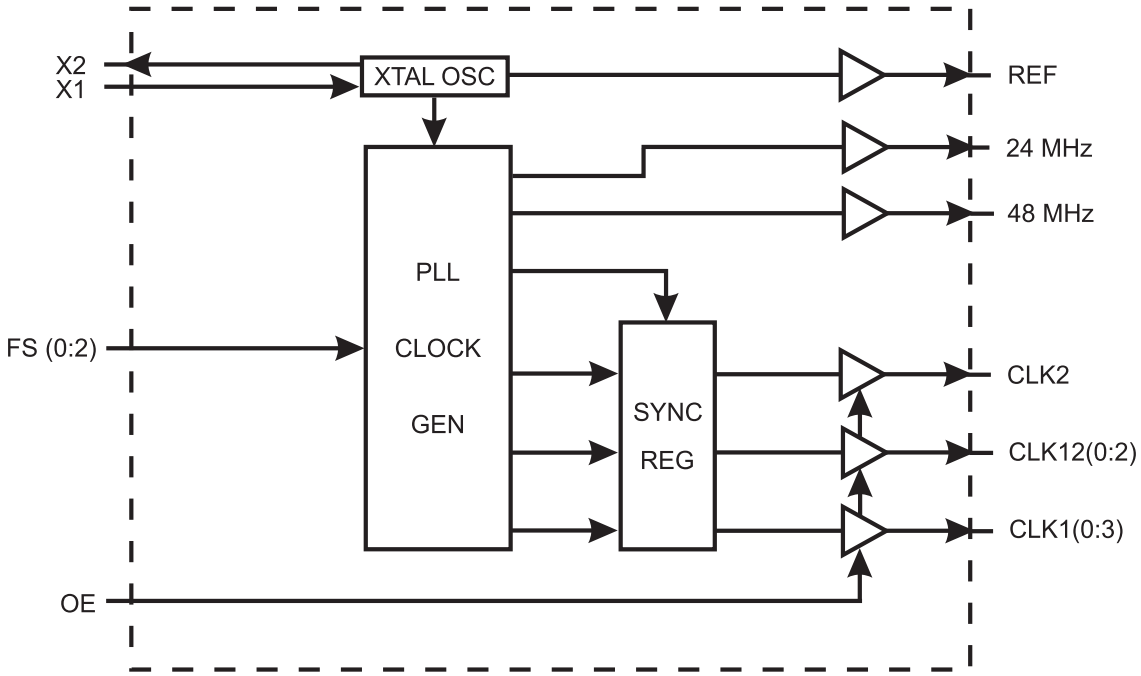
Features

- 8 skew-free, high drive CPU/BUS clocks
- Reference, floppy and keyboard clocks
- ±250ps skew between all outputs
- Less than ±250ps absolute jitter
- Outputs can drive up to 30pF load at 1.5V/ns
- 50±10% duty cycle
- Compatible with 486 and Pentium CPUs
- On-chip loop filter components
- 3.0V - 5.5V supply range
- 24-pin SOIC package

Applications

Ideal for RISC or CISC systems such as 486, Pentium,™ PowerPC,™ etc., requiring multiple CPU and BUS clocks.

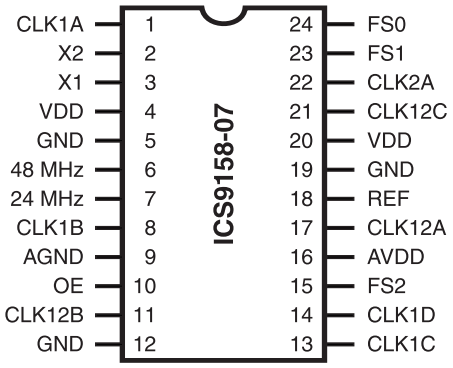
Block Diagram



Pentium is a trademark of Intel Corporation.
PowerPC is a trademark of Motorola Corporation.

NOTE: THIS DATA SHEET, ICS9158-07, IS AN ADDENDUM TO THE EXISTING ICS9158 DATA SHEET. ALL INFORMATION IN THIS DATA SHEET SUPERSEDES THE DATA FOUND IN THE ORIGINAL ICS9158 DATA SHEET.

Pin Configuration



24-Pin SOIC

Functionality

V_{DD}=5±10% or 3.3V±10%, TEMP=0-70°C

OE	FS2	FS1	FS0	CLK2 Ratio	CLK2 (Mhz)	CLK1(0:3) (Mhz)	CLK12(0:2) (MHz)
1	0	0	0	29/13 X1	31.9	16	31.9
1	0	0	1	29/13 X1	31.9	16	31.9
1	0	1	0	29/13 X1	31.9	16	31.9
1	0	1	1	29/13 X1	31.9	16	31.9
1	1	0	0	14/3 X1	66.8	33.4	66.8
1	1	0	1	7/2 X1	50.1	25	50.1
1	1	1	0	14/3 X1	66.8	33.4	66.8
1	1	1	1	21/5 X1	60.1	30	60.1
0	X	X	X	--	Tristate	Tristate	Tristate

Note 1: All frequencies in MHz, assuming 14.31818 MHz reference frequency.

Note 2: OE equals Low, tristates CLK2, CLK12(0:2), CLK1(0:3), the REF, 24 MHz and 48 MHz clocks keep running.

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 8, 13, 14	CLK1A	OUT	CPU clock 1 outputs.
2	X2	OUT	Crystal connection.
3	X1	IN	Crystal connection.
4	VDD	PWR	Digital POWER SUPPLY (+5V).
5, 12	GND	PWR	Digital GROUND/
6	48 MHz	OUT	48 MHz clock output.
7	24 MHz	OUT	24 MHz floppy disk/combination I/O clock output.
9	AGND	PWR	ANALOG GROUND.
10	OE	IN	OUTPUT ENABLE. Tristates all clock outputs when low.
11, 17, 21, 22	CLK12	OUT	CPU clock 12 outputs.
15	FS2	IN	CPU clock frequency select 2.
16	AVDD	PWR	ANALOG power supply (+5V).
18	REF	OUT	14.318 MHz reference clock output.
19	GND	PWR	Digital GROUND.
20	VDD	PWR	Digital POWER SUPPLY (+5V).
22	CLK2	OUT	CPU clock 2 outputs.
23	FS1	IN	CPU clock frequency select #1.
24	FS0	IN	CPU clock frequency select #0.

Absolute Maximum Ratings

AVDD, VDD referenced to GND 7V
Operating temperature under bias. . . . . 0°C to +70°C
Storage temperature . . . . . -40°C to +150°C
Voltage on I/O pins referenced to GND. . . . . GND -0.5V to VDD +0.5V
Power dissipation . . . . . 0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 5V

V_{DD} = +5V±10%, T_A=0°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		2.0			V
Input Low Current	I_{IL}	V_{IN}=0V	-5		5	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-5		5	µA
Output Low Voltage	V_{OL}	I_{OL}=20.0mA		0.25	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH}=-30mA	2.4	3.5		V
Output Low Current[1]	I_{OL}	V_{OL}=0.8V	45	65		mA
Output High Current[1]	I_{OH}	V_{OH}=2.0V		-55	-35	mA
Supply Current	I_{DD}	No load, 80 MHz		43	65	mA
Output Frequency Change over Supply and Temperature[1]	F_D	With respect to typical frequency		0.002	0.01	%
Short circuit current[1]	I_{SC}	Each output clock	25	56		mA
Pull-up resistor value[1]	R_{PU}	Input pin		680		kΩ
Input Capacitance[1]	C_i	Except X1, X2			8	pf
Load Capacitance[1]	C_L	Pins X1, X2		20		pf

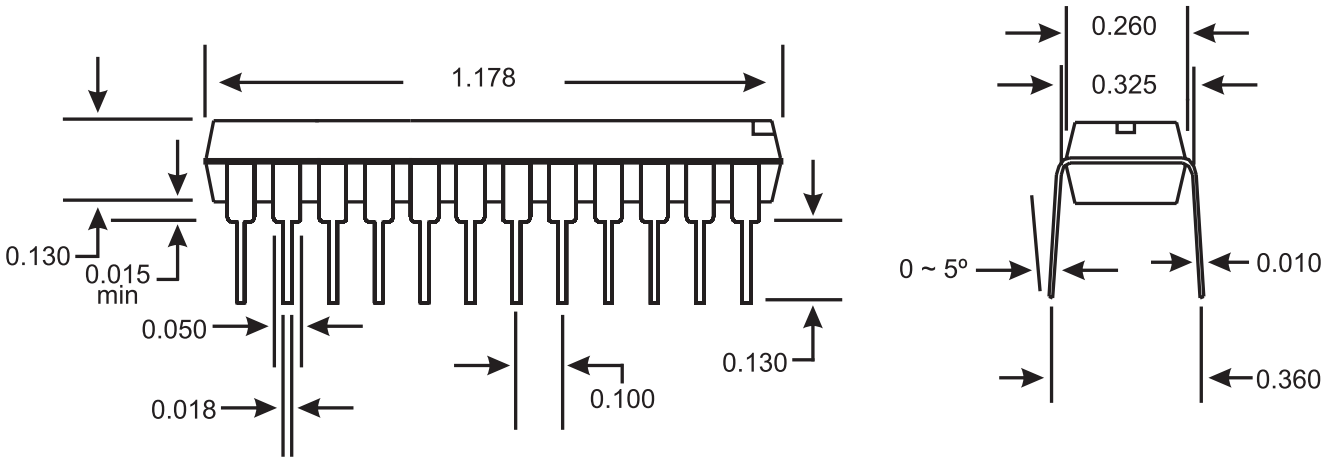
Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics *(continued)*

V_{DD} = +5V±10%, T_A=0°C to 70°C unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Rise time, 0.8 to 2.0V[1]	t_r	30pf load	-	1	2	ns
Rise time, 20% to 80% V_{DD}[1]	t_r	30pf load	-	2.5	3	ns
Output Fall time, 2.0 to 0.8V[1]	t_f	30pf load	-	0.5	1	ns
Fall time, 80% to 20% V_{DD}[1]	t_f	30pf load	-	1.5	2	ns
Duty cycle[1]	d_t	30pf load	45	50	55	%
Jitter, one sigma[1]	t_{j1s}	As compared with clock period	-	0.5	2.0	%
Jitter, absolute	t_{jab}		-	2	5	%
Jitter, absolute	t_{jab}	16-100 MHz clocks	-		500	ps
Input Frequency	f_i		-	14.318		MHz
Clock skew between CPU and 2XCPU outputs	T_{sk}		-	100	250	ps
Frequency Transition time[1]	t_{ft}	From 4 to 50 MHz	-	13	20	ms

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.



24-Pin DIP Package

Ordering Information

ICS9158-07N

Example:

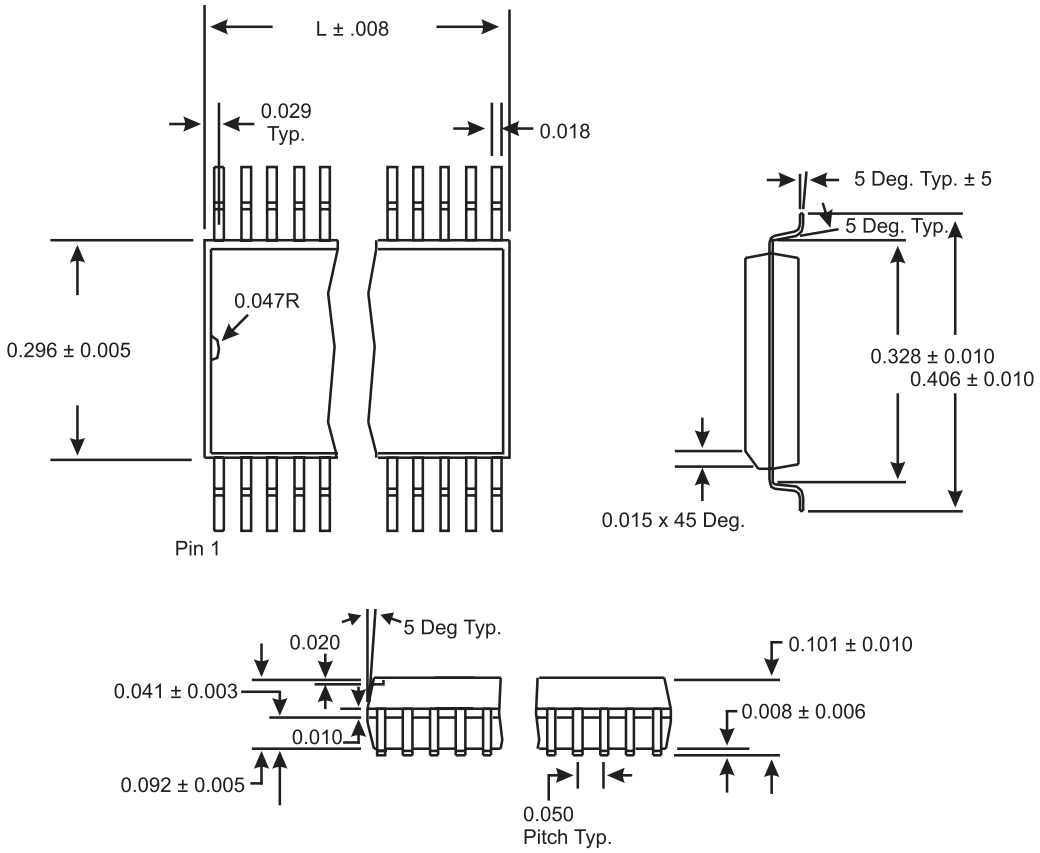
ICS XXXX-PPP M

Package Type
N=DIP (Plastic#)

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device



LEAD COUNT	24L
DIMENSION L	0.604

24-Pin SOIC (wide body

Ordering Information

ICS9158-07M

Example:

ICS XXXX-PPP M

Package Type
M=SOIC

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device