LXT304A

Low-Power T1/E1 Short-Haul Transceiver with Receive JA

General Description

The LXT304A is a fully integrated low-power transceiver for both North American 1.544 Mbps (T1), and International 2.048 Mbps (E1) applications. It features a constant low output impedance transmitter allowing for high transmitter return loss in T1/E1 applications. Transmit pulse shapes (DSX-1 or E1) are selectable for various line lengths and cable types.

The LXT304A provides receive jitter attenuation starting at 3 Hz, and is microprocessor controllable through a serial interface.

It offers a variety of diagnostic features including transmit and receive monitoring. The device incorporates an on-chip crystal oscillator, and also accepts digital clock inputs. It uses an advanced double-poly, double-metal CMOS process and requires only a single 5-volt power supply.

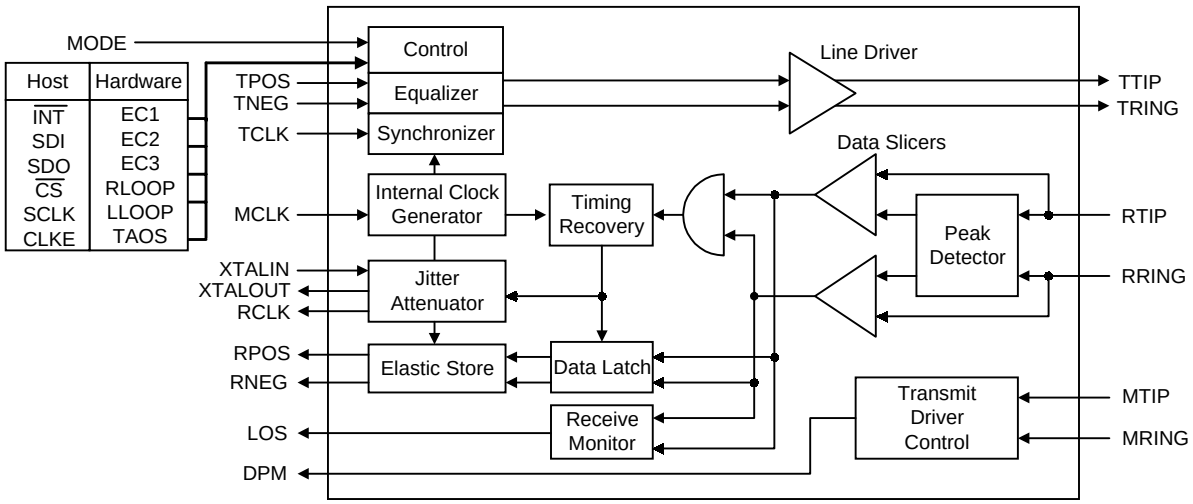
Applications

- PCM/Voice Channel Banks
- Data Channel Bank/Concentrator
- T1/E1 multiplexer
- Digital Access and Cross-connect Systems (DACS)
- Computer to PBX interface (CPI & DMI)
- High-speed data transmission lines
- Interfacing Customer Premises Equipment to a CSU
- Digital Loop Carrier (DLC) terminals

Features

- Low power consumption (400 mW maximum) 40% less than the LXT300
- Constant low output impedance transmitter regardless of data pattern (3 Ω typical)
- High transmit and receive return loss exceeds ETSI ETS 300166 and G.703 recommendations
- Meets or exceeds all industry specifications including ITU G.703, ANSI T1.403 and AT&T Pub 62411
- Compatible with most popular PCM framers
- Line driver, data recovery and clock recovery functions
- Minimum receive signal of 500 mV
- Selectable slicer levels (E1/DSX-1) improve SNR
- Programmable transmit equalizer shapes pulses to meet DSX-1 pulse template from 0 to 655 ft
- Local and remote loopback functions
- Transmit/Receive performance monitors with DPM and LOS outputs
- Receiver jitter tolerance 0.4 UI from 40 kHz to 100 kHz
- Receive jitter attenuation starting at 3 Hz meets TBR12/13 specification
- Serial control interface
- Analog/digital LOS monitor per G.775
- Available in 28-pin DIP or PLCC

LXT304A Block Diagram



PIN ASSIGNMENTS & SIGNAL DESCRIPTIONS

Figure 1: Pin Assignments

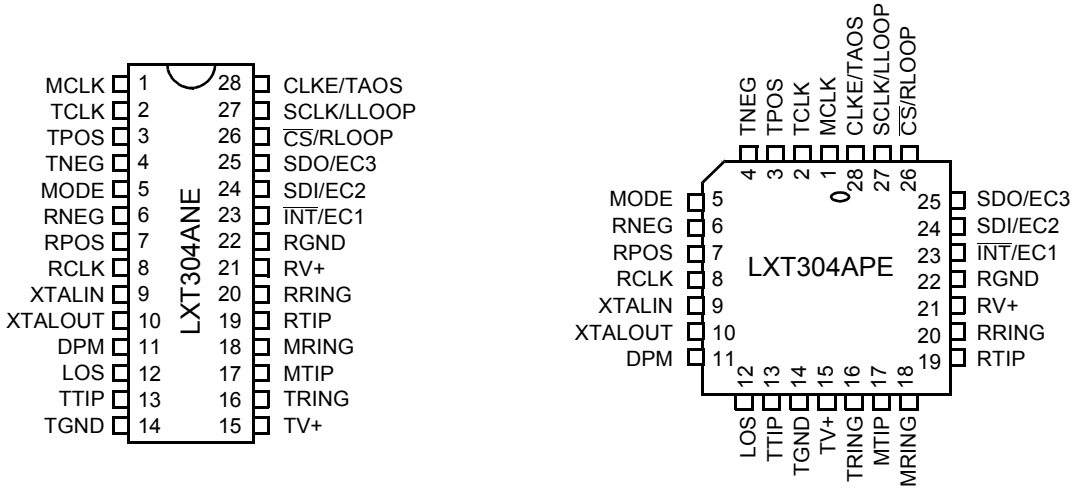


Table 1: Pin Descriptions

Pin #	Sym	I/O[1]	Description
1	MCLK	DI	**Master Clock.** A 1.544 or 2.048 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. If MCLK is not applied, this pin should be grounded.
2	TCLK	DI	**Transmit Clock.** Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK. If TCLK is not supplied, the transmitter remains powered down.
3	TPOS	DI	**Transmit Positive Data.** Input for positive pulse to be transmitted on the twisted-pair line.
4	TNEG	DI	**Transmit Negative Data.** Input for negative pulse to be transmitted on the twisted-pair line.
5	MODE	DI	**Mode Select.** Setting MODE to logic 1 puts the LXT304A in the Host Mode. In the Host Mode, the serial interface is used to control the LXT304A and determine its status. Setting MODE to logic 0 puts the LXT304A in the Hardware (H/W) Mode. In the Hardware Mode, the serial interface is disabled and hard-wired pins are used to control configuration and report status.
6	RNEG	DO	**Receive Negative Data; Receive Positive Data.** Received data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP and RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP and RRING. RNEG and RPOS outputs are Non-Return-to-Zero (NRZ). Both outputs are stable and valid on the rising edge of RCLK. In the Host Mode, CLKE determines the clock edge at which these outputs are stable and valid. In the Hardware Mode both outputs are stable and valid on the rising edge of RCLK.
7	RPOS	DO	

1. Entries in I/O column are: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output; S = Supply.

Table 1: Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
8	RCLK	DO	**Recovered Clock.** This is the clock recovered from the signal received at RTIP and RRING.
9	XTALIN	AI	**Crystal Input; Crystal Output.** An external crystal operating at four times the bit rate (6.176 MHz for DSX-1, 8.192 MHz for E1 applications with an 18.7 pF load) is required to enable the jitter attenuation function of the LXT304A. These pins may also be used to disable the jitter attenuator by connecting the XTALIN pin to the positive supply through a resistor, and tying the XTALOUT pin to ground.
10	XTALOUT	AO	
11	DPM	DO	**Driver Performance Monitor.** DPM goes to a logic 1 when the transmit monitor loop (MTIP and MRING) does not detect a signal for 63 ±2 clock periods. DPM remains at logic 1 until a signal is detected.
12	LOS	DO	**Loss of Signal.** LOS goes to a logic 1 when 175 consecutive spaces have been detected. LOS returns to a logic 0 when the received signal reaches 12.5% ones density, based on 4 ones in any 32-bit period with no more than 15 consecutive zeros.
13	TTIP	AO	**Transmit Tip; Transmit Ring.** Differential Driver Outputs. These low impedance outputs achieve maximum power savings through a 1:1.15 transformer (T1), or a 1:1 (75 Ω) or 1:1.26 (120 Ω) transformer (E1) without additional components. To provide higher return loss, resistors may be used in series with a transformer as specified in Application Information.
16	TRING	AO	
14	TGND	S	**Transmit Ground.** Ground return for the transmit drivers power supply TV+.
15	TV+	S	**Transmit Power Supply.** +5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ±0.3 V.
17	MTIP	AI	**Monitor Tip; Monitor Ring.** These pins are used to monitor the tip and ring transmit outputs. The transceiver can be connected to monitor its own output or the output of another LXT304A on the board. To prevent false interrupts in the Host Mode if the monitor is not used, apply a clock signal to one of the monitor pins and tie the other monitor pin to approximately the clock's mid-level voltage. The monitor clock can range from 100 kHz to the TCLK frequency.
18	MRING	AI	
19	RTIP	AI	**Receive Tip; Receive Ring.** The AMI signal received from the line is applied at these pins. A center-tapped, center-grounded, 2:1 step-up transformer is required on these pins. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG and RCLK pins.
20	RRING	AI	
21	RV+	S	**Receive Power Supply.** +5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
22	RGND	S	**Receive Ground.** Ground return for power supply RV+.

1. Entries in I/O column are: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output; S = Supply.

Table 1: Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
23	$\overline{\text{INT}}$	DO	**Interrupt *(Host Mode)*.** This LXT304A Host Mode output goes Low to flag the host processor when LOS or DPM go active. $\overline{\text{INT}}$ is an open-drain output and should be tied to power supply RV+ through a resistor. $\overline{\text{INT}}$ is reset by clearing the respective register bit (LOS and/or DPM.)
	EC1	DI	**Equalizer Control 1 *(H/W Mode)*.** The signal applied at this pin in the LXT304A Hardware Mode is used in conjunction with EC2 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
24	SDI	DI	**Serial Data In *(Host Mode)*.** The serial data input stream is applied to this pin when the LXT304A operates in the Host Mode. SDI is sampled on the rising edge of SCLK.
	EC2	DI	**Equalizer Control 2 *(H/W Mode)*.** The signal applied at this pin in the LXT304A Hardware Mode is used in conjunction with EC1 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
25	SDO	DO	**Serial Data Out *(Host Mode)*.** The serial data from the on-chip register is output on this pin in the LXT304A Host Mode. If CLKE is High, SDO is valid on the rising edge of SCLK. If CLKE is Low, SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to and when $\overline{\text{CS}}$ is High.
	EC3	DI	**Equalizer Control 3 *(H/W Mode)*.** The signal applied at this pin in the LXT304A Hardware Mode is used in conjunction with EC1 and EC2 inputs to determine shape and amplitude of AMI output transmit pulses.
26	$\overline{\text{CS}}$	DI	**Chip Select *(Host Mode)*.** This input is used to access the serial interface in the LXT304A Host Mode. For each read or write operation, $\overline{\text{CS}}$ must transition from High to Low, and remain Low.
	RLOOP	DI	**Remote Loopback *(H/W Mode)*.** This input controls loopback functions in the LXT304A Hardware Mode. Setting RLOOP High enables the Remote Loopback Mode. Setting both RLOOP and LLOOP causes a Reset.
27	SCLK	DI	**Serial Clock *(Host Mode)*.** This clock is used in the LXT304A Host Mode to write data to or read data from the serial interface registers.
	LLOOP	DI	**Local Loopback *(H/W Mode)*.** This input controls loopback functions in the LXT304A Hardware Mode. Setting LLOOP High enables the Local Loopback Mode.
28	CLKE	DI	**Clock Edge *(Host Mode)*.** Setting CLKE High causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is Low, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
	TAOS	DI	**Transmit All Ones *(H/W Mode)*.** When set High, TAOS causes the LXT304A (Hardware Mode) to transmit a continuous stream of marks at the TCLK frequency. Activating TAOS causes TPOS and TNEG inputs to be ignored. TAOS is inhibited during Remote Loopback.

1. Entries in I/O column are: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output; S = Supply.

FUNCTIONAL DESCRIPTION

The LXT304A is a fully integrated PCM transceiver for both 1.544 Mbps (DSX-1) and 2.048 Mbps (E1) applications. It allows full-duplex transmission of digital data over existing twisted-pair installations.

The LXT304A transceiver interfaces with two twisted-pair lines, one twisted-pair for transmit, one twisted-pair for receive.

Power Requirements

The LXT304A is a low-power CMOS device. It operates from a single +5 V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ± .3 V of each other, and decoupled to their respective grounds separately. Refer to Application Information for typical decoupling circuitry. Isolation between the transmit and receive circuits is provided internally. During normal operation, TAOS or LLOOP, the transmitter powers down if TCLK is not supplied.

Reset Operation

Upon power up, the transceiver is held static until the power supply reaches approximately 3 V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and lock the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines. The transmitter reference is provided by TCLK. MCLK provides the receiver reference. If the crystal oscillator is grounded, MCLK is used as the receiver reference clock.

The transceiver can also be reset from the Host or Hardware Mode. In Host Mode, reset is commanded by simultaneously writing RLOOP and LLOOP to the register. In Hardware Mode, reset is commanded by holding RLOOP and LLOOP High simultaneously for 200 ns. Reset is initiated on the falling edge of the reset request. In either mode, reset clears and sets all registers to 0 and then begins calibration.

Receiver

The LXT304A receives the signal input from one twisted-pair line on each side of a center-grounded transformer. Positive pulses are received at RTIP and negative pulses are received at RRING. Recovered data is output at RPOS and RNEG, and the recovered clock is output at RCLK. Refer to Test Specifications for LXT304A receiver timing.

The signal received at RPOS and RNEG is processed through the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For DSX-1 applications (determined by Equalizer Control inputs EC1 - EC3 ≠ 000) the threshold is set to 70% of the peak value. This threshold is maintained above 65% for up to 15 successive zeros over the range of specified operating conditions. For E1 applications (EC inputs = 000 or 001) the threshold is 50%.

The receiver is capable of accurately recovering signals with up to -13.6 dB of attenuation (from 2.4 V), corresponding to a received signal level of approximately 500 mV. Maximum line length is 1500 feet of ABAM cable (approximately 6 dB of attenuation). Regardless of received signal level, the peak detectors are held above a minimum level of .3 V to provide immunity from impulsive noise.

After processing through the data slicers, the received signal is routed to the data and clock recovery sections, and to the receive monitor. The data and clock recovery circuits are highly tolerant with an input jitter tolerance significantly better than required by Pub 62411. Refer to Test Specifications for additional information.

The receiver monitor loads a digital counter at the RCLK frequency. The count is incremented each time a zero is received, and reset to zero each time a one (mark) is received. Upon receipt of 175 consecutive zeros the LOS pin goes high, and a smooth transition replaces the RCLK output with the MCLK. (If MCLK is not supplied the RCLK output will be replaced with the centered crystal clock.) The LOS pin is reset when the received signal reaches 12.5% ones density (4 marks in 32 bits) with no more than 15 consecutive zeros.

Recovered clock signals are supplied to the Jitter Attenuator and the data latch. The recovered data is passed to the Elastic Store where it is buffered and synchronized with the dejittered recovered clock (RCLK).

Jitter Attenuation

Jitter attenuation of the LXT304A clock and data outputs is provided by a Jitter Attenuation Loop (JAL) and an Elastic Store (ES). An external crystal oscillating at 4 times the bit rate provides clock stabilization. Refer to Application Information for crystal specifications. The ES is a 32 x 2-

bit register. Recovered data is clocked into the ES with the recovered clock signal, and clocked out of the ES with the dejittered clock from the JAL. When the bit count in the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by 1/8 of a bit period. The ES produces an average delay of 16 bits in the receive path.

Transmitter

Data received for transmission onto the line is clocked serially into the device at TPOS and TNEG. Input synchronization is supplied by the transmit clock (TCLK). If TCLK is not supplied the transmitter remains powered down, except during remote loopback. Refer to Test Specifications for master and transmit clock timing characteristics.

The transmitted pulse shape is determined by Equalizer Control signals EC1 through EC3 as shown in Table 2. Equalizer Control signals may be hardwired in the Hardware mode, or input as part of the serial data stream (SDI) in the Host mode. Shaped pulses are applied to the AMI line driver for transmission onto the line at TTIP and TRING. The line driver provides a constant low output impedance of 3 Ω (typical). This well controlled output impedance provides excellent return loss (> 18 dB) when used with external 9.1 Ω precision resistors (± 1% accuracy) in series with a transmit transformer with a turns ratio of 1:2.3 (± 2% accuracy). Series resistors also provide increased surge protection and reduce short circuit current flow.

Pulses can be shaped for either 1.544 or 2.048 Mbps applications. 1.544 Mbps pulses for DSX-1 applications can be programmed to match line lengths from 0 to 655 feet of ABAM cable. The LXT304A also matches FCC and ECSA specifications for CSU applications. A 1:1.15 transmit transformer is used for 1.544 Mbps systems. For higher return loss in DSX-1 applications, use 9.1 Ω resistors in series with a 1:2.3 transmit transformer.

2.048 Mbps pulses can drive coaxial or shielded twisted-pair lines. For E1 systems, a 1:2 transmit transformer and series resistors are recommended. This design meets or exceeds all ITU and ETSI specifications for transmit and receive return loss. A 1:1 or 1:1.26 transformer may be used without series resistors.

Driver Performance Monitor

The transceiver incorporates a Driver Performance Monitor (DPM) in parallel with TTIP and TRING at the output transformer. The DPM output goes High upon detection of 63 consecutive zeros. It is reset when a one is detected on the transmit line, or when a reset command is received.

Line Code

The LXT304A transmits data as a 50% AMI line code as shown in Figure 2. The output driver maintains a constant low output impedance regardless of whether it is driving marks or spaces.

Operating Modes

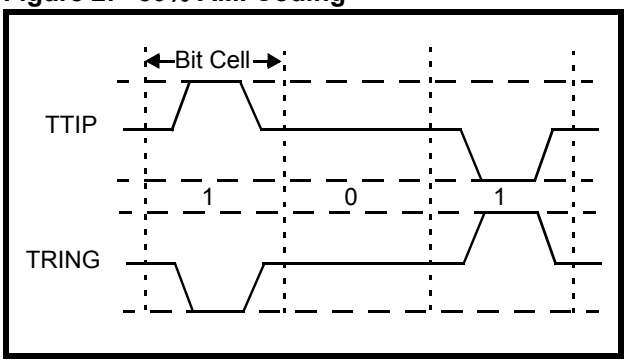
The LXT304A can be controlled through hard-wired pins (Hardware Mode) or by a microprocessor through a serial interface (Host Mode). The mode of operation is set by the MODE pin logic level. The LXT304A can also be commanded to operate in one of several diagnostic modes.

Table 2: Equalizer Control Inputs

EC3	EC2	EC1	Line Length[1]	Cable Loss[2]	Application	Bit Rate
0	1	1	0 ~ 133 ft ABAM	0.6 dB	DSX-1	1.544 Mbps
1	0	0	133 ~ 266 ft ABAM	1.2 dB		
1	0	1	266 ~ 399 ft ABAM	1.8 dB		
1	1	0	399 ~ 533 ft ABAM	2.4 dB		
1	1	1	533 ~ 655 ft ABAM	3.0 dB		
0	0	0	ITU Recommendation G.703		E1 - Coax (75 Ω)	2.048 Mbps
0	0	1			E1 - Twisted-pair (120 Ω)	
0	1	0	FCC Part 68, Option A		CSU (DS-1)	1.544 Mbps

1. Line length from transceiver to DSX-1 cross-connect point.
2. Maximum cable loss at 772 kHz.

Figure 2: 50% AMI Coding



Host Mode Operation

To allow a host microprocessor to access and control the LXT304A through the serial interface, MODE is set High.

The serial interface (SDI/SDO) uses a 16-bit word consisting of an 8-bit Command/Address byte and an 8-bit Data byte. Figure 3 shows the serial interface data structure and relative timing.

The Host Mode provides a latched Interrupt output ($\overline{INT}$) which is triggered by a change in the Loss of Signal (LOS) and/or Driver Performance Monitor (DPM) bits. The Interrupt is cleared when the interrupt condition no longer exists, and the host processor enables the respective bit in the serial input data byte. Host Mode also allows control of the serial data and receive data output timing. The Clock Edge (CLKE) signal determines when these outputs are valid, relative to the Serial Clock (SCLK) or RCLK as listed in Table 3.

Table 3: Valid CLKE Settings

CLKE	Output	Clock	Valid Edge
LOW	RPOS RNEG SDO	RCLK RCLK SCLK	Rising Rising Falling
HIGH	RPOS RNEG SDO	RCLK RCLK SCLK	Falling Falling Rising

Table 4: LXT304A Serial Data Output Bits (See Figure 4)

Bit D5	Bit D6	Bit D7	Status
0	0	0	Reset has occurred, or no program input.
0	0	1	TAOS is active.
0	1	0	Local Loopback is active.
0	1	1	TAOS and Local Loopback are active.
1	0	0	Remote Loopback is active.
1	0	1	DPM has changed state since last Clear DPM occurred.
1	1	0	LOS has changed state since last Clear LOS occurred.
1	1	1	LOS and DPM have both changed state since last Clear DPM and Clear LOS occurred.

The LXT304A serial port is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. The LXT304A contains only a single output data register so no complex chip addressing scheme is required. The register is accessed by causing the Chip Select ($\overline{CS}$) input to transition from High to Low. Bit 1 of the serial Address/Command byte provides Read/Write control when the chip is accessed. A logic 1 indicates a read operation, and a logic 0 indicates a write operation. Table 4 lists serial data output bit combinations for each status. Serial data I/O timing characteristics are shown in the Test Specifications section.

Hardware Mode Operation

In Hardware Mode the transceiver is accessed and controlled through individual pins. With the exception of the INT and CLKE functions, Hardware Mode provides all the functions provided in the Host Mode. In the Hardware Mode RPOS and RNEG outputs are valid on the rising edge of RCLK. To operate in Hardware Mode, MODE must be set Low. Equalizer Control signals (EC1 through EC3) are input on the Interrupt, Serial Data In and Serial Data Out pins. Diagnostic control for Remote Loopback (RLOOP), Local Loopback (LLOOP), and Transmit All Ones (TAOS) modes is provided through the individual pins used to control serial interface timing in the Host Mode.

Diagnostic Mode Operation

Transmit All Ones

In Transmit All Ones (TAOS) mode the TPOS and TNEG inputs to the transceiver are ignored. The transceiver transmits a continuous stream of ones when the TAOS mode is activated. TAOS can be commanded simultaneously with Local Loopback, but is inhibited during Remote Loopback.

Remote Loopback

In Remote Loopback (RLOOP) mode, the transmit data and clock inputs (TPOS, TNEG and TCLK) are ignored. The RPOS and RNEG outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RPOS, RNEG and RCLK signals received from the twisted-pair line.

Local Loopback

In Local Loopback (LLOOP) mode, the receiver circuits are inhibited. The transmit data and clock inputs (TPOS, TNEG and TCLK) are looped back onto the receive data and clock outputs (RPOS, RNEG and RCLK) through the Rx jitter attenuator. The transmitter circuits are unaffected by the LLOOP command. The TPOS and TNEG inputs (or a stream of ones if the TAOS command is active) will be transmitted normally.

Figure 3: LXT304A Serial Interface Data Structure

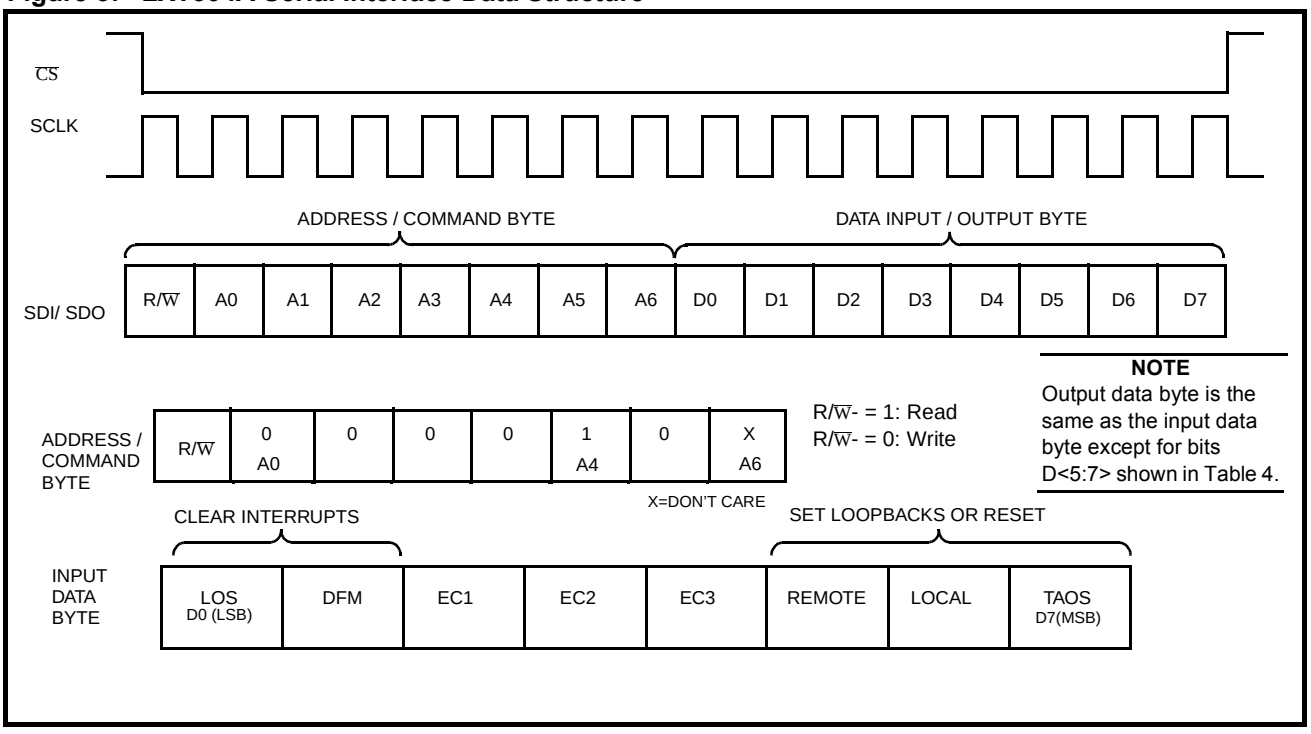


Table 5: LXT304A Crystal Specifications (External)

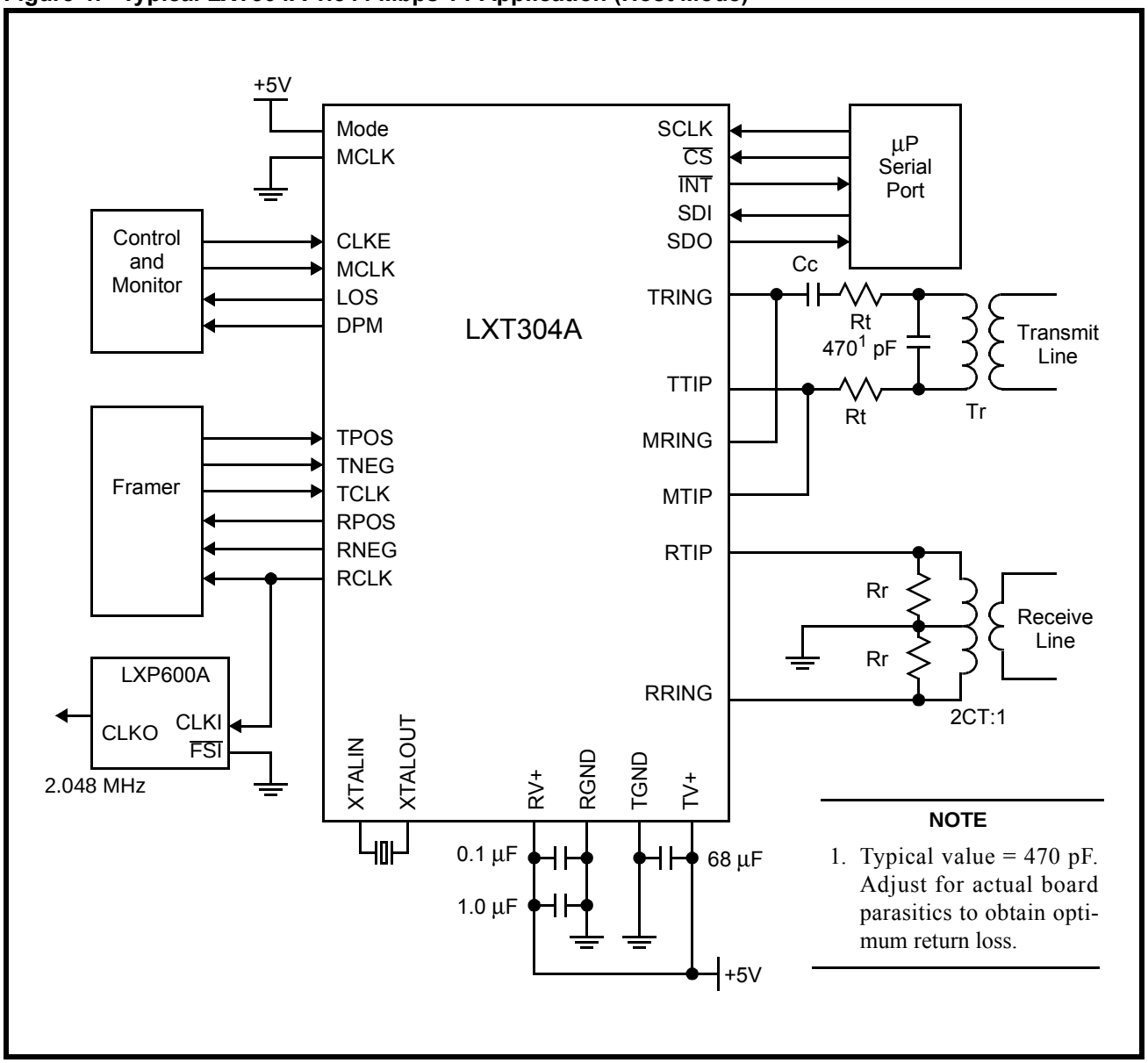
Parameter	T1	E1
Frequency	6.176 MHz	8.192 MHz
Frequency stability	± 20 ppm @ 25 °C ± 25 ppm from -40 °C to 85 °C (Ref 25 °C reading)	± 20 ppm @ 25 °C ± 25 ppm from -40 °C to +85 °C (Ref 25 °C reading)
Pullability	CL = 11 pF to 18.7 pF, +ΔF = 175 to 195 ppm CL = 18.7 pF to 34 pF, -ΔF = 175 to 195 ppm	CL = 11 pF to 18.7 pF, +ΔF = 95 to 115 ppm CL = 18.7 pF to 34 pF, -ΔF = 95 to 115 ppm
Effective series resistance	40 Ω Maximum	30 Ω Maximum
Crystal cut	AT	AT
Resonance	Parallel	Parallel
Maximum drive level	2.0 mW	2.0 mW
Mode of operation	Fundamental	Fundamental
Crystal holder	HC49 (R3W), C_O = 7 pF maximum C_M = 17 fF typical	HC49 (R3W), C_O = 7 pF maximum C_M = 17 fF typical

APPLICATION INFORMATION

1.544 Mbps T1 Interface Application

Figure 4 is a typical 1.544 Mbps T1 application. The LXT304A is shown in the Host Mode with a T1/ESF framer providing the digital interface with the host controller. Both devices are controlled through the serial interface. An LXP600A Clock Adapter (CLAD) provides the 2.048 MHz system backplane clock, locked to the recovered 1.544 MHz clock signal. The power supply inputs are tied to a common bus with appropriate decoupling capacitors installed (68 µF on the transmit side, 1.0 µF and 0.1 µF on the receive side).

Figure 4: Typical LXT304A 1.544 Mbps T1 Application (Host Mode)



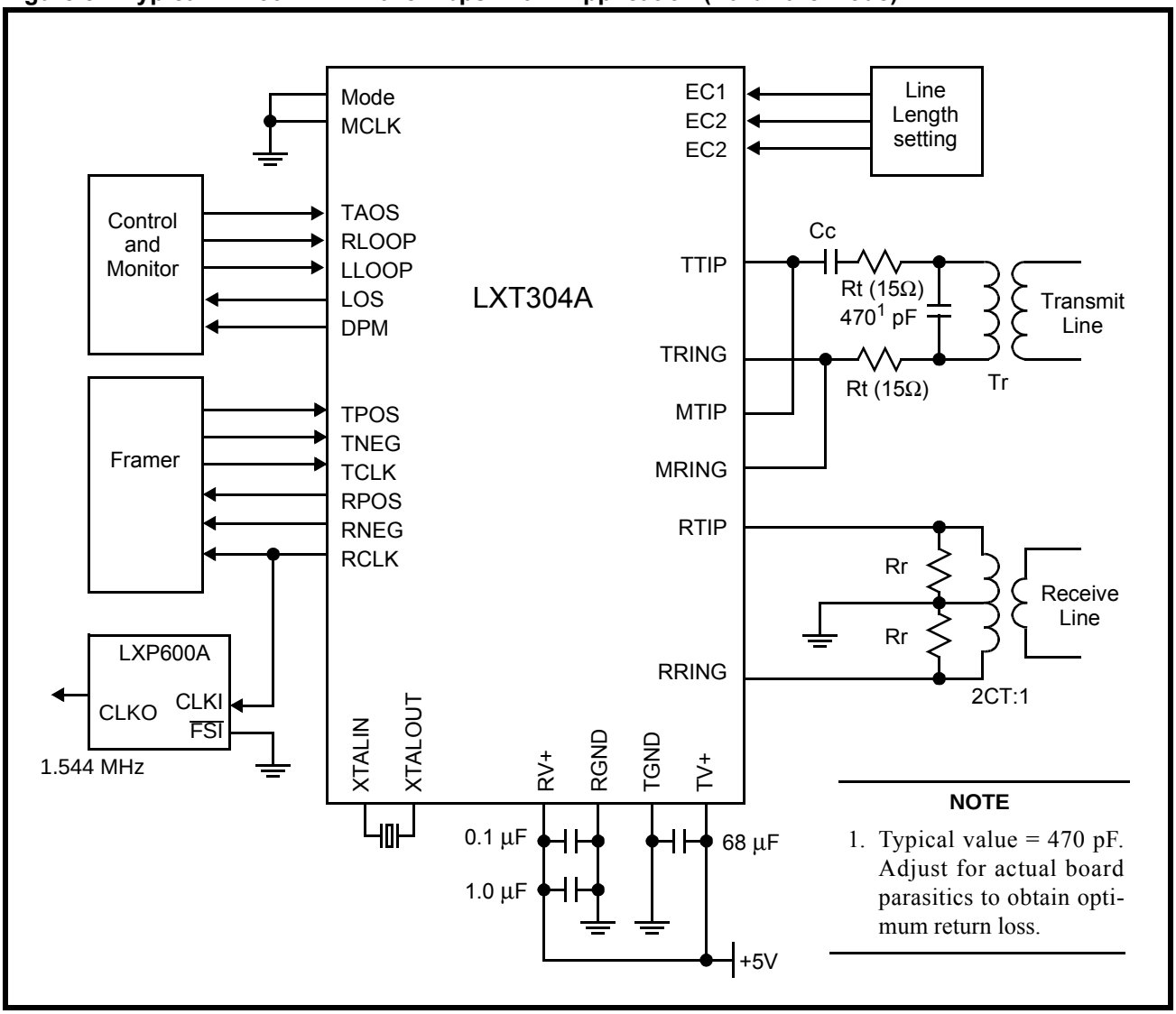
NOTE

1. Typical value = 470 pF. Adjust for actual board parasitics to obtain optimum return loss.

2.048 Mbps E1 Interface Applications

Figure 5 is a 2.048 Mbps E1 TWP application using 15 Ω Rt resistors in line with the transmit transformer to provide high return loss and surge protection. When high return loss is not a critical factor, a 1:1 or 1:1.26 transformer without in-line resistors provides maximum power savings. The LXT304A is shown in Hardware Mode with a typical E1/CRC4 Framer. The hard-wired control lines for TAOS, LLOOP and RLOOP are individually controllable, and the LLOOP and RLOOP lines are also tied to a single control for the Reset function. This configuration is illustrated with a crystal in place to enable the LXT304A Jitter Attenuation Loop, and a single power supply bus.

Figure 5: Typical LXT304A E1 2.048 Mbps 120 Ω Application (Hardware Mode)



D4 Channel Bank Applications

Existing D4 Channel Bank architectures frequently employ: (1) a plug-in card for T1 pulse generation (6.0 V peak); and (2) a separate card for pulse shaping and Line Build-Out (LBO). The LXT304A integrates the functions of both cards on a single chip producing a DSX-1 compatible, 3.0 V peak output pulse with a standard transformer. In new designs, the LXT304A can replace two cards with one. However, the LXT304A is also compatible with existing dual-card architectures. With an appropriate output transformer, the LXT304A can produce full 6.0 V peak amplitude pulses suitable for D4 Channel Bank applications with separate pulse shaping/LBO cards.

To achieve the 6.0 V peak output, the FCC Part 68-010 Equalizer Code setting is used. (EC = 010.) With the standard 1:1.15 transformer, this code produces a 3.0 V peak pulse. However, doubling the transformer turns ratio to 1:2.30 produces the desired 6.0 V peak pulse.

Table 6: T1/E1 Input/Output Configurations

Bit Rate (Mbps)	Crystal XTAL	Cable (Ω)	Rr[2] (Ω)	EC3/2/1	Transmit Transformer[1] (Tr)	Rt[2] (Ω)	Typical TX Return Loss[3] (dB)	Cc (µF)
1.544 (T1)	LXC6176	100	200	0/1/1 - 1/1/1 0/1/0[4]	1:1.15 1:2 1:2.3 1:2.3	0 9.1 9.1 0	0.5 18 18 0[4]	0.47 0 0 0.47
2.048 (E1)	LXC8192	120	240	0/0/0 0/0/0 0/0/1 0/0/1	1:1.26 1:2 1:1 1:2	0 9.1 0 1.5	0.5 12 0.5 18	0.47 0 0.47 0
		75	150	0/0/0 0/0/0 0/0/1 0/0/1	1:1 1:2 1:1 1:2	0 9.1 10 14.3	0.5 18 5 10	0.47 0 0 0

1. Transformer turns ratio accuracy is ± 2%.
2. Rr and Rt values are ± 1%.
3. Typical return loss, 51 kHz to 3.072 MHz band.
4. D4 Channel Bank application.

TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 7 through 13 and Figures 6 through 11 represent the performance specifications of the LXT304A and are guaranteed by test, except where noted by design.

Table 7: Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
DC supply (referenced to GND)	RV+, TV+	–0.3	6.0	V
Input voltage, any pin[1]	V_{IN}	RGND - 0.3	RV+ + 0.3	V
Input current, any pin[2]	I_{IN}	-10	10	mA
Storage temperature	T_{STG}	-65	150	°C

CAUTION

Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

1. Excluding RTIP and RRING which must stay between -6V and (RV+ + 0.3) V.
2. Transient currents of up to 100 mA will not cause SCR latch up. TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

Table 8: Recommended Operating Conditions and Characteristics

Parameter	Sym	Min	Typ	Max	Units
DC supply[1]	RV+, TV+	4.75	5.0	5.25	V
Ambient operating temperature	T_A	-40	25	85	° C

1. TV+ must not exceed RV+ by more than 0.3 V.

Table 9: Electrical Characteristics (Under Recommended Operating Conditions)

Parameter	Sym	Min	Max	Units	Test Conditions
Total power dissipation[1,3]	P_D	–	400	mW	100% ones density & maximum line length @ 5.25 V
High level input voltage[2,3] (pins 1-5, 10, 23-28)	V_{IH}	2.0	–	V	
Low level input voltage[2,3] (pins 1-5, 10, 23-28)	V_{IL}	–	0.8	V	
High level output voltage[2,3] (pins 6-8, 11, 12, 23, 25)	V_{OH}	2.4	–	V	I_{OUT} = -400 µA

1. Power dissipation while driving 75 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
2. Functionality of pins 23 and 25 depends on mode. See Host/Hardware Mode descriptions.
3. Output drivers will output CMOS logic levels into CMOS loads.
4. Except MTIP and MRING ILL = ± 50 µA.

Table 9: Electrical Characteristics (Under Recommended Operating Conditions) – continued

Parameter	Sym	Min	Max	Units	Test Conditions
Low level output voltage[2,3] (pins 6-8, 11, 12, 23, 25)	V_{OL}	–	0.4	V	I_{OUT} = 1.6 mA
Input leakage current[4]	I_{LL}	-10	+10	µA	
Three-state leakage current[2] (pin 25)	I_{3L}	-10	+10	µA	

1. Power dissipation while driving 75 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
2. Functionality of pins 23 and 25 depends on mode. See Host/Hardware Mode descriptions.
3. Output drivers will output CMOS logic levels into CMOS loads.
4. Except MTIP and MRING ILL = ± 50 µA.

Table 10: Analog Characteristics (Under Recommended Operating Conditions)

Parameter		Min	Typ[1]	Max	Units	Test Conditions
AMI output pulse amplitudes	DSX-1	2.4	3.0	3.6	V	measured at the DSX
	E1	2.7	3.0	3.3	V	measured at line side
Recommended output load at TTIP and TRING		–	75	–	Ω	
Jitter added by the transmitter[2]	10 Hz - 8 kHz	–	–	0.01	UI	
	8 kHz - 40 kHz	–	–	0.025	UI	
	10 Hz - 40 kHz	–	–	0.025	UI	
	Broad Band	–	–	0.05	UI	
Sensitivity below DSX	(0 dB = 2.4 V)	13.6	–	–	dB	
		500	–	–	mV	
Loss of Signal threshold		–	0.3	–	V	
Data decision threshold	DSX-1	63	70	77	% peak	
	E1	43	50	57	% peak	
Allowable consecutive zeros before LOS		160	175	190	–	
Input jitter tolerance	10 kHz - 100 kHz	0.4	–	–	UI	
Jitter attenuation curve corner frequency[3]		–	3	–	Hz	
Minimum return loss[4,5]		**Transmit** Min	Typ	**Receive** Min	Typ	dB
	51 kHz - 102 kHz	18	–	20	–	dB
	102 kHz - 2.048 kHz	18	–	20	–	dB
	2.048 kHz - 3.072 kHz	18	–	20	–	dB

1. Typical values are measured at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Input signal to TCLK is jitter-free.
3. Circuit attenuates jitter at 20 dB/decade above the corner frequency.
4. In accordance with ITU G.703/ETS 300166 return loss specifications when wired per Figure 7 (E1).
5. Guaranteed by design.

Figure 6: Typical Receive Input Jitter Tolerance (Loop Mode)

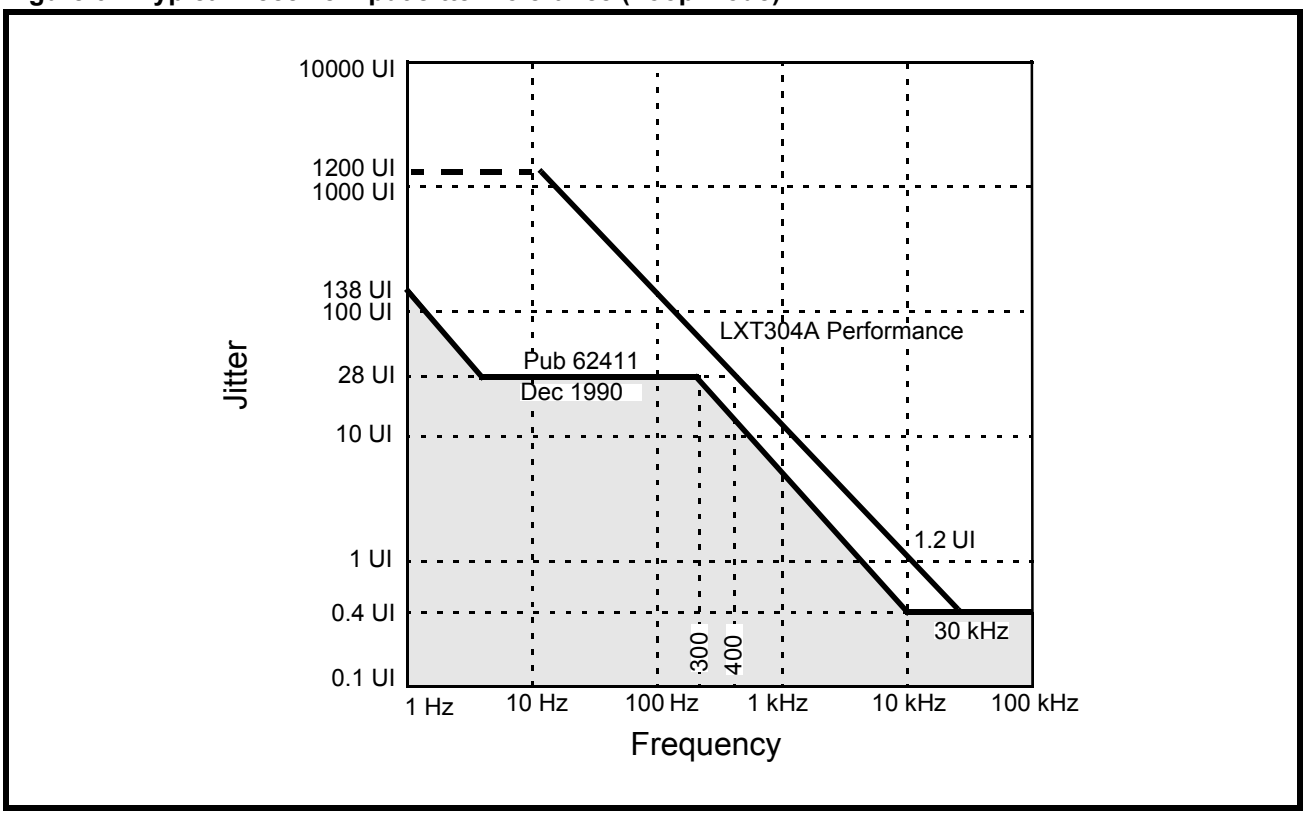


Figure 7: LXT304A Receive Jitter Transfer Performance (Typical)

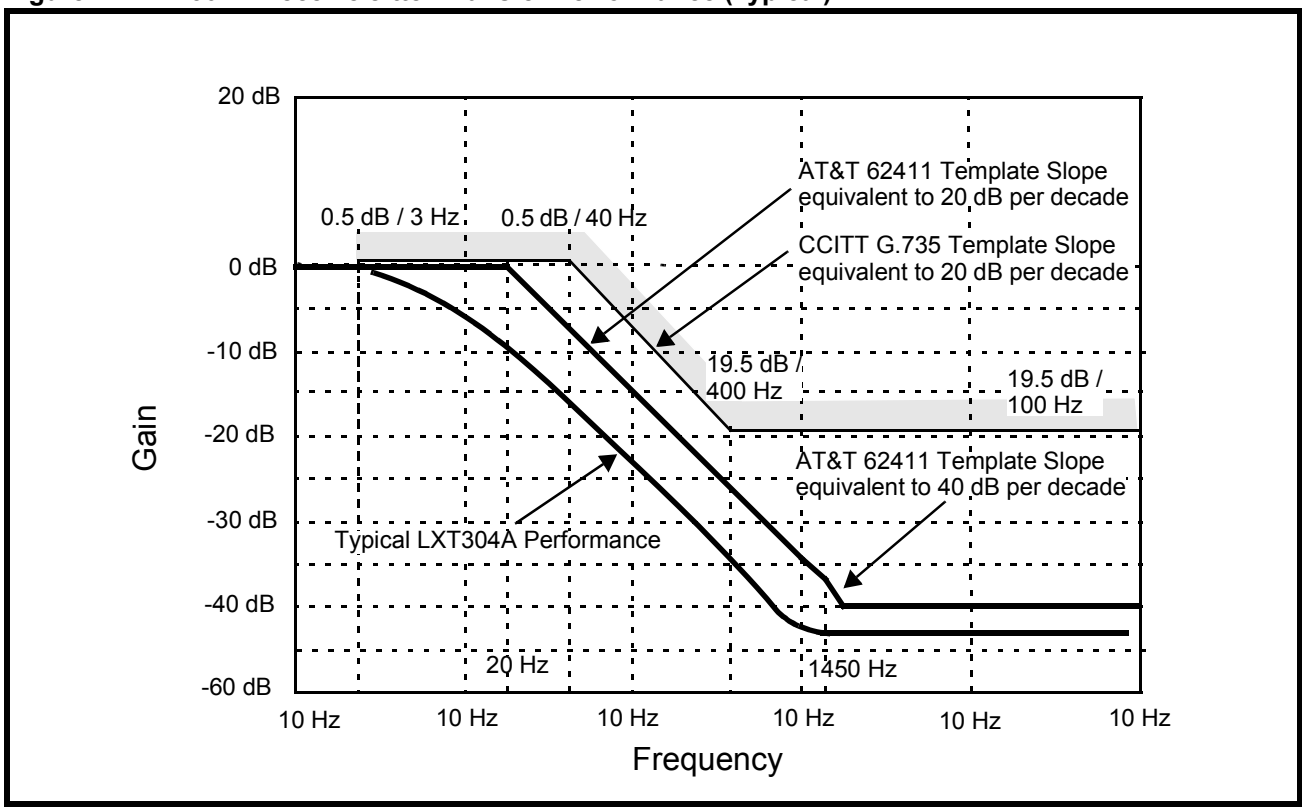


Table 11: LXT304A Receive Timing Characteristics (See Figure 8)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Receive clock duty cycle		RCLKd	40	–	60	%	
Receive clock pulse width	DSX-1	t_{PW}	–	324	–	ns	
	E1	t_{PW}	–	244	–	ns	
RPOS/RNEG to RCLK rising setup time	DSX-1	t_{SUR}	–	274	–	ns	
	E1	t_{SUR}	–	194	–	ns	
RCLK rising to RPOS/RNEG hold time	DSX-1	t_{HR}	–	274	–	ns	
	E1	t_{HR}	–	194	–	ns	

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 8: LXT304A Receive Clock Timing Diagram

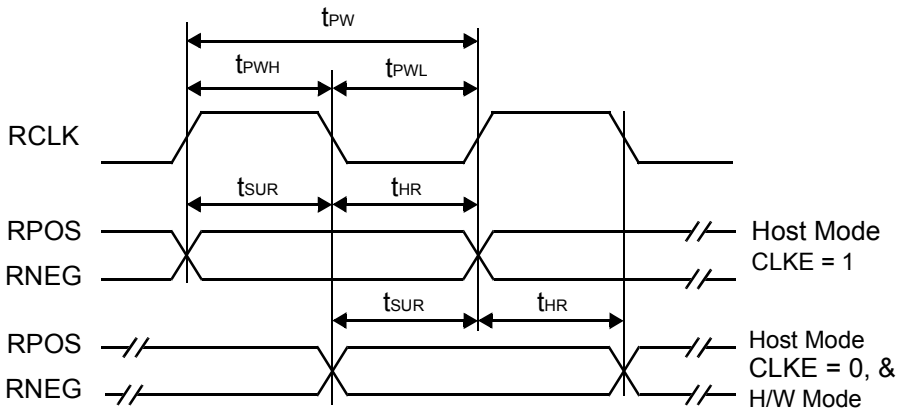


Table 12: LXT304A Master Clock and Transmit Timing Characteristics
(See Figure 9)

Parameter		Sym	Min	Typ[1]	Max	Units
Master clock frequency	DSX-1	MCLK	–	1.544	–	MHz
	E1	MCLK	–	2.048	–	MHz
Master clock tolerance		MCLKt	–	±100	–	ppm
Master clock duty cycle		MCLKd	40	–	60	%
Crystal frequency	DSX-1	fc	–	6.176	–	MHz
	E1	fc	–	8.192	–	MHz
Transmit clock frequency	DSX-1	TCLK	–	1.544	–	MHz
	E1	TCLK	–	2.048	–	MHz
Transmit clock tolerance		TCLKt	–	±50	–	ppm
Transmit clock duty cycle		TCLKd	10	–	90	%
TPOS/TNEG to TCLK setup time		t_{SUT}	25	–	–	ns
TCLK to TPOS/TNEG hold time		t_{HT}	25	–	–	ns

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 9: LXT304A Transmit Clock Timing Diagram

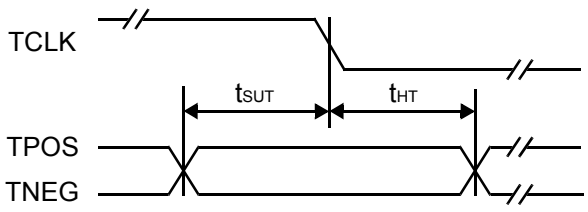


Table 13: LXT304A Serial I/O Timing Characteristics (See Figures 10 and 11)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Rise/Fall time - any digital output	t_{RF}	–	–	100	ns	Load 1.6 mA, 50 pF
SDI to SCLK setup time	t_{DC}	50	–	–	ns	
SCLK to SDI hold time	t_{CDH}	50	–	–	ns	
SCLK low time	t_{CL}	240	–	–	ns	
SCLK high time	t_{CH}	240	–	–	ns	
SCLK rise and fall time	t_R, t_F	–	–	50	ns	
$\overline{CS}$ to SCLK setup time	t_{CC}	50	–	–	ns	
SCLK to $\overline{CS}$ hold time	t_{CCH}	50	–	–	ns	
$\overline{CS}$ inactive time	t_{CWH}	250	–	–	ns	
SCLK to SDO valid	t_{CDV}	–	–	200	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO high Z	t_{CDZ}	–	100	–	ns	

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 10: LXT304A Serial Data Input Timing Diagram

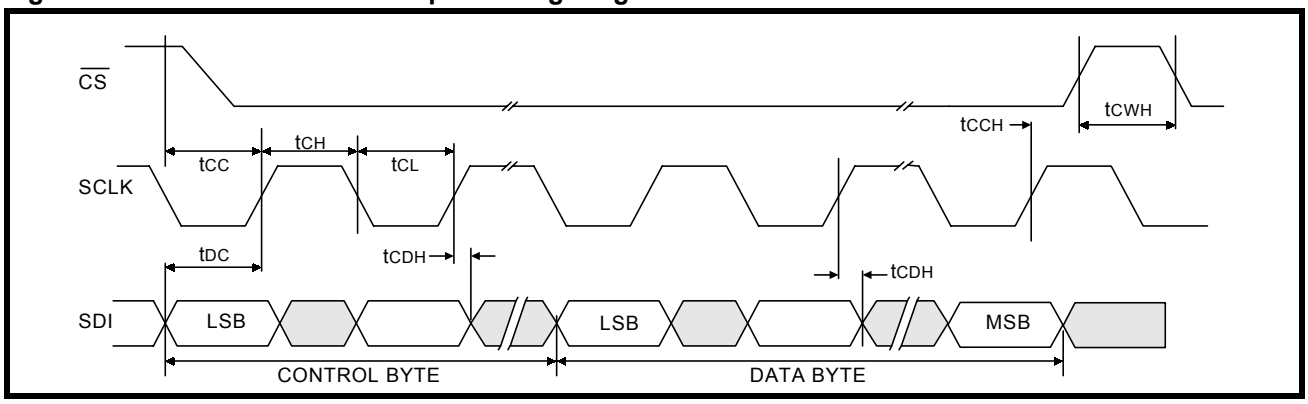


Figure 11: LXT304A Serial Data Output Timing Diagram