

**Features :**

- \* 65,536 words by 16 bits organization.
- \* Fast access time and cycle time.
- \* Dual  $\overline{WE}$  Input.
- \* Low power dissipation.
- \* Read-Modify-Write,  $\overline{RAS}$ -Only Refresh,  $\overline{CAS}$ -Before- $\overline{RAS}$  Refresh, Hidden Refresh and Test Mode Capability.
- \* 256 refresh cycles per 4ms.
- \* Available in 40-pin 400 mil SOJ, and 40/44 pin TSOP(II).
- \* Single 5.0V $\pm$ 10% Power Supply, Except 5V+5%,-10% for 30ns TSOP(II) Package.
- \* All inputs and Outputs are TTL compatible.
- \* Extended Data-Out(EDO) Page Mode operation.

**Description :**

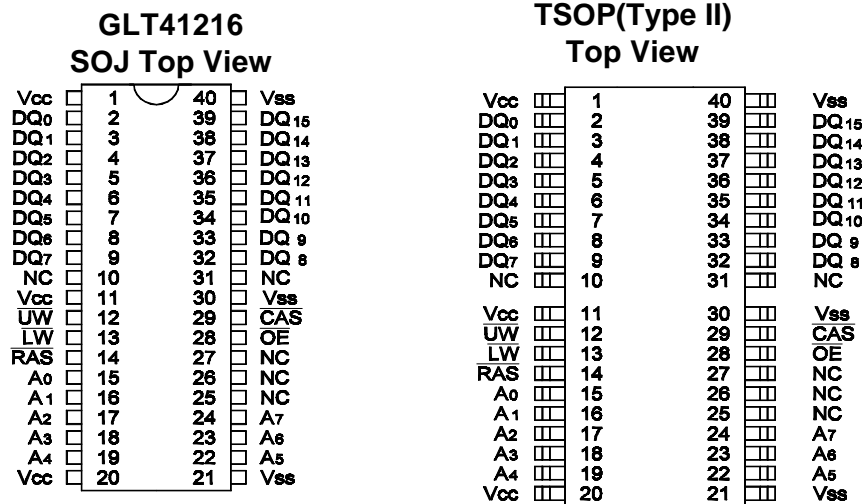
The GLT41216 is a 65,536 x 16 bit high-performance CMOS dynamic random access memory. The GLT41216 offers Fast Page mode with Extended Data Output, and has both BYTE WRITE and WORD WRITE access cycles via two  $\overline{WE}$  pins. The GLT41216 accepts 256-cycle refresh in 4ms interval.

All inputs are TTL compatible. EDO Page Mode operation allows random access up to 256 x 16 bits, within a page, with cycle times as short as 12ns.

The GLT41216 is best suited for graphics, and DSP applications requiring high performance memories.

<b>HIGH PERFORMANCE</b>	<b>30</b>	<b>35</b>	<b>40</b>	<b>45</b>
Max. $\overline{RAS}$ Access Time, ( $t_{RAC}$ )	30 ns	35 ns	40 ns	45 ns
Max. Column Address Access Time, ( $t_{AA}$ )	15 ns	18 ns	20 ns	22 ns
Min. Extended Data Out Page Mode Cycle Time, ( $t_{PC}$ )	12 ns	13 ns	15 ns	18 ns
Min. Read/Write Cycle Time, ( $t_{RC}$ )	65 ns	70 ns	75 ns	80 ns
Max. $\overline{CAS}$ Access Time ( $t_{CAC}$ )	10 ns	11 ns	12 ns	12 ns

**Pin Configuration :**



**Pin Descriptions:**

Name	Function
A <sub>0</sub> - A <sub>7</sub>	Address Inputs
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{UW}}$	Read/Upper Byte Write Enable
$\overline{\text{LW}}$	Read/Lower Byte Write Enable
$\overline{\text{OE}}$	Output Enable
DQ <sub>0</sub> - DQ <sub>15</sub>	Data Inputs / Outputs
V <sub>CC</sub>	+5V Power Supply
V <sub>SS</sub>	Ground
NC	No Connection

**Absolute Maximum Ratings\***

Operating Temperature, T<sub>A</sub> (ambient)  
 .....-0°C to +70°C  
 Storage Temperature(plastic)....-55°C to +150°C  
 Voltage Relative to V<sub>SS</sub>.....-1.0V to + 7.0V  
 Short Circuit Output Current.....50mA  
 Power Dissipation.....1.0W

\*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

**Capacitance\***

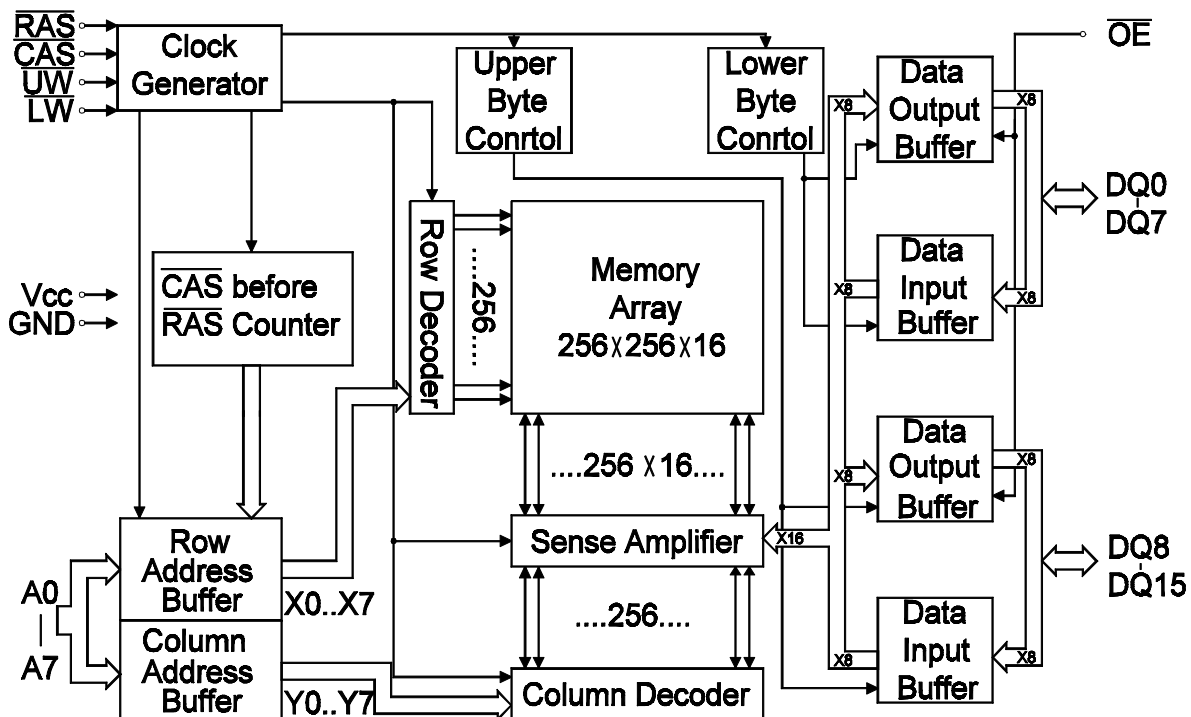
T<sub>A</sub>=25°C, V<sub>CC</sub>=5V±10%, V<sub>SS</sub>=0V

Symbol	Parameter	Max.	Unit
C <sub>IN1</sub>	Address Input	5	pF
C <sub>IN2</sub>	RAS, CAS, UW, LW, OE	7	pF
C <sub>OUT</sub>	Data Input/ Output	7	pF

\*Note: Capacitance is sampled and not 100% tested

**Electrical Specifications**

- WE means UW and LW .
- All voltages are referenced to GND.
- After power up, wait more than 100µs and then, execute eight  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  or  $\overline{\text{RAS}}$ -only refresh cycles as dummy cycles to initialize internal circuit.

**Block Diagram :**


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### **Extended Data Output (EDO) Page Mode**

The EDO page mode is a kind of page mode with enhanced features. The two major features of the EDO page mode are as follows.

1. Data output time is extended.

In the EDO page mode, the output data is held to the next  $\overline{\text{CAS}}$  cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the EDO page mode is extended compared with the fast page mode (=data extend function). In the fast page mode, the data output time becomes shorter as the  $\overline{\text{CAS}}$  cycle time becomes shorter. Therefore, in the EDO page mode, the timing margin in read cycle is larger than of the fast page mode even if the  $\overline{\text{CAS}}$  cycle time becomes shorter.

2. The  $\overline{\text{CAS}}$  cycle time in the EDO page mode is shorter than that in the fast page mode.

In the EDO page mode, due to the data extend function, the  $\overline{\text{CAS}}$  cycle time can be shorter than in the fast page mode if the timing margin is the same.

Taking a device whose  $t_{\text{RAC}}$  is 60ns as an example, the  $\overline{\text{CAS}}$  cycle time in the EDO page mode is 25ns while that in the fast page mode is 40ns.

In the EDO page mode, read (data out) and write (data in) cycles can be executed repeatedly during one  $\overline{\text{RAS}}$  cycle. The EDO page mode allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

**Truth Table: GLT41216**

Function		RAS	CAS	UW	LW	OE	ADDRESS	DQs	Notes
Standby		H	H→X	X	X	X		High-Z	
Read: Word		L	L	H	H	L	ROW/COL	Data Out	
Write: Word(Early Write)		L	L	L	L	X	ROW/COL	Data-In	
Write: Lower Byte (Early)		L	L	H	L	X	ROW/COL	Lower Byte,Data-In Upper Byte,High-Z	
Write: Upper Byte (Early)		L	L	L	H	X	ROW/COL	Lower Byte,High-Z Upper Byte,Data-In	
Read Write		L	L	H→L	H→L	L→H	ROW/COL	Data-Out,Data-In	1,2
EDO-Page-Mode Read	1st Cycle	L	H→L	H	H	L	ROW/COL	Data-Out	1
	2nd Cycle	L	H→L	H	H	L	COL	Data-Out	1
EDO-Page-Mode Write	1st Cycle	L	H→L	L	L	X	ROW/COL	Data-In	2
	2nd Cycle	L	H→L	L	L	X	COL	Data-In	2
EDO-Page-Mode Read-Write	1st Cycle	L	H→L	H→L	H→L	L→H	ROW/COL	Data-Out,Data-In	1,2
	2st Cycle	L	H→L	H→L	H→L	L→H	COL	Data-Out,Data-In	1,2
Hidden Refresh	Read	L→H→L	L	H	H	L	ROW/COL	Data-Out	1
	Write	L→H→L	L	L	L	X	ROW/COL	Data-In	2,3
RAS -Only Refresh		L	H	X	X	X	ROW	High-Z	
CBR Refresh		H→L	L	X	X	X		High-Z	

**Notes:**

1. These READ cycles are always WORD READ cycles.
2. These WRITE cycles may also be BYTE READ cycles (either  $\overline{UW}$  or  $\overline{LW}$  active).
3. EARLY WRITE only.

**DC and Operating Characteristics (1-2)**
 $T_A = 0^\circ\text{C to } 70^\circ\text{C}$ ,  $V_{CC}=5V\pm 10\%$ ,  $V_{SS}=0V$ , unless otherwise specified.

Sym.	Parameter	Test Conditions	Access Time	Min.	Typ	Max.	Unit	Notes
$I_{LI}$	Input Leakage Current (any input pin)	$0V \leq V_{IN} \leq 5.5V$ (All other pins not under test=0V)		-10		+10	$\mu\text{A}$	
$I_{LO}$	Output Leakage Current (for High-Z State)	$0V \leq V_{out} \leq 5.5V$ Output is disabled (Hiz)		-10		+10	$\mu\text{A}$	
$I_{CC1}$	Operating Current, Random READ/WRITE	$t_{RC} = t_{RC} (\text{min.})$	$t_{RAC} = 30\text{ns}$ $t_{RAC} = 35\text{ns}$ $t_{RAC} = 40\text{ns}$ $t_{RAC} = 45\text{ns}$			180 170 160 150	mA	1,2
$I_{CC2}$	Standby Current,(TTL)	$\overline{\text{RAS}}, \overline{\text{CAS}}$ , at $V_{IH}$ other inputs $\geq V_{SS}$				2	mA	
$I_{CC3}$	Refresh Current, RAS -Only	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ , at $V_{IH}$ $t_{RC} = t_{RC} (\text{min.})$	$t_{RAC} = 30\text{ns}$ $t_{RAC} = 35\text{ns}$ $t_{RAC} = 40\text{ns}$ $t_{RAC} = 45\text{ns}$			180 170 160 150	mA	2
$I_{CC4}$	Operating Current, EDO Page Mode	$\overline{\text{RAS}}$ at $V_{IL}$ , $\overline{\text{CAS}}$ address cycling: $t_{PC} = t_{PC}(\text{min.})$	$t_{RAC} = 30\text{ns}$ $t_{RAC} = 35\text{ns}$ $t_{RAC} = 40\text{ns}$ $t_{RAC} = 45\text{ns}$			180 170 160 150	mA	1,2
$I_{CC5}$	Refresh Current, CAS Before RAS	$\overline{\text{RAS}}, \overline{\text{CAS}}$ , address cycling: $t_{RC} = t_{RC} (\text{min.})$	$t_{RAC} = 30\text{ns}$ $t_{RAC} = 35\text{ns}$ $t_{RAC} = 40\text{ns}$ $t_{RAC} = 45\text{ns}$			180 170 160 150	mA	1
$I_{CC6}$	Standby Current, (CMOS)	$\overline{\text{RAS}} \geq V_{CC}-0.2V$ , $\overline{\text{CAS}} \geq V_{CC}-0.2V$ , All other inputs $V_{SS}$				1	mA	
$V_{IL}$	Input Low Voltage			-1		+0.8	V	3
$V_{IH}$	Input High Voltage			2.4		$V_{CC}+1$	V	3
$V_{OL}$	Output Low Voltage	$I_{OL} = 4.2\text{mA}$				0.4	V	
$V_{OH}$	Output High Voltage	$I_{OH} = -5\text{mA}$		2.4			V	

**Notes:**

- $I_{CC}$  is dependent on output loading when the device output is selected. Specified  $I_{CC}(\text{max.})$  is measured with the output open.
- $I_{CC}$  is dependent upon the number of address transitions specified  $I_{CC}(\text{max.})$  is measured with a maximum of one transition per address cycle in random Read/Write and EDO Fast Page Mode.
- Specified  $V_{IL}(\text{min.})$  is steady state operation. During transitions  $V_{IL}(\text{min.})$  may undershoot to -1.0V for a period not to exceed 20ns. All AC parameters are measured with  $V_{IL}(\text{min.}) \geq V_{SS}$  and  $V_{IH}(\text{max.}) \leq V_{CC}$ .

## AC Characteristics

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{IH}/V_{IL} = 2.4/0.8\text{ V}$ ,  $V_{OH}/V_{OL} = 2.0/0.8\text{ V}$

An initial pause of 100  $\mu\text{s}$  and 8  $\overline{\text{CAS}}$ -before-RAS or RAS-only refresh cycles are required after power-up.

Parameter	Symbol	30		35		40		45		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Read or Write Cycle Time	$t_{RC}$	65		70		75		80		ns	
Read Modify Write Cycle Time	$t_{RWC}$	85		87		93		103		ns	
RAS Precharge Time	$t_{RP}$	25		25		25		30		ns	
RAS Pulse Width	$t_{RAS}$	30	100k	35	100k	40	100k	45	100k	ns	
Access Time from $\overline{\text{RAS}}$	$t_{RAC}$		30		35		40		45	ns	1,2,3
Access Time from $\overline{\text{CAS}}$	$t_{CAC}$		10		11		12		12	ns	1,5,10
Access Time from Column Address	$t_{AA}$		15		18		20		22	ns	1,5,6
$\overline{\text{CAS}}$ to Output Low-Z	$t_{CLZ}$	0		0		0		0		ns	
$\overline{\text{CAS}}$ to Output High-Z	$t_{CEZ}$	3		3	8	3	8	3	8	ns	
RAS Hold Time	$t_{RSH}$	10		12		12		13		ns	
RAS Hold Time Referenced to $\overline{\text{OE}}$	$t_{ROH}$	7		8		8		9		ns	
$\overline{\text{CAS}}$ Hold Time	$t_{CSH}$	25		30		34		40		ns	
$\overline{\text{CAS}}$ Pulse Width	$t_{CAS}$	4.5		6	10K	6	10K	7	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	$t_{RCD}$	13		17	24	18	28	18	33	ns	
$\overline{\text{RAS}}$ to Column Address Delay Time	$t_{RAD}$	10		12	17	13	20	13	23	ns	7
$\overline{\text{CAS}}$ to RAS Precharge Time	$t_{CRP}$	5		5		5		5		ns	
Row Address Set-Up Time	$t_{ASR}$	0		0		0		0		ns	
Row Address Hold Time	$t_{RAH}$	6		7		8		8		ns	
Column Address Set-Up Time	$t_{ASC}$	0		0		0		0		ns	
Column Address Hold Time	$t_{CAH}$	6		6		6		6		ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	$t_{RAL}$	15		18		20		23		ns	
Column Address Hold Time Referenced to $\overline{\text{RAS}}$	$t_{AR}$	26		30		34		39		ns	
Read Command Set-Up Time	$t_{RCS}$	0		0		0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	$t_{RCH}$	0		0		0		0		ns	4
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	$t_{RRH}$	0		0		0		0		ns	4
Write Command Set-Up Time	$t_{WCS}$	0		0		0		0		ns	8,9
Write Command Hold Time	$t_{WCH}$	6		6		6		6		ns	
Write Command Pulse Width	$t_{WCP}$	6		6		6		6		ns	

## AC Characteristics

Parameter	Symbol	30		35		40		45		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Write Command to $\overline{\text{RAS}}$ Lead Time	$t_{\text{RWL}}$	10		11		12		12		ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	$t_{\text{CWL}}$	10		11		12		12		ns	
Data Set-Up Time	$t_{\text{DS}}$	0		0		0		0		ns	
Data Hold Time	$t_{\text{DH}}$	6		7		8		8		ns	
Data Hold Time Referenced to $\overline{\text{RAS}}$	$t_{\text{DHR}}$	26		31		36		41		ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	$t_{\text{RWD}}$	44		49		54		59		ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	$t_{\text{CWD}}$	22		23		24		24		ns	
Column Address to $\overline{\text{WE}}$ Delay Time	$t_{\text{AWD}}$	25		30		32		34		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	$t_{\text{RPC}}$	0		0		0		0		ns	
Access Time from $\overline{\text{CAS}}$ Precharge	$t_{\text{CPA}}$		17		20		22		24	ns	
EDO Page Mode Cycle Time	$t_{\text{PC}}$	12		13		15		18		ns	
EDO Page Mode Read-Modify-Write Cycle Time	$t_{\text{PRWC}}$	43		47		50		52		ns	
$\overline{\text{CAS}}$ Precharge Time (EDO Page Mode)	$t_{\text{CP}}$	4.5		5		5		7		ns	
$\overline{\text{RAS}}$ Pulse Width (EDO Page Mode Only)	$t_{\text{RASP}}$	30	100k	35	100k	40	100k	45	100k	ns	
Access Time from $\overline{\text{OE}}$	$t_{\text{OEA}}$		10		11		12		12	ns	
$\overline{\text{OE}}$ to Data Delay Time	$t_{\text{OED}}$	8		8		8		8		ns	
$\overline{\text{OE}}$ to Output High-Z	$t_{\text{OEZ}}$	3	8	3	8	3	8	3	8	ns	
$\overline{\text{OE}}$ Command Hold Time	$t_{\text{OEH}}$	6		6		7		7		ns	
Data Output Hold after $\overline{\text{CAS}}$ low	$t_{\text{DOH}}$	3		3		3		5		ns	
$\overline{\text{RAS}}$ to Output High-Z	$t_{\text{REZ}}$	3	8	3	8	3	8	3	8	ns	
$\overline{\text{WE}}$ to Output High-Z	$t_{\text{WEZ}}$	3	10	3	10	3	10	3	10	ns	
$\overline{\text{OE}}$ to $\overline{\text{CAS}}$ Hold Time	$t_{\text{OCH}}$	8		8		8		8		ns	
$\overline{\text{CAS}}$ Hold Time to $\overline{\text{OE}}$	$t_{\text{CHO}}$	8		8		8		8		ns	
$\overline{\text{OE}}$ Precharge Time	$t_{\text{OEP}}$	8		8		8		8		ns	
$\overline{\text{CAS}}$ Set-Up Time for $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Cycle	$t_{\text{CSR}}$	10		10		10		10		ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Cycle	$t_{\text{CHR}}$	10		10		10		10		ns	
Transition Time	$t_{\text{T}}$	1.5	50	2	50	2	50	2	50	ns	
Refresh Period	$t_{\text{REF}}$		4		4		4		4	ms	

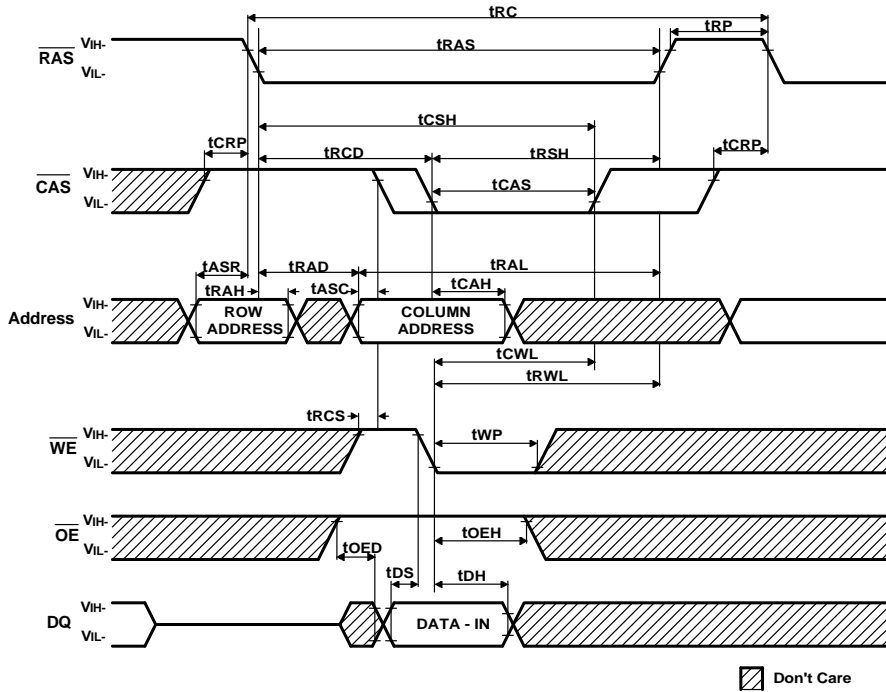


**Notes:**

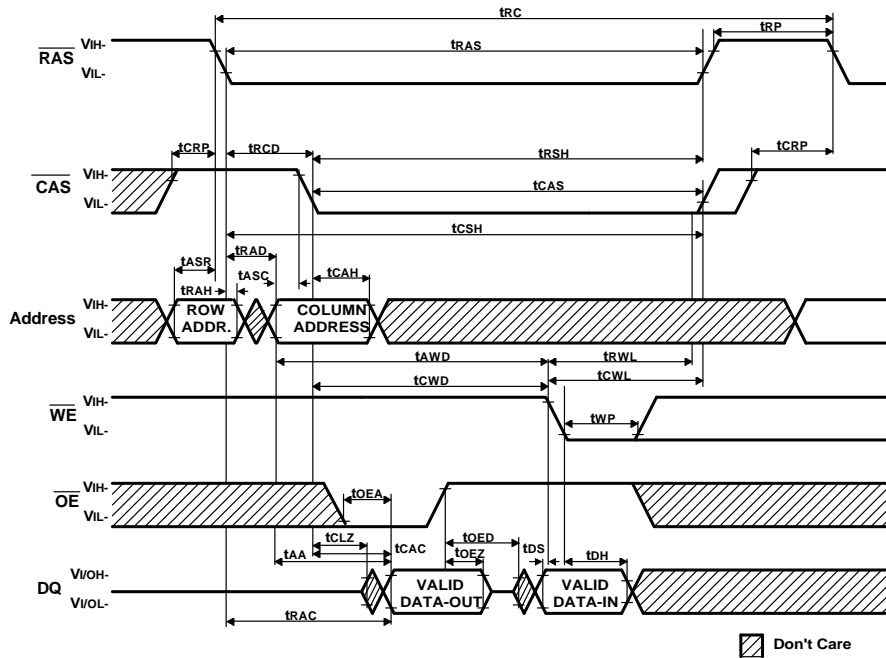
1. Measure with a load equivalent to 1TTL inputs and 50 pF.
2. Assumes that  $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max.})$ . If  $t_{\text{RCD}}$  is greater than  $t_{\text{RCD}}(\text{max.})$ , access time will be  $t_{\text{AA}}$  dominant.
3. Assumes that  $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max.})$ . If  $t_{\text{RAD}}$  is greater than  $t_{\text{RCD}}(\text{max.})$ , access time will be controlled by  $t_{\text{CAC}}$ .
4. Either  $t_{\text{RRH}}$  or  $t_{\text{RCH}}$  must be satisfied for a Read Cycle.
5. Access time is determined by the longest of  $t_{\text{AA}}$ ,  $t_{\text{CAC}}$  and  $t_{\text{CPA}}$ .
6. Assumes that  $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max.})$ .
7. Operation within the  $t_{\text{RAD}}(\text{max.})$  limit ensures that  $t_{\text{RAC}}(\text{max.})$  can be met.  $t_{\text{RAD}}(\text{max.})$  is specified as a reference point only. If  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}(\text{max.})$  limit, the access time is controlled by  $t_{\text{AA}}$  and  $t_{\text{CAC}}$ .
8.  $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{AWD}}$  and  $t_{\text{CWD}}$  are not restrictive operating parameters.
9.  $t_{\text{WCS}}(\text{min.})$  must be satisfied in an Early Write Cycle.
10.  $t_{\text{DS}}$  and  $t_{\text{DH}}$  are referenced to the latter occurrence of  $\overline{\text{CAS}}$  or  $\overline{\text{WE}}$ .
11.  $t_{\text{T}}$  is measured between  $V_{\text{IH}}(\text{min.})$  and  $V_{\text{IL}}(\text{max.})$ . AC-measurements assume  $t_{\text{T}} = 2 \text{ ns}$ .



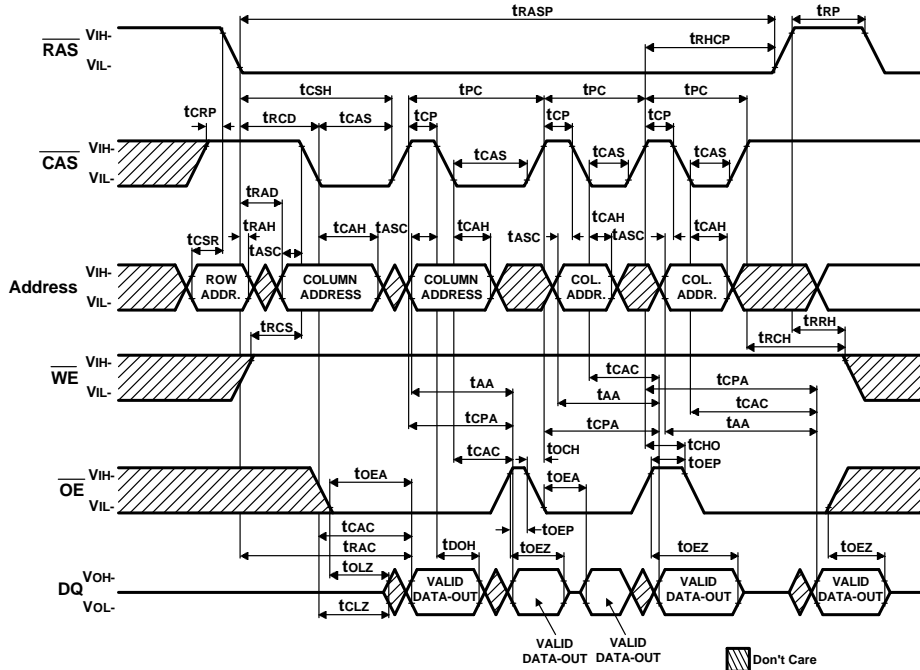
**OE Controlled Write Cycle** NOTE : D<sub>OUT</sub> = OPEN



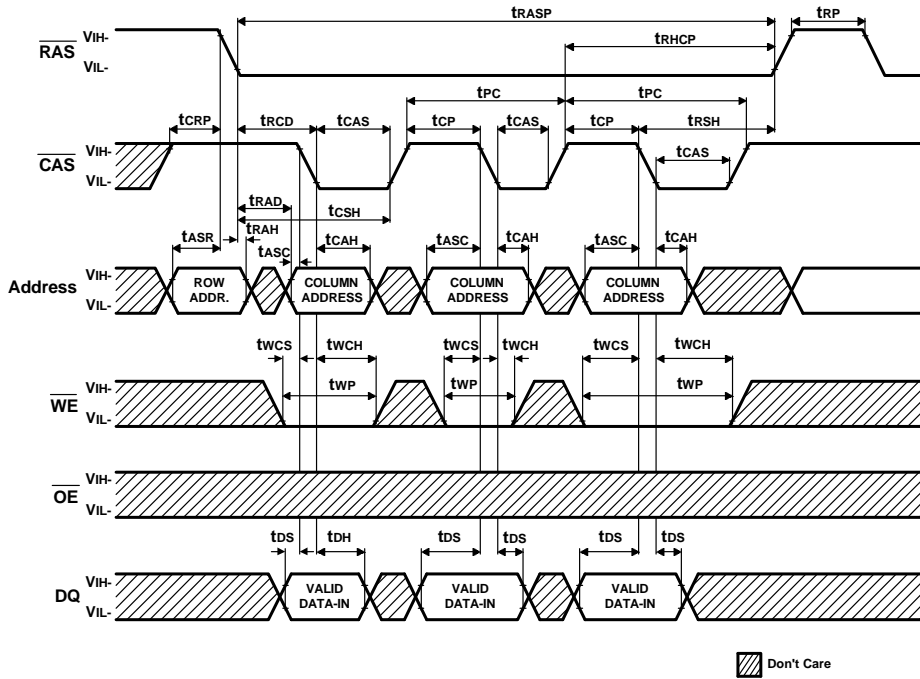
**Read - Modify - Write Cycle**



**EDO Page Mode Read Cycle** NOTE : D<sub>OUT</sub> = OPEN



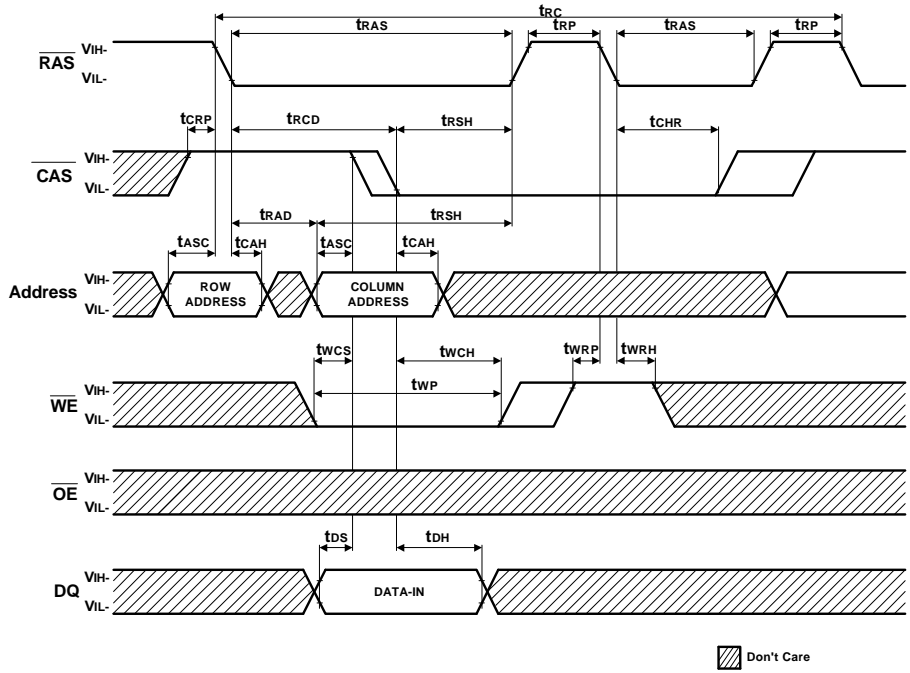
**EDO Page Mode Early Write Cycle** NOTE : D<sub>OUT</sub> = OPEN







**Hidden Refresh Cycle ( Write )** NOTE : D<sub>OUT</sub> = OPEN

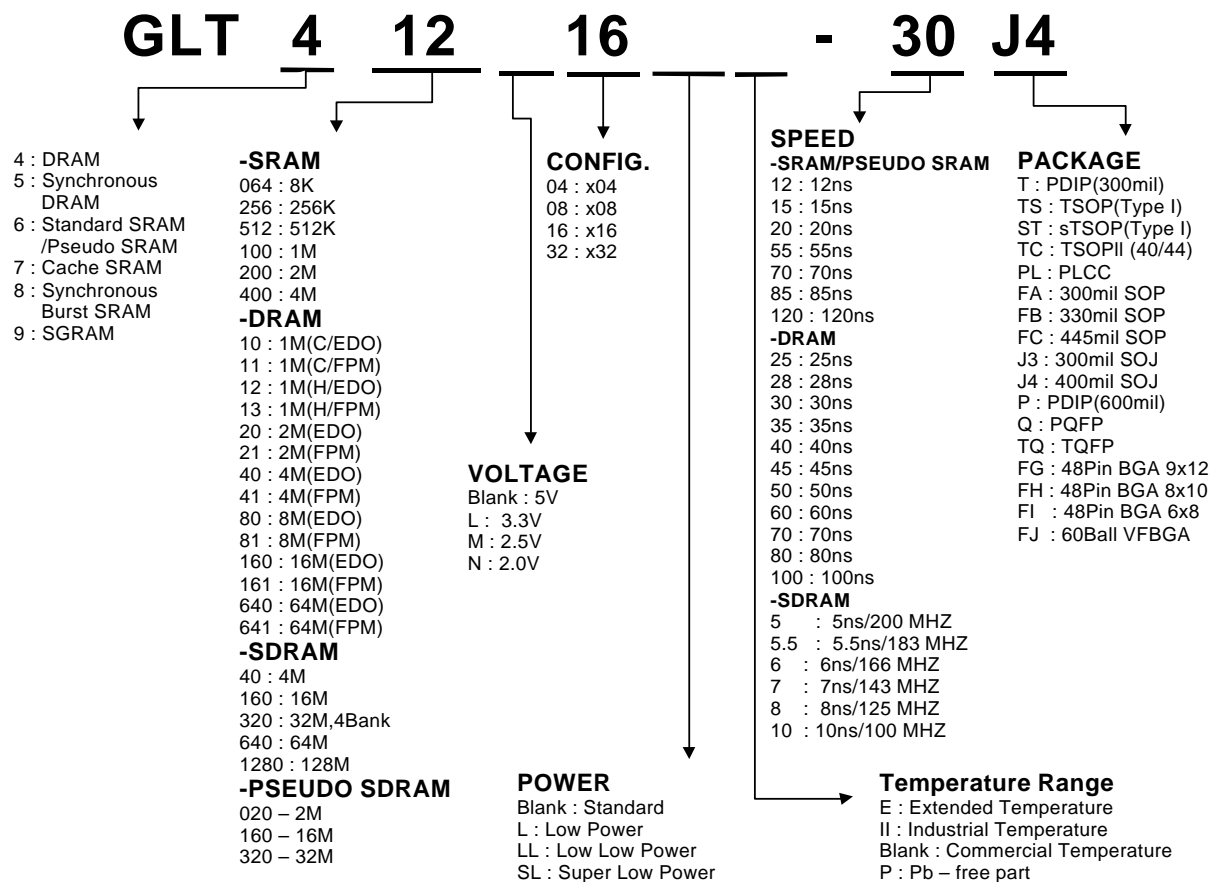






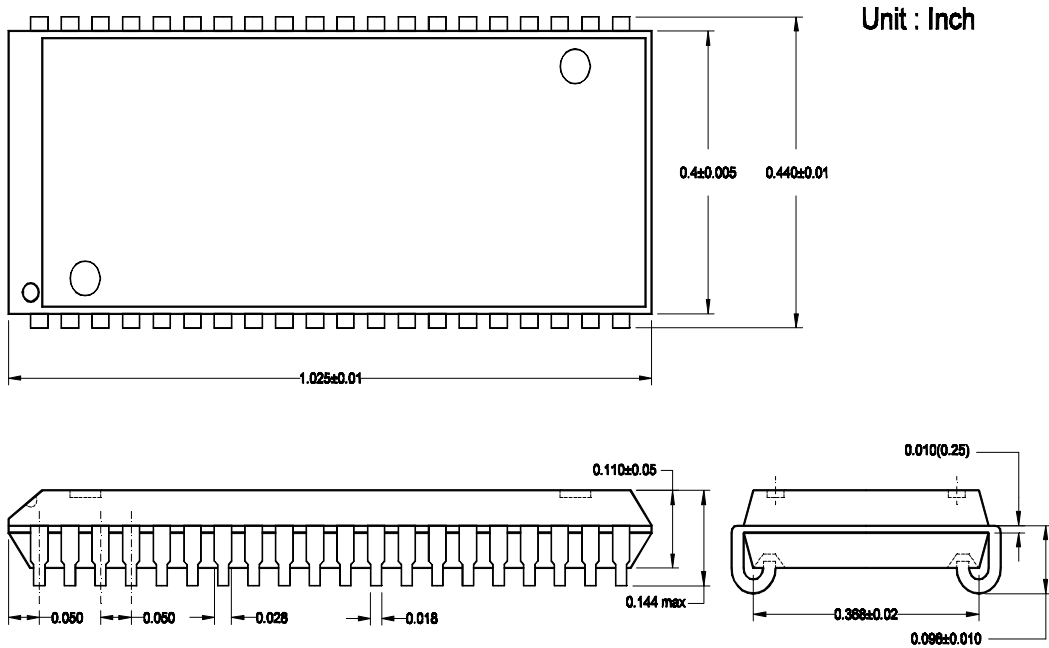
**Ordering Information**

<b>Part Number</b>	<b>SPEED</b>	<b>POWER</b>	<b>FEATURE</b>	<b>PACKAGE</b>
GLT41216-30J4	30ns	Normal	EDO	SOJ 400mil 40L
GLT41216-35J4	35ns	Normal	EDO	SOJ 400mil 40L
GLT41216-40J4	40ns	Normal	EDO	SOJ 400mil 40L
GLT41216-45J4	45ns	Normal	EDO	SOJ 400mil 40L
GLT41216-30TC	30ns	Normal	EDO	TSOP 400mil 44L
GLT41216-35TC	35ns	Normal	EDO	TSOP 400mil 44L
GLT41216-40TC	40ns	Normal	EDO	TSOP 400mil 44L
GLT41216-45TC	45ns	Normal	EDO	TSOP 400mil 44L

**Parts Numbers (Top Mark) Definition :**


**Package Information**

400mil 40 pin Small Outline J-form Package (SOJ)



40/44 Lead Thin Small Outline Package TSOP(Type II)

