VT82C596A
“Mobile South” South Bridge

MPIPC
Mobile PCI Integrated Peripheral Controller

PC98 Compliant PCI-to-ISA Bridge with ACPI, Enhanced Power Management, SMBus, Distributed DMA, Serial IRQ, Plug and Play, UltraDMA-33 Master Mode PCI-EIDE Controller USB Controller, Keyboard Controller, and RTC in a PIIX4 Pin Compatible BGA Package

Revision 1.1
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VIA TECHNOLOGIES, INC.

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REVISION HISTORY

Document Release	Date	Revision	Initials
Revision 0.1	11/5/97	Initial release based on 82C586B Data Sheet revision 1.0 - Updated pinouts to reflect BGA package and new/changed pin definitions - Changed mechanical spec to 324-pin BGA - Updated part name, description, and feature bullets - Updated registers to reflect changes from 586B	DH
Revision 0.2	11/11/97	Fixed miscellaneous typographical errors Updated power management feature bullets Renamed CLKRUN#->PCKRUN#, PCICLK->PCLK, VCCRTC->VBAT Added SLPBTN# function to GPI13 Added descriptions for pins CFG1-2 and TEST# Moved reference of PWROK & RSMRST# from VBAT to VCCSUS Added Keyboard Controller SRAM Data R/W (I/O Ports 21-3F and 61-7F) Register Updates: - Function 0, Rx68 (SERIRQ control register). Added note about frame size - Function 1 (IDE) - Rx43[7] definition changed - Rx43[6-5] changed to 3-bit field in bits 6-4 (bit-4 formerly reserved) - Rx44[2] defined - Rx44[1-0] changed to reserved - Rx50[31] fixed typo (was bit-6, changed to bit-30) - Rx50[26, 18, 10, 2] extended cycle time fields from 2 bits to 3 bits - Rx50[3, 19] changed to reserved (do not program) - Function 2 (USB) – Rx3C[3-0] = 1111 now disables USB interrupt - Function 3 (Power Management) - Rx4C[7-4] – Thermal Duty Cycle changed to 4-bit field (bit-4 redefined) - I/O Space Rx10 – Added clarifying notes, added bit names, fixed typos - I/O Space Rx4C – Fixed typo Power management functional description rewritten & moved to new section Added more detailed block diagram in Functional Description section	DH
Revision 0.3	1/30/98	Updated Feature Bullets Updated Pin Descriptions: Added strap options on SD7:4 Updated Register Descriptions: - Func 0 Rx4, Rx59, Rx5A - Func 1 Rx45 - Func 3 Rx8, Rx0D, Rx48, Rx4C, Rx80 –88 (& added SMBus I/O registers) - Pwr Mgmt I/O offsets 14, 15, 20, 2C Changed I/O register headers from “Offset” to “I/O Offset”	DH
Revision 0.4	2/17/98	Updated feature bullets: Apollo P6 => Apollo Pro; PC97 =>PC98 Fixed pin directions: SERIRQ,SERR#,IOCHRDY,MCS16#,IOCS16#,SPKR Changed pin direction “B” to “IO” for consistency Added missing pin directions on MCCS# and IDE “CS” and address pins Fixed default on Rx50 & removed Rx57 pin # reference note	DH
Revision 1.0	9/15/98	Fixed pinouts: H3=USBP0-, G2=USBP0+, H2=USBP1-, F1=USBP1+ Fixed PIRQ Routing (register definitions Rx55[7-4], Rx56, Rx57[7-4]) Changed default from 0 to 1 for I/O offset 3-2 bit-8 Power Button Enable	DH
Revision 1.1	12/9/98	Changed part number to 596A Swapped pinouts of RTCCS# and ROMCS# (balls K2 and M2) Fixed polarity of Function 2 USB Rx41[2]	DH

VT82C596 MPIPC

MOBILE PCI INTEGRATED PERIPHERAL CONTROLLER

PC98 COMPLIANT PCI-TO-ISA BRIDGE WITH ACPI, ENHANCED POWER MANAGEMENT, SMBUS, DISTRIBUTED DMA, SERIAL IRQ, PLUG AND PLAY, ULTRADMA-33 MASTER MODE PCI-EIDE CONTROLLER, USB CONTROLLER, KEYBOARD CONTROLLER, AND RTC IN A PIIX4 PIN COMPATIBLE BGA PACKAGE

- **Inter-operable with VIA and other Host-to-PCI Bridges**
  - Combine with VT82C597 for a complete 66MHz Socket-7 PCI / AGP / ISA system (Apollo VP3)
  - Combine with VT82C598 for a complete 66 / 75 / 83 / 100MHz Socket-7 PCI / AGP / ISA system (Apollo MVP3)
  - Combine with VT82C691 for a complete Socket-8 or Slot-1 PCI / ISA system (Apollo Pro)
  - Inter-operable with Intel or other Host-to-PCI bridges for a complete PC97 compliant PCI / AGP / ISA system
- **Pin-compatible upgrade for PIIX4 for existing designs**
- **PC98 Compliant PCI to ISA Bridge**
  - Integrated ISA Bus Controller with integrated DMA, timer, and interrupt controller
  - Integrated Keyboard Controller with PS2 mouse support
  - Integrated DS12885-style Real Time Clock with extended 256 byte CMOS RAM and Day/Month Alarm for ACPI
  - Integrated USB Controller with root hub and two function ports
  - Integrated UltraDMA-33 master mode EIDE controller with enhanced PCI bus commands
  - PCI-2.1 compliant with delay transaction
  - Eight double-word line buffer between PCI and ISA bus
  - One level of PCI to ISA post-write buffer
  - Supports type F DMA transfers
  - Distributed DMA support for ISA legacy DMA across the PCI bus
  - Sideband signal support for PC/PCI and serial interrupt for docking and non-docking applications
  - Fast reset and Gate A20 operation
  - Edge trigger or level sensitive interrupt
  - Flash EPROM, 2Mb EPROM and combined BIOS support
  - Supports positive and subtractive decoding
  - Supports external APIC interface for symmetrical multiprocessor configurations
- **UltraDMA-33 Master Mode PCI EIDE Controller**
  - Dual channel master mode PCI supporting four Enhanced IDE devices
  - Transfer rate up to 33MB/sec to cover PIO mode 4, multi-word DMA mode 2 drives, and UltraDMA-33 interface
  - Thirty-two levels (doublewords) of prefetch and write buffers
  - Dual DMA engine for concurrent dual channel operation
  - Bus master programming interface for SFF-8038i rev.1.0 and Windows-95 compliant
  - Full scatter gather capability
  - Support ATAPI compliant devices including DVD devices
  - Support PCI native and ATA compatibility modes
  - Complete software driver support
  - Supports glue-less “Swap-Bay” option with full electrical isolation

- **Universal Serial Bus Controller**
  - USB v.1.0 and Intel Universal HCI v.1.1 compatible
  - Eighteen level (doublewords) data FIFO with full scatter and gather capability
  - Root hub and two function ports
  - Integrated physical layer transceivers with over-current detection status on USB inputs
  - Legacy keyboard and PS/2 mouse support
- **System Management Bus Interface**
  - Host interface for processor communications
  - Slave interface for external SMBus masters
- **Sophisticated PC97-Compatible Mobile Power Management**
  - Supports both ACPI (Advanced Configuration and Power Interface) and legacy (APM) power management
  - ACPI v1.0 Compliant
  - APM v1.2 Compliant
  - CPU clock throttling and clock stop control for complete ACPI C0 to C3 state support
  - PCI bus clock run and PCI/CPU clock generator stop control
  - Supports multiple system suspend types: power-on suspends with flexible CPU/PCI bus reset options, suspend to DRAM, and suspend to disk (soft-off), all with hardware automatic wake-up
  - Multiple suspend power plane controls and suspend status indicators
  - One idle timer, one peripheral timer and one general purpose timer, plus 24/32-bit ACPI compliant timer
  - Normal, doze, sleep, suspend and conserve modes
  - Global and local device power control
  - System event monitoring with two event classes
  - Primary and secondary interrupt differentiation for individual channels
  - Dedicated input pins for power and sleep buttons, external modem ring indicator, and notebook lid open/close for system wake-up
  - Up to 22 general purpose input ports and 31 output ports
  - Multiple internal and external SMI sources for flexible power management models
  - Two programmable chip selects and one microcontroller chip select
  - Enhanced integrated real time clock (RTC) with date alarm, month alarm, and century field
  - Thermal alarm support
  - Cache SRAM power-down control
  - Hot docking support
  - I/O pad leakage control
- **Plug and Play Controller**
  - PCI interrupts steerable to any interrupt channel
  - Three steerable interrupt channels for on-board plug and play devices
  - Microsoft Windows 95™ and plug and play BIOS compliant
- **Built-in NAND-tree pin scan test capability**
- **0.5u, 3.3V, low power CMOS process**
- **Single chip 324 pin BGA**

OVERVIEW

The VT82C596 MPIPC (Mobile PCI Integrated Peripheral Controller) is a high integration, high performance, power-efficient, and high compatibility device that supports Intel and non-Intel based processor to PCI bus bridge functionality to make a complete Microsoft PC97-compliant PCI/ISA system. In addition to complete ISA extension bus functionality, the VT82C596 includes standard intelligent peripheral controllers:

a) Master mode enhanced IDE controller with dual channel DMA engine and interlaced dual channel commands. Dedicated FIFO coupled with scatter and gather master mode operation allows high performance transfers between PCI and IDE devices. In addition to standard PIO and DMA mode operation, the VT82C596 also supports the UltraDMA-33 standard to allow reliable data transfer rates up to 33MB/sec throughput. The IDE controller is SFF-8038i v1.0 and Microsoft Windows-95 compliant.

b) Universal Serial Bus controller that is USB v1.0 and Universal HCI v1.1 compliant. The VT82C596 includes the root hub with two function ports with integrated physical layer transceivers. The USB controller allows hot plug and play and isochronous peripherals to be inserted into the system with universal driver support. The controller also implements legacy keyboard and mouse support so that legacy software can run transparently in a non-USB-aware operating system environment.

c) Keyboard controller with PS2 mouse support.

d) Real Time Clock with 256 byte extended CMOS. In addition to the standard ISA RTC functionality, the integrated RTC also includes the date alarm, century field, and other enhancements for compatibility with the ACPI standard.

e) Notebook-class power management functionality compliant with ACPI and legacy APM requirements. Multiple sleep states (power-on suspend, suspend-to-DRAM, and suspend-to-Disk) are supported with hardware automatic wake-up. Additional functionality includes event monitoring, CPU clock throttling and stop (Intel processor protocol), PCI bus clock stop control, modular power, clock and leakage control, hardware-based and software-based event handling, general purpose I/O, chip select and external SMI.

f) Full System Management Bus (SMBus) interface.

g) Distributed DMA capability for support of ISA legacy DMA over the PCI bus. PC/PCI and Serial IRQ mechanisms are also supported for docking and non-docking applications.

h) Plug and Play controller that allows complete steerability of all PCI interrupts to any interrupt channel. Three additional steerable interrupt channels are provided to allow plug and play and reconfigurability of on-board peripherals for Windows 95 compliance.

i) External IOAPIC interface for Intel-compliant symmetrical multiprocessor systems.

The VT82C596 also enhances the functionality of the standard ISA peripherals. The integrated interrupt controller supports both edge and level triggered interrupts channel by channel. The integrated DMA controller supports type F DMA in addition to standard ISA DMA modes. Compliant with the PCI-2.1 specification, the VT82C596 supports delayed transactions so that slower ISA peripherals do not block the traffic of the PCI bus. Special circuitry is built in to allow concurrent operation without causing dead lock even in a PCI-to-PCI bridge environment. The chip also includes eight levels (doublewords) of line buffers from the PCI bus to the ISA bus to further enhance overall system performance.

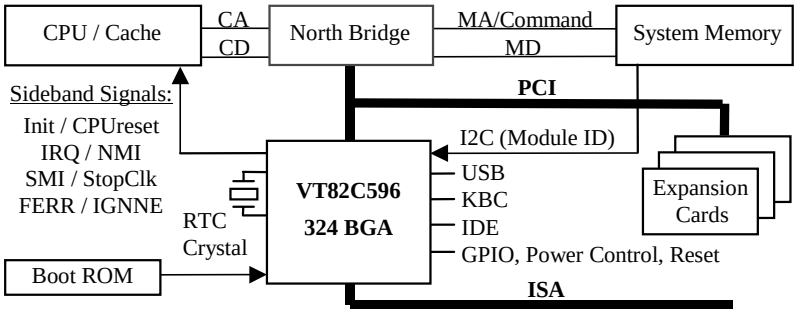

Figure 1. PC System Configuration Using the VT82C596