CEP740A/CEB740A
CEI740A/CEF740A

N-Channel Enhancement Mode Field Effect Transistor

FEATURES

Type	V_{DSS}	$R_{DS(ON)}$	I_D	@V_{GS}
CEP740A	400V	650mΩ	10A	10V
CEB740A	400V	650mΩ	10A	10V
CEI740A	400V	650mΩ	10A	10V
CEF740A	400V	650mΩ	10A [e]	10V

■ Super high dense cell design for extremely low $R_{DS(ON)}$.

■ High power and current handing capability.

■ Lead free product is acquired.

■ TO-220 & TO-263 & TO-262 package & TO-220F full-pak for through hole.
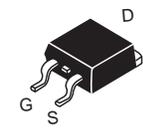
CEB SERIES
TO-263(DD-PAK)

CEI SERIES
TO-262(I2-PAK)
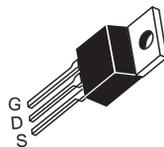
CEP SERIES
TO-220
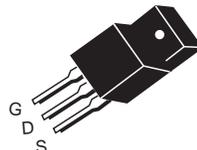
CEF SERIES
TO-220F
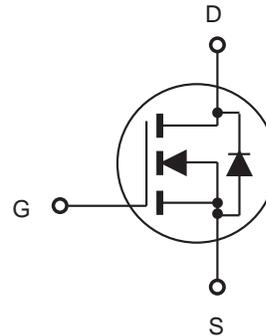
ABSOLUTE MAXIMUM RATINGS $T_C = 25^{\circ}C$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263/262	TO-220F	
Drain-Source Voltage	V_{DS}	400		V
Gate-Source Voltage	V_{GS}	±30		V
Drain Current-Continuous	I_D	10	10 [e]	A
Drain Current-Pulsed [a]	I_{DM} [f]	40	40 [e]	A
Maximum Power Dissipation @ $T_C = 25^{\circ}C$	P_D	125	43	W
- Derate above 25°C		1	0.34	W/$^{\circ}$C
Single Pulsed Avalanche Energy [d]	E_{AS}	400	400	mJ
Single Pulsed Avalanche Current [d]	I_{AS}	10	10	A
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 150		$^{\circ}$C

Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	RθJC	1.0	2.9	$^{\circ}$C/W
Thermal Resistance, Junction-to-Ambient	RθJA	62.5	65	$^{\circ}$C/W

Electrical Characteristics $T_C = 25°C$ unless otherwise noted

4

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	400			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 400V, V_{GS} = 0V$			50	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -30V, V_{DS} = 0V$			-100	nA
On Characteristics [b]						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 6A$			650	$m\Omega$
Forward Transconductance	g_{FS}	$V_{DS} = 50V, I_D = 6A$	3	5.4		S
Dynamic Characteristics [c]						
Input Capacitance	C_{iss}	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0 MHz$		835		pF
Output Capacitance	C_{oss}			145		pF
Reverse Transfer Capacitance	C_{rss}			85		pF
Switching Characteristics [c]						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 200V, I_D = 10A,$ $V_{GS} = 10V, R_{GEN} = 9.1\Omega$		16	75	ns
Turn-On Rise Time	t_r			25	125	ns
Turn-Off Delay Time	$t_{d(off)}$			80	100	ns
Turn-Off Fall Time	t_f			35	60	ns
Total Gate Charge	Q_g	$V_{DS} = 320V, I_D = 10A,$ $V_{GS} = 10V$		52	65	nC
Gate-Source Charge	Q_{gs}			6.5		nC
Gate-Drain Charge	Q_{gd}			27		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current	I_S [g]				10	A
Drain-Source Diode Forward Voltage [b]	V_{SD}	$V_{GS} = 0V, I_S = 10A$			2	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature .
b.Pulse Test : Pulse Width $\leq$ 300μs, Duty Cycle $\leq$ 2% .
c.Guaranteed by design, not subject to production testing.
d.L =9.16mH, I_{AS} =10A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C .
e.Limited only by maximum temperature allowed .
f .Pulse width limited by safe operating area .
g.Full package $I_{S(max)}$ = 5A .
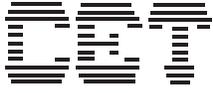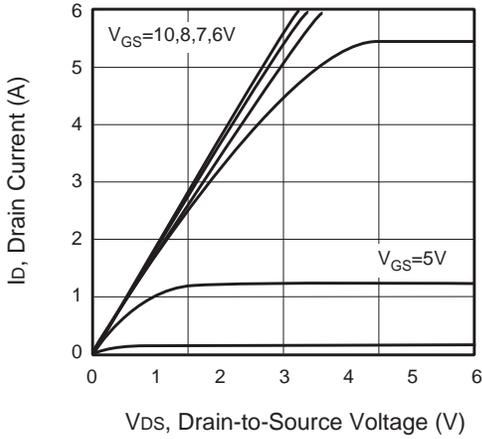
Figure 1. Output Characteristics
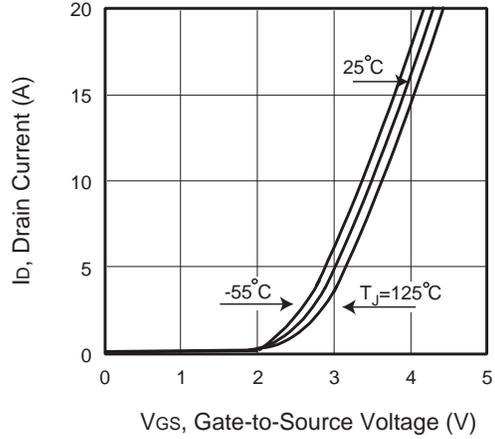
**Figure 2. Transfer Characteristics**
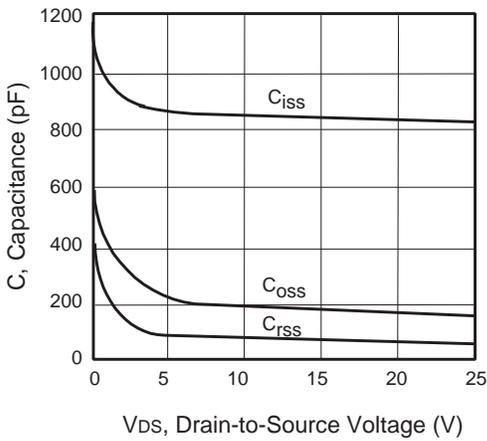
**Figure 3. Capacitance**
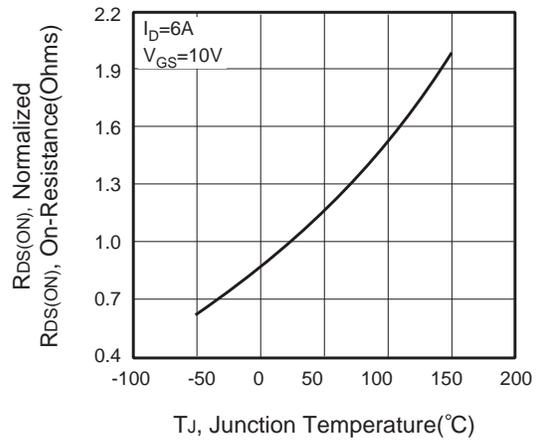
**Figure 4. On-Resistance Variation
with Temperature**
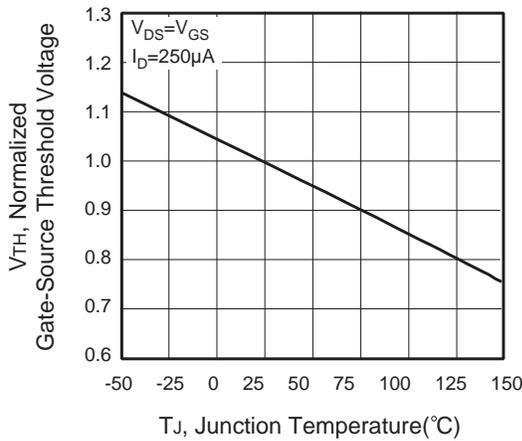
**Figure 5. Gate Threshold Variation
with Temperature**
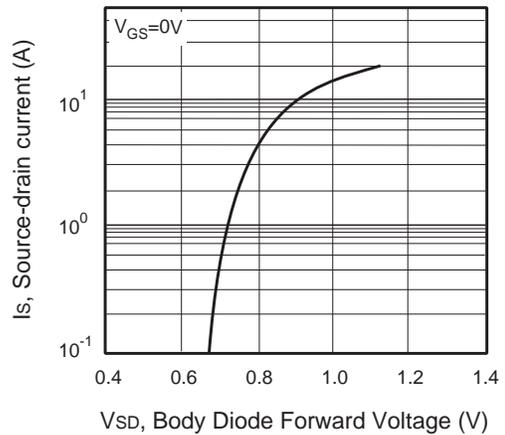
**Figure 6. Body Diode Forward Voltage
Variation with Source Current**
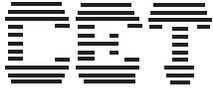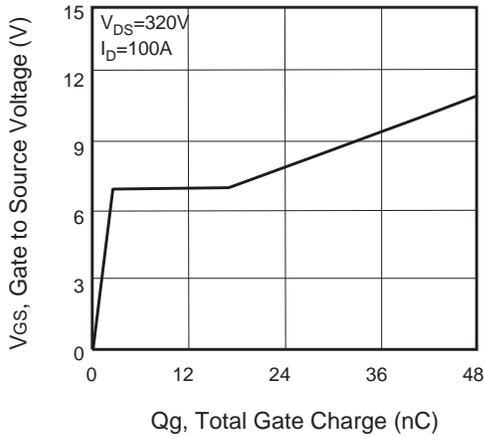
Figure 7. Gate Charge
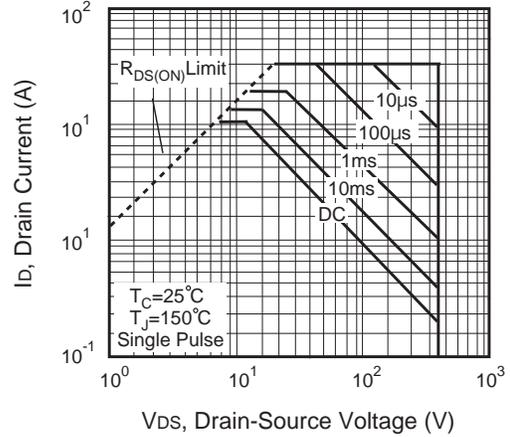
Figure 8. Maximum Safe Operating Area
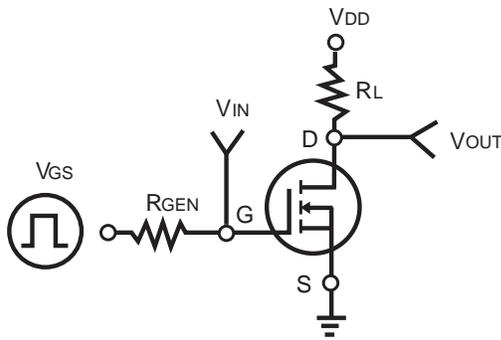
Figure 9. Switching Test Circuit
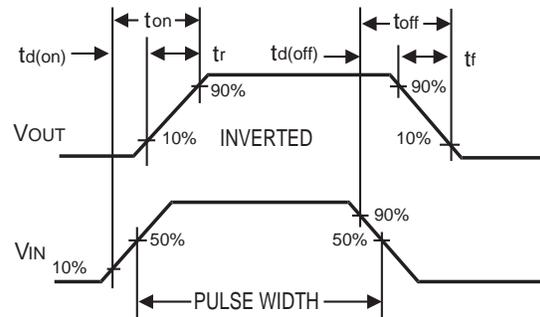
Figure 10. Switching Waveforms

1. $R_{JC}(t) = r(t) * R_{JC}$
2. R_{JC}=See Datasheet
3. $T_{JM} - T_C = P * R_{JC}(t)$
4. Duty Cycle, D=t1/t2
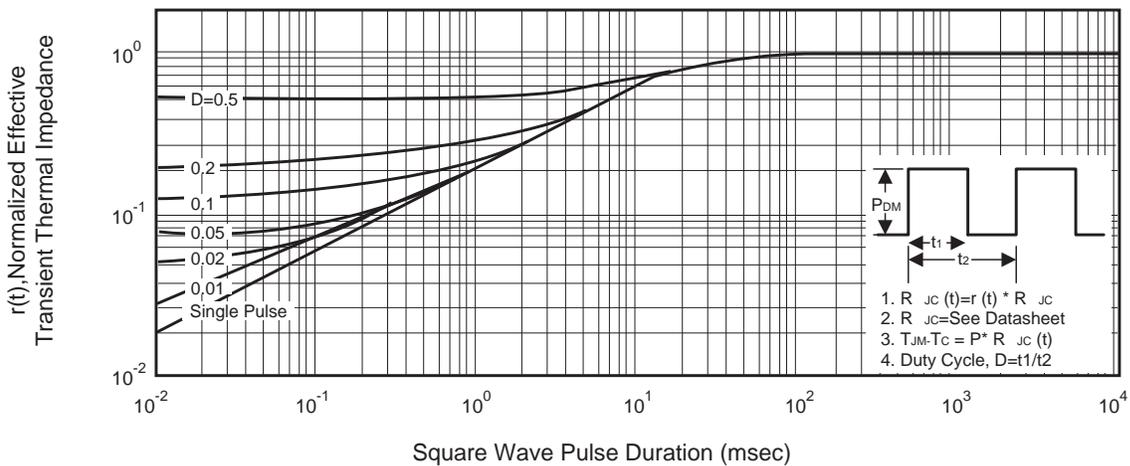
Figure 11. Normalized Thermal Transient Impedance Curve