82C206
Integrated Peripheral Controller

The 82C206 Integrated Peripheral Controller incorporates two 8237 DMA controllers, two 8259 Interrupt controllers, one 8254 Timer/Counter, one MC146818 Real Time Clock, a 74LS612 memory mapper, as well as several TTL/SSI interface logic chips. This offers a single chip integration of all the peripherals attached to the peripheral bus (x-bus) in the IBM PC/AT.

While offering a complete compatibility to the IBM PC/AT architecture, the 82C206 offers enhanced features and improved speed performance. These include an additional 64 bytes of user RAM for the Real Time Clock, and drastically reduced recovery specifications for the 8237, 8259, and 8254.

Variable wait state option is provided for the DMA cycles. Programmable delays are provided for the CPU access to the internal registers of the chip. The chip also provides an option to select 8 or 4 MHz system clock.

The 82C206, along with the CS8220 PC/AT compatible CHIPSet, provides a highly integrated high performance solution for a PC/AT compatible implementation.

The 82C206 is implemented using advanced CMOS technology and is packaged in an 84-pin PLCC.

Features

- 100% comaptible to IBM PC/AT
- Fully compatible to the Intel 8237 DMA controller, 8259 Interrupt controller, 8254 Timer/Counter, and the Motorola 146818 Real Time Clock
- Offers seven DMA channels, thirteen Interrupt request channels, two Timer/Counter channels, and a Real Time Clock
- Reduced recovery time (120 ns) between control
- 114 bytes of CMOS RAM memory
- 8 MHz DMA clock with programmable internal divider for 4 MHz operation
- Programmable wait states for the DMA cycle
- 16 MB DMA address space
- Single chip 84-pin CMOS implementation

Figure 1-2. *82C206 Integrated Peripheral Controller Block Diagram*