Am79Q4457/5457

Quad Subscriber Line Audio Processing Circuit-Non-Programmable (QSLAC™-NP) Devices

Legerity™
Formerly AMD's Communication Products Division

DISTINCTIVE CHARACTERISTICS

- **Performs the function of four Codec/Filters**
- **A-law or µ-law coding**
- **Single PCM port**
  - — Up to 4.096 MHz operation (64 channels)
- **Hardware programmable (via external components)**
  - — Transhybrid balance impedance
  - — Transmit and receive gains
- **Additional Am79Q4457 device capabilities (per channel, set external)**
  - — Three selectable transmit gains
  - — Three selectable receive gains
  - — Two selectable balance networks
  - — Simple serial control interface
- **Separate PCM and Master clocks**
- **1.536 MHz, 1.544 MHz, 2.048 MHz, or 4.096 MHz master clock options**
  - — Internal timing automatically adjusted based on MCLK and frame sync signal
- **Low power 5.0 V CMOS technology**
- **5.0 V only operation**

GENERAL DESCRIPTION

The Am79Q4457/5457 Quad Subscriber Line Audio Processing Circuit-Non-Programmable (QSLAC-NP) device integrates the key functions of analog linecards into a high-performance, four-channel Codec/Filter device. The QSLAC-NP devices are based on the proven design of the reliable Am79C02/03/031(A) Dual Subscriber Line Audio-Processing Circuit (DSLAC™) devices, and the Am79C202 Advanced Subscriber Line Audio-Processing Circuit (ASLAC™) device. The advanced architecture of the QSLAC-NP devices implements four independent channels in a single integrated circuit, providing a cost-effective solution for the audio-processing function of Plain Old Telephone Service (POTS) linecards.

The Am79Q4457/5457 QSLAC-NP device provides four industry-standard Codec/Filter devices in a single integrated circuit. The Am79Q4457/5457 device provides a transmit and receive frame synchronization input per channel. A-law or µ-law compression is selected via a device pin.

In addition, the Am79Q4457 device provides the ability to select one of three independent gain settings (both transmit and receive) and one of two balance networks on a per-channel basis. The transmit and receive gain levels are set once for the device via external components. Gain level selection and the balance network selection is achieved through an integrated serial shift register and latch per channel.

The Am79Q5457 device provides four industry-standard Codec/Filter devices in a 32-pin PLCC or 44-pin TQFP package. The Am79Q4457 device provides four industry-standard Codec/Filter devices and selectable gain and balance functions in a 44-pin PLCC or 44-pin TQFP package.

Advanced submicron CMOS technology enables the Am79Q4457/5457 QSLAC-NP device to have both the functionality and the low power consumption required in linecard designs, maximizing linecard density at a minimum cost. When used with four Legerity SLICs, a QSLAC-NP device provides a complete solution to the BORSCHT function of a POTS linecard.

Although the name and logo have changed, the data contained herein remains the same as the most recent AMD revision of this document.

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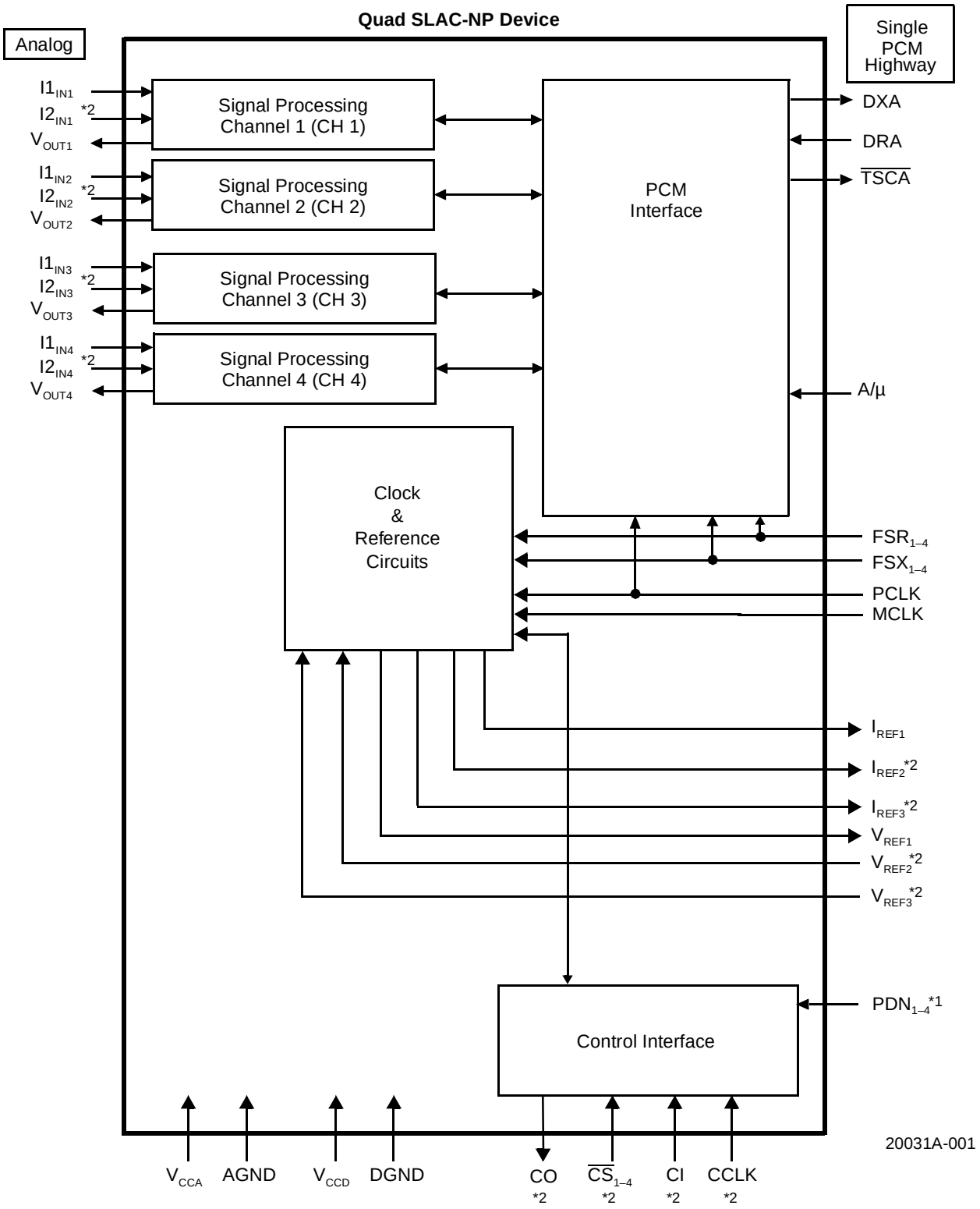
TABLE OF CONTENTS

List of Figures

List of Tables

BLOCK DIAGRAM



Notes:

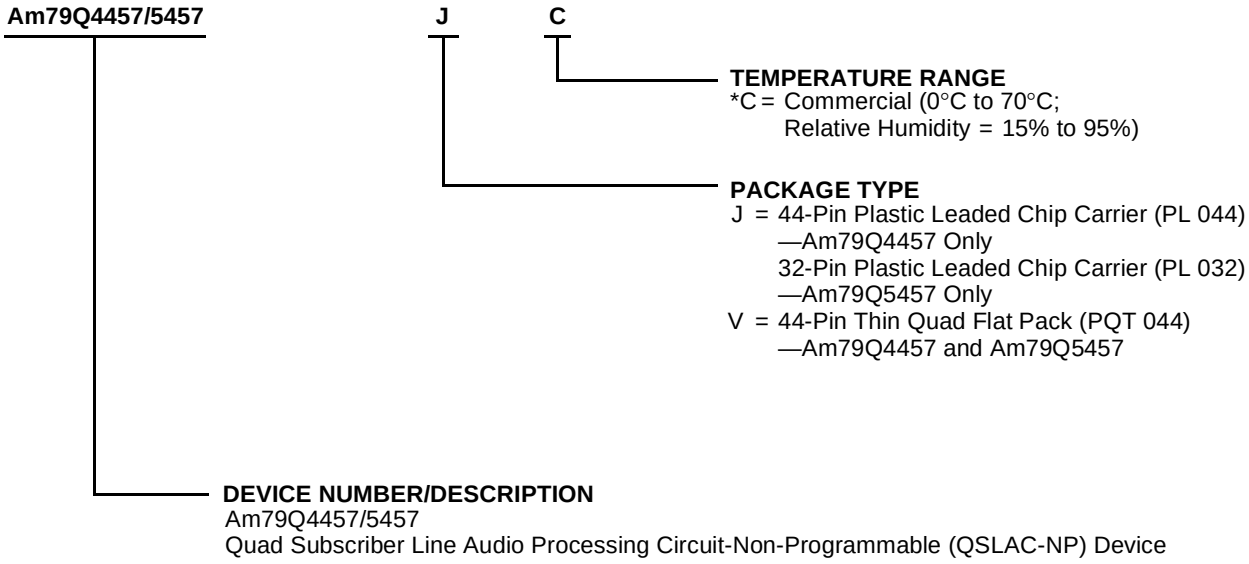
**1 = Am79Q5457 only.*

**2 = Am79Q4457 only.*

ORDERING INFORMATION

Standard Products

Legerity standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
Am79Q4457	JC
Am79Q5457	JC
Am79Q4457	VC
Am79Q5457	VC

Valid Combinations

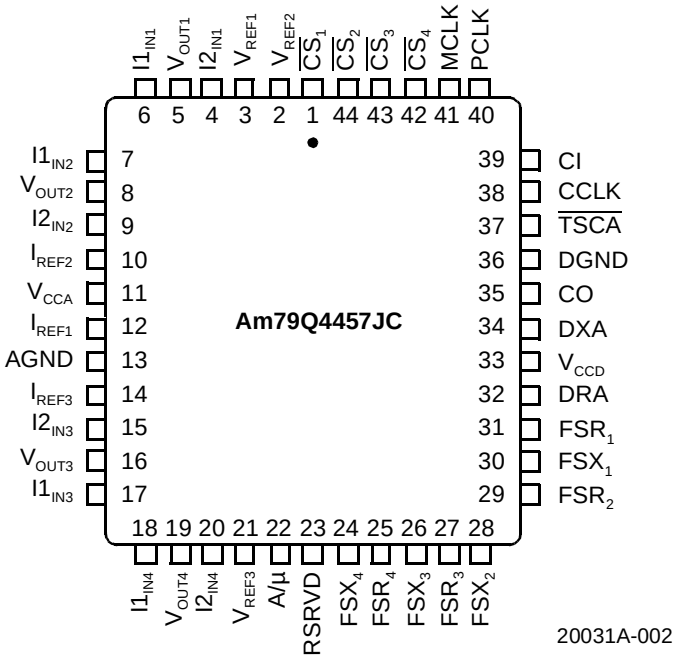
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Legerity sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on Legerity's standard military–grade products.

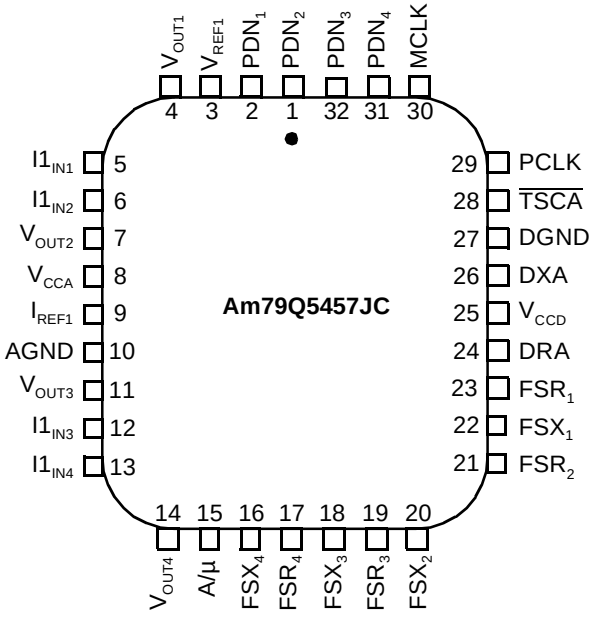
Note:

** The performance specifications contained in this data sheet for 0°C to +70°C operation are guaranteed by 100% factory testing at 65°C. Extended temperature range specifications (–40°C to +85°C) are guaranteed by characterization and periodic sampling of production units.*

CONNECTION DIAGRAMS (PLCC PACKAGES)

Top View



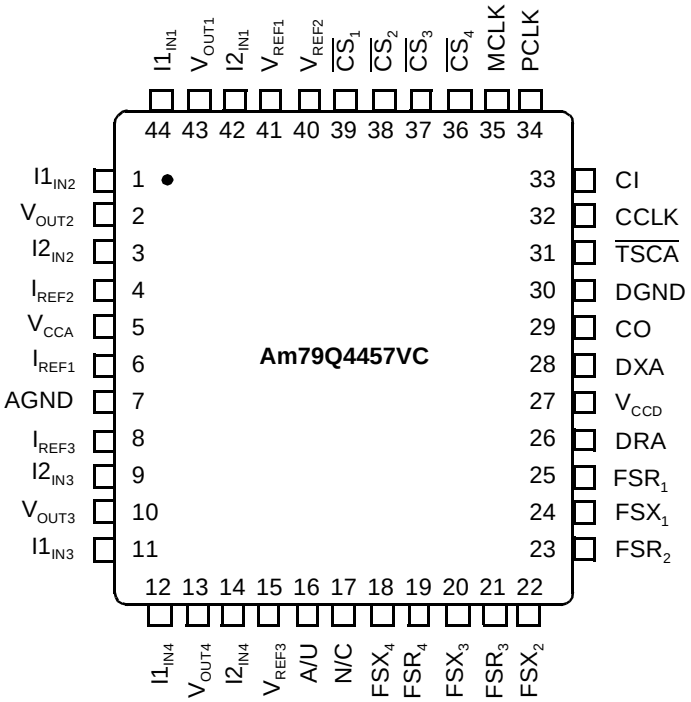


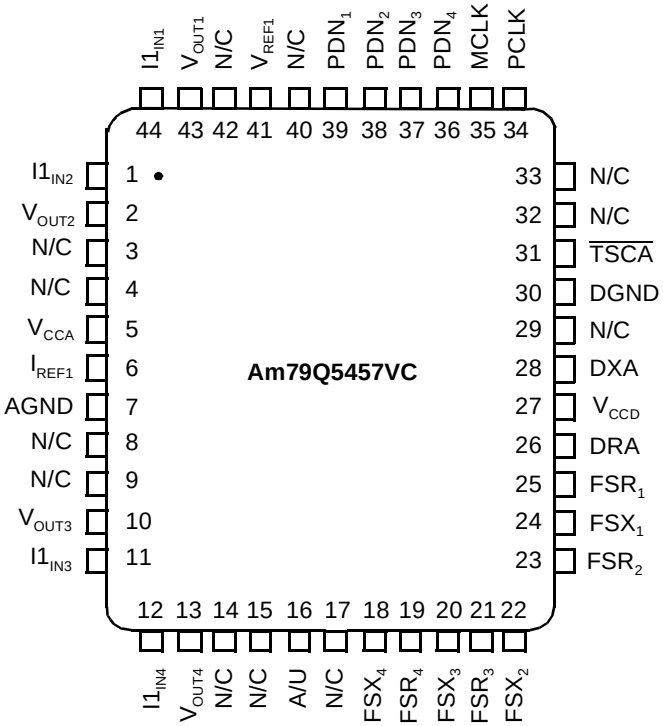
Note:

Pin 1 is marked for orientation.

CONNECTION DIAGRAMS (44-PIN TQFP PACKAGES)

Top View





Note:
Pin 1 is marked for orientation.

PIN DESCRIPTIONS

Pin Name	Type	Description
A/μ	Input	A-law or μ-law Select. The A-law/μ-law select pin is used to inform the QSLAC-NP device which compression/expansion standard to use. A logic Low signal (0 V) on the A-law/μ-law pin selects the μ-law standard, and a logic High (+5 V) selects the A-law standard. The A-law/μ-law input can be connected to V_{CCD} directly, eliminating the need for a external pull-up resistor. Therefore, the device can be programmed for A-law by connecting the A/μ input to V_{CCD} and can be programmed for μ-law by connecting the device pin to DGND.
CCLK	Input	(Am79Q4457 Device Only) Control Clock. The Control Clock input shifts data into and out of the Serial Interface of the QSLAC-NP device. The maximum clock rate is 4.096 MHz. (Serial control on the Am79Q4457 device only.)
CI	Input	(Am79Q4457 Device Only) Control Data. Control Data is written into the selected Channel Control Register (see $\overline{CS}_N$) via the CI pin. The data is shifted in the Most Significant Bit (MSB) first. The data rate is determined by CCLK. (Serial control on the Am79Q4457 device only.)
CO	Output	(Am79Q4457 Device Only) Control Data. Control Data is read in serial form from the Enabled Channel Register (see $\overline{CS}_N$) via the CO pin. Data is shifted out with the MSB first. The data rate is determined by the Control Clock (CCLK). (Serial control available on the Am79Q4457 device only.)
$\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$, $\overline{CS}_4$	Input	(Am79Q4457 Device Only) Chip Select. The Chip Select ($\overline{CS}_N$) input (active Low) enables Channel N of the device so that control data can be written to or read from the channel. $\overline{CS}_1$ enables Channel 1, $\overline{CS}_2$ enables Channel 2, $\overline{CS}_3$ enables Channel 3, and $\overline{CS}_4$ enables Channel 4. (Serial control on the Am79Q4457 device only.)
DRA	Input	PCM. The PCM data for Channels 1, 2, 3, and 4 is serially received on the DRA port during the time slot determined by the Receive Frame Sync Signal (FSR_N). Data is always received with the MSB first. A byte of data for each channel is received every 125 μs at the PCLK rate.
DXA	Output	PCM. The transmit data from Channels 1, 2, 3, and 4 is sent serially out the DXA port during time slots determined by the Transmit Frame Sync (FSX_N) signal for that channel. Data is always transmitted with the MSB first. The output is available every 125 μs and the data is shifted out in 8-bit bursts at the PCLK rate. DXA is high impedance between time slots.
FSR_1, FSR_2, FSR_3, FSR_4	Input	Receive Frame Sync. The Receive Frame Sync pulse for Channel N is an 8 kHz signal that identifies the receive time slot for Channel N on a system's receive PCM frame. The QSLAC-NP device references channel time slots with respect to this input, which must be synchronized to PCLK. There are both Long-Frame Sync and Short-Frame Sync modes available on the QSLAC-NP device.
FSX_1, FSX_2, FSX_3, FSX_4	Input	Transmit Frame Sync. The Transmit Frame Sync pulse for Channel N is an 8 kHz signal that identifies the transmit time slot for Channel N during the system's transmit PCM frame. The QSLAC-NP device references individual channel time slots with respect to this input, which must be synchronized to PCLK. There are both Long Frame Sync and Short Frame Sync modes available on the QSLAC-NP device.
$I1_{IN1}$, $I2_{IN1}$, $I1_{IN2}$, $I2_{IN2}$, $I1_{IN3}$, $I2_{IN3}$, $I1_{IN4}$, $I2_{IN4}$	Current	($I2_{IN}$ on Am79Q4457 Device Only) Analog Inputs. The analog voice band voltage signal is applied to the I_{IN} input of the QSLAC-NP device through a resistor. The I_{IN} input is a virtual AC ground input (summing node). I_{IN} is biased at the voltage on the V_{REF1} pin. The audio signal is sampled, digitally processed and encoded, and then made available at the TTL-compatible PCM output (DXA). There are two inputs per channel in the 44-pin QSLAC-NP device. $I1_{IN1}$ is input 1 of Channel 1 and $I2_{IN1}$ is input 2 of Channel 1; $I1_{IN2}$ and $I2_{IN2}$ are inputs 1 and 2 of Channel 2; $I1_{IN3}$ and $I2_{IN3}$ are inputs 1 and 2 of Channel 3; and $I1_{IN4}$ and $I2_{IN4}$ are inputs 1 and 2 of Channel 4. See Figure 9 for more details.
I_{REF1}, I_{REF2}, I_{REF3}	Output	(I_{REF2} and I_{REF3} on Am79Q4457 Device Only). Reference Current. The I_{REF} outputs are biased at the internal reference voltage, which is the same as the voltage on the V_{REF1} pin. A resistor placed from I_{REFn} (n = 1, 2, or 3) to ground sets one of three reference currents used by the Analog-to-Digital (A-to-D) converter to encode the signal current present on Iy_{INn} (n = channel number [1 to 4] and y = input number [1 or 2]) into digital form. By setting different levels for I_{REFx}, three different transmit gains can be achieved. The reference current used by a channel A-to-D is determined by the Transmit Gain Select (TGS) bits in the channel control register. The absolute transmit gain is determined by the reference current selected and the input resistance connected to I_{IN}. See Figure 9 and Table 2 for more details.

Pin Name	Type	Description
MCLK	Input	Master Clock. The Master Clock frequency can be 1.536 MHz, 1.544 MHz, 2.048 MHz, or 4.096 MHz for use by the digital signal processor. Using the Transmit Frame Sync (FSX) Inputs, the QSLAC-NP device determines the MCLK frequency and makes the necessary internal adjustments automatically. The master clock frequency must be an exact integer multiple of the frame sync frequency.
PCLK	Input	PCM Clock. The PCM clock determines the rate at which PCM data is serially shifted into or out of the PCM ports. PCLK is an integer multiple of the frame sync frequency. The maximum clock frequency is 4.096 MHz, and the minimum clock frequency is 256 kHz, due to a single PCM highway. PCLK frequencies between 1.03 MHz and 1.53 MHz are not allowed. The digital signal processor clock can be derived from PCLK by connecting MCLK and PCLK together. See frequency restrictions under MCLK.
PDN_1, PDN_2, PDN_3, PDN_4	Input	(Am79Q5457 Device Only) Power Down. The power-down inputs provide direct control over the channel circuitry. A logic High on PDN_n (n = 1 to 4) powers Channel n down while a logic Low powers the channel up. PDN_1 controls Channel 1, PDN_2 controls Channel 2, PDN_3 controls Channel 3, and PDN_4 controls Channel 4. The PDN pins are used in the initialization of the internal circuitry. Refer to the Power-Up Sequence section on 24 for initialization using the PDN pins.
$\overline{TSCA}$	Output	Time Slot Control. The Time Slot Control output is an open drain output (requiring a pull-up resistor to V_{CCD}) and is normally inactive (high impedance). $\overline{TSCA}$ is active (Low) when PCM data is transmitted on the DXA pin for any of the four channels.
V_{OUT1}, V_{OUT2}, V_{OUT3}, V_{OUT4}	Voltage	Analog Outputs. The received digital data at DRA is processed and converted to an analog signal at the V_{OUT} pin. V_{OUT1} is the output from Channel 1; V_{OUT2} is the output for Channel 2; V_{OUT3} is the output from Channel 3; and V_{OUT4} is the output for Channel 4. The V_{OUT} voltages are referenced to V_{REF1}.
V_{REF1}	Output	Voltage Reference. The V_{REF1} output is provided in order for an external 0.1-µF capacitor (or larger) to be connected from V_{REF1} to ground, filtering noise present on the internal voltage reference. V_{REF1} is buffered before it is used by internal circuitry. The voltage on V_{REF1} is nominally 2.1 V, and the output resistance is 115 kW. The leakage current in the capacitor must be less than 20 nA. A larger filter capacitor will provide better filtering, but will increase the settling time.
V_{REF2}, V_{REF3}	Input	(Am79Q4457 Device Only). Voltage Reference. V_{REF2} and V_{REF3} are buffered and are available as alternative reference voltages for the channel Digital-to-Analog (D-to-A) converters. The D-to-A converters decode the received PCM data into analog voltage levels. V_{REF1}, V_{REF2}, or V_{REF3} can be selected by the Receive Gain Select (RGS) bits as the reference for the D-to-A converter in order to select the receive gain of the channel.

Power Supply for the Am79Q4457/5457 Devices:

AGND Analog Ground
DGND Digital Ground
V_{CCA} +5.0 V Analog Power Supply
V_{CCD} +5.0 V Digital Power Supply

Two separate power supply inputs are provided to allow for noise isolation and good power supply decoupling techniques; however, the two pins have a low impedance connection inside the part. For best performance, all of the +5.0 power supply pins should be connected together at the connector of the printed circuit board, and all of the grounds should be connected together at the connector of the printed circuit board.

FUNCTIONAL DESCRIPTION

The QSLAC-NP device performs the Codec/Filter and two-to-four-wire conversion function (requires external balance impedance) required of the subscriber line interface circuitry in telecommunications equipment. These functions involve converting an audio signal into digital PCM samples and converting digital PCM samples back into an audio signal. During conversion, digital filters are used to band limit the voice signals. All of the digital filtering is performed in digital signal processors operating from an internal clock, which is derived from MCLK. The fixed filters set the transmit and receive gain and frequency response.

The transmit and receive gain can be altered on a per-channel basis and the per-channel balance impedance can be selected between two external impedances by the Am79Q4457 QSLAC-NP device. Control of these functions is provided by an integrated serial shift register and latch per channel. These additional functions are available on the Am79Q4457 device only.

Data transmitted or received on the PCM highway is an 8-bit, A-law or μ-law companded code. The QSLAC-NP device is compatible with both codes. Code selection is provided via a device pin (A/μ). The 8-bit codes appear 1 byte per time slot. The PCM data is read and written to the PCM highway in time slots determined by the individual Frame Sync signals (FSR_N and FSX_N) at rates from 256 kHz to 4.096 MHz. Both Long- and Short-Frame Sync modes are available in the QSLAC-NP device.

Two configurations of the QSLAC-NP device are offered as pictured previously. The Am79Q4457 device with serial control of gain and balance impedance is available in the 44-pin PLCC package and 44-pin TQFP package. The Am79Q5457 device without serial control is available in a 32-pin PLCC package and 44-pin TQFP package.

Serial Control	Package	Part Number
Yes	44 PLCC	Am79Q4457 JC
No	32 PLCC	Am79Q5457 JC
Yes	44 TQFP	Am79Q4457 VC
No	44 TQFP	Am79Q5457 VC

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –60°C < T_A < +125°C

Ambient Operating Temp . . . . . –40°C < T_A < +85°C

Ambient Relative Humidity . . . . . 5% to 95% (non condensing)

V_{CCA} with respect to V_{CCD} . . . . . ±50 mV

V_{CCA} with respect to AGND. . . . . –0.4 V to +7.0 V

V_{CCD} with respect to DGND . . . . . –0.4 V to +7.0 V

AGND with respect to DGND . . . . . ±0.4 V

I_{IN} Current . . . . . ±10 mA

Other pins
with respect to DGND . . . . . –0.4 V to V_{CCD} +0.4 V

Latch-up immunity (any pin). . . . . ±30 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

V_{CCA}, Analog Supply . . . . . V_{CCD} ±10 mV

V_{CCA}, Analog Supply . . . . . +5.0 V ± 0.25 V

V_{CCD}, Digital Supply . . . . . +5.0 V ± 0.25 V

DGND . . . . . .0 V

AGND . . . . . ±50 mV

Ambient Temperature . . . . . .0°C < T_A < +70°C

Ambient Relative Humidity . . . . . .15% to 95%

Operating Ranges define those limits between which functionality of the device is guaranteed by 100% production testing.

Specifications in this data sheet are guaranteed by testing from 0°C to +70°C. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.

ELECTRICAL CHARACTERISTICS over operating ranges (unless otherwise noted)

Typical values are for T_A = 25°C and nominal supply voltages. Minimum and maximum specifications are over the temperature and supply voltage ranges shown in Operating Ranges.

Symbol	Parameter Descriptions	Min	Typ	Max	Unit
V_{IL}	Input Low voltage			0.8	V
V_{IH}	Input High voltage	2.0			V
I_{IL}	Input leakage current	–10		10	µA
V_{OL}	Output Low voltage $\overline{TSCA}$ (I_{OL} =14 mA) All other digital outputs (I_{OL} = 2 mA)			 0.4 0.4	 V V
V_{OH}	Output High voltage All digital outputs (I_{OH} = 400 µA)	 2.4			 V
I_{OL}	Output leakage current (H_I = Z State)	–10		10	µA
I_{IR}	Analog input current range, R_{REF} = 13 kΩ		±40		µA
I_{IOS}	Offset current allowed on I_{IN}	–1.6		1.6	µA
V_{IOS}	Offset voltage on I_{IN} relative to V_{REF1}	–16		16	mV
Z_{OUT}	V_{OUT} output impedance		1	4	Ω
Z_{REF1}	V_{REF1} output impedance (F < 3400 Hz)	80		150	kΩ
I_{OUT}	V_{OUT} output current (F<3400 Hz) (Note 1)	–4		4	mA
V_{OR}	V_{OUT} voltage range		±1.584		V
V_{OOS}	V_{OUT} offset voltage (Relative to V_{REF1})	–40		40	mV
PD	Power dissipation All channels active 1 channel active All channels inactive (Note 2)		180 60 1	240 90 6	mW mW mW
C_I	Input capacitance (Digital)		15		pF
C_O	Output capacitance (Digital)		15		pF
PSRR	Power supply rejection ratio (1.02 kHz, 100 mVrms, either path, GX = GR = 0 dB)	40			dB

Notes:

1. *When the QSLAC-NP device is in the Inactive mode, the analog output (V_{OUT}) will present a V_{REF1} DC output level through a ~400-kΩ resistor.*
2. *Power dissipation in the Inactive mode is measured with all digital inputs at V_{IH} = V_{CC} and V_{IL} = DGND, and with no load connected to V_{OUT1}, V_{OUT2}, V_{OUT3}, or V_{OUT4}.*

Transmission Characteristics

Table 1. 0 dBm0 Voltage Definitions

Signal at Digital Interface	Transmit	Receive	Unit	Note
A-law digital mW or equivalent (0 dBm0)	0.6776/Gt	0.6776 x Gr	Vrms	1
µ-law digital mW or equivalent (0 dBm0)	0.6778/Gt	0.6778 x Gr	Vrms	1

Description	Test Conditions	Min	Typ	Max	Unit	Note
Gain accuracy, either path	0 dBm0, 1014 Hz 0°C to 85°C Am79Q5457, or Am79Q4457, Gt = Gt1, Gr = Gr1	–0.25		+0.25	dB	
	–40°C (All), or Am79Q4457, Gt = Gt2 or Gt = Gt3, or Gr = Gr2 or Gr = Gr3	–0.35		+0.35	dB	
Attenuation distortion	300 Hz to 3 kHz	–0.125		+0.125	dB	2
Single frequency distortion				–46	dB	3
Idle channel noise — Analog out	unweighted			–55	dBm0	4
Analog out	digital input = 0, A-law			–78	dBm0p	4
Analog out	digital input = 0, µ-law			12	dBrnc0	4
Digital out	analog V_{IN} = 0, A-law			–68	dBm0p	4
Digital out	analog V_{IN} = 0, µ-law			16	dBrnc0	4
Crosstalk between channels	0 dBm0					
TX or RX to TX	1014 Hz			–76	dBm0	
	Average			–76	dBm0	5
TX or RX to RX	1014 Hz			–78	dBm0	
	Average			–78	dBm0	5
End-to-end group delay	PCLK ≥ 1.53 MHz		500	540	µs	6, 7
Analog-to-analog overload compression loss relative to 0 dBm0 loss	3 dBm0, 1004 Hz input, C-weight			0.5	dB	
	6 dBm0, 1004 Hz input, C-weight			2	dB	
	9 dBm0, 1004 Hz input, C-weight			5	dB	

Notes:

1. *Gt and Gr are defined in the Transmit Gain Select and Receive Gain Select tables on 28 and 29. Gr must be in the range: 0.4 ≤ Gr ≤ 1. R_{REF} must be in the range: 13K ≤ R_{REF} ≤ 26K, where R_{REF} is R_{REF1}, R_{REF2A} + R_{REF2B}, or R_{REF3A} + R_{REF3B}.*
2. *Also see the following Attenuation Distortion figure.*
3. *Measured with a 0 dBm0 input signal, 300 Hz to 3400 Hz; output measured at any other frequency 300 Hz to 3400 Hz.*
4. *No single frequency component in the range above 3800 Hz may exceed a level of –55 dBm0.*
5. *The weighted average of the crosstalk is defined by the following equation, where C(f) is the crosstalk in dB as a function of frequency, f_N = 3300 Hz, f_1 = 300 Hz, and the frequency points (f_j, j = 2..N) are closely spaced:*

$$\text{Average} = 20 \bullet \log \left[\frac{\sum_{j} \frac{10^{\frac{1}{20} \bullet C(f_j)} + 10^{\frac{1}{20} \bullet C(f_{j-1})}}{2} \bullet \log \left(\frac{f_j}{f_{j-1}} \right)}{\log \left(\frac{f_N}{f_1} \right)} \right]$$

6. *See following Group Delay Distortion figure also.*
7. *The End-to-End Group Delay is the sum of the transmit and receive group delays where both are measured using the same time slot.*

Attenuation Distortion

If a capacitive coupling network is used in series with either the transmit input or the receive output of the part, that network must have a corner frequency of less than 20 Hz to meet the template in Figure 1. If the corner frequency is above 20 Hz, the loss in the coupling network must be taken into account.

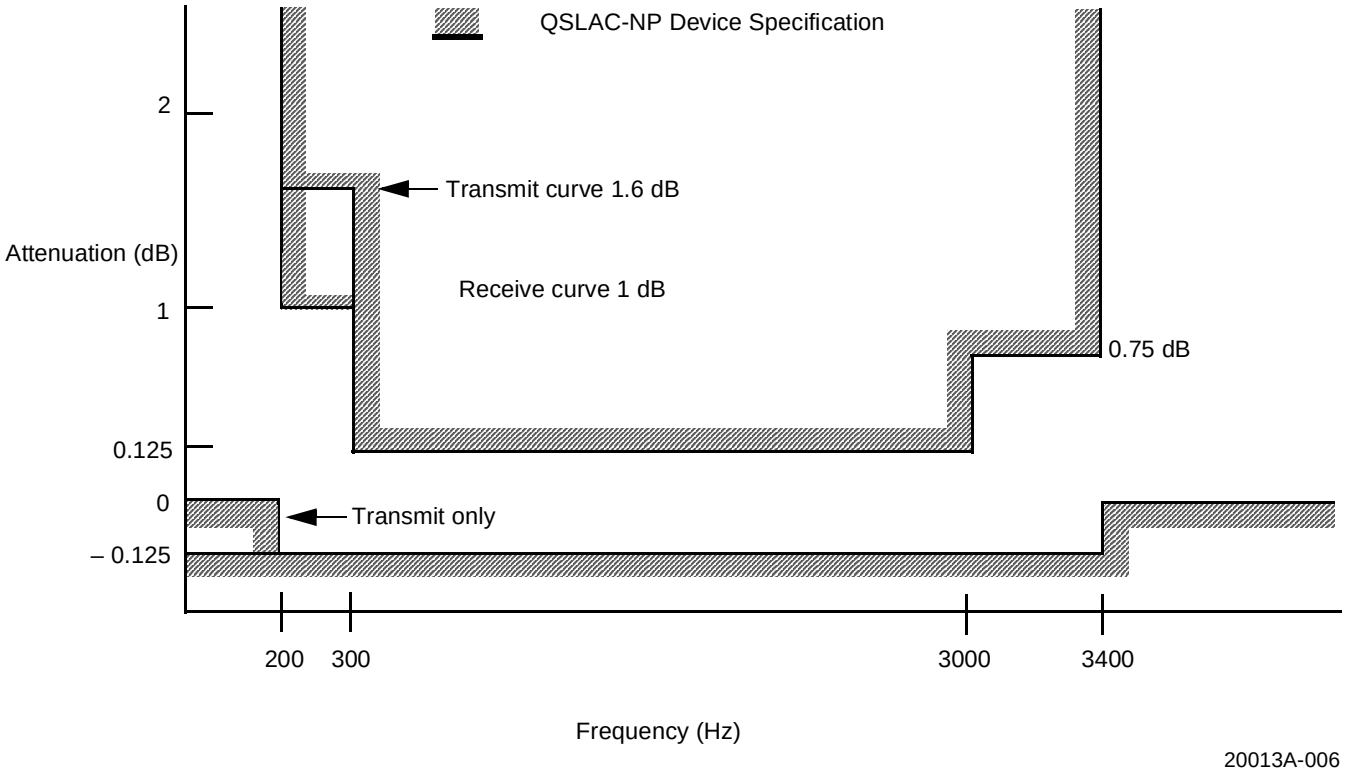


Figure 1. Attenuation Distortion

Group Delay Distortion

For either transmission path, the group delay distortion is within the limits shown in Figure 2. The minimum value of the group delay is taken as the reference. The signal level should be 0 dBm0.

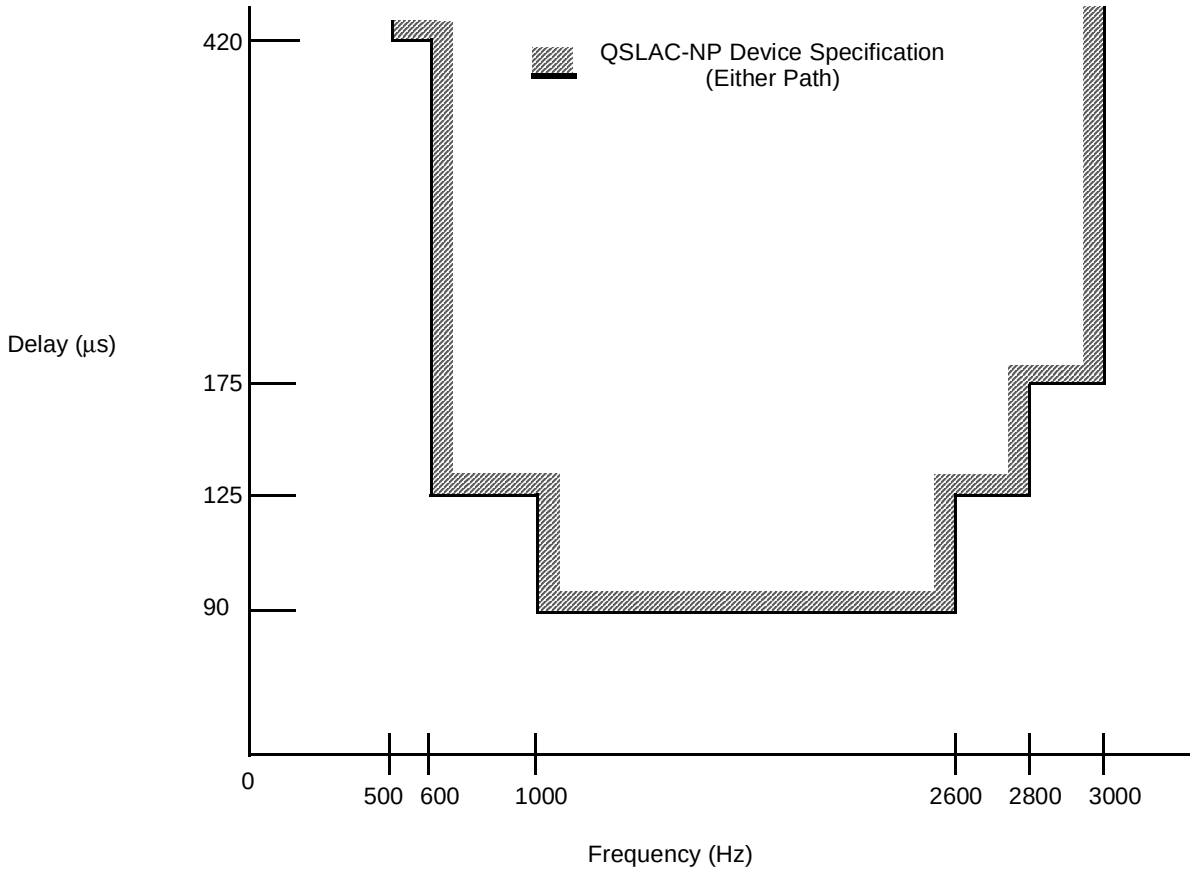


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Figure 2. Group Delay Distortion

Variation of Gain with Input Level

The gain deviation relative to the gain at –10 dBm0 is within the limits shown in Figure 3 for either transmission path when the input is a sine wave signal of frequency 1014 Hz.

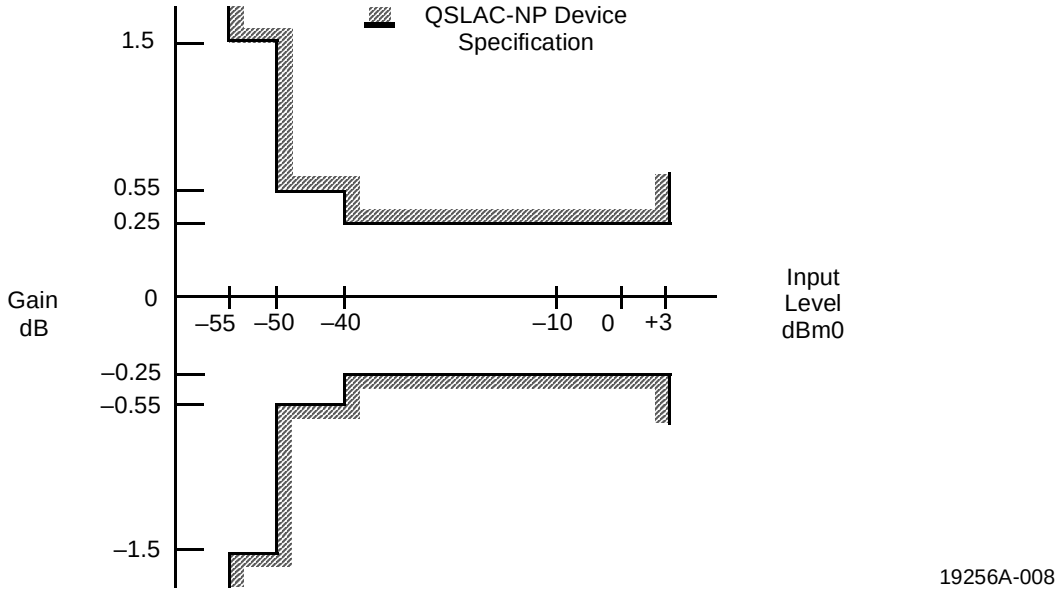


Figure 3a. A-law Gain Tracking with Tone Input (Both Paths)

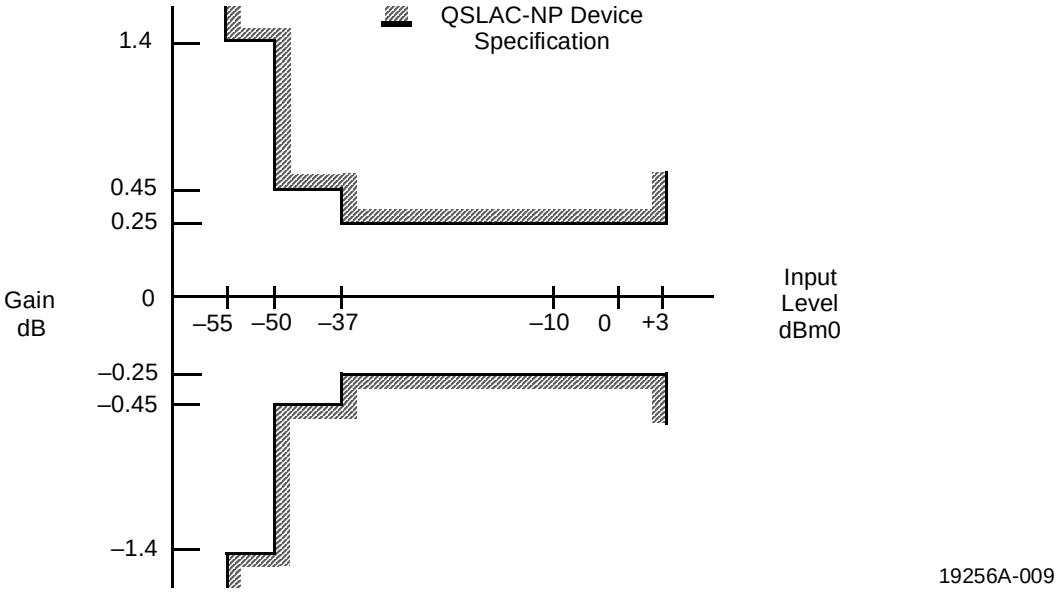


Figure 3b. μ-law Gain Tracking with Tone Input (Both Paths)

Total Distortion, Including Quantizing Distortion

The signal-to-total distortion will exceed the limits shown in Figure 4 for either transmission path when the input is a sine wave signal of frequency 1014 Hz.

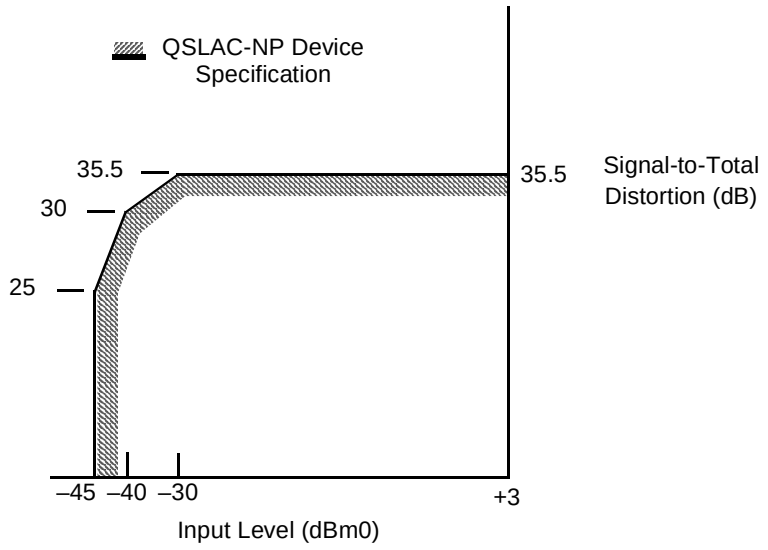


Figure 4a. A-law Total Distortion with Tone Input (Both Paths)

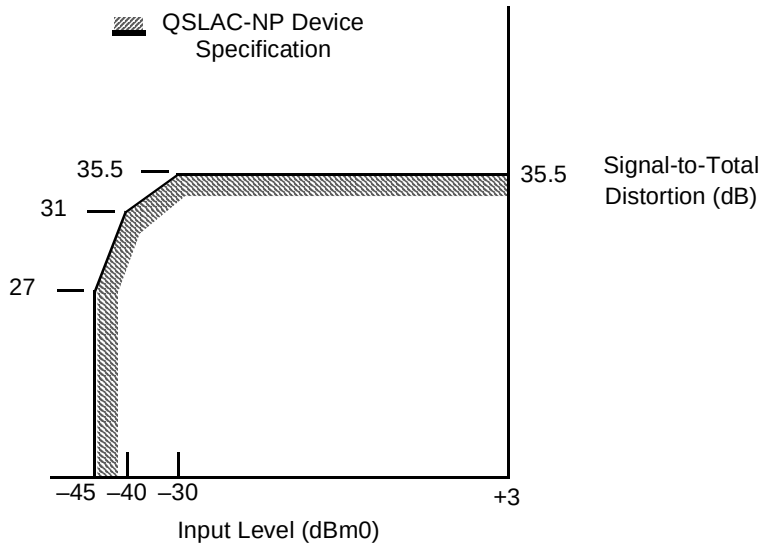
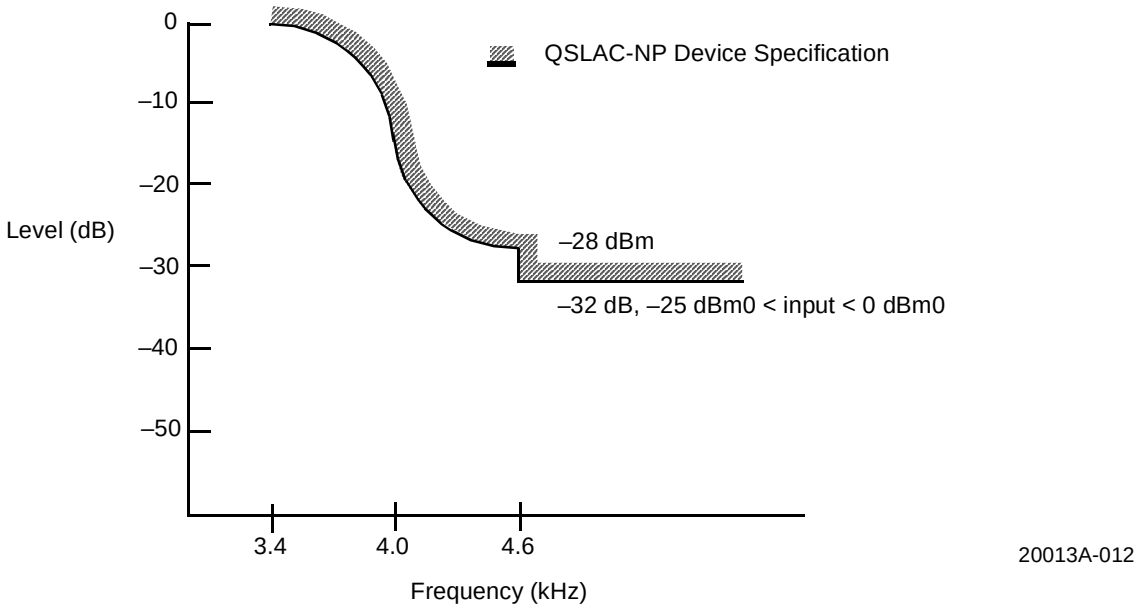


Figure 4b. μ-law Total Distortion with Tone Input (Both Paths)

Discrimination against Out-of-Band Input Signals

When an out-of-band sine wave signal with frequency and level A is applied to the analog input, there may be frequency components below 4 kHz at the digital output caused by the out-of-band signal. These components are at least the specified dB level below the level of a signal at the same output originating from a 1014-Hz sine wave signal with a level of A dBm0 also applied to the analog input. The minimum specifications are shown in Figure 5.

Frequency of Out-of-Band Signal	Amplitude of Out-of-Band Signal	Level below A
16.6 Hz < f < 45 Hz	–25 dBm0 < A ≤ 0 dBm0	18 dB
45 Hz < f < 65 Hz	–25 dBm0 < A ≤ 0 dBm0	25 dB
65 Hz < f < 100 Hz	–25 dBm0 < A ≤ 0 dBm0	10 dB
3400 Hz < f < 4600 Hz	–25 dBm0 < A ≤ 0 dBm0	see Figure 5
4600 Hz < f < 100 kHz	–25 dBm0 < A ≤ 0 dBm0	32 dB



Note:

The attenuation of the waveform below amplitude A between 3400 Hz and 4600 Hz is given by the formula:

$$\text{Attenuation (db)} = 14 - 14\sin\frac{\pi(4000 - f)}{1200}$$

Figure 5. Discrimination against Out-of-Band Signals

Discrimination against 12 kHz and 16 kHz Metering Signals

If the QSLAC-NP device is used in a metering application where 12 kHz or 16 kHz tone bursts are injected onto the telephone line toward the subscriber, a portion of those tones may also appear at the I_{IN} terminal. These out-of-band signals may cause frequency components to appear below 4 kHz at the digital output. For a 12 kHz or 16 kHz tone, the frequency components below 4 kHz will be reduced from the input by at least 70 dB. The sum of the peak metering and signal currents must be within the analog input current range.

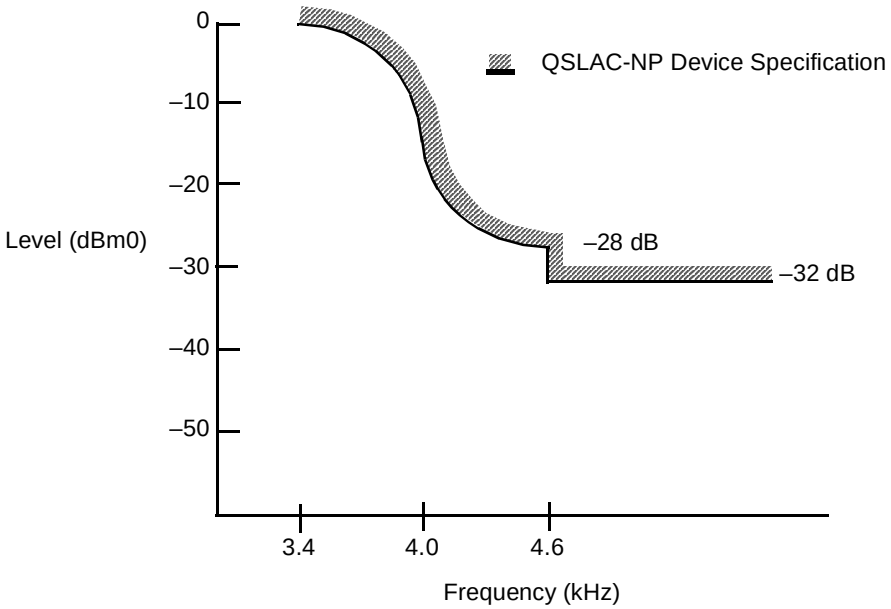
Spurious Out-of-Band Signals at the Analog Output

With PCM code words representing a sine wave signal in the range of 300 Hz to 3400 Hz at a level of 0 dBm0 applied to the digital input, the level of the spurious out-of-band signals at the analog output is less than the limits shown in the following table.

Frequency	Level
4.6 kHz to 40 kHz	–32 dBm0
40 kHz to 240 kHz	–46 dBm0
240 kHz to 1 MHz	–36 dBm0

With code words representing any sine wave signal in the range 3.4 kHz to 4.0 kHz at a level of 0 dBm0 applied to the digital input, the level of the signals at the analog output are below the limits in Figure 6. The amplitude of the spurious out-of-band signals between 3400 Hz and 4600 Hz is given by the formula:

$$A = -14 - 14\sin\frac{\pi(f-4000)}{1200}\ \text{dBm0}$$



19256A-013

Figure 6. Spurious Out-of-Band Signals

SWITCHING CHARACTERISTICS over operating ranges (unless otherwise noted)

Min and Max values are valid for all digital outputs with a 150 pF load.

Control Interface

No.	Symbol	Parameter	Min	Typ	Max	Units
1	t_{CCY}	Control Clock Period	244			ns
2	t_{CCH}	Control Clock High Pulse Width	97			ns
3	t_{CCL}	Control Clock Low Pulse Width	97			ns
4	t_{CCR}	Rise Time of Clock			25	ns
5	t_{CCF}	Fall Time of Clock			25	ns
6	t_{ICSS}	Chip Select Setup Time, Input Mode	70		t_{CCY} –10	ns
7	t_{ICSH}	Chip Select Hold Time, Input Mode	0		t_{CCH} –20	ns
8	t_{ICSL}	Chip Select Pulse Width, Input Mode		$8t_{CCY}$		ns
9	t_{ICSO}	Chip Select Off Time, Input Mode	2			µs
10	t_{IDS}	Input Data Setup Time	30			ns
11	t_{IDH}	Input Data Hold Time	30			ns
12	t_{OLH}	Output Latch Valid (Internal)			100	ns
13	t_{OCSS}	Chip Select Setup Time, Output Mode	70		t_{CCY} –10	ns
14	t_{OCSH}	Chip Select Hold Time, Output Mode	0		t_{CCH} –20	ns
15	t_{OCSL}	Chip Select Pulse Width, Output Mode		$8t_{CCY}$		ns
16	t_{OCSO}	Chip Select Off Time, Output Mode	1			µs
17	t_{ODD}	Output Data Turn On Delay			50	ns
18	t_{ODH}	Output Data Hold Time	0			ns
19	t_{ODOF}	Output Data Turn Off Delay			50	ns
20	t_{ODC}	Output Data Valid	0		50	ns

PCM Interface

PCLK not to exceed 4.096 MHz.

Pull-up resistor of 360 Ω is attached to $\overline{\text{TSCA}}$.

No.	Symbol	Parameter	Min	Typ	Max	Units
21	t_{PCY}	PCM Clock Period (Note 1)	244			ns
22	t_{PCH}	PCM Clock High Pulse Width	97			ns
23	t_{PCL}	PCM Clock Low Pulse Width	97			ns
24	t_{PCF}	Fall Time of Clock			25	ns
25	t_{PCR}	Rise Time of Clock			25	ns
26	t_{FSS}	FS Setup Time	55		t_{PCY}–50	ns
27	t_{FSH}	FS Hold Time	50			ns
28	t_{FSJ}	FS or PCLK Jitter Time	–68		+68	ns
29	t_{TSD}	Delay to $\overline{\text{TSCA}}$ Valid (Short Frame Sync Mode)	5		80	ns
30	t_{TSO}	Delay to $\overline{\text{TSCA}}$ Off (Note 2)	50		220 t_{PCL}+70	ns
31	t_{DXD}	PCM Data Output Delay (Short Frame Sync Mode)	5		70	ns
32	t_{DXH}	PCM Data Output Hold Time	5		70	ns
33	t_{DXZ}	PCM Data Output Delay to High-Z (Note 3)	50		220 t_{PCL}+70	ns
34	t_{DRS}	PCM Data Input Setup Time	25			ns
35	t_{DRH}	PCM Data Input Hold Time	5			ns
36	t_{TSD}	Delay to $\overline{\text{TSCA}}$ Valid (Long Frame Sync Mode)	5		40	ns
37	t_{DXD}	PCM Data Output Delay (Long Frame Sync Mode)	5		40	ns

Master Clock

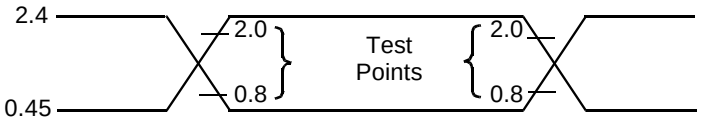
No.	Symbol	Parameter	Min	Typ	Max	Units
38	A_{MCY}	Master Clock Accuracy	–100		+100	ppM
39	t_{MCR}	Rise Time of Clock			15	ns
40	t_{MCF}	Fall Time of Clock			15	ns
41	t_{MCH}	MCLK High Pulse Width	97			ns
42	t_{MCL}	MCLK Low Pulse Width	97			ns

Notes:

1. *The PCM clock frequency must be an integer multiple of the frame sync frequency. The maximum allowable PCM clock frequency is 4.096 MHz. The actual PCM clock rate is dependent on the number of channels allocated within a frame. The minimum clock frequency is 256 kHz.*
2. *t_{TSO} is defined as the time at which the output achieves the open circuit condition.*
3. *There is a special conflict detection circuitry that will prevent high-power dissipation from occurring when the DX pins of two QSLAC-NP devices are tied together and one QSLAC-NP device starts to transmit before the other has gone into a high-impedance state.*

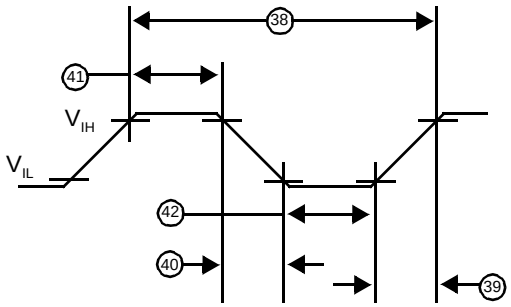
SWITCHING WAVEFORMS

Input and Output Waveforms for AC Tests



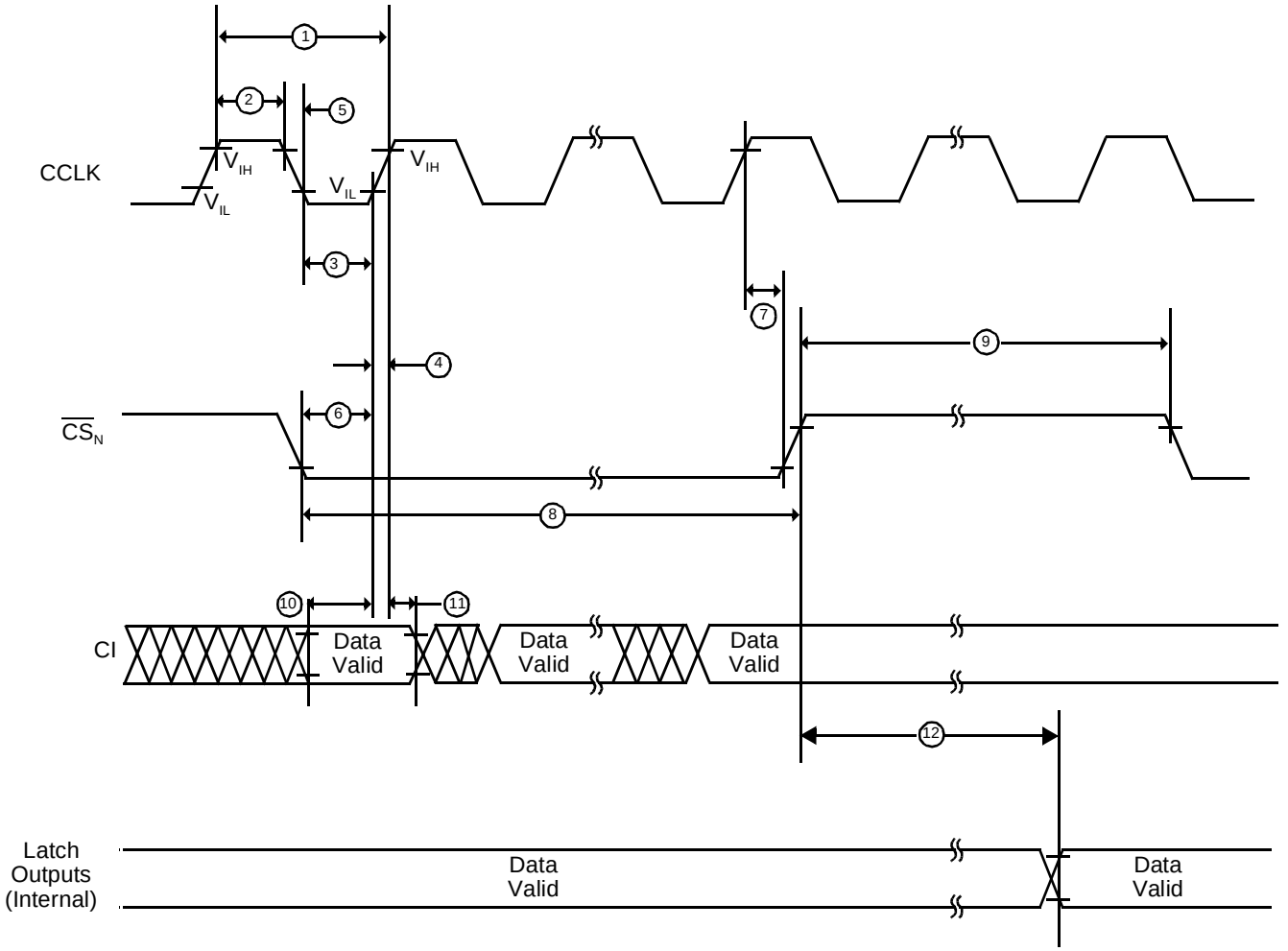
19256A-015

Master Clock Timing



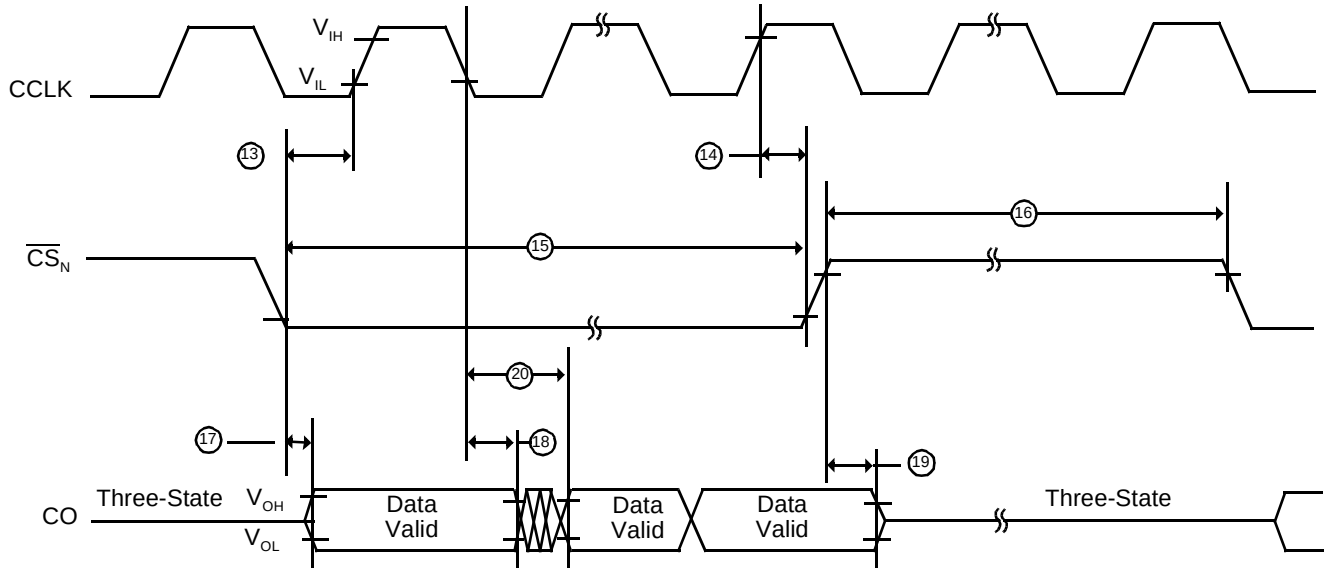
20031A-005

Control Interface (Input Mode)



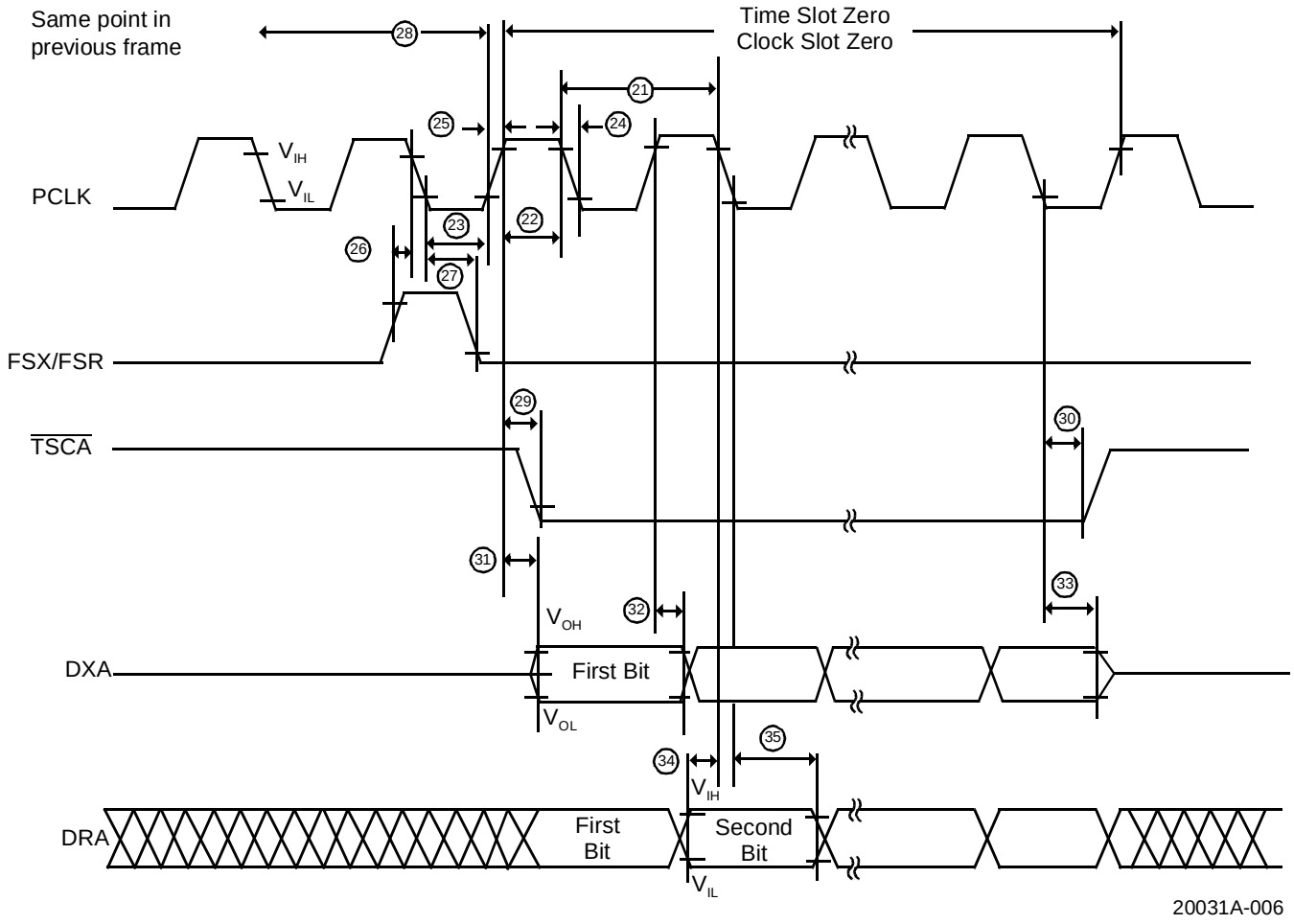
20013A-017

Control Interface (Output Mode)

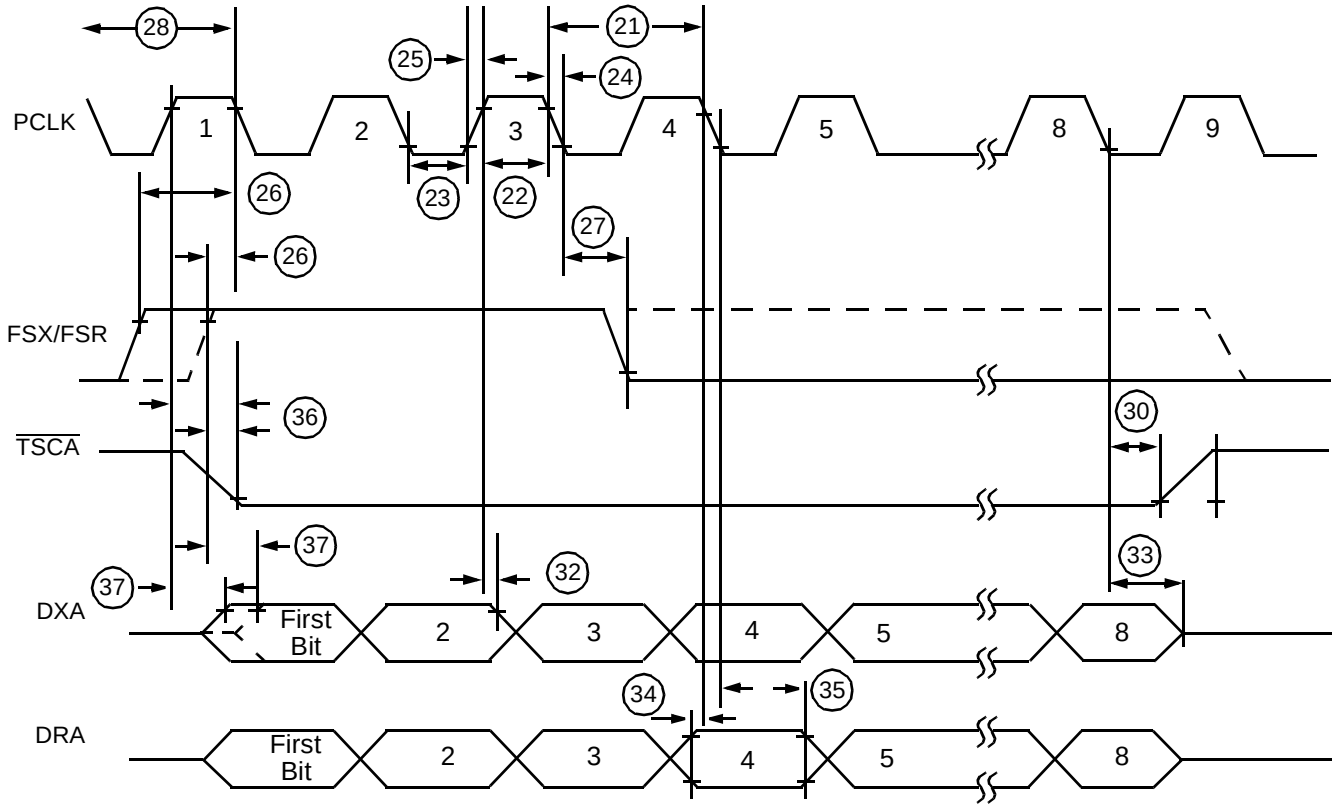


20013A-018

PCM Highway Timing (Short Frame Sync Mode)



PCM Highway Timing (Long Frame Sync Mode)



20031A-007

OPERATING THE QSLAC-NP DEVICES

The following describes the operation of the four independent channels of the QSLAC-NP device. The description is valid for Channel 1, 2, 3, or 4; consequently, the channel subscripts have been dropped. For example, VOUT refers to either VOUT1, VOUT2, VOUT3, or VOUT4. Also, the additional features provided by the Am79Q4457 device (over the Am79Q5457 device) are described.

Power-Up Sequence

The signal pins have protection diodes to V_{CC} and ground; consequently, if the signal leads are connected before V_{CC} or ground, the transient signal current must be limited in order to prevent latch-up of the part. Following initial power application, it is necessary to place all channels in an inactive state. This ensures a hardware reset is initiated upon activation of any channel. For these reasons, the following power-up sequence is recommended:

1. V_{CC} and ground
2. Signal connections
3. In the case of device Am79Q5457, take pins PDN1, PDN2, PDN3, and PDN4 to a logic high state, (device Am79Q4457 will default to all channels powered down).

Following any subsequent occurrence of all channels inactivated, upon activation of any channel, a hardware reset will be initiated.

Master Clock

The master clock, MCLK, is used to derive internal clocks and timing signals. The master clock must be essentially jitter free and it must be an integer multiple of the frame sync frequency. The allowed frequencies for MCLK are 1.536 MHz, 1.544 MHz, 2.048 MHz, and 4.096 MHz. Internal circuitry determines the MCLK frequency based on the FSX inputs and adjusts the internal timing circuitry automatically.

CONTROL OF THE Am79Q4457/5457 QSLAC-NP DEVICES

The QSLAC-NP device is controlled either directly via device pins (PDN and A/µ for the Am79Q5457 device) or through the serial control interface (Am79Q4457 device).

Parallel Control (Am79Q5457 Device)

The Am79Q5457 QSLAC-NP device is controlled directly via device pins. There are two different control input pins on the Am79Q5457 device, an A-law/µ-law select (A/µ) pin and four power-down (PDN) pins, one per channel. Logic levels on these pins determine the operating state of the individual channels, active (power-up) or idle (power-down), and A-law or µ-law operation.

Each channel of the QSLAC-NP device can operate in either the Powered-Up (Active) or Powered-Down (Standby) mode. In the Active mode, individual channels of the QSLAC™ device are able to transmit and receive PCM and analog information. The Active mode is required when a telephone call is in progress. The Standby mode requires the least amount of power per channel and should be used whenever the line circuit is on hook and a telephone call is not in progress.

Power Down Input (PDN_n):

0 — Powers the channel up

1 — Powers the channel down

A-Law/µ-Law Select Input (A/µ):

0 — Selects µ-law operation

1 — Selects A-law operation

Serial Control Register (Am79Q4457 Device Only)

The Am79Q4457 device provides an A-law/µ-law select pin in the same manner as the Am79Q5457 device. The Am79Q4457 QSLAC-NP device provides several additional features over the Am79Q5457 device. The Am79Q4457 device provides the ability to program three different gain levels on both the transmit and receive side of each channel. One of two balance impedances (connected externally) can be selected on a per-channel basis with the Am79Q4457 device. The individual channels of the Am79Q4457 device can be powered down. Control of the power-down function is through the per-channel serial control register.

Each channel of the Am79Q4457 QSLAC-NP device contains a serial shift register and latch in order to easily control the additional functionality of the device. The registers are connected as shown in Figure 7. The channel control registers are enabled for reading or writing by their corresponding Chip Select ($\overline{CS}_n$) signal. Data on the Control Input (CI) is shifted into the enabled register by the Control Clock (CCLK). Each channel register contains a Balance Network Select (BNS1) bit, two Receive Gain Select (RGS1/2) bits, two Transmit Gain Select (TGS1/2) bits and a Power-Down (PDN) bit. As indicated in Figure 7, the PDN bit is the most significant bit in the register and is shifted in first. The balance network select bit is the least significant bit and is shifted in last.

The Balance Network is selected with the BNS1 bit, where:

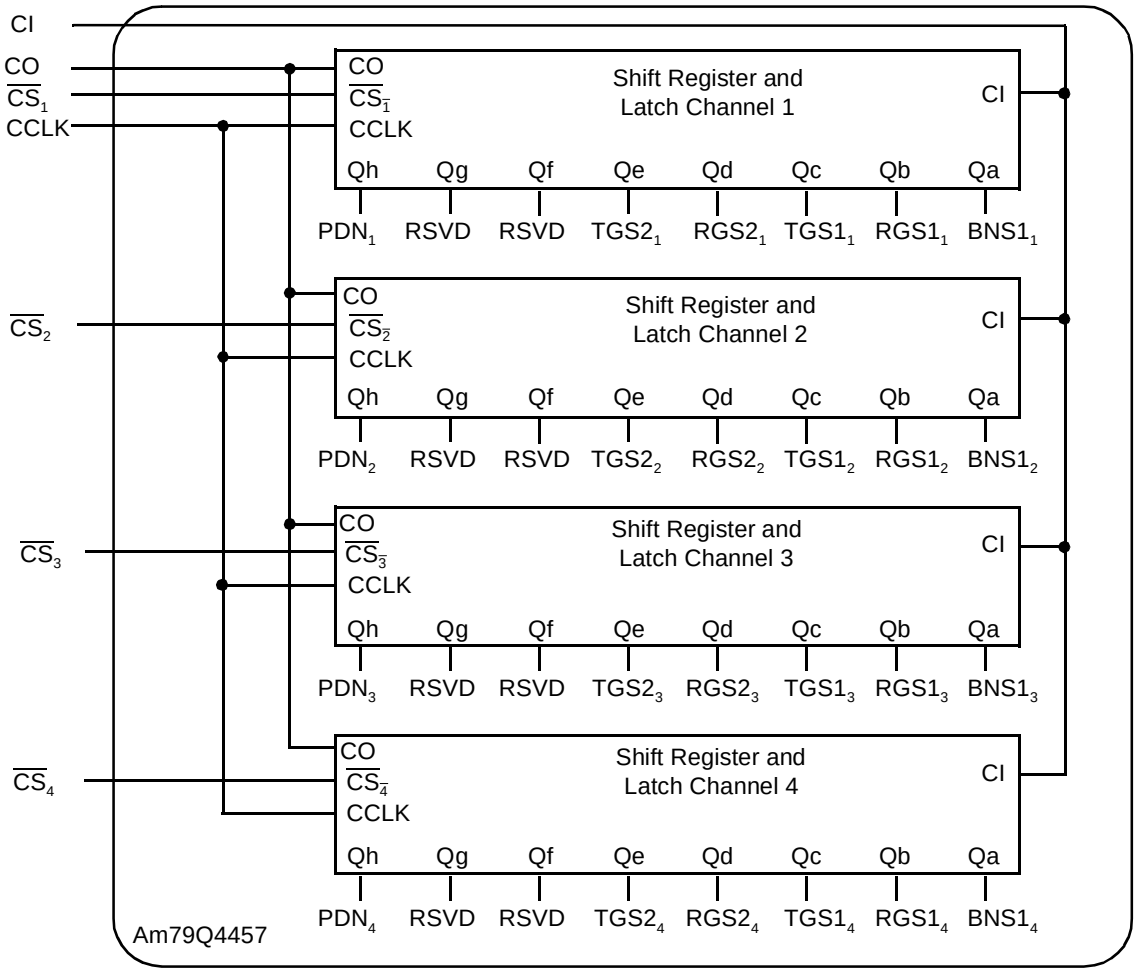
0 —Selects the balance network connected to $I1_{IN}$ of the channel.

1 —Selects the balance network connected to $I2_{IN}$ of the channel.

Transmit and Receive gains are selected according to the TGS1/2 and RGS1/2 bits as shown in the gain select tables, Table 2 and Table 3. The register layout for each channel is as follows:

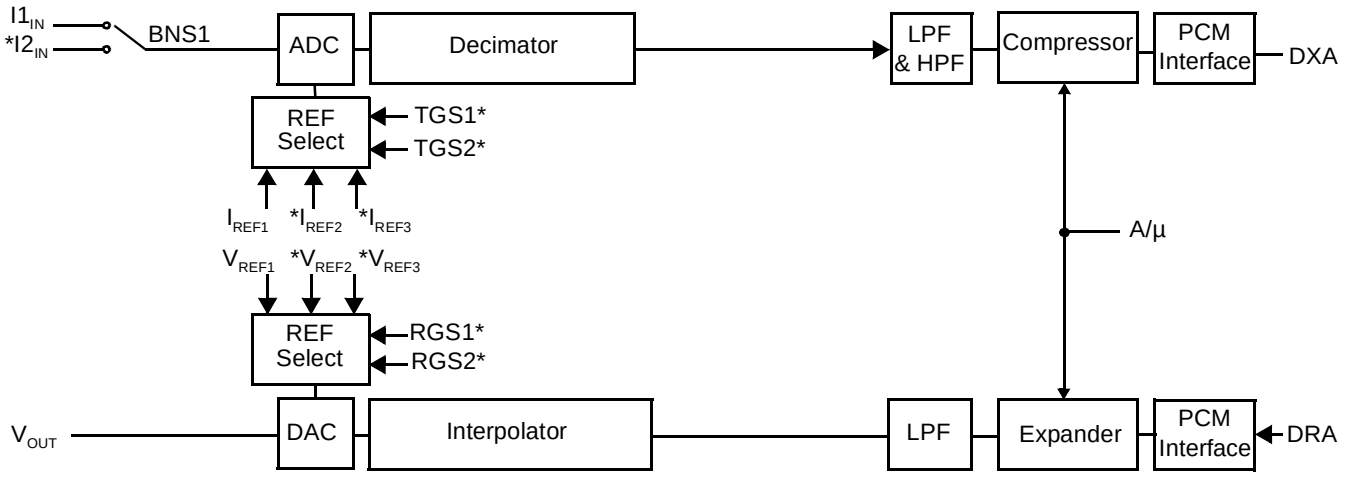
PDN	RSVD	RSVD	TGS2	RGS2	TGS1	RGS1	BNS1

Note:
PDN is loaded first.



20031A–008

Figure 7. Am79Q4457 QSLAC-NP Device Serial Control Interface



20031A-009

*Am79Q4457 device only

Figure 8. QSLAC-NP Device Block Diagram

Power Down (PDN_n):

0 — Powers the channel up

1 — Powers the channel down

Reset State

All four channel control registers are reset by the application of power. This resets the QSLAC-NP device to the following state: TGS, RGS, BNS = 0 and PDN = 1 for all four channels.

Signal Processing

Overview of Digital Filters

Several elements in the signal processing section of the Am79Q4457 device provide user options. These options allow the user to optimize the performance of the QSLAC-NP device for the application. Figure 8 shows the QSLAC-NP device signal processing section and indicates the user-programmable blocks, the reference current selector, the reference voltage selector, the balance network selector, and the A-law/µ-law selector. The High-Pass Filter (HPF) and the Low-Pass Filter (LPF) sections of the signal processor are implemented in the digital domain. The advantages of digital filters are high reliability, no drift with time or temperature, unit-to-unit repeatability, and superior transmission performance.

Transmit Signal Processing

In the transmit path, the analog input signal (I_{IN}) is A/D converted, filtered, compressed, and made available to the PCM highway in A-law or µ-law form. The signal processor contains an ALU, RAM, ROM, and control logic to implement the filter sections.

The decimator reduces the high input sampling rate to 16 kHz for input to the Low-Pass and High-Pass Filters. The High-Pass Filter rejects low frequencies such as 50 Hz or 60 Hz and the Low-Pass Filter limits the voice band to 3400 Hz.

Transmit PCM Interface

The transmit PCM interface receives 1 byte (8 bits) every 125 µs from the A-law/µ-law compressor. The data is transmitted onto the PCM highway under control of the transmit logic, synchronized by the Transmit Frame Synchronization signal (FSX_N). The frame synchronization signal (FSX_N) identifies the transmit time slot of the PCM frame for Channel N. The QSLAC-NP devices (Am79Q4457/5457) are compatible with both a long- and a short-frame synchronization signal. See the PCM interface timing specifications (20 to 24) for more details. While the PCM data is output on the DXA port, the $\overline{TSCA}$ buffer control signal is Low.

Receive Signal Processing

Digital data received from the PCM highway is expanded from A-law or µ-law, filtered, converted to analog, and passed to the V_{OUT} pin. The signal processor contains an ALU, RAM, ROM, and control logic to implement the filter sections.

The Low-Pass Filter band limits the signal. The interpolator increases the sampling rate prior to D/A conversion.

Receive PCM Interface

The receive PCM interface receives 1 byte (8 bits) every 125 µs from the PCM highway. The data is received under control of the receive logic and synchronized by the receive frame synchronization signal (FSR_N). The receive frame sync (FSX_N) pulse identifies the receive time slot of the PCM frame for Channel N. The QSLAC-NP devices (Am79Q4457/5457) are compatible with both a long- and a short-frame synchronization signal. See the PCM interface timing specifications (20 to 24) for more details. The receive PCM data is expanded by the A-law/µ-law expansion logic, and passed on to the signal processor.

Speech Coding

The A/D and D/A conversions follow either the A-law or the µ-law standard as defined in ITU-T Recommendation G.711. A-law or µ-law operation is programmed using the A-law/µ-law program (A/µ) pin. Alternate bit inversion is performed as part of the A-law coding.

Short-Frame Sync Mode

If each of the transmit (FSX_N) frame sync pulses overlap either one or two negative-going transitions of PCLK, the part operates in what is called Short-Frame Sync mode. In this mode, the part operates like a DSLAC, ASLAC, or QSLAC device programmed for time slot 0, clock slot 0, and XE=1. If a frame sync overlaps two transitions, the first of these transitions defines the beginning of the time slot.

The first positive PCLK transition after the beginning of a transmit time slot enables the DXA output with the sign bit as the first output. It also drives the $\overline{TSCA}$ output Low. The succeeding seven positive clock transitions shift out the remainder of the data, and the eighth negative transition tri-states DXA and turns off $\overline{TSCA}$. During the latter part of each output period, the transmit data is held by a weak driver in order to minimize bus contention if one time slot starts before the preceding one ends.

The first negative PCLK transition after the beginning of a receive time slot latches in the first data bit (sign bit) from the DRA input. The succeeding seven negative clock transitions shift in the remainder of the data.

Long-Frame Sync Mode

If each of the transmit (FSX_N) frame sync pulses overlap three or more negative-going transitions of PCLK, the part operates in what is called Long-Frame Sync mode. The time slot begins at the first point where both frame sync and PCLK are High.

The beginning of a transmit time slot enables the DXA output with the sign bit as the first output. It also drives the $\overline{TSCA}$ output Low. The succeeding seven positive clock transitions shift out the remainder of the data. The eighth negative transition of PCLK or the end of FSX, whichever comes later, tri-states DXA and turns off $\overline{TSCA}$. If FSX extends beyond the eighth PCLK edge, the eighth bit is held at DXA. During the latter part of each output period, the transmit data is held by a weak driver in order to minimize bus contention if one time slot starts before the preceding one ends.

The first negative PCLK transition after the beginning of a receive time slot latches in the first data bit (sign bit) from the DRA input. The succeeding seven negative clock transitions shift in the remainder of the data.

APPLICATIONS

The QSLAC-NP device family consists of two devices, the Am79Q5457 device and the Am79Q4457 device. The Am79Q5457 device is a four-channel Codec/Filter device with eight frame synchronization inputs, two per channel. Both the Am79Q4457 and Am79Q5457 devices are A-law or µ-law compatible. The Am79Q4457 device provides all the functions of the Am79Q5457 device and the additional functions of selecting transmit and receive gain levels and balance networks on a per-channel basis.

If the application requires a fixed transmit and receive gain level and one balance network, the Am79Q5457 device is ideal. If the application requires more than one gain setting or balance network, the Am79Q4457 device is ideal. If full programmability of gain, frequency response, balance impedance, input impedance, and time slot assignment are required, then the Am79Q02/021/031 Quad SLAC (QSLAC) device is ideal.

The QSLAC-NP device performs the Codec/Filter function for four telephone lines. It interfaces to the telephone lines through four Legerity SLIC devices as shown in Figure 10 and Figure 11. The QSLAC-NP device may require an external buffer to drive transformer SLICs.

Connection to a PCM back plane is implemented by means of a simple buffer IC. See Figure 10 and Figure 11. Several QSLAC-NP devices can be tied together in one bus interfacing the back plane through a single buffer. An intelligent bus interface chip is not required because each QSLAC-NP device provides its own buffer control ($\overline{TSCA}$).

SETTING GAIN LEVELS

Gain Settings for the Am79Q4457 Device

The possible transmit and receive gain levels are set once for the four channels via three reference currents and three reference voltages (see Figure 9a). The three I_{REF} outputs are biased at the internal reference voltage so that a resistor placed from the output to ground sets up a reference current in the device. These reference currents are buffered and provided as inputs to the 3-to-1 analog multiplexers, one per channel. One of three reference currents can be selected for use by the transmit A/D converter. Each reference current set up by the user corresponds to one transmit gain setting. The transmit gain is a function of the input resistor RTX and the reference resistor R_{REF} as shown in Figure 9a and Table 2.

In much the same way, three reference voltages are set up, one internally and two externally, as shown in Figure 9a. These voltages are internally buffered and provided to the 3-to-1 analog multiplexers, one per channel. One of three reference voltages can be selected and provided to the receive D/A converter for use in decoding the data. Each reference voltage level corresponds to a receive gain setting. The receive gain is a function of the internally generated reference voltage V_{REF1} and the scaled version V_{REF2} or V_{REF3}, as shown in Figure 9a and Table 3.

One of two balance networks per channel is selected via the serial control register. As shown in Figure 9a, this is achieved by providing two inputs to the transmit A/D converter and using a 2-to-1 analog multiplexer to select the desired input.

Table 2. Transmit Gain Select (Am79Q4457 Device Only)

Transmit Gain Select 1 (TGS1) and Transmit Gain Select 2 (TGS2)		
TGS2	**TGS1**	**A-to-D Gain**
0	0	$Gt = Gt1 = \frac{3 \bullet R_{REF1}}{Rb_{TX}}$
0	1	$Gt = Gt2 = \frac{3 \bullet (R_{REF2A} + R_{REF2B})}{Rb_{TX}}$
1	0	$Gt = Gt3 = \frac{3 \bullet (R_{REF3A} + R_{REF3B})}{Rb_{TX}}$
1	1	Do Not Use

See Figure 9. "b" represents the value of BNS1.

Table 3. Receive Gain Select (Am79Q4457 Device Only)

Receive Gain Select 1 (RGS1) and Receive Gain Select 2 (RGS2)		
RGS2	**RGS1**	**D-to-A Voltage Reference**
0	0	$Gr = Gr1 = 1$
0	1	$Gr = Gr2 = \frac{1.4 \bullet R_{REF2A}}{R_{REF2A} + R_{REF2B}}$
1	0	$Gr = Gr3 = \frac{1.4 \bullet R_{REF3A}}{R_{REF3A} + R_{REF3B}}$
1	1	Do Not Use

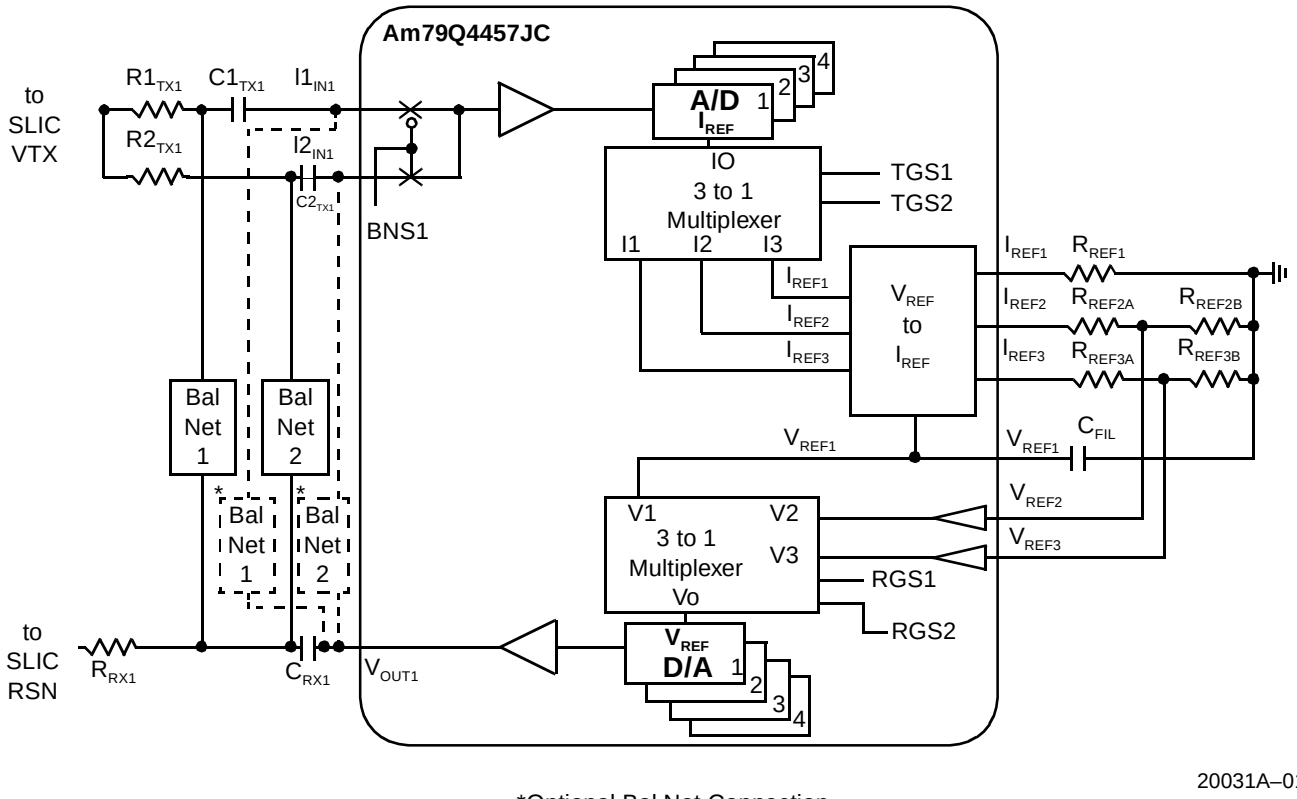
Note:
$0.4 \le Gr \le 1$

Gain Settings for the Am79Q5457 Device

The transmit and receive gains for each of the four channels are set for the Am79Q5457 device similarly to those of the Am79Q4457 device. The Am79Q5457 device has only one I_{REF} output and one V_{REF} input as shown in Figure 9b, and only one gain setting is available. The transmit gain is a function of the reference current set up by the R_{REF1} resistor and by the R_{TX1} input resistor, and is set by the following equation:

$$Gt = \frac{3 \bullet R_{REF1}}{R1_{TX1}}$$

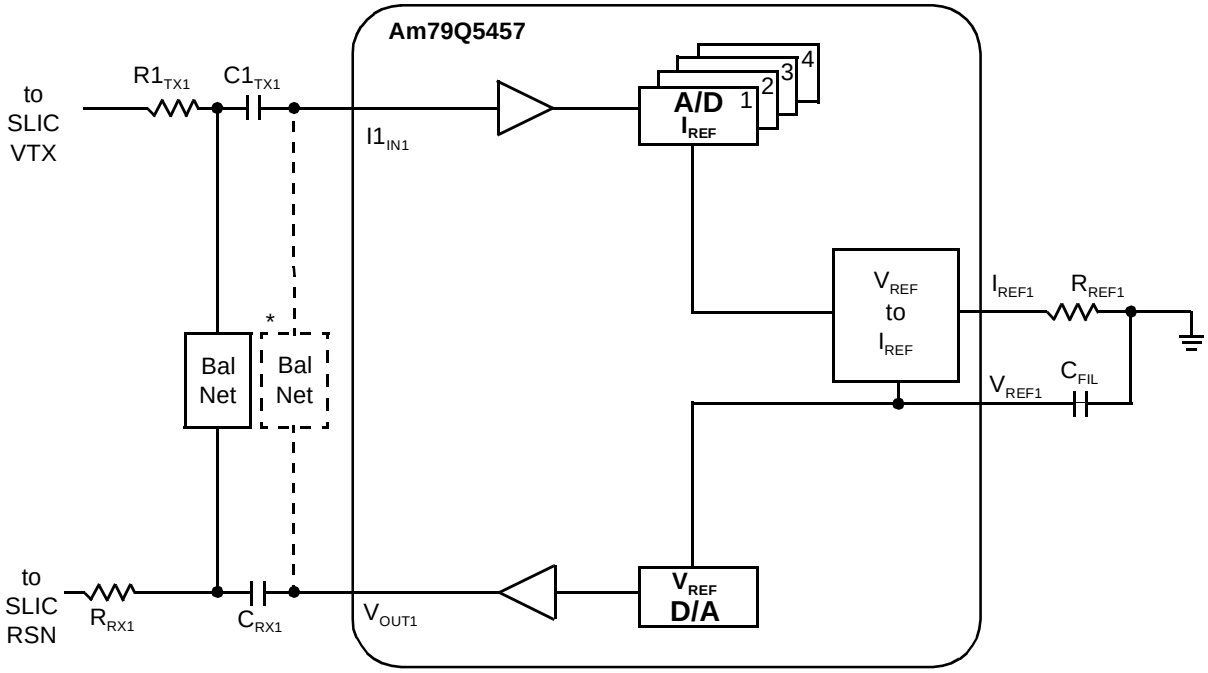
The receive gain Gr through the QSLAC-NP device is equal to 1 and is not adjustable. However, this gain typically is set by choice of component values in the SLIC portion of the circuit.



20031A–010

*Optional Bal Net Connection

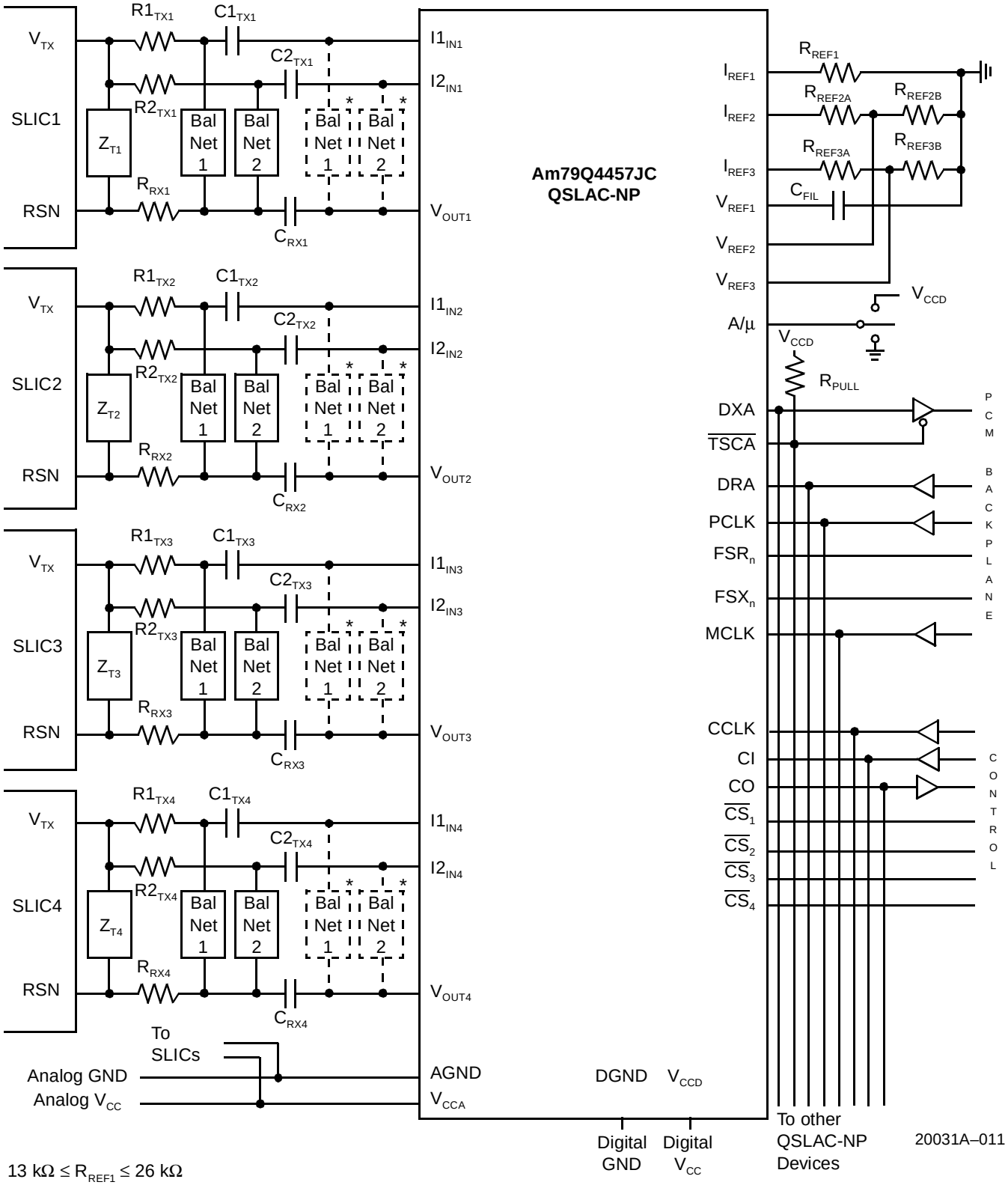
Figure 9a. Am79Q4457JC Device (Channel 1 Shown)



*Optional Bal Net Connection

20031A–012

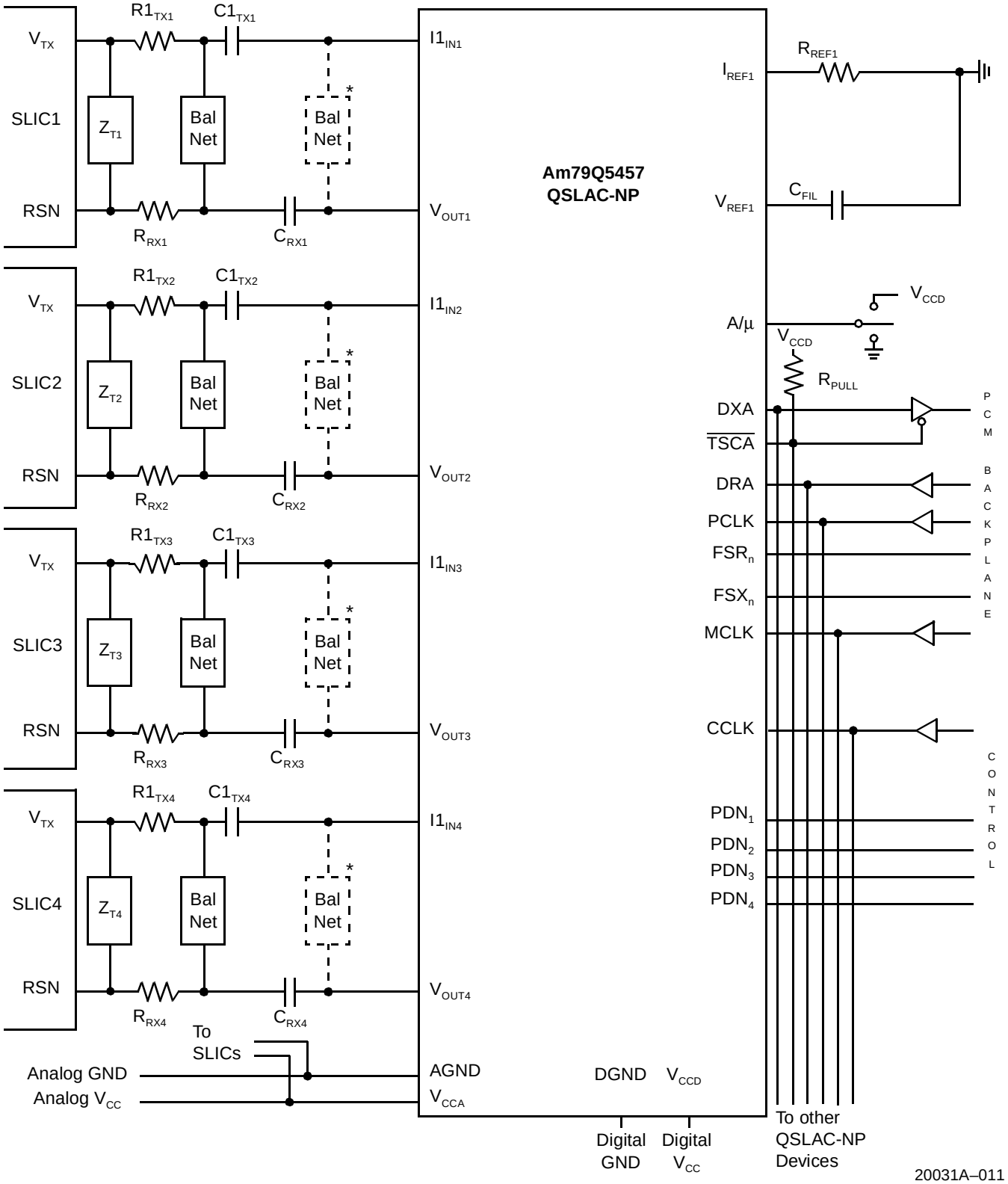
Figure 9b. Am79Q5457 Device (Channel 1 Shown)



$13\ k\Omega \le R_{REF1} \le 26\ k\Omega$
$13\ k\Omega \le R_{REF2A} + R_{REF2B} \le 26\ k\Omega$
$13\ k\Omega \le R_{REF3A} + R_{REF3B} \le 26\ k\Omega$
R_{PULL} = 360 Ω ± 5%
$R1_{TX1}$, $R1_{TX2}$, $R1_{TX3}$, $R1_{TX4}$ - See Transmit Gain Select 1, Table 2
$R2_{TX1}$, $R2_{TX2}$, $R2_{TX3}$, $R2_{TX4}$ - See Transmit Gain Select 2, Table 2
$Z_{T1–4}$ = SLIC Programming Impedance - See SLIC Data Sheet

R_{RX1}, R_{RX2}, R_{RX3}, R_{RX4} - See SLIC Data Sheet
C_{FIL} = 0.1 µF ± 20%, X7R
$C1_{TX1}$, $C1_{TX2}$, $C1_{TX3}$, $C1_{TX4}$ = 0.1 µF ± 20%, X7R, typ.
$C2_{TX1}$, $C2_{TX2}$, $C2_{TX3}$, $C2_{TX4}$ = 0.1 µF ± 20%, X7R, typ.
C_{RX1}, C_{RX2}, C_{RX3}, C_{RX4} = 0.1 µF ± 20%, X7R, typ.
*Optional Balance Network connection.

Figure 10. Am79Q4457JC Device



13 kΩ ≤ R_{REF1} ≤ 26 kΩ
R_{PULL} = 360 Ω ± 5%
$R1_{TX1}$, $R1_{TX2}$, $R1_{TX3}$, $R1_{TX4}$ - See Transmit Gain Select 1, Table 2
R_{RX1}, R_{RX2}, R_{RX3}, R_{RX4} - See SLIC Data Sheet
$Z_{T1–4}$ = SLIC Programming Impedance - See SLIC Data Sheet

C_{FIL} = 0.1 µF ± 20%, X7R, typ.
$C1_{TX1}$, $C1_{TX2}$, $C1_{TX3}$, $C1_{TX4}$ = 0.1 µF ± 20%, X7R, typ.
C_{RX1}, C_{RX2}, C_{RX3}, C_{RX4} = 0.1 µF ± 20%, X7R, typ.
*Optional Balance Network connection.

Figure 11. Am79Q5457JC Device

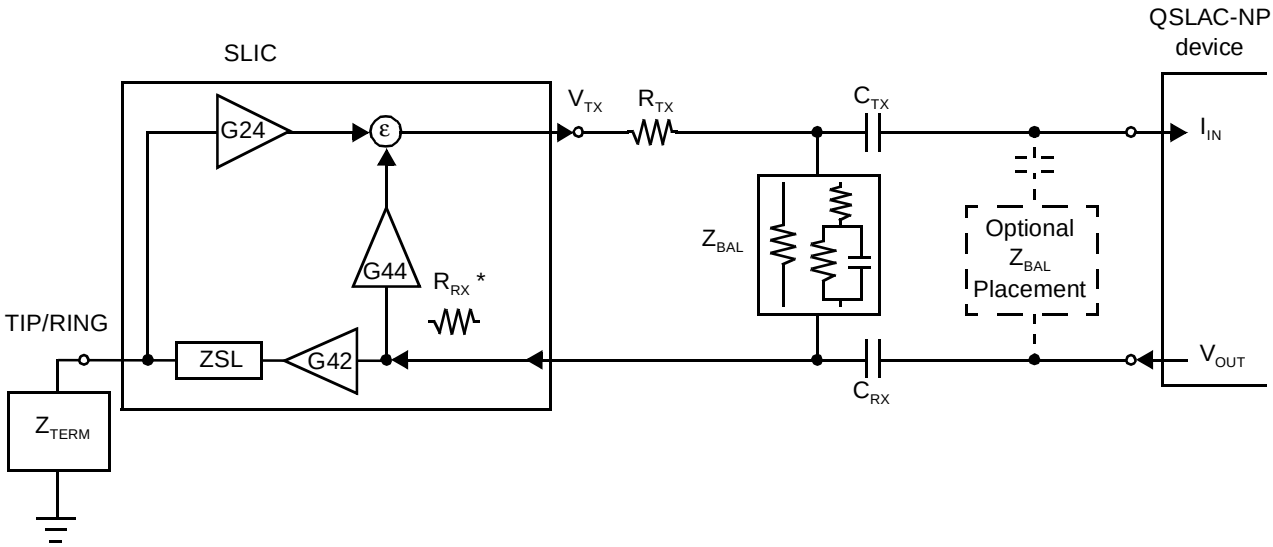
Calculation of Balance Network

The balance function is implemented with the QSLAC-NP device by connecting an external balance network (Z_{BAL}) between the V_{OUT} and I_{IN} terminals. Assuming the uncancelled receive path signal, which appears in the SLIC's transmit path, is out of phase with the originating receive path (the QSLAC-NP device's V_{OUT}) signal, this external network will provide a path for the needed cancellation. The I_{IN} terminal is a current summing node and is a virtual ac ground, simplifying the implementation of this balance function. In many cases, this balance network can be a single resistor, and in other cases, depending on the balance impedance and the transfer characteristics of the SLIC, it may be necessary to add a capacitor. Complete definition of the balance network is dependent on the SLIC and the balance impedance and, as such, cannot be completely defined within this document. However, a general method of calculation can be described as follows:

Figure 12 shows a simplified equivalent circuit of a SLIC, along with the balance impedance and interconnecting networks to the QSLAC device. A SLIC circuit can be represented by four gain parameters (G-parameters), where each of these blocks represents a complex transfer function: G24 is the gain from the tip/ring two-wire port toward the four-wire port; G42 is the unterminated gain from the four-wire port toward the two-wire port; ZSL is the two-wire SLIC impedance; and G44 is the gain that appears from the four-wire input toward the four-wire output with the two-wire port shorted. Considering only the SLIC, plus the externally connected balance impedance, Z_{TERM}, any signal that is presented to the SLIC's four-wire input will have a representation at the V_{TX} four-wire output defined by the SLIC's G-parameters and the Z_{BAL} termination. G44L (G44 loaded) can then be defined as the four-wire to four-wire gain through the SLIC when loaded by Z_{TERM}. The R_{TX} resistor establishes the transmit path gain by translating the SLIC's V_{TX} output voltage so that it appears as a current into the QSLAC-NP device's I_{IN} current input and, as such, provides the scaling necessary to define the transmit gain. If the G44L gain is then known, the balance network can be calculated as follows:

$$Z_{BAL} = \frac{R_{TX1}}{G44L}$$

G44L is a complex value, which implies that Z_{BAL} must also be complex. However, in many cases, satisfactory balance over the voice band can be achieved by using only one resistor. This configuration assumes that $R_{TX} \bullet C_{TX}$ and $R_{RX} \bullet C_{RX}$ have time constants greater than 10 ms. If that is not true, the balance network should be moved to the QSLAC-NP device side of the coupling capacitors and should also have a capacitor placed in series with the network.



Note:
**G-parameter model includes the R_{RX} resistor inside SLIC.*

Figure 12. Balance Network

CONSIDERATIONS FOR CONNECTION TO SLICS

There are several factors to consider with the connection method used between the QSLAC-NP device and the SLIC. The R_{TX} resistor controls the transmit path gain by establishing the current into the QSLAC-NP device's I_{IN} pin. The RRX resistor controls the receive path gain in conjunction with the other SLIC circuit elements, by establishing the current into the SLIC's RSN pin. The balance network provides a path for passing a representative portion of the receive path signal back into the transmit path for setting the transhybrid balance. Additionally, the capacitors used to provide DC isolation between the SLIC and the QSLAC device also have an effect on system performance. Figure 13 shows the connection scheme as described earlier in this document. An alternative connection scheme is shown in Figure 14. The only difference in these connection methods is the placement of the balance network, but in each case, there are specific factors to be considered.

Effects of C_{RX} and C_{TX} Capacitors

While the purpose of the C_{RX} and C_{TX} capacitors is to provide DC isolation, they have a finite impedance that is a function of frequency. Nominal values of the R_{RX} and R_{TX} resistors typically are large compared to the capacitors' impedances at most voice band frequencies; but at lower frequencies, the capacitor impedances may have an effect. For example, a 0.1 uF capacitor at 1000 Hz has an impedance of 1592 Ω, but at 300 Hz, that impedance increases to 5305 Ω. While this is still a small change compared to the resistor values, it is not this change alone that may need to be considered. For example, in Figure 14, the I_{IN} input pin of the QSLAC-NP device has two sources feeding it: One is the Z_{BAL} balance network, and the other is the series path of R_{TX} and C_{TX} that are fed from the SLIC's V_{TX} output. The I_{IN} pin is a virtual ground, so currents from the two source paths do not effect one another. However, in Figure 13, the Z_{BAL} network is connected between the C_{TX} and R_{TX} components. So long as the capacitor's impedance is low, it has little effect on signals from either Z_{BAL} or from R_{TX}, and both of those signal's currents continue to flow into the I_{IN} virtual ground. As the capacitor's impedance begins to become significant with lower frequencies, a portion of the transmit path current from R_{TX} will begin to flow into Z_{BAL} toward the low impedance output of the QSLAC-NP device's V_{OUT} pin. The net effect is a low frequency attenuation to the transmit path signal. A similar situation also exists in the receive path.

Placement of the Balance Network

The only difference in the two circuit connection methods shown in Figure 13 and Figure 14 is the placement of the Z_{BAL} network. Both methods have benefits and both have different issues to consider for the overall design performance. Depending on the SLIC and the termination impedance for which balance is specified, the circuit of Figure 13 may reduce the complexity needed of the Z_{BAL} network so that only a single resistor is required. This would be especially true of short loop applications where the actual termination in service is a relatively constant resistance. Since in this configuration the C_{TX} and C_{RX} capacitors are both external to the echo loop being canceled by Z_{BAL}, the frequency dependent echo responses due to their effects need not be considered. In Figure 14, however, the capacitors are in series with the receive and transmit paths. Since the resistor values are unequal, the frequency rolloff characteristics will likely be unequal without corresponding changes of the C_{RX} and C_{TX} values. This frequency dependent characteristic now implies that the Z_{BAL} network also contains the necessary complex components to maintain proper phase response.

SLIC Connection Consideration Summary

Two different interconnection schemes are described in Figure 13 and Figure 14. The configuration shown in Figure 13 may simplify the Z_{BAL} network, or possibly even remove the need for it to contain capacitive elements, provided that the balance termination impedance and SLIC characteristics are compatible. It may be necessary in this configuration to use larger C_{RX} or C_{TX} capacitor values if frequency response at very low frequencies becomes a concern. The configuration shown in Figure 14 may allow smaller transmit and receive path coupling capacitors, but may require a slightly more complex Z_{BAL} network. Variations of the configurations from either of these figures are also possible. In any case, the designer must consider all of the effects of SLIC characteristics, balance termination impedance values, coupling capacitor values, and balance network values.

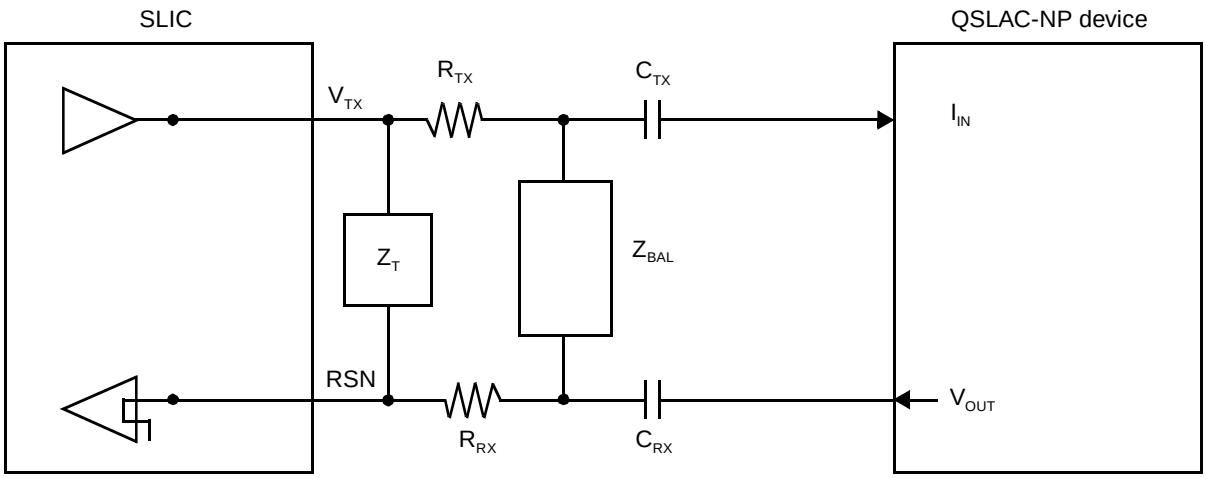


Figure 13. Balance Network Connection

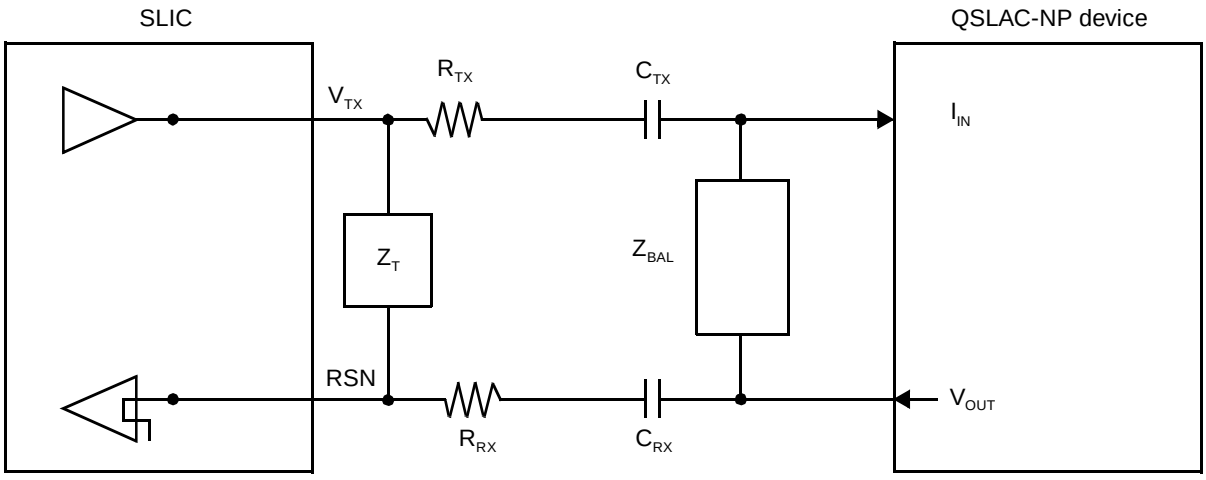
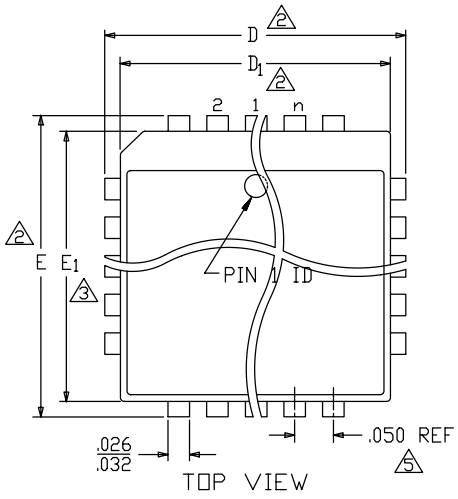
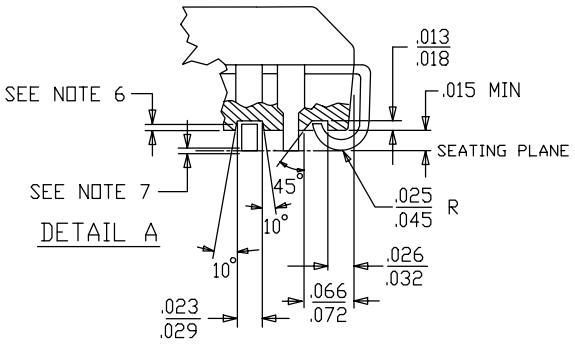


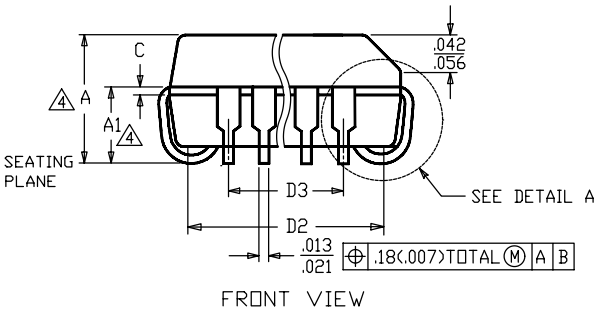
Figure 14. Alternate Balance Network Connection

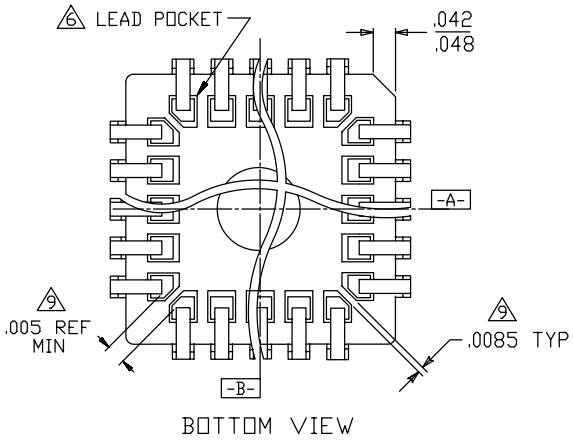
PHYSICAL DIMENSIONS

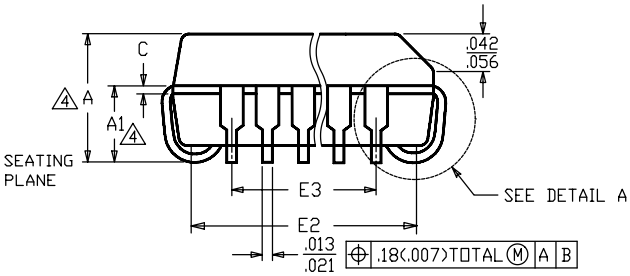
PL032











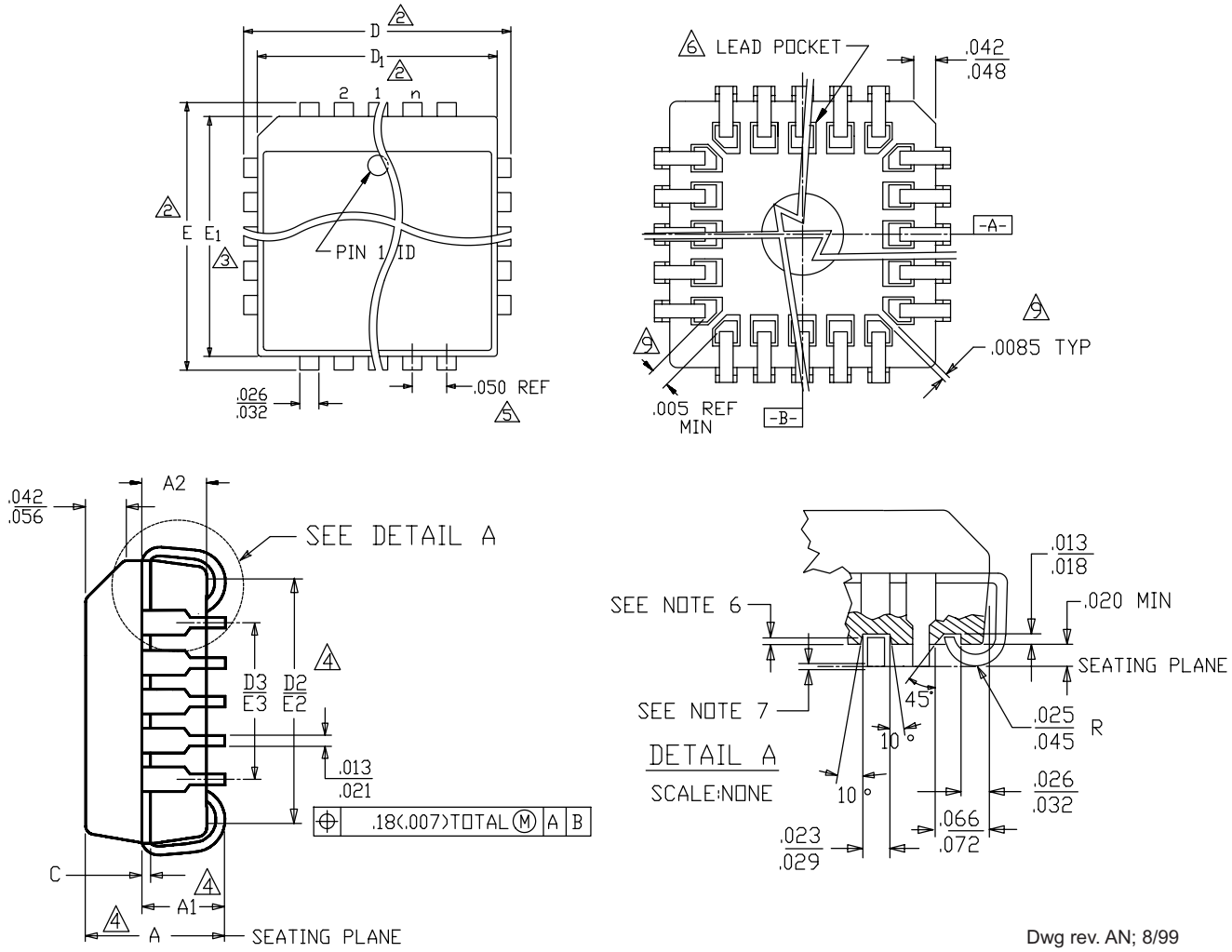
PACKAGE	PL32	
JEDEC	MO-052(A)AE	
SYMBOL	MIN	MAX
A	.125	.140
A1	.080	.095
D	.485	.495
D1	.447	.453
D2	.390	.430
D3	.300	REF
E	.585	.595
E1	.547	.553
E2	.490	.530
E3	.400	REF
C	.009	.015

NOTES:

Dwg rev AH; 10/99

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONS "D" AND "E" ARE MEASURED FROM OUTERMOST POINT.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE CORNER MOLD FLASH. ALLOWABLE CORNER MOLD FLASH IS .010"
4. DIMENSIONS "A", "A1", "D2" AND "E2" ARE MEASURED AT THE POINTS OF CONTACT TO BASE PLANE
5. LEAD SPACING AS MEASURED FROM CENTERLINE TO CENTERLINE SHALL BE WITHIN ±.005".
6. J-LEAD TIPS SHOULD BE LOCATED INSIDE THE "POCKET.
7. LEAD COPLANARITY SHALL BE WITHIN .004" AS MEASURED FROM SEATING PLANE. COPLANARITY IS MEASURED PER AMD 06-500.
8. LEAD TWEEZE SHALL BE WITHIN .0045" ON EACH SIDE AS MEASURED FROM A VERTICAL FLAT PLANE. TWEEZE IS MEASURED PER AMD 06-500.
9. LEAD POCKET MAY BE RECTANGULAR (AS SHOWN) OR OVAL. IF CORNER LEAD POCKETS ARE CONNECTED THEN 5 MILS MINIMUM CORNER LEAD SPACING IS REQUIRED.

PL044



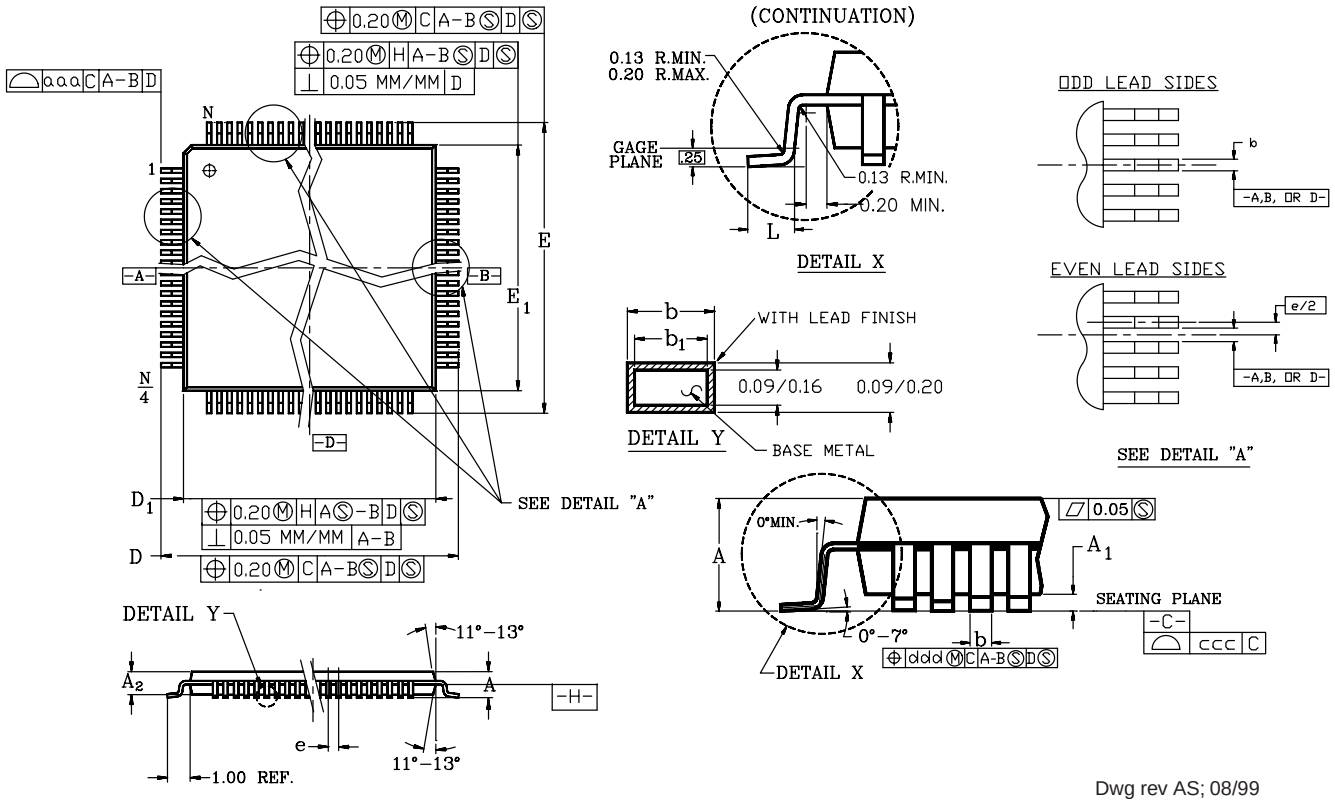
Dwg rev. AN; 8/99

PACKAGE	PL44	
JEDEC	MS-018(A)AC	
SYMBOL	MIN	MAX
A	.165	.180
A1	.090	.120
A2	.062	.083
D	.685	.695
D1	.650	.656
D2	.590	.630
D3	.500	REF
E	.685	.695
E1	.650	.656
E2	.590	.630
E3	.500	REF
C	.009	.015

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONS "D" AND "E" ARE MEASURED FROM OUTERMOST POINT.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE CORNER MOLD FLASH. ALLOWABLE CORNER MOLD FLASH IS .010 INCH
4. DIMENSIONS "A", "A1", "D2" AND "E2" ARE MEASURED AT THE POINTS OF CONTACT TO BASE PLANE
5. LEAD SPACING AS MEASURED FROM CENTERLINE TO CENTERLINE SHALL BE WITHIN ±.005 INCH.
6. J-LEAD TIPS SHOULD BE LOCATED INSIDE THE "POCKET.
7. LEAD COPLANARITY SHALL BE WITHIN .004 INCH AS MEASURED FROM SEATING PLANE. COPLANARITY IS MEASURED PER AMD 06-500.
8. LEAD TWEEZE SHALL BE WITHIN .0045 INCH ON EACH SIDE AS MEASURED FROM A VERTICAL FLAT PLANE. TWEEZE IS MEASURED PER AMD 06-500.
9. LEAD POCKET MAY BE RECTANGULAR (AS SHOWN) OR OVAL. IF CORNER LEAD POCKETS ARE CONNECTED THEN 5 MILS MINIMUM CORNER LEAD SPACING IS REQUIRED.

PQT044



Dwg rev AS; 08/99

PACKAGE	PQT 44		
JEDEC	MS-026 (C) ACB		
SYMBOL	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	--	0.15
A2	0.95	1.00	1.05
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
L	0.45	0.60	0.75
N	44		
e	0.80 BASIC		
b	0.30	0.37	0.45
b1	0.30	0.35	0.40
ccc	—	—	0.10
ddd	—	—	0.20
aaa	—	—	0.20

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982.
2. DATUM PLANE -H- IS LOCATED AT THE MOLD PARTING LINE AND IS COINCIDENT WITH THE BOTTOM OF THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY.
3. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.254mm PER SIDE. DIMENSIONS "D1" AND "E1" INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-
4. DIMENSION "B" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
5. CONTROLLING DIMENSIONS: MILLIMETER.
6. DIMENSIONS "D" AND "E" ARE MEASURED FROM BOTH INNERMOST AND OUTERMOST POINTS.
7. DEVIATION FROM LEAD–TIP TRUE POSITION SHALL BE WITHIN ±0.076 mm.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm. COPLANARITY IS MEASURED PER SPECIFICATION 06–500.
9. HALF SPAN (CENTER OF PACKAGE TO LEAD TIP) SHALL BE 15.30±.165 mm.
10. "N" IS THE TOTAL NUMBER OF TERMINALS.
11. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF THE PACKAGE BY 0.15 mm.
12. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–136, MS–026.

REVISION SUMMARY

Revision B to Revision C

- The physical dimensions (PL032, PL044 and PQT044) were added to the Physical Dimension section.
- Updated the Pin Description table to correct inconsistencies.

Revision C to Revision D

- All the physical dimensions were updated.

Notes:

Notes:

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P.O. Box 18200
Austin, Texas 78760-8200

Telephone: (512) 228-5400
Fax: (512) 228-5510
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