SILICON LABORATORIES

Si3035

3.3 V FCC/JATE DIRECT ACCESS ARRANGEMENT

Features

Complete DAA includes the following:

- 3.3 V to 5 V Digital/Analog Power Supplies
- JATE Filter Option
- 86 dB Dynamic Range TX/RX Paths
- Daisy-Chaining for Up to Eight Devices
- Integrated Ring Detector
- 3000 V Isolation
- Support for Caller ID
- Low Profile SOIC Packages
- Direct Interface to DSPs
- Integrated Modem Codec
- Compliant with FCC Part 68
- Low-Power Standby Mode
- Proprietary ISOcap™ Technology
- Pin Compatible with Si3034, Si3032
- Optional IIR Digital Filter

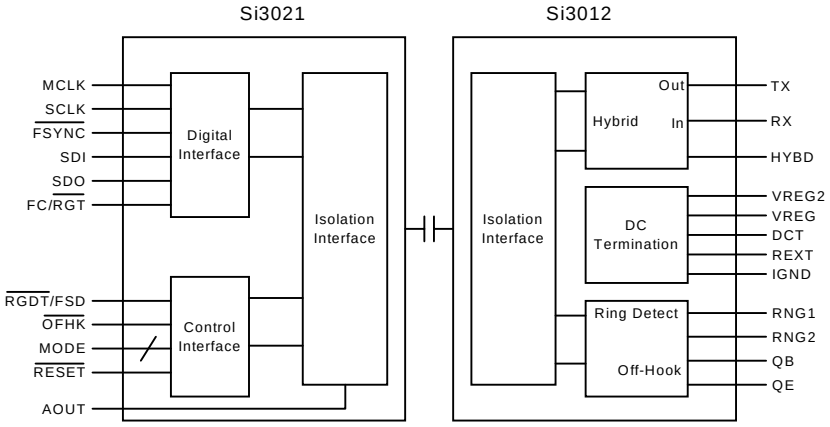
Applications

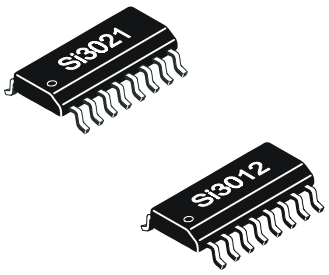
- V.90 Modems
- Voice Mail Systems
- Fax Machines
- Set Top Boxes

Description

The Si3035 is an integrated direct access arrangement (DAA) chipset that provides a digital, low-cost, solid-state interface to a telephone line. Available in two 16-pin small outline packages, it eliminates the need for an analog front end (AFE), an isolation transformer, relays, opto-isolators, and a 2- to 4-wire hybrid. The Si3035 dramatically reduces the number of discrete components and cost required to achieve compliance with FCC Part 68. The Si3035 interfaces directly to standard modem DSPs and supports all FCC and JATE out-of-band noise requirements. International support is provided by the pin compatible Si3034.

Functional Block Diagram



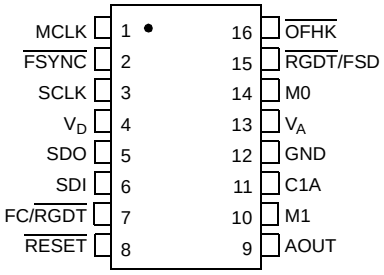


Ordering Information

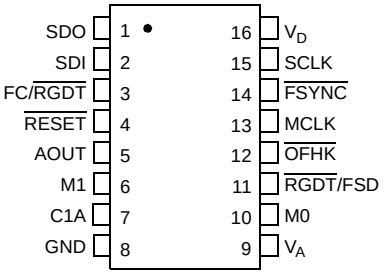
See page 50.

Pin Assignments

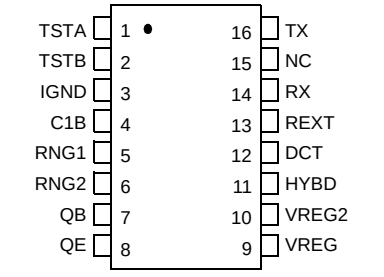
Si3021 (SOIC)



Si3021 (TSSOP)



Si3012 (SOIC or TSSOP)



US Patent # 5,870,046
US Patent # 6,061,009
Other Patents Pending

TABLE OF CONTENTS

Section **Page**

Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter[1]	Symbol	Test Condition	Min[2]	Typ	Max[2]	Unit
Ambient Temperature	T_A	K-Grade	0	25	70	°C
Si3021 Supply Voltage, Analog	V_A		4.75	5.0	5.25	V
Si3021 Supply Voltage, Digital[3]	V_D		3.0	3.3/5.0	5.25	V

Notes:

1. The Si3035 specifications are guaranteed when the typical application circuit (including component tolerances) and any Si3021 and any Si3012 are used. See Figure 16 on page 15 for typical application circuit.
2. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
3. The digital supply, V_D, can operate from either 3.3 V or 5.0 V. The Si3021 supports interface to 3.3 V logic when operating from 3.3 V. The 3.3 V operation applies to both the serial port and the digital signals $\overline{RGDT}$, $\overline{OFHK}$, $\overline{RESET}$, M0, and M1.

Table 2. Loop Characteristics

(V_A = Charge Pump, V_D = +3.3 V ± 0.3 V, T_A = 0 to 70°C for K-Grade, Refer to Figure 1)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Termination Voltage	V_{TR}	I_L = 20 mA	—	—	7.7	V
DC Termination Voltage	V_{TR}	I_L = 105 mA	12	—	—	V
DC Ring Current (with caller ID)	I_{RDC}		—	—	1	mA
DC Ring Current (w/o caller ID)	I_{RDC}		—	—	20	µA
AC Termination Impedance	Z_{ACT}		—	600	—	Ω
Operating Loop Current	I_{LP}		20	—	120	mA
Loop Current Sense Bits	LCS	LCS = Fh	180	155	—	mA
Ring Voltage Detect	V_{RD}		13	18	26	V_{RMS}
Ring Frequency	F_R		15	—	68	Hz
On-Hook Leakage Current	I_{LK}	V_{BAT} = –48 V	—	—	1	µA
Ringer Equivalence Num. (with caller ID)	REN		—	1.0	1.67	—
Ringer Equivalence Num. (w/o caller ID)	REN		—	0.2	—	—

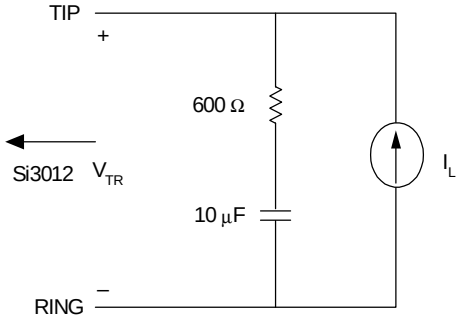


Figure 1. Test Circuit for Loop Characteristics

Table 3. DC Characteristics, V_D = +5 V

(V_A = +5 V ±5%, V_D = +5 V ±5%, T_A = 0 to 70°C for K-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		3.5	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	I_O = –2 mA	3.5	—	—	V
Low Level Output Voltage	V_{OL}	I_O = 2 mA	—	—	0.4	V
Input Leakage Current	I_L		–10	—	10	µA
Power Supply Current, Analog	I_A	V_A pin	—	0.3	1	mA
Power Supply Current, Digital[1]	I_D	V_D pin	—	14	18	mA
Total Supply Current, Sleep Mode[1]	$I_A + I_D$	PDN = 1, PDL = 0	—	1.3	2.5	mA
Total Supply Current, Deep Sleep[1,2]	$I_A + I_D$	PDN = 1, PDL = 1	—	0.04	0.5	mA

Notes:
1. All inputs at 0.4 or V_D – 0.4 (CMOS levels). All inputs held static except clock and all outputs unloaded (Static I_{OUT} = 0 mA).
2. $\overline{\text{RGDT}}$ is not functional in this state.

Table 4. DC Characteristics, V_D = +3.3 V

(V_A = Charge Pump, V_D = +3.3 V ± 0.3 V, T_A = 0 to 70℃ for K-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	I_O = –2 mA	2.4	—	—	V
Low Level Output Voltage	V_{OL}	I_O = 2 mA	—	—	0.35	V
Input Leakage Current	I_L		–10	—	10	µA
Power Supply Current, Analog[1,2]	I_A	V_A pin	—	0.3	1	mA
Power Supply Current, Digital[3]	I_D	V_D pin	—	9	12	mA
Total Supply Current, Sleep Mode[3]	$I_A + I_D$	PDN = 1, PDL = 0	—	1.2	2.5	mA
Total Supply Current, Deep Sleep[3,4]	$I_A + I_D$	PDN = 1, PDL = 1	—	0.04	0.5	
Power Supply Voltage, Analog[1,5]	V_A	Charge Pump On	4.3	4.6	5.00	V

Notes:
1. Only a decoupling capacitor should be connected to V_A when the charge pump is on.
2. There is no I_A current consumption when the internal charge pump is enabled and only a decoupling cap is connected to the V_A pin.
3. All inputs at 0.4 or V_D – 0.4 (CMOS levels). All inputs held static except clock and all outputs unloaded (Static I_{OUT} = 0 mA).
4. $\overline{\text{RGDT}}$ is not functional in this state.
5. The charge pump is recommended to be used only when V_D < 4.5 V. When the charge pump is not used, V_A should be applied to the device before V_D is applied on power up if driven from separate supplies.

Table 5. AC Characteristics

(V_A = Charge Pump, V_D = +3.3 V ± 0.3 V, T_A = 0 to 70°C for K-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sample Rate[1]	Fs	Fs = F_{PLL2}/5120	7.2	—	11.025	kHz
PLL1 Output Clock Frequency	F_{PLL1}	FPLL1 = F_{MCLK} • M1/N1	36	—	58	MHz
Transmit Frequency Response		Low –3 dB corner	—	16	—	Hz
Receive Frequency Response		Low –3 dB corner	—	16	—	Hz
Transmit Full Scale Level[2] (0 dB gain)	V_{TX}		—	0.98	—	V_{PEAK}
Receive Full Scale Level [2,3] (0 dB gain)	V_{RX}		—	0.98	—	V_{PEAK}
Dynamic Range[4]	DR	VIN = 1 kHz, –3 dBFS	80	86	—	dB
Dynamic Range[5]	DR	VIN = 1 kHz, –3 dBFS	—	84	—	dB
Total Harmonic Distortion[6]	THD	VIN = 1 kHz, –3 dBFS	—	–84	—	dB
Dynamic Range (call progress AOUT)	DR_{AO}	VIN = 1 kHz	60	—	—	dB
THD (call progress AOUT)	THD_{AO}	VIN = 1 kHz	—	1.0	—	%
AOUT Full Scale Level			—	0.75 V_D	—	V_{PP}
AOUT Output Impedance			—	10	—	kΩ
Mute Level (call progress AOUT)			–90	—	—	dB
Dynamic Range (caller ID mode)	DR_{CID}	VIN = 1 kHz, –13 dBFS	—	60	—	dB
Caller ID Full Scale Level (0 dB gain)[2]	V_{CID}		—	0.8	—	V_{PEAK}

Notes:

1. See Figure 23 on page 22.
2. Parameter measured at TIP and RING of Figure 16 on page 15.
3. Receive Full Scale Level will produce – 0.9 dBFS at SDO.
4. DR = 3 dB + 20 log (RMS signal/RMS noise). Applies to both the transmit and receive paths. Measurement bandwidth is 300 to 3400 Hz. Sample Rate = 9.6 kHz, Loop Current = 40 mA.
5. DR = 3 dB + 20 log (RMS signal/RMS noise). Applies to both the transmit and receive paths. Measurement bandwidth is 15 to 3400 Hz. Sample Rate = 9.6 kHz, Loop Current = 40 mA.
6. THD = 20 log (RMS distortion/RMS signal). Applies to both the transmit and receive paths. Sample Rate = 9.6 kHz, Loop Current = 40 mA.

Table 6. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_D, V_A	–0.5 to 6.0	V
Input Current, Si3021 Digital Input Pins	I_{IN}	±10	mA
Digital Input Voltage	V_{IND}	–0.3 to (V_D + 0.3)	V
Operating Temperature Range	T_A	–40 to 100	°C
Storage Temperature Range	T_{STG}	–65 to 150	°C

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Switching Characteristics—General Inputs

(V_A = Charge Pump, V_D = 3.0 to 5.25 V, T_A = 0 to 70°C for K-Grade, C_L = 20 pF)

Parameter[1]	Symbol	Min	Typ	Max	Unit
Cycle Time, MCLK	t_{mc}	16.67	—	1000	ns
MCLK Duty Cycle	t_{dty}	40	50	60	%
Rise Time, MCLK	t_r	—	—	5	ns
Fall Time, MCLK	t_f	—	—	5	ns
MCLK Before $\overline{\text{RESET}}$ ↑	t_{mr}	10	—	—	cycles
$\overline{\text{RESET}}$ Pulse Width[2]	t_{rl}	250	—	—	ns
M0, M1 Before $\overline{\text{RESET}}$↑[3]	t_{mxr}	150	—	—	ns

Notes:
1. All timing (except Rise and Fall time) is referenced to the 50% level of the waveform. Input test levels are V_{IH} = V_D – 0.4 V, V_{IL} = 0.4 V. Rise and Fall times are referenced to the 20% and 80% levels of the waveform.
2. The minimum $\overline{\text{RESET}}$ pulse width is the greater of 250 ns or 10 MCLK cycle times.
3. M0 and M1 are typically connected to V_D or GND and should not be changed during normal operation.

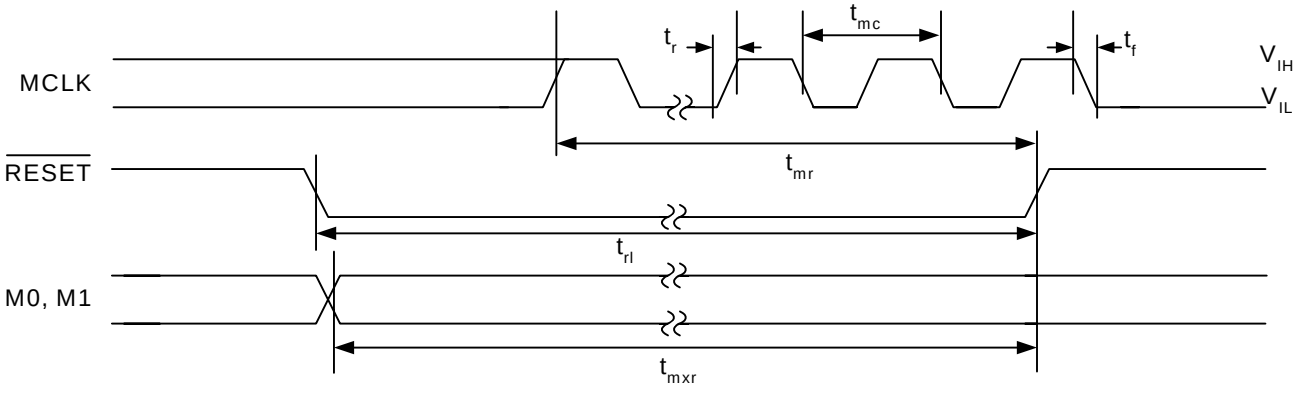


Figure 2. General Inputs Timing Diagram

Table 8. Switching Characteristics—Serial Interface (DCE = 0)
(V_A = Charge Pump, V_D = 3.0 to 5.25 V, T_A = 0 to 70°C for K-Grade, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Cycle time, SCLK	t_c	354	1/256 Fs	—	ns
SCLK duty cycle	t_{dty}	—	50	—	%
Delay time, SCLK ↑ to $\overline{\text{FSYNC}}$ ↓	t_{d1}	—	—	10	ns
Delay time, SCLK ↑ to SDO valid	t_{d2}	—	—	20	ns
Delay time, SCLK ↑ to $\overline{\text{FSYNC}}$ ↑	t_{d3}	—	—	10	ns
Setup time, SDI before SCLK ↓	t_{su}	25	—	—	ns
Hold time, SDI after SCLK ↓	t_h	20	—	—	ns
Setup time, FC ↑ before SCLK ↑	t_{sfc}	40	—	—	ns
Hold time, FC ↑ after SCLK ↑	t_{hfc}	40	—	—	ns
Note: All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D - 0.4$ V, $V_{IL} = 0.4$ V					

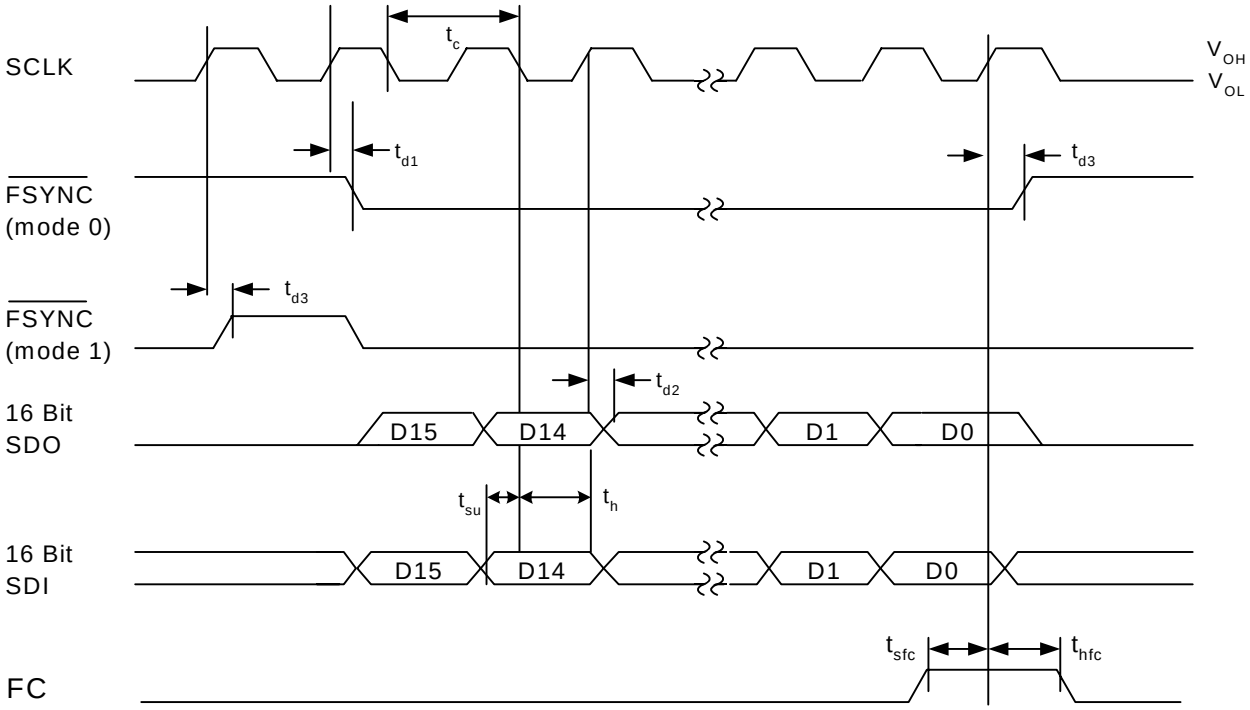


Figure 3. Serial Interface Timing Diagram

Table 9. Switching Characteristics—Serial Interface (DCE = 1, FSD = 0)
(V_A = Charge Pump, V_D = 3.0 to 5.25 V, T_A = 0 to 70°C for K-Grade, C_L = 20 pF)

Parameter[1,2]	Symbol	Min	Typ	Max	Unit
Cycle Time, SCLK	t_c	354	1/256 Fs	—	ns
SCLK Duty Cycle	t_{dty}	—	50	—	%
Delay Time, SCLK ↑ to $\overline{\text{FSYNC}}$ ↑	t_{d1}	—	—	10	ns
Delay Time, SCLK ↑ to $\overline{\text{FSYNC}}$ ↓	t_{d2}	—	—	10	ns
Delay Time, SCLK ↑ to SDO valid	t_{d3}	$0.25t_c - 20$	—	$0.25t_c + 20$	ns
Delay Time, SCLK ↑ to SDO Hi-Z	t_{d4}	—	—	20	ns
Delay Time, SCLK ↑ to $\overline{\text{RGDT}}$ ↓	t_{d5}	—	—	20	ns
Delay Time, SCLK ↑ to $\overline{\text{RGDT}}$ ↑	t_{d6}	—	—	20	ns
Setup Time, SDO Before SCLK ↓	t_{su}	25	—	—	ns
Hold Time, SDO After SCLK ↓	t_h	20	—	—	ns
Setup Time, SDI Before SCLK	t_{su2}	25	—	—	ns
Hold Time, SDI After SCLK	t_{h2}	20	—	—	ns

Notes:
1. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D - 0.4$ V, $V_{IL} = 0.4$ V.
2. Refer to the section "Multiple Device Support" on page 25 for functional details.

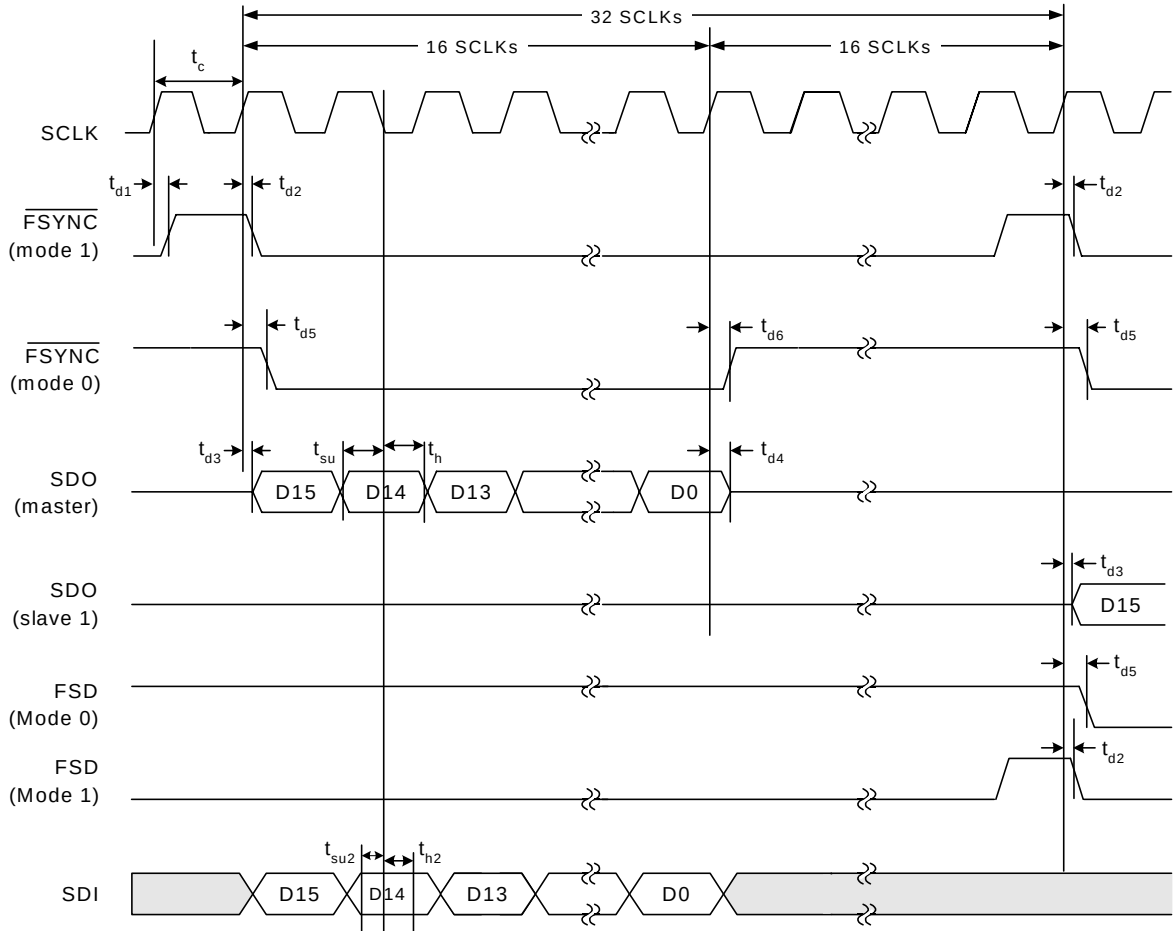


Figure 4. Serial Interface Timing Diagram (DCE = 1, FSD = 0)

Table 10. Switching Characteristics—Serial Interface (DCE = 1, FSD = 1)
(V_A = Charge Pump, V_D = 3.0 to 5.25 V, T_A = 0 to 70°C for K-Grade, C_L = 20 pF)

Parameter[1,2]	Symbol	Min	Typ	Max	Unit
Cycle Time, SCLK	t_c	354	1/256 Fs	—	ns
SCLK Duty Cycle	t_{dty}	—	50	—	%
Delay Time, SCLK ↑ to $\overline{\text{FSYNC}}$ ↑	t_{d1}	—	—	10	ns
Delay Time, SCLK ↑ to $\overline{\text{FSYNC}}$ ↓	t_{d2}	—	—	10	ns
Delay Time, SCLK ↑ to SDO valid	t_{d3}	$0.25t_c - 20$	—	$0.25t_c + 20$	ns
Delay Time, SCLK ↑ to SDO Hi-Z	t_{d4}	—	—	20	ns
Delay Time, SCLK ↑ to $\overline{\text{RGDT}}$ ↓	t_{d5}	—	—	20	ns
Setup Time, SDO Before SCLK ↓	t_{su}	25	—	—	ns
Hold Time, SDO After SCLK ↓	t_h	20	—	—	ns
Setup Time, SDI Before SCLK	t_{su2}	25	—	—	ns
Hold Time, SDI After SCLK	t_{h2}	20	—	—	ns

Notes:
1. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D - 0.4$ V, $V_{IL} = 0.4$ V.
2. Refer to the section "Multiple Device Support" on page 25 for functional details.

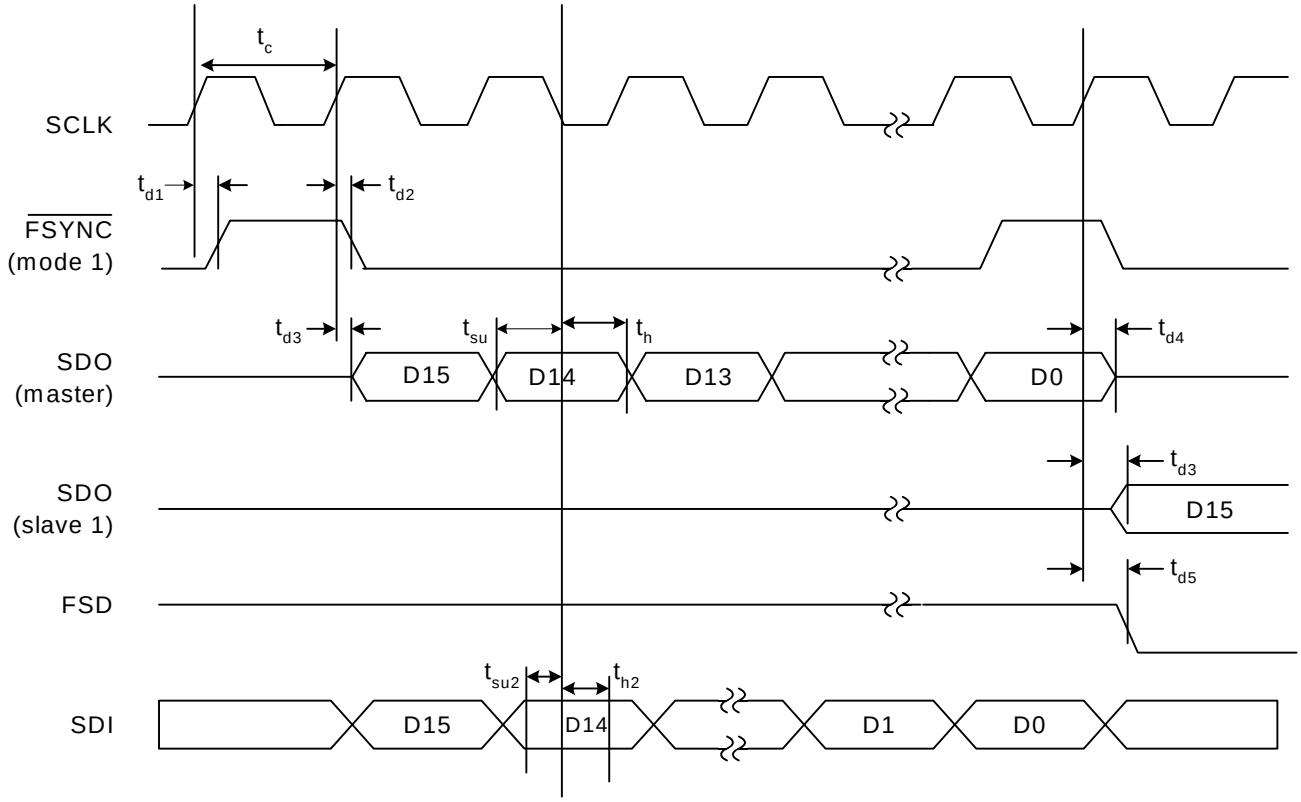


Figure 5. Serial Interface Timing Diagram (DCE = 1, FSD = 1)

Table 11. Digital FIR Filter Characteristics—Transmit and Receive
(V_A = Charge Pump, V_D = +5 V ±5%, Sample Rate = 8 kHz, T_A = 0 to 70°C for K-Grade)

Parameter	Symbol	Min	Typ	Max	Unit
Passband (0.1 dB)	$F_{(0.1\ dB)}$	0	—	3.3	kHz
Passband (3 dB)	$F_{(3\ dB)}$	0	—	3.6	kHz
Passband Ripple Peak-to-Peak		–0.1	—	0.1	dB
Stopband		—	4.4	—	kHz
Stopband Attenuation		–74	—	—	dB
Group Delay	t_{gd}	—	12/Fs	—	sec
Note: Typical FIR filter characteristics for Fs = 8000 Hz are shown in Figures 6, 7, 8, and 9.					

Table 12. Digital IIR Filter Characteristics—Transmit and Receive
(V_A = Charge Pump, V_D = +5 V ±5%, Sample Rate = 8 kHz, T_A = 0 to 70°C for K-Grade)

Parameter	Symbol	Min	Typ	Max	Unit
Passband (3 dB)	$F_{(3\ dB)}$	0	—	3.6	kHz
Passband Ripple Peak-to-Peak		–0.2	—	0.2	dB
Stopband		—	4.4	—	kHz
Stopband Attenuation		–40	—	—	dB
Group Delay	t_{gd}	—	1.6/Fs	—	sec
Note: Typical IIR filter characteristics for Fs = 8000 Hz are shown in Figures 10, 11, 12, and 13. Figures 14 and 15 show group delay versus input frequency.					

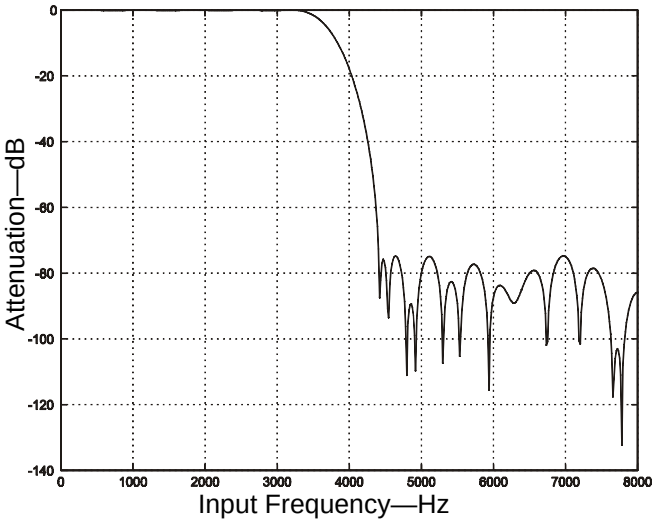


Figure 6. FIR Receive Filter Response

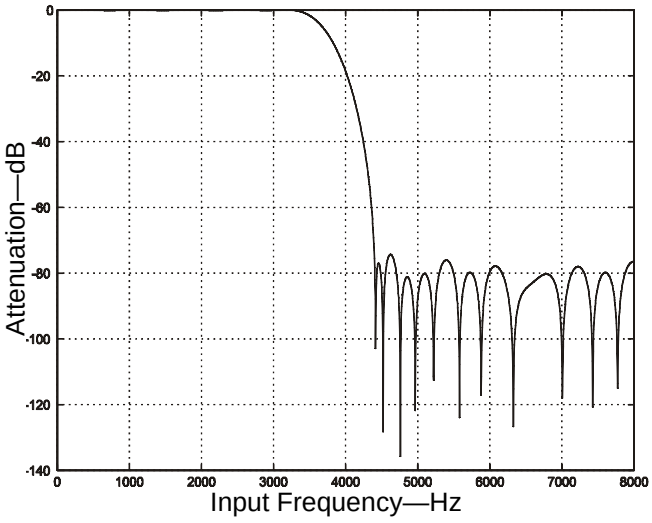


Figure 8. FIR Transmit Filter Response

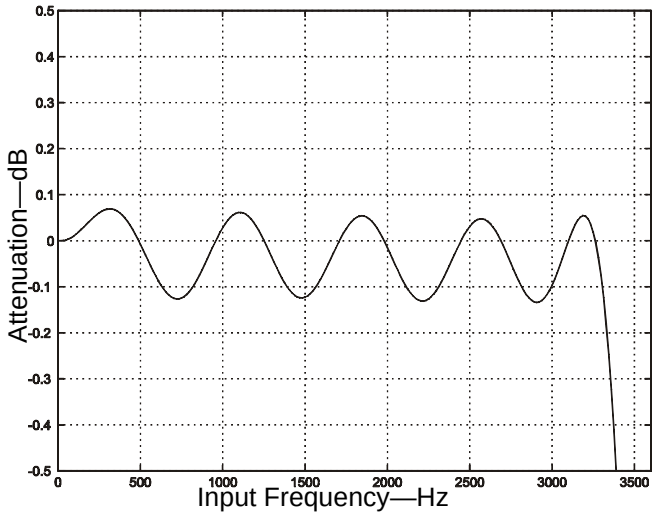


Figure 7. FIR Receive Filter Passband Ripple

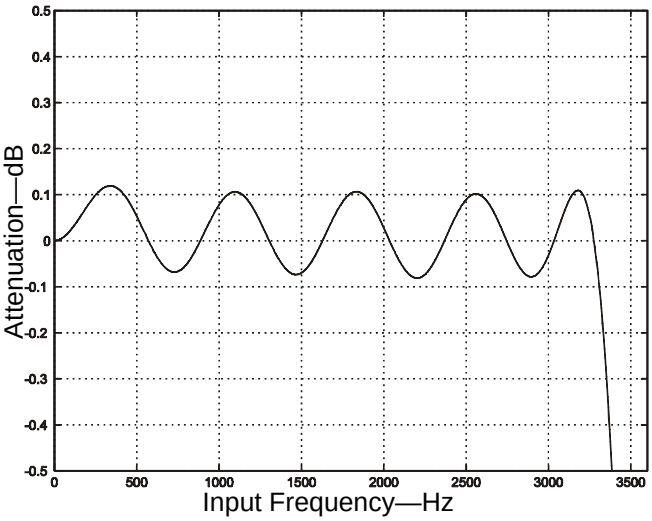


Figure 9. FIR Transmit Filter Passband Ripple

For Figures 6–9, all filter plots apply to a sample rate of Fs = 8 kHz. The filters scale with the sample rate as follows:

$$F_{(0.1\ dB)} = 0.4125\ Fs$$

$$F_{(-3\ dB)} = 0.45\ Fs$$

where Fs is the sample frequency.

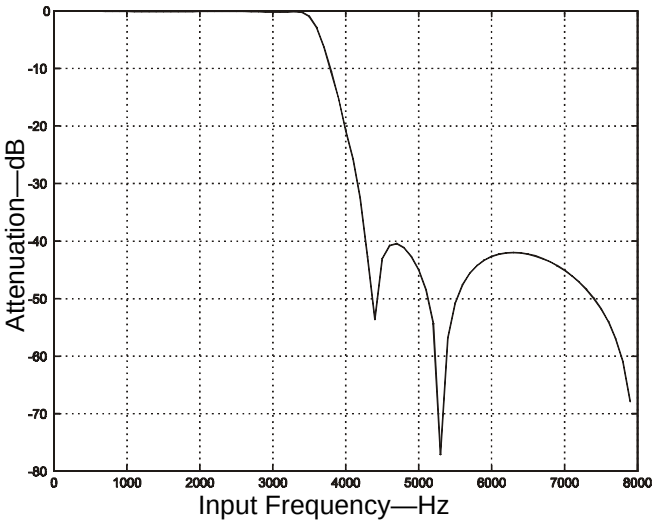


Figure 10. IIR Receive Filter Response

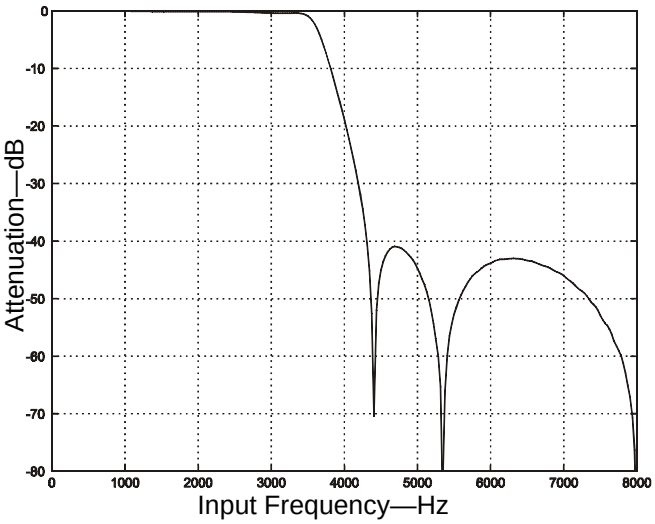


Figure 12. IIR Transmit Filter Response

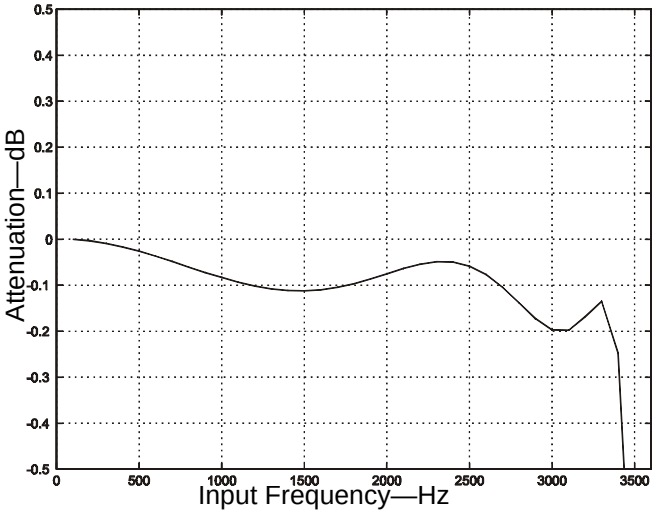


Figure 11. IIR Receive Filter Passband Ripple

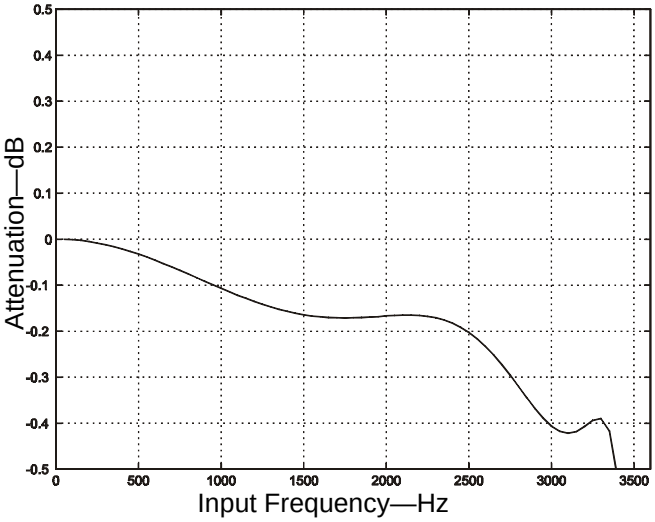


Figure 13. IIR Transmit Filter Passband Ripple

For Figures 10–13, all filter plots apply to a sample rate of Fs = 8 kHz. The filters scale with the sample rate as follows:

$$F_{(-3\ dB)} = 0.45\ Fs$$

where Fs is the sample frequency.

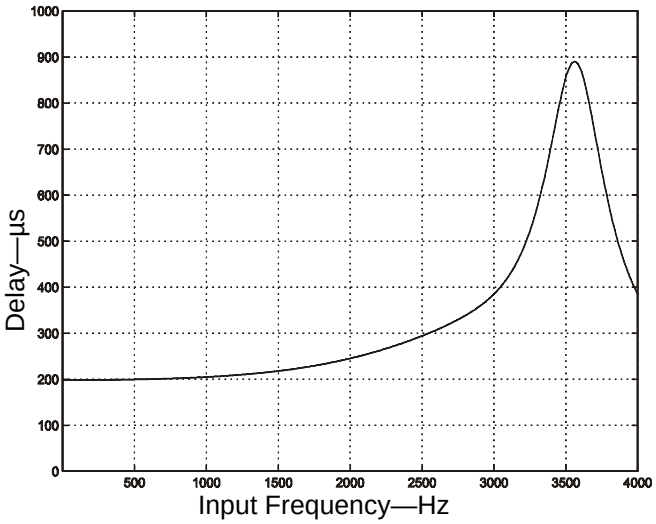


Figure 14. IIR Receive Group Delay

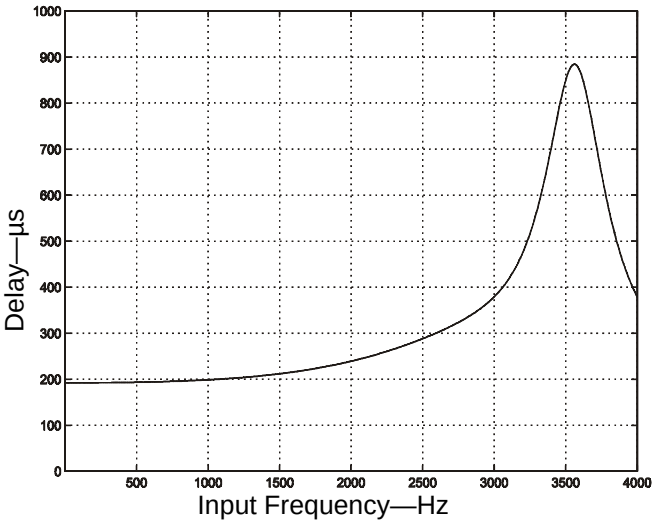
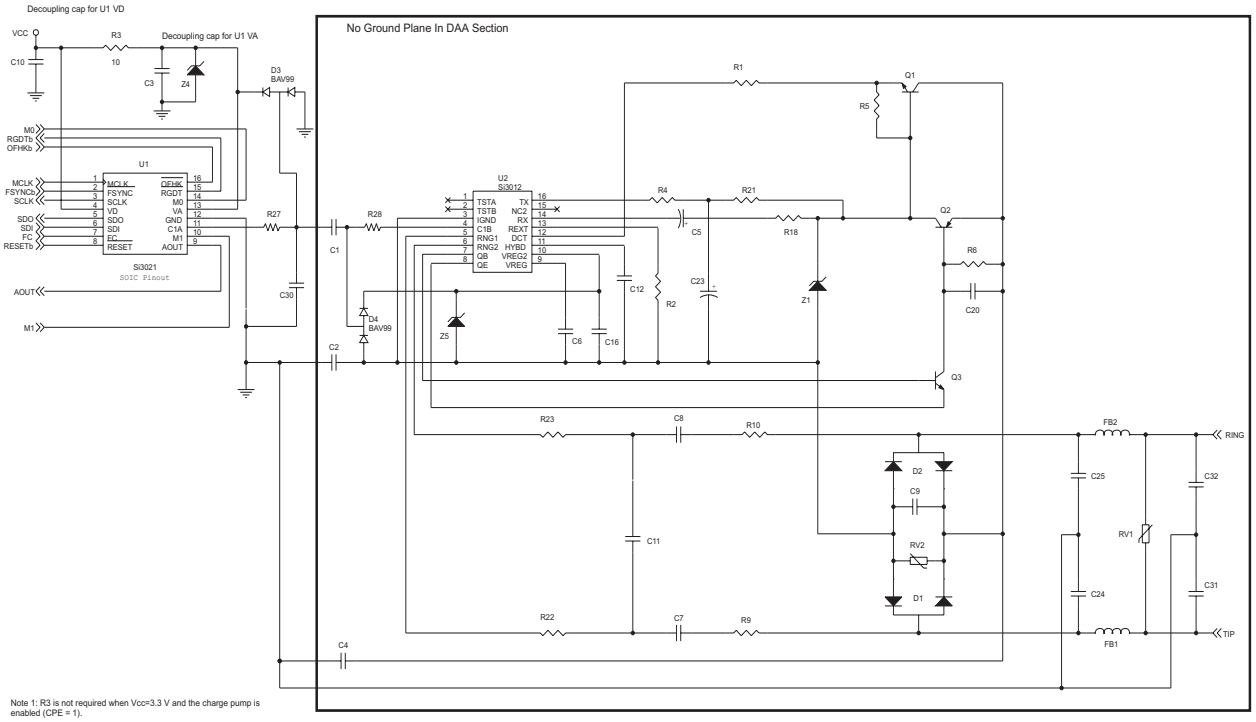


Figure 15. IIR Transmit Group Delay



Note 1: R3 is not required when Vcc=3.3 V and the charge pump is enabled (CPE = 1).

Note 2: If JATE support is not required, R21, C12 and C23 may be removed (R21 is effectively 0 ohms) and R4 should be changed to a 604 ohm, 1/4 W, +- 1%.

Note 3: See Appendix for applications requiring UL 1950 3rd Edition compliance.

Figure 16. Typical Application Schematic

Bill of Materials

Table 13. Component Values—Typical Application

Component[1]	Value	Supplier(s)
C1,C4	150 pF, 3 kV, X7R, ±20%	Novacap, Venkel, Johanson, Murata, Panasonic, SMEC
C2	Not Installed	
C3	0.22 µF, 16 V, X7R, ±20%	
C5	1 µF, 16 V, Tant/Elec, ±20%	
C6,C10,C16	0.1 µF, 16 V, X7R, ±20%	
C7,C8,C9	15 nF, 250 V, X7R, ±20%	Novacap, Johanson, Murata, Panasonic, SMEC
C11	39 nF, 16 V, X7R, ±20%	
C12[2]	2.7 nF, 16 V, X7R, ±20%	
C23[2]	0.1 µF, 16 V, Tant/Elec/X7R, ±20%	
C24, C25, C31,C32[3]	1000 pF, 3 kV, X7R, ±10%	Novacap, Venkel, Johanson, Murata, Panasonic, SMEC
C30[4]	Not Installed	
D1,D2[5]	Dual Diode, 300 V, 225 mA	Central Semiconductor
D3,D4	BAV99 Dual Diode, 70 V, 350 mW	Diodes, Inc., OnSemiconductor, Fairchild
FB1,FB2	Ferrite Bead	Murata
Q1,Q3	A42, NPN, 300 V	OnSemiconductor, Fairchild
Q2	A92, NPN, 300 V	OnSemiconductor, Fairchild
RV1	Sidactor, 275 V, 100 A	Teccor, ST Microelectronics, Microsemi, TI
RV2	MOV, 240 V	Panasonic
R1	51 Ω, 1/2 W ±5%	
R2	15 Ω, 1/4 W ±5%	
R3[6]	Not Installed	
R4[2],R18,R21[2]	301 Ω, 1/10 W, ±1%	
R5,R6	36 kΩ, 1/10 W ±5%	
R9,R10	2 kΩ, 1/10 W ±5%	
R22,R23	20 kΩ, 1/10 W ±5%	
R27,R28	10 Ω, 1/10 W ±5%	
U1	Si3021	Silicon Labs
U2	Si3012	Silicon Labs
Z1	Zener diode, 18 V	Vishay, Rohm, OnSemiconductor
Z4,Z5	Zener diode, 5.6 V, 1/2 W	Diodes, Inc., OnSemiconductor, Fairchild

Notes:

1. The following reference designators were intentionally omitted: C13–C15, C17–C22, C26–C29, R7, R8, R11–R17, R19, and R20.
2. If JATE support is not required, C12, and C23 may be removed.
3. Alternate population option is C24, C25 (2200 pF, 3 kV, X7R, ±10% and C31, C32 not installed).
4. Install only if needed for improved radiated emissions performance (10 pF, 16 V, NPO, ±10%).
5. Several diode bridge configurations are acceptable (suppliers include General Semi, Diodes Inc.)
6. If the charge pump is not enabled (with the CPE bit in Register 6), V_A must be 4.75 to 5.25 V. R3 can be installed with a 10 Ω, 1/10 W, ±5% if V_D is also 4.75 to 5.25 V.

Analog Output

Figure 17 illustrates an optional application circuit to support the analog output capability of the Si3035 for call progress monitoring purposes. The ARM bits in Register 6 allow the receive path to be attenuated by 0 dB, –6 dB, or –12 dB. The ATM bits, which are also in Register 6, allow the transmit path to be attenuated by –20 dB, –26 dB, or –32 dB. Both the transmit and receive paths can also be independently muted.

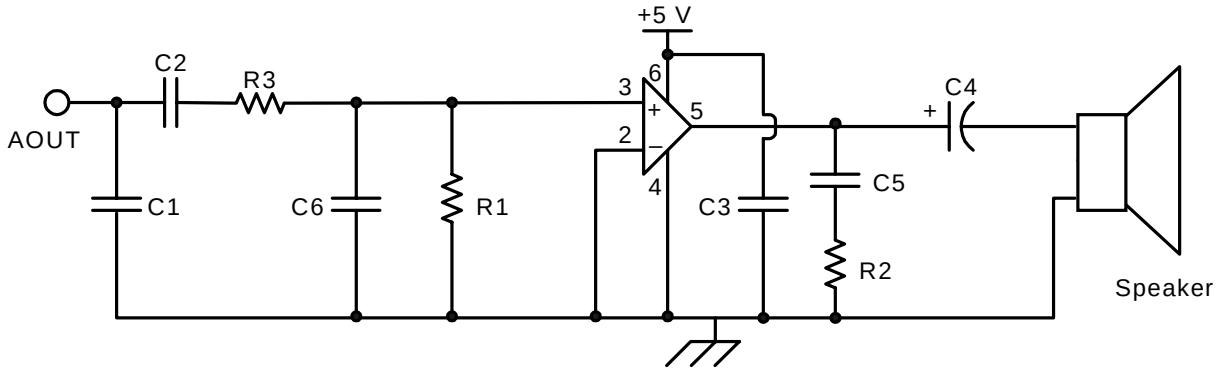


Figure 17. Optional Connection to AOUT for a Call Progress Speaker

Table 14. Component Values—Optional Connection to AOUT

Symbol	Value
C1	2200 pF, 16 V, ±20%
C2, C3, C5	0.1 µF, 16 V, ±20%
C4	100 µF, 16 V, Elec. ±20%
C6	820 pF, 16 V, ±20%
R1	3 kΩ, 1/10 W, ±5%
R2	10 Ω, 1/10 W, ±5%
R3	47 kΩ, 1/10 W, ±5%
U1	LM386

Functional Description

The Si3035 is an integrated chipset that provides a low-cost, isolated, silicon-based interface to the telephone line. The Si3035 saves cost and board area by eliminating the need for a modem AFE or serial codec. It also eliminates the need for an isolation transformer, relays, opto-isolators, and a 2- to 4-wire hybrid. The Si3035 solution requires only a few low-cost, discrete components to achieve full compliance with FCC Part 68 and JATE out-of-band noise requirements. See Figure 16 on page 15 for a typical application circuit. See the pin-compatible Si3034 or Si3044 data sheets for designs requiring global support.

The Si3035 North America/Japan DAA offers a number of new features not supported by the Si3032 device. These include operation from a single 3.3 V power supply, JATE (Japan) filter option, finer resolution for both transmit and receive levels on AOUT (call progress output), daisy-chaining for up to eight devices, and an optional IIR filter. Table 15 summarizes the new Si3035 features.

Table 15. New Si3035 Features

Category	Si3032	Si3035
Daisy-Chaining	—	Up to 8 Devices
Optional IIR Filter	—	Yes
Receive Gain	0, 6 dB	0, 3, 6, 9, 12 dB
Transmit Attenuation	0, –3 dB	0, –3, –6 –9, –12 dB
V_A	5 V	3.3 V* or 5 V
V_D	3.3 V or 5 V	3.3 V or 5 V
JATE Support	—	Yes
AOUT Levels (dB)	0, mute	0, –6, –12, mute
***Note:** The V_A supply is internally generated by an on-chip charge pump.		

Initialization

When the Si3035 is initially powered up, the $\overline{\text{RESET}}$ pin should be asserted. When the $\overline{\text{RESET}}$ pin is deasserted, the registers will have default values. This reset condition guarantees the line-side chip (Si3012) is powered down with no possibility of loading the line (i.e., off-hook). The following is an example initialization procedure:

1. Program the PLLs with registers 7 to 9 (N1[7:0], M1[7:0], N2[3:0] and M2[3:0]) to the appropriate divider ratios for the supplied MCLK frequency and desired sample rate, as defined in "Clock Generation Subsystem" on page 20.
2. Wait until the PLLs are locked. This time is between 100 µS and 1 ms.
3. Write an 0x80 into Register 6. This enables the charge pump for the V_A pin, powers up the line-side chip (Si3012), and enables the AOUT for call progress monitoring.

After this procedure is complete, the Si3035 is ready for ring detection and off-hook.

Isolation Barrier

The Si3035 achieves an isolation barrier through a low-cost, high-voltage capacitor in conjunction with Silicon Laboratories' proprietary ISOcap signal processing techniques. These techniques eliminate any signal degradation due to capacitor mismatches, common mode interference, or noise coupling. As shown in Figure 16 on page 15, the C1, C2, and C4 capacitors isolate the Si3021 (DSP-side) from the Si3012 (line-side). All transmit, receive, control, and caller ID data are communicated through this barrier.

The ISOcap inter-chip communication is disabled by default. To enable it, the PDL bit in Register 6 must be cleared. No communication between the Si3021 and Si3012 can occur until this bit is cleared. The clock generator *must* be programmed to an acceptable sample rate prior to clearing the PDL bit.

Off-Hook

The communication system generates an off-hook command by applying logic 0 to the $\overline{\text{OFHK}}$ pin or writing a logic 1 to bit 0 of control Register 5. The $\overline{\text{OFHK}}$ pin must be enabled by setting bit 1 (OHE) of Register 5. With $\overline{\text{OFHK}}$ at logic 0, the system is in an off-hook state. This state is used to seize the line for incoming/outgoing calls and can also be used for pulse dialing. With $\overline{\text{OFHK}}$ at logic 1, negligible DC current flows through the hookswitch. When a logic 0 is applied to the $\overline{\text{OFHK}}$ pin, the hookswitch transistor pair, Q1 and Q2, turn on. The net effect of the off-hook signal is the application of a termination impedance across TIP and RING and the flow of DC loop current. The termination impedance has both an AC and a DC component.

The AC termination impedance is a 604-Ω resistor, which is connected to the TX pin. The DC termination is a 51-Ω resistor, which is connected to the DCT pin.

When executing an off-hook sequence, the Si3035 requires 1548/Fs seconds to complete the off-hook and provide phone line data on the serial link. This includes the 12/Fs filter group delay. If necessary, for the shortest

delay, a higher Fs may be established prior to executing the off-hook, such as an Fs of 10.286 kHz. The delay allows line transients to settle prior to normal use.

Ring Detect

The ring signal enters the Si3035 through low value capacitors connected to TIP and RING. RGDT is a clipped, half-wave rectified version of the ringing waveform. See Figure 18 for a timing diagram of the RGDT pin.

The integrated ring detect of the Si3035 allows the device to present the ring signal to the DSP, through the serial port, with no additional signaling required. The signal sent to the DSP is a clipped version of the original ring signal. In addition, the Si3035 passes through the caller ID data unaltered.

The system can also detect an occurring ring by the status of the RDT bit of Register 5. This bit is a read-only bit that is set when the line-side device detects a ring signal at RNG1 and RNG2. The RDT bit clears when the system either goes off-hook or 4.5 to 9 seconds after the last ring is detected.

If caller ID is supported in the system, the designer can enable the Si3035 to pass this information to the SDO output. Following the completion of the first ring, the system should set the ONHM bit (Register 5, bit 3). This bit must be cleared at the conclusion of the receipt of the caller ID data and prior to the next ring burst.

The Si3021 can support a wake-up-on-ring function using the RGDT signal. Refer to "Power Management" on page 24 for more details

.

Improved JATE Support

The HYBD pin connects to a node on the internal hybrid cancellation circuit providing a pin for a balancing capacitor, C12. C23 adds the necessary transmit out-of-band filtering required to meet JATE out-of-band noise specifications. The addition of C23 alters the transmit path frequency response which must be balanced with capacitor C12 to obtain maximum hybrid cancellation.

Products using the Si3035 which have been submitted for JATE approval should document a waiver for the JATE DC Termination specification. This specification is met in the Si3034 global DAA device.

Digital Interface

The Si3035 has two serial interface modes that support most standard modem DSPs. The M0 and M1 mode pins select the interface mode. The key difference between these two serial modes is the operation of the FSYNC signal. Table 16 summarizes the serial mode definitions.

Table 16. Serial Modes

Mode	M1 M0	Description
0	0 0	FSYNC frames data
1	0 1	FSYNC pulse starts data frame
2	1 0	Slave mode
3	1 1	Reserved

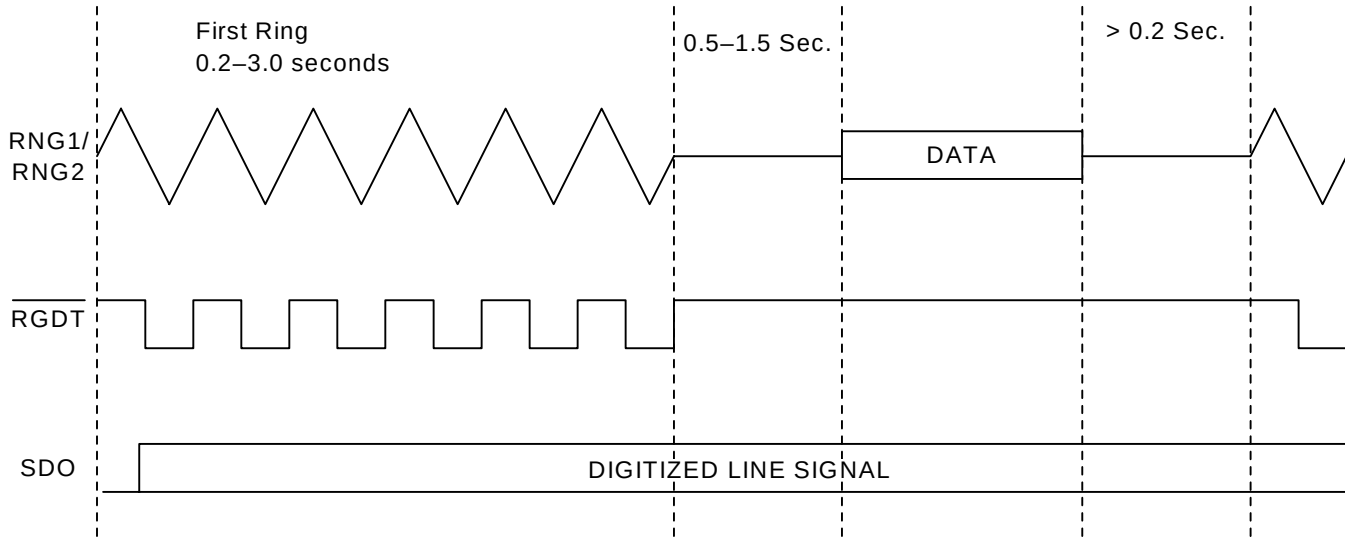


Figure 18. Ring Detect Timing

The digital interface consists of a single, synchronous serial link which communicates both telephony and control data.

In Serial mode 0 or 1, the Si3021 operates as a master, where the master clock (MCLK) is an input, the serial data clock (SCLK) is an output, and the frame sync signal (FSYNC) is an output. The MCLK frequency and the value of the sample rate control registers 7, 8, 9, and 10 determine the sample rate (Fs). The serial port clock, SCLK, runs at 256 bits per frame, where the frame rate is equivalent to the sample rate. Refer to "Clock Generation Subsystem" on page 20 for more details on programming sample rates.

The Si3035 transfers 16-bit or 15-bit telephony data in the primary timeslot and 16-bit control data in the secondary timeslot. Figure 19 and Figure 20 show the relative timing of the serial frames. Primary frames occur at the frame rate and are always present. To minimize overhead in the external DSP, secondary frames are present only when requested.

Two methods exist for transferring control information in the secondary frame. The default power-up mode uses the LSB of the 16-bit transmit (TX) data word as a flag to request a secondary transfer. In this mode, only 15-bit TX data is transferred, resulting in a loss of SNR but allowing software control of the secondary frames. As an alternative method, the FC pin can serve as a hardware flag for requesting a secondary frame. The external DSP can turn on the 16-bit TX mode by setting the SB bit of Register 1. In the 16-bit TX mode, the hardware FC pin must be used to request secondary transfers.

Figure 21 and Figure 22 illustrate the secondary frame read cycle and write cycle, respectively. During a read cycle, the R/W bit is high and the 5-bit address field contains the address of the register to be read. The contents of the 8-bit control register are placed on the SDO signal. During a write cycle, the R/W bit is low and the 5-bit address field contains the address of the register to be written. The 8-bit data to be written immediately follows the address on SDI. Only one register can be read or written during each secondary frame. See "Control Registers" on page 34 for the register addresses and functions.

In serial mode 2, the Si3021 operates as a slave device, where the MCLK is an input, the SCLK is a no connect (except for the master device for which it is an output), and the FSYNC is an input. In addition, the RGDT/FSD pin operates as a delayed frame sync (FSD) and the FC/RGDT pin operates as ring detect (RGDT). In this mode, FC operation is not supported. For further details on operating the Si3021 as a slave device, refer to "Multiple Device Support" on page 25.

Clock Generation Subsystem

The Si3035 contains an on-chip clock generator. Using a single MCLK input frequency, the Si3035 can generate all the desired standard modem sample rates, as well as the common 11.025 kHz rate for audio playback.

The clock generator consists of two PLLs (PLL1 and PLL2) that achieve the desired sample frequencies. Figure 23 on page 22 illustrates the clock generator.

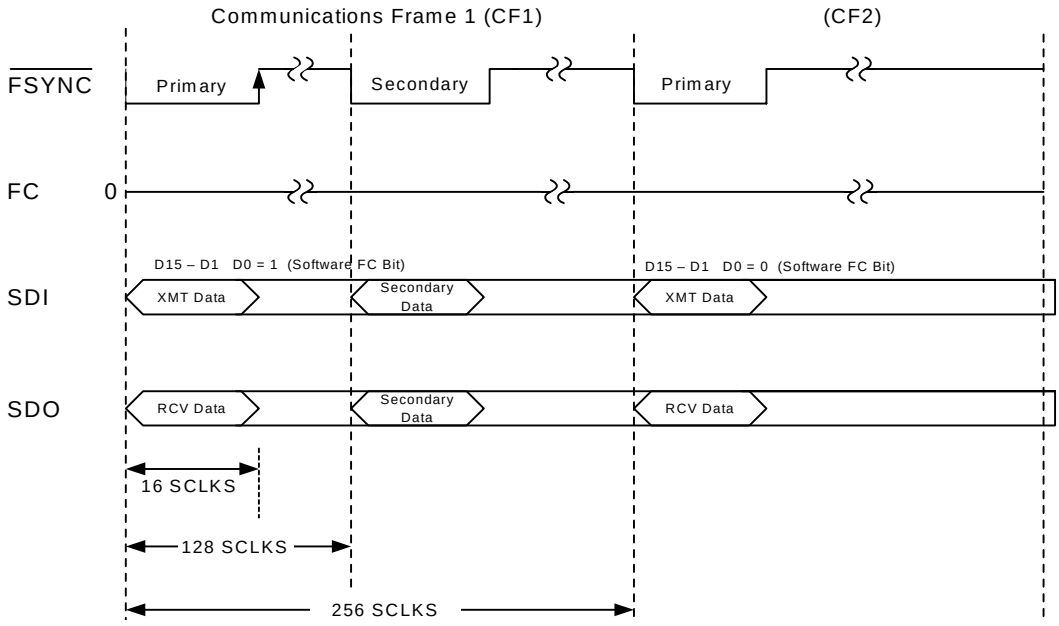


Figure 19. Software FC Secondary Request

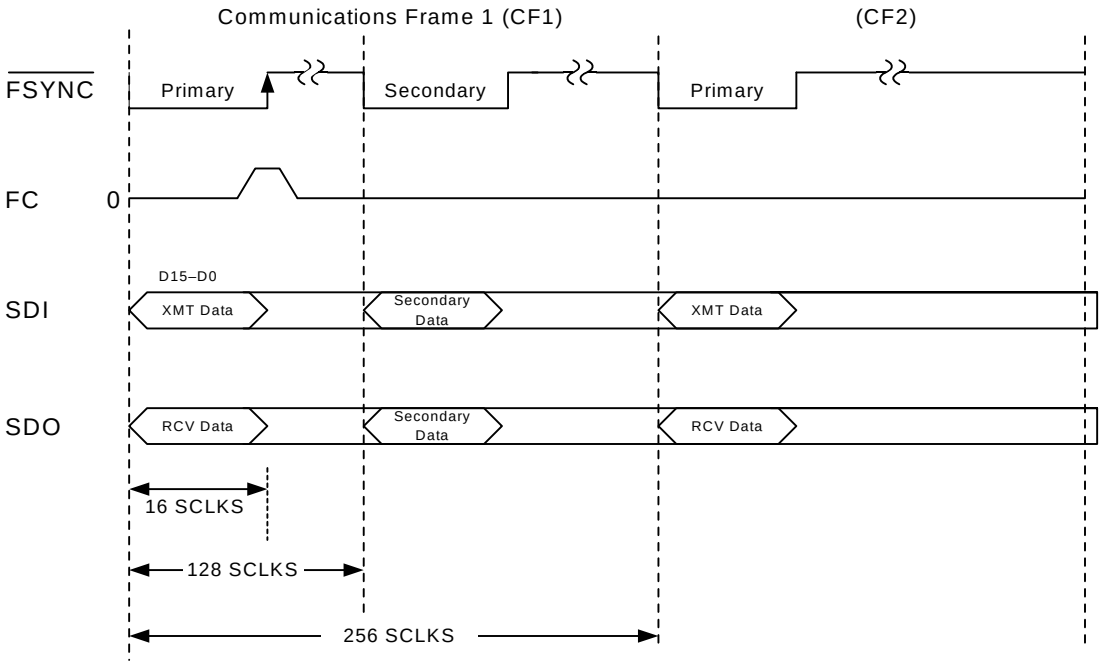


Figure 20. Hardware FC Secondary Request

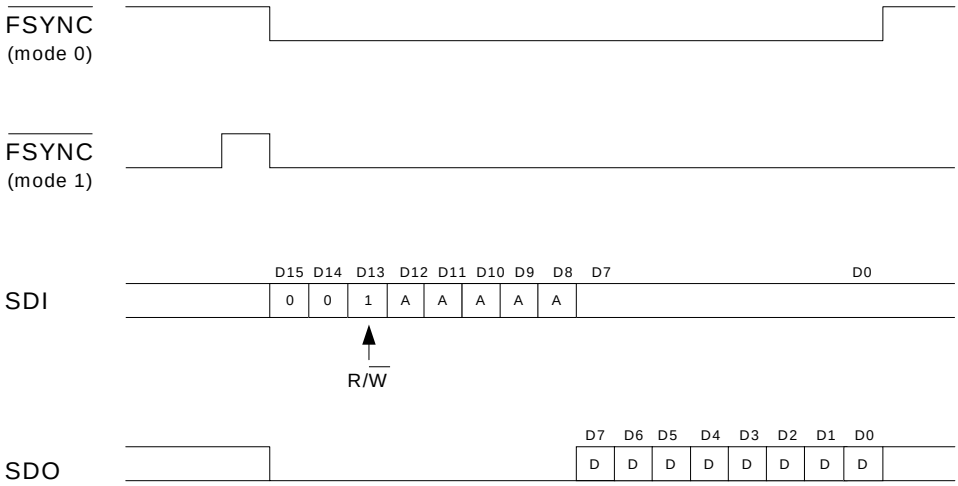


Figure 21. Secondary Communication Data Format—Read Cycle

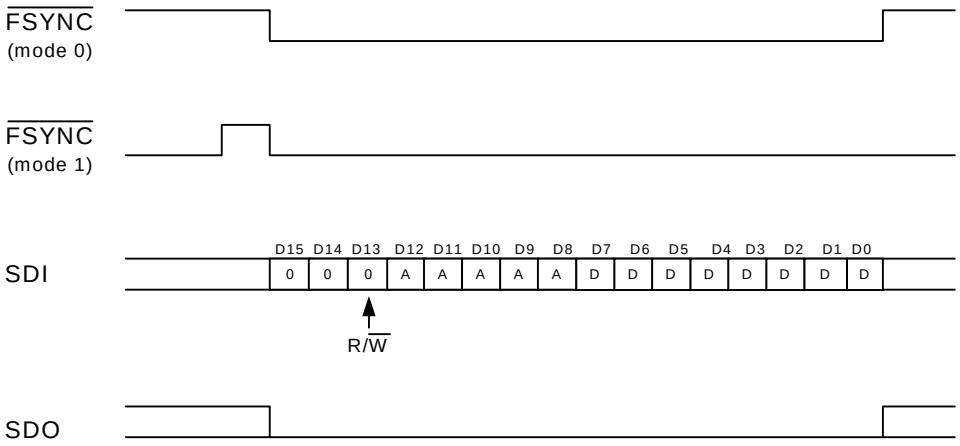


Figure 22. Secondary Communication Data Format—Write Cycle

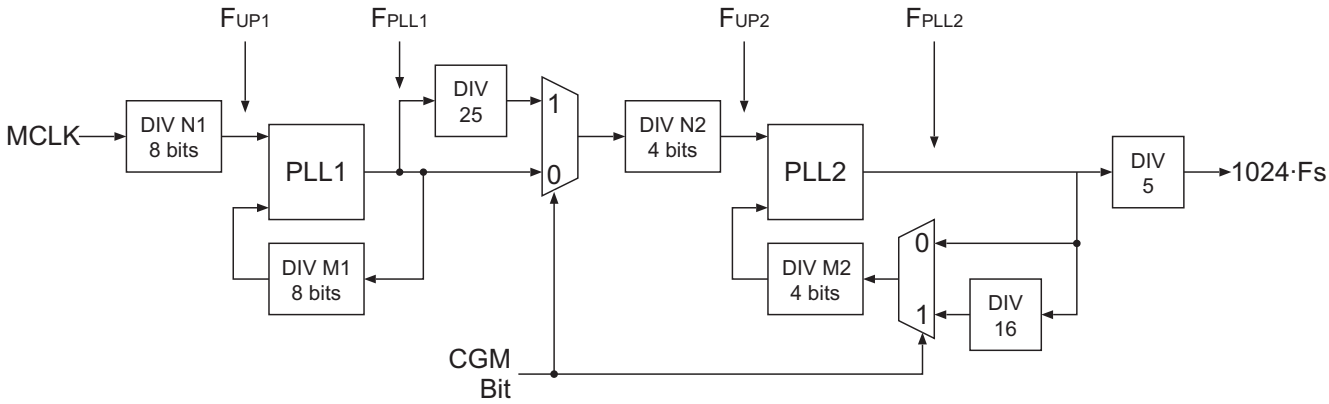


Figure 23. Clock Generation Subsystem

The architecture of the dual PLL scheme allows for fast lock time on initial start-up, fast lock time when changing modem sample rates, high noise immunity, and the ability to change modem sample rates with a single register write. A large number of MCLK frequencies between 1 MHz and 60 MHz are supported. MCLK should be from a clean source, preferably directly from a crystal with a constant frequency and no dropped pulses.

In serial mode 2, the Si3021 operates as a slave device. The clock generator is configured (by default) to set the SCLK output equal to the MCLK input. The net effect is the clock generator multiplies the MCLK input by 20. For further details of slave mode operation, refer to "Multiple Device Support" on page 25.

Programming the Clock Generator

As noted in Figure 23, the clock generator must output a clock equal to 1024 • Fs, where Fs is the desired sample rate. The 1024 • Fs clock is determined through programming of the following registers:

- Register 7—N1 divider, 8 bits.
- Register 8—M1 divider, 8 bits.
- Register 9—N2/M2 dividers, 4 bits/4 bits.
- Register 10—CGM, 1 bit.

When using the Si3035 for modem applications, the clock generator can be programmed to allow for a single register write to change the modem sampling rate. These standard sample rates are shown in Table 17. The programming method is described below.

Table 17. N2, M2 Values (CGM = 0, 1)

Fs (Hz)	N2	M2
7200	2	2
8000	9	10
8229	7	8
8400	6	7
9000	4	5
9600	3	4
10286	7	10

The main design consideration is the generation of a base frequency, defined as the following:

$$F_{Base} = \frac{F_{MCLK} \cdot M1}{N1} = 36.864MHz, CGM = 0$$

$$F_{Base} = \frac{F_{MCLK} \cdot M1 \cdot 16}{N1 \cdot 25} = 36.864MHz, CGM = 1$$

N1 (Register 7) and M1 (Register 8) are 8-bit unsigned values. F_{MCLK} is the clock provided to the MCLK pin. Table 18 lists several standard crystal oscillator rates that could be supplied to MCLK. This list simply represents a sample of MCLK frequency choices. Many more are possible.

After the first PLL has been setup, the second PLL can be programmed easily. The values for N2 and M2 (Register 9) are shown in Table 17. N2 and M2 are 4-bit unsigned values.

When programming the registers of the clock generator, the order of register writes is important. For PLL1 updates, N1 (Register 7) must always be written first, immediately followed by a write to M1 (Register 8). For PLL2, the CGM bit must be set as desired prior to writing N2/M2 (Register 9). Changes to the CGM bit only take effect when N2/M2 are written.

Note: The values shown in Table 17 and Table 18 satisfy the equations above. However, when programming the registers for N1, M1, N2, and M2, the value placed in these registers must be one less than the value calculated from the equations. For example, for CGM = 0 with a MCLK of 48.0 MHz, the values placed in the N1 and M1 registers would be 0x7C and 0x5F, respectively. If CGM = 1, a non-zero value must be programmed to Register 9 in order for the 16/25 ratio to take effect.

Table 18. MCLK Examples

MCLK (MHz)	N1	M1	CGM
1.8432	1	20	0
4.0000	5	72	1
4.0960	1	9	0
5.0688	11	80	0
6.0000	5	48	1
6.1440	1	6	0
8.1920	32	225	1
9.2160	1	4	0
10.0000	25	144	1
10.3680	9	32	0
11.0592	3	10	0
12.288	1	3	0
14.7456	2	5	0
16.0000	5	18	1
18.4320	1	2	0
24.5760	32	75	1
25.8048	7	10	0
33.8688	147	160	0
44.2368	96	125	1
46.0800	5	4	0
47.9232	13	10	0
48.0000	125	96	0
56.0000	35	36	1
60.0000	25	24	1

PLL Lock Times

The Si3035 changes sample rates very quickly. However, lock time will vary based on the programming of the clock generator. The major factor contributing to PLL lock time is the CGM bit. When the CGM bit is used (set to 1), PLL2 will lock slower than when CGM is 0. The following relationships describe the boundaries on PLL locking time:

PLL1 lock time < 1 ms (CGM = 0,1)

PLL2 lock time: 100 us to 1 ms (CGM = 0)

PLL2 lock time <1 ms (CGM = 1)

For modem designs, it is recommended that PLL1 be programmed during initialization. No further programming of PLL1 is necessary. The CGM bit and PLL2 can be programmed for the desired initial sample

rate, typically 7200 Hz. All further sample rate changes are then made by simply writing to Register 9 to update PLL2.

The final design consideration for the clock generator is the update rate of PLL1. The following criteria must be satisfied in order for the PLLs to remain stable:

$$F_{UP1} = \frac{F_{MCLK}}{N1} \geq 144 \text{ kHz}$$

Where F_{UP1} is shown in Figure 23 on page 22.

Setting Generic Sample Rates

The above clock generation description focuses on the common modem sample rates. An application may require a sample rate not listed in Table 17, such as the common audio rate of 11.025 kHz. The restrictions and equations above still apply; however, a more generic relationship between MCLK and Fs (the desired sample rate) is needed. The following equation describes this relationship:

$$\frac{M1 \cdot M2}{N1 \cdot N2} = ratio \cdot \frac{5 \cdot 1024 \cdot Fs}{MCLK}$$

where Fs is the sample frequency, ratio is 1 for CGM = 0 and 25/16 for CGM = 1, and all other symbols are shown in Figure 23 on page 22.

By knowing the MCLK frequency and desired sample rate, the values for the M1, N1, M2, N2 registers can be determined. When determining these values, remember to consider the range for each register as well as the minimum update rate for the first PLL.

The values determined for M1, N1, M2, and N2 must be adjusted by minus one when determining the value written to the respective registers. This is due to internal logic, which adds one to the value stored in the register. This addition allows the user to write a zero value in any of the registers and the effective divide by is one. A special case occurs when both M1 and N1 and/or M2 and N2 are programmed with a zero value. When Mx and Nx are both zero, the corresponding PLLx is bypassed. Note that if M2 and N2 are set to zero, the ratio of 25/16 is eliminated and cannot be used in the above equation. In this condition the CGM bit has no effect.

Power Management

The Si3035 supports four basic power management operation modes: normal operation, reset operation, sleep, and full power down. The power management modes are controlled by the PDN and PDL bits of Register 6.

On power up, or following a reset, the Si3035 is in reset operation. In this mode, the PDL bit is set, while the PDN bit is cleared. The Si3021 is fully operational, except for the ISOcap link. No communication between the Si3021 and Si3012 can occur during reset operation. Any bits associated with the Si3012 are not valid in this mode.

The most common mode of operation is the normal operation. In this mode, the PDL and PDN bits are cleared. The Si3021 is fully operational and the ISOcap link is passing information between the Si3021 and the Si3012. The clock generator must be programmed to a valid sample rate prior to entering this mode.

The Si3035 supports a low-power sleep mode. This mode supports the popular wake-up-on-ring feature of many modems. The clock generator registers 7, 8, and 9 must be programmed with valid non-zero values prior to enabling sleep mode. Then, the PDN bit must be set and the PDL bit cleared. When the Si3035 is in sleep mode, the MCLK signal may be stopped or remain active, but it *must* be active before waking up the Si3035. The Si3021 is non-functional except for the ISOcap and $\overline{\text{RGDT}}$ signal. To take the Si3035 out of sleep mode, pulse the reset pin ($\overline{\text{RESET}}$) low.

In summary, the power down/up sequence for sleep mode is as follows:

1. Registers 7, 8, and 9 must have valid non-zero values.
2. Set the PDN bit (Register 6, bit 3) and clear the PDL bit (Register 6, bit 4).
3. MCLK may stay active or stop.
4. Restore MCLK before initiating the power-up sequence.
5. Reset the Si3035 using $\overline{\text{RESET}}$ pin (after MCLK is present).
6. Program registers to desired settings.

The Si3035 also supports an additional power-down mode. When both the PDN (Register 6, bit 3) and PDL (Register 6, bit 4) are set, the chipset enters a complete power-down mode and draws negligible current (deep sleep mode). PLL2 should be turned off prior to entering deep sleep mode (i.e., set Register 9 to 0 and then Register 6 to 0x18). In this mode, the $\overline{\text{RGDT}}$ pin does not function. Normal operation may be restored using the same process for taking the chipset out of sleep mode.

Analog Output

The Si3035 supports an analog output (AOUT) for driving the call progress speaker found with most of today's modems. AOUT is an analog signal that is comprised of a mix of the transmit and receive signals. The receive portion of this mixed signal has a 0 dB gain, while the transmit signal has a gain of –20 dB.

The AOUT level can be adjusted via the ATM and ARM bits in control Register 6. The transmit portion of the

AOUT signal can be set to –20 dB, –26 dB, –32 dB, or mute. The receive portion of the AOUT signal can be set to 0 dB, –6 dB, –12 dB, or mute. Figure 17 on page 17 illustrates a recommended application circuit. In the configuration shown, the LM386 provides a gain of 26 dB. Additional gain adjustments may be made by varying the voltage divider created by R1 and R3 of Figure 17.

On-Hook Line Monitor

The Si3035 allows the user to detect line activity when the device is in an on-hook state. When the system is on-hook, the line data can be passed to the DSP across the serial port while drawing a small amount of DC current from the line. This feature is similar to the passing of line information (such as caller ID), while on-hook, following a ring signal detection. To activate this feature, set the ONHM bit in Register 5.

The on-hook line monitor can also be used to detect whether a phone line is physically connected to the Si3012 and associated circuitry. When the on-hook line monitor is activated (if no line is connected), the output of SDO will move towards a negative full scale value (–32768). The value is guaranteed to be at least 89% of negative full scale.

If a line is present while in on-hook line monitor mode, SDO will have a near zero value. The designer must allow for the group delay of the receive filter (12/Fs) before making a decision.

Loop Current Monitor

When the system is in an off-hook state, the LCS bits of Register 12 indicate the approximate amount of DC loop current that is flowing in the loop. The LCS is a 4-bit value ranging from zero to fifteen. Each unit represents approximately 6 mA of loop current from LCS codes 1–14. The typical LCS transfer function is shown in Figure 24.

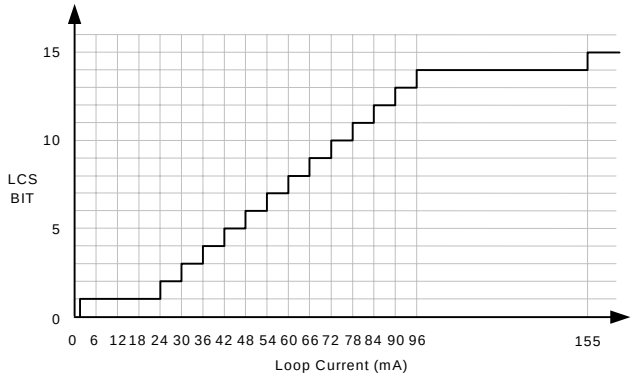


Figure 24. Typical LCS Transfer Function

An LCS value of zero means the loop current is less than required for normal operation and the system should be on-hook. Typically, an LCS value of 15 means the loop current is greater than 155 mA.

The LCS detector has a built-in hysteresis of 2 mA of current. This allows for a stable LCS value when the loop current is near a transition level. The LCS value is a rough approximation of the loop current, and the designer is advised to use this value in a relative means rather than an absolute value.

This feature enables the host processor to detect if an additional line has “picked up” while the modem is transferring information. In the case of a second phone going off-hook, the loop current falls approximately 50% and is reflected in the value of the LCS bits.

Multiple Device Support

The Si3035 supports the operation of up to seven additional devices on a single serial interface. Figure 25 on page 27 shows the typical connection of the Si3035 and one additional serial voice codec (Si3000).

The Si3035 must be the master in this configuration. The secondary codec should be configured as a slave device with SCLK and FSYNC as inputs. On power up, the Si3035 master will be unaware of the additional codec on the serial bus. The FC/RGDT pin is an input, operating as the hardware control for secondary frames. The RGDT/FSD pin is an output, operating as the active low ring detection signal. It is recommended that the master device be programmed for master/slave mode prior to enabling the ISOcap, because a ring signal would cause a false transition to the slave device’s FSYNC.

Register 14 provides the necessary control bits to configure the Si3035 for master/slave operation. Bit 0 (DCE) sets the Si3035 in master/slave mode, also referred to as daisy-chain mode. When the DCE bit is set, the FC/RGDT pin becomes the ring detect output and the RGDT/FSD pin becomes the frame sync delay output.

Bits 7:5 (NSLV2:NSLV0) set the number of slaves to be supported on the serial bus. For each slave, the Si3035 will generate a FSYNC to the DSP. In daisy-chain mode, the polarity of the ring signal can be controlled by bit 1 (RPOL). When RPOL = 1, the ring detect signal (now output on the FC/RGDT pin) is active high.

The Si3035 supports a variety of codecs (e.g., Si3000) as well as additional Si3035s. The type of slave codec(s) used is set by bits 4:3 (SSEL1:SSEL0). These bits determine the type of signalling used in the LSB of SDO. This assists the DSP in isolating which data stream is the master and which is the slave. If the LSB is used for

signalling, the master device will have a unique setting relative to the slave devices. The DSP can use this information to determine which FSYNC marks the beginning of a sequence of data transfers.

The delayed frame sync (FSD) of each device is supplied as the FSYNC of each subsequent slave device in the daisy chain. The master Si3035 will generate an FSYNC signal for each device every 16 or 32 SCLK periods. The delay period is set by Register 14, bit 2 (FSD). Figures 26–29 show the relative timing for daisy chaining operation. Primary communication frames occur in sequence, followed by secondary communication frames, if requested. When writing/reading the master device via a secondary frame, all secondary frames of the slave devices must be written as well. When writing/reading a slave device via a secondary frame, the secondary frames of the master and all other slaves must be written as well. "No operation" writes/reads to secondary frames are accomplished by writing/reading a zero value to address zero.

If FSD is set for 16 SCLK periods between FSYNCs, only serial mode 1 can be used. In addition, the slave devices must delay the tri-state to active transition of their SDO sufficiently from the rising edge of SCLK to avoid bus contention.

The Si3035 supports the operation of up to eight Si3035 devices on a single serial bus. The master Si3035 must be configured in serial mode 1. The slave(s) Si3035 is configured in serial mode 2. Figure 30 shows a typical master/slave connection using three Si3035 devices.

When in serial mode 2, FSYNC becomes an input, RGDT/FSD becomes the delay frame sync output, and FC/RGDT becomes the ring detection output. In addition, the internal PLLs are fixed to a multiply by 20. This provides the desired sample rate when the master's SCLK is provided to the slave's MCLK. The SCLK of the slave is a no connect in this configuration. The delay between FSYNC input and delayed frame sync output (RGDT/FSD) will be 16 SCLK periods. The RGDT/FSD output has a waveform identical to the FSYNC signal in serial mode 0. In addition, the LSB of SDO is set to zero by default for all devices in serial mode 2.

Gain Control

The Si3035 supports multiple gain and attenuation settings for the receive and transmit paths, respectively, via Register 13. When the ARX bit is set, 6 dB of gain is applied to the receive path. When the ATX bit is set, –3 dB of gain is applied to the transmit path.

Register 15 can be used to provide additional gain control. For Register 15 to have an effect on the receive and transmit paths, the ATX and ARX bits of Register 13 must be 0.

The receive path can support gains of 0, 3, 6, 9, and 12 dB. The gain is selected by bits 2:0 (ARX2:ARX0). The receive path can also be muted by setting bit 3 (RXM). The transmit path can support attenuations of 0, 3, 6, 9, and 12 dB. The attenuation is selected by bits 6:4 (ATX2:ATX0). The transmit path can also be muted by setting bit 7 (TXM).

Filter Selection

The Si3035 supports additional filter selections for the receive and transmit signals. When set, the IIRE bit of Register 16 enables the IIR filters defined in Table 12 on page 11. This filter provides a much lower, however non-linear, group delay than the default FIR filters.

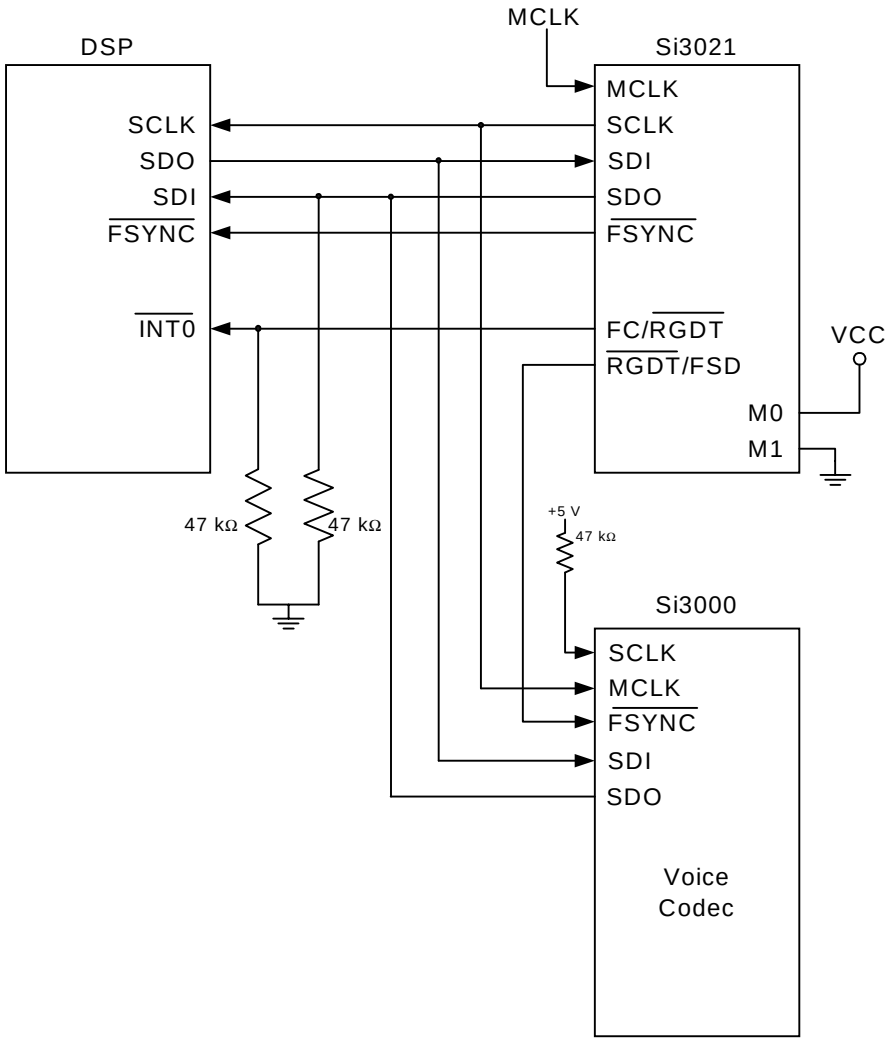


Figure 25. Typical Connection for Master/Slave Operation (e.g., Data/Fax/Voice Modem)

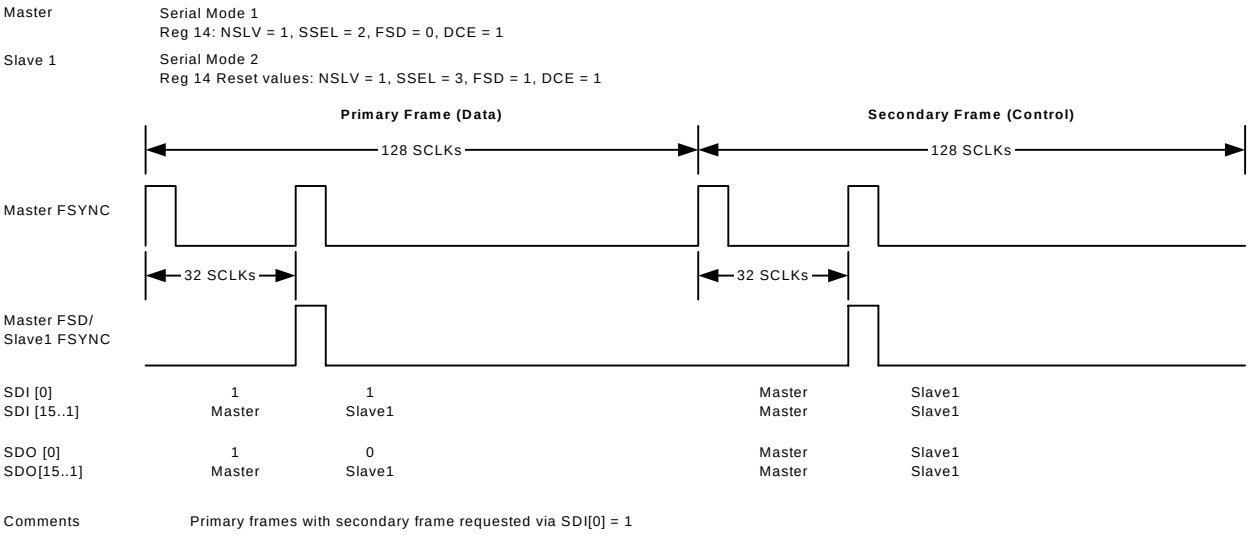


Figure 26. Daisy Chaining of a Single Slave (Pulse FSD)

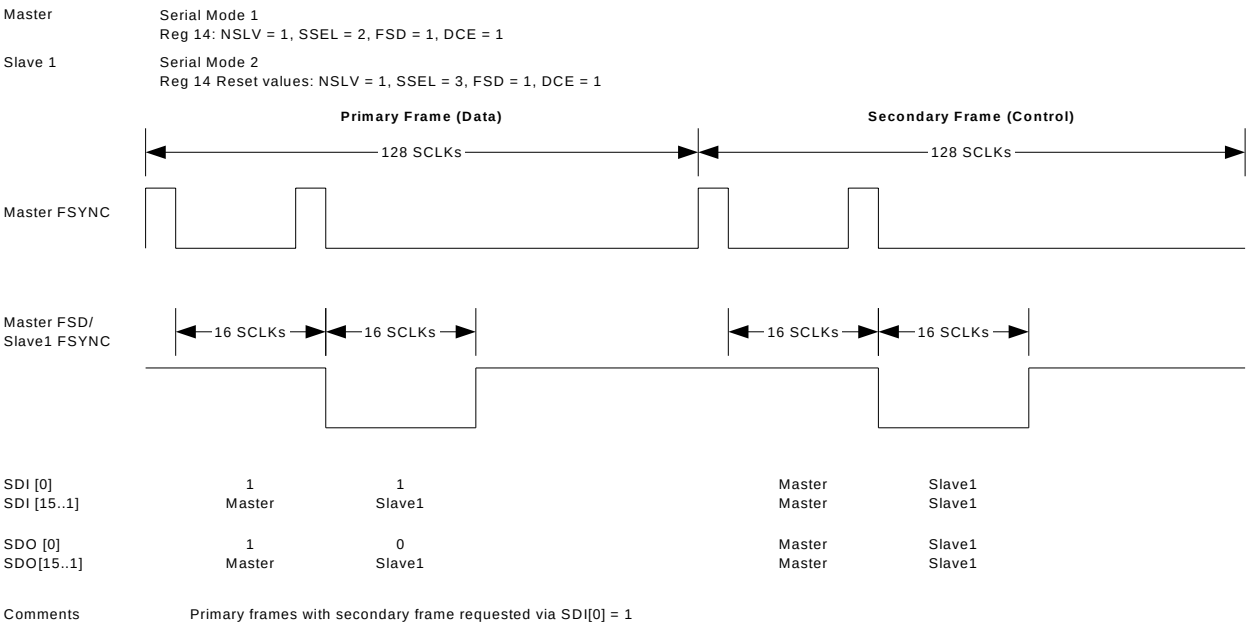


Figure 27. Daisy Chaining of a Single Slave (Frame FSD)

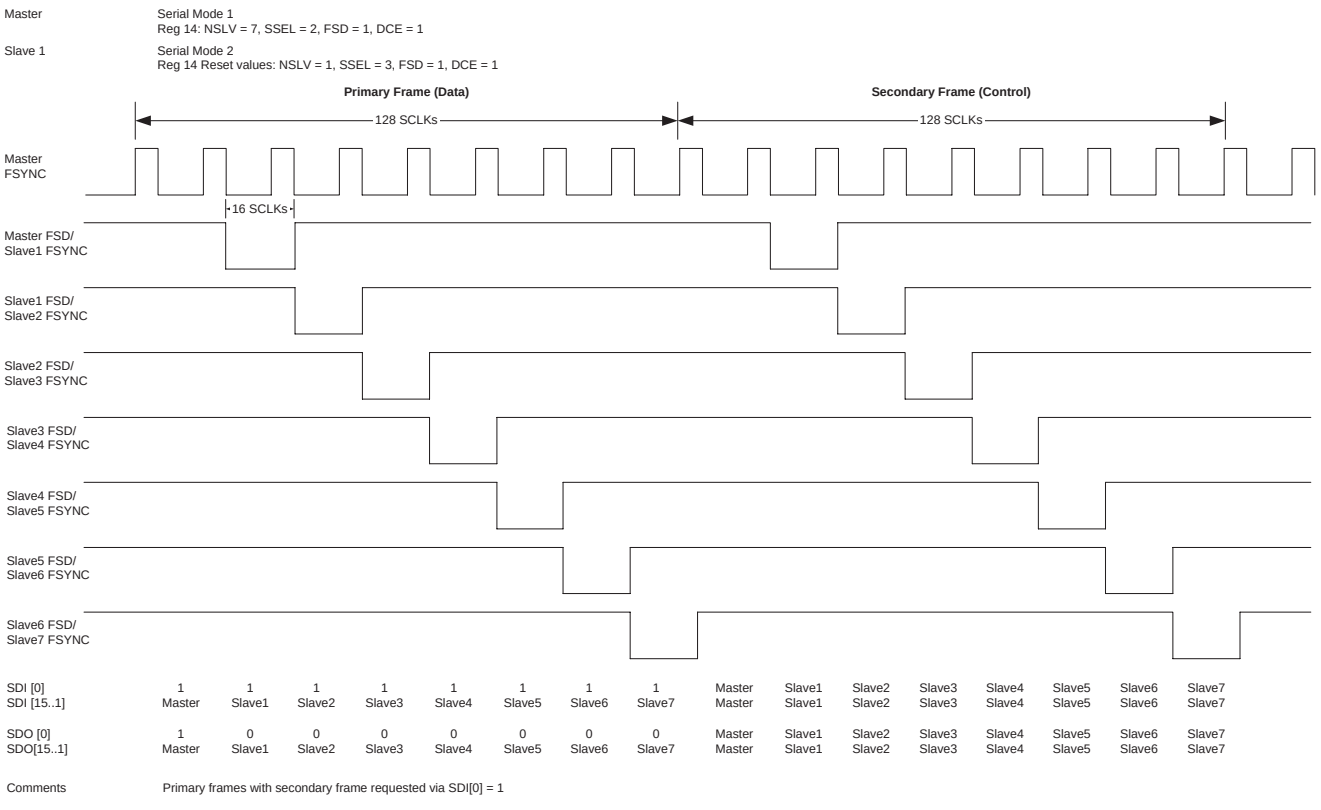


Figure 28. Daisy Chaining of Eight DAAs

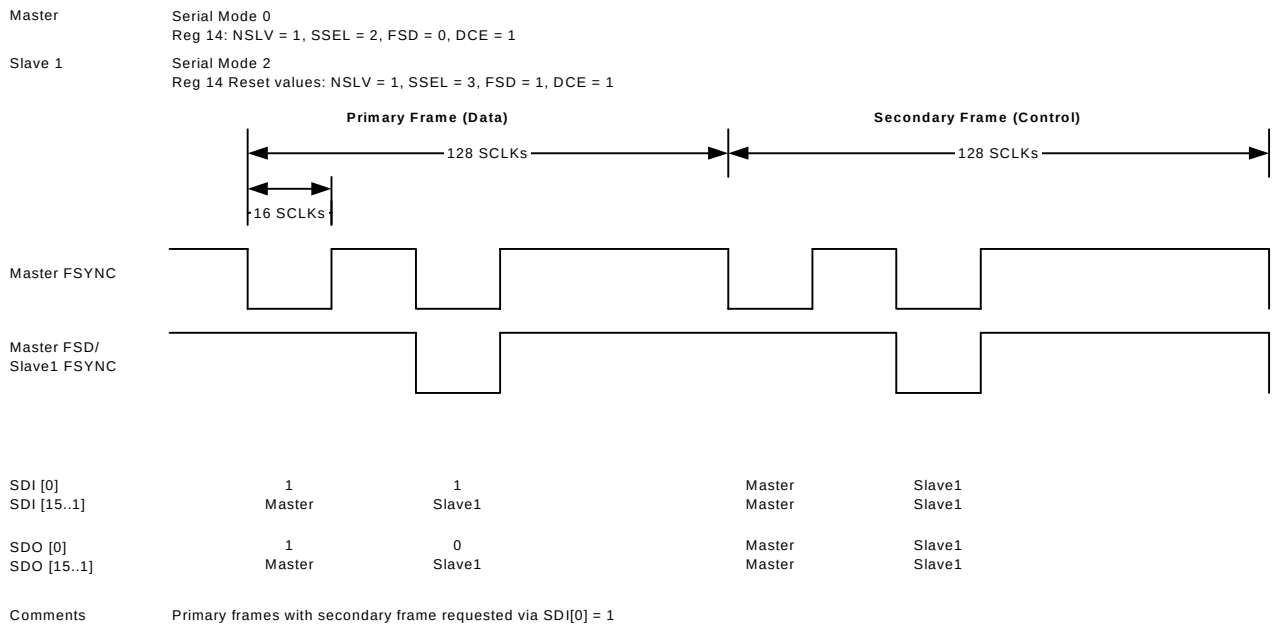


Figure 29. Daisy Chaining with Framed FSYNC and Framed FSD

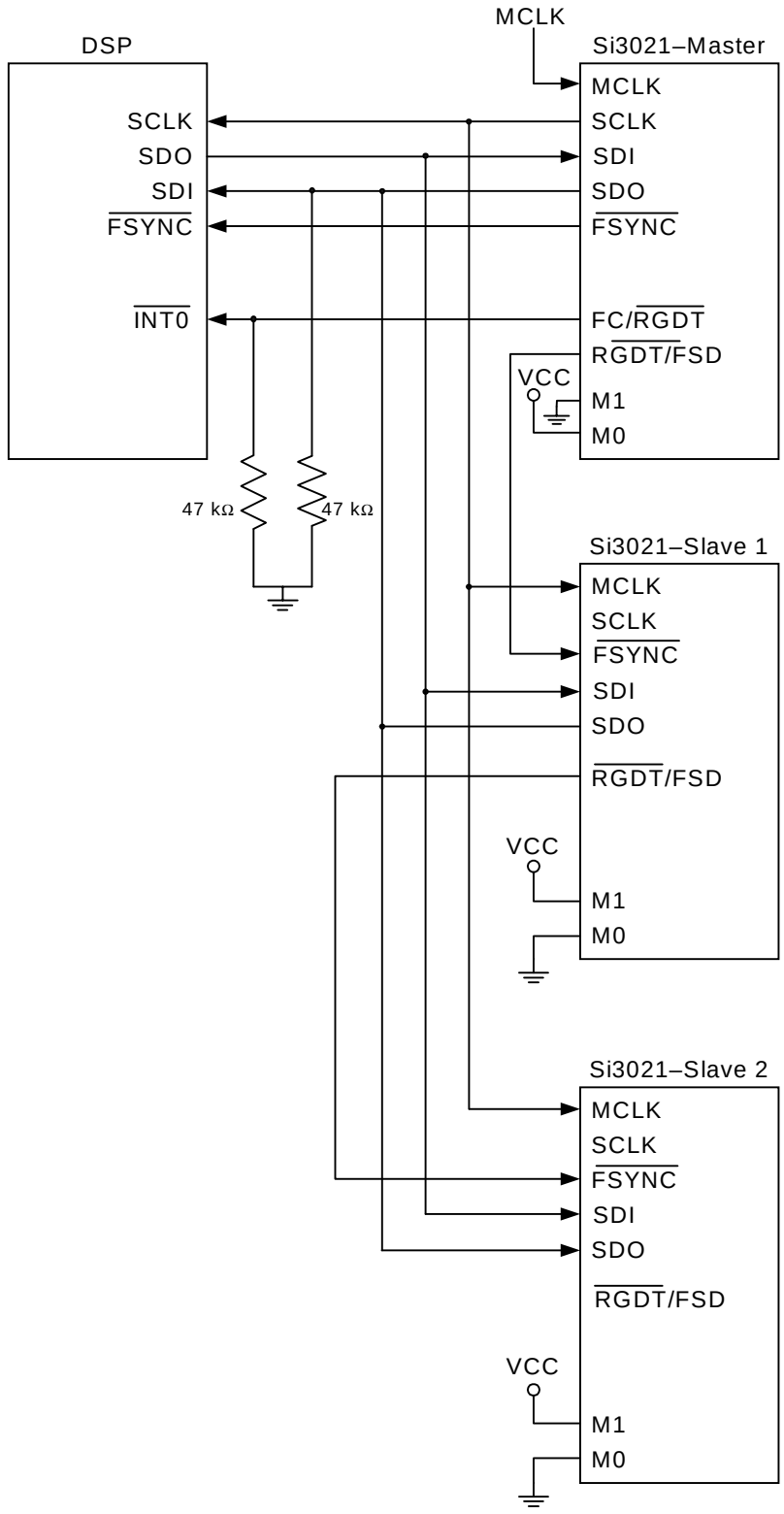


Figure 30. Typical Connection for Multiple Si3035s

Revision Identification

The Si3035 provides the system designer the ability to determine the revision of the Si3021 and/or the Si3012. Register 11 identifies the revision of the Si3021 with 4 bits named REVA. Register 13 identifies the revision of the Si3012 with 4 bits named REVB. Table 19 shows the values for the various revisions.

Table 19. Revision Values

Revision	Si3021	Si3012
A	1000	—
B	1001	—
C	1010	—
D	—	0100
E	—	0101
G	—	0111

Calibration

The Si3035 initiates an auto-calibration by default whenever the device goes off-hook or experiences a loss in line power. Calibration is used to remove any offsets that may be present in the on-chip A/D converter which could affect the A/D dynamic range. Auto-calibration is typically initiated after the DAA DC termination stabilizes and takes 512/Fs seconds to complete. Due to the large variation in line conditions and line card behavior that may be presented to the DAA, it can be beneficial to use manual calibration in lieu of auto-calibration. Manual calibration should be executed as close as possible to 512/Fs seconds before valid transmit/receive data is expected.

The following steps should be taken to implement manual calibration:

1. The CALD (auto-calibration disable—Register 17) bit must be set to 1.
2. The MCAL (manual calibration) bit must be toggled to 1 and then 0 to begin and complete the calibration.
3. The calibration will be completed in 512/Fs seconds.

In-Circuit Testing

The Si3035's advanced design provides the modem manufacturer with an increased ability to determine system functionality during production line tests, as well as support for end-user diagnostics. Four loopback modes exist allowing increased coverage of system components. For three of the test modes, a line-side power source is needed. While a standard phone line can be used, the test circuit in Figure 1 on page 4 is adequate. In addition, an off-hook sequence must be performed to connect the power source to the line-side chip.

For the start-up test mode, no line-side power is necessary and no off-hook sequence is required. The start-up test mode is enabled by default. When the PDL bit (Register 6, bit 4) is set (the default case), the line side is in a power-down mode and the DSP-side is in a digital loop-back mode. In this mode, data received on SDI is passed through the internal filters and transmitted on SDO. This path will introduce approximately 0.9 dB of attenuation on the SDI signal received. The group delay of both transmit and receive filters will exist between SDI and SDO. Clearing the PDL bit disables this mode and the SDO data is switched to the receive data from the line side. When the PDL bit is cleared the FDT bit (Register 12, bit 6) will become active, indicating the successful communication between the line-side and DSP-side. This can be used to verify that the ISOcap link is operational.

The remaining test modes require an off-hook sequence to operate. The following sequence defines the off-hook requirement:

1. Power up or reset.
2. Program clock generator to desired sample rate.
3. Enable line-side by clearing PDL bit.
4. Issue off-hook
5. Delay 1548/Fs to allow calibration to occur.
6. Set desired test mode.

The ISOcap digital loopback mode allows the data pump to provide a digital input test pattern on SDI and receive that digital test pattern back on SDO. To enable this mode, set the DL bit of Register 1. In this mode, the isolation barrier is actually being tested. The digital stream is delivered across the isolation capacitor, C1 of Figure 16 on page 15, to the line-side device and returned across the same barrier. In this mode, the 0.9 dB attenuation and filter group delays also exist.

The analog loopback mode allows an external device to drive the RX pin of the line-side chip and receive the signal from the TX pin. This mode allows testing of external components connecting the RJ-11 jack (TIP and RING) to the line side of the Si3035. To enable this mode, set the AL bit of Register 2.

The final testing mode, internal analog loopback, allows the system to test the basic operation of the transmit/receive path of the line side and the external components R4, R18, R21, and C5 of Figure 16 on page 15. In this test mode, the data pump provides a

digital test waveform on SDI. This data is passed across the isolation barrier, looped from the TX to the RX pin, passed back across the isolation barrier, and presented to the data pump on SDO. To enable this mode, clear the HBE bit of Register 2.

Clearing the HBE bit will cause a DC offset which affects the signal swing of the transmit signal. In this test mode, it is recommended that the transmit signal be 12 dB lower than normal transmit levels. This lower level will eliminate clipping caused by the DC offset which results from disabling the hybrid. It is assumed in this test that the line AC impedance is nominally 600 Ω.

Note: All test modes are mutually exclusive. If more than one test mode is enabled concurrently, the results are unpredictable.

Exception Handling

The Si3035 provides several mechanisms to determine if an error occurs during operation. Through the secondary frames of the serial link, the controlling DSP can read several status bits. The bit of highest importance is the frame detect bit (FDT, Register 12, bit 6). This bit indicates that the DSP-side (Si3021) and line-side (Si3012) devices are communicating. During normal operation, the FDT bit can be checked before reading any bits that indicate information about the line side. If FDT is not set, the following bits related to the line-side are invalid: RDT, LCS, CBID, and REVB. The RGDT operation will also be non-functional.

Following power-up and reset, the FDT bit is not set because the PDL bit (Register 6, bit 4) defaults to 1. In this state, the ISOcap link is not operating and no information about the line-side can be determined. The user must program the clock generator to a valid configuration for the system and clear the PDL bit to activate the ISOcap link. While the Si3021 and Si3012 are establishing communication, the Si3035 will not generate FSYNC signals. Establishing communication will take less than 10 ms. Therefore, if the controlling DSP serial interface is interrupt driven, based on the FSYNC signal, the controlling DSP does not require a special delay loop to wait for this event to complete.

The FDT bit can also indicate if the line-side executes an off-hook request successfully. If the line-side is not connected to a phone line (i.e., the user fails to connect a phone line to the modem), the FDT bit remains cleared. The controlling DSP must allow sufficient time for the line-side to execute the off-hook request. The maximum time for FDT to be valid following an off-hook request is 10 ms. At this time, the LCS bits indicate the amount of loop current flowing. For more information, see “Loop Current Monitor” on page 25. If the FDT bit fails to be set following an off-hook request, the line-side chip must be reset. This is accomplished by setting the PDL bit for at least 1 ms.

Another useful bit is the communication link error (CLE) bit (Register 12, bit 7). The CLE bit indicates a time-out error for the ISOcap link following a change to either PLL1 or PLL2. For more information, see “Clock Generation Subsystem” on page 20. When the CLE bit is set, the DSP-side chip has failed to receive verification from the line side that the clock change has been accepted in an expected period of time (less than 10 ms). This condition indicates a severe error in programming the clock generator or possibly a defective line-side chip.

Control Registers

Any register not listed here is reserved and should not be written.

Table 20. Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Control 1	SR						DL	SB
2	Control 2					AL		HBE	RXE
3	Control 3								
4	Control 4								
5	DAA Control 1				OPOL	ONHM	RDT	OHE	OH
6	DAA Control 2	CPE	ATM1	ARM1	PDL	PDN		ATM0	ARM0
7	PLL1 Divide N1	N1[7:0]							
8	PLL1 Multiply M1	M1[7:0]							
9	PLL2 Div./Mult. N2/M2	N2[3:0]				M2[3:0]			
10	PLL Control								CGM
11	Chip Revision					REVA[3:0]			
12	Line Side Status	CLE	FDT			LCS[3:0]			
13	Transmit and Receive Gain		CBID	REVB[3:0]				ARX	ATX
14	Daisy-Chain Control	NSLV2	NSLV1	NSLV0	SSEL1	SSEL0	FSD	RPOL	DCE
15	TX/RX Gain Control	TXM	ATX2	ATX1	ATX0	RXM	ARX2	ARX1	ARX0
16	IIR Filter Control	0	0	0	IIRE	1	0	0	0
17	Calibration	0	MCAL	CALD					

Register 1. Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SR						DL	SB
Type	R/W						R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	SR	**Software Reset**. 0 = Enables chip for normal operation. 1 = Sets all registers to their reset value.
6:2	Reserved	Read returns zero.
1	DL	**Isolation Digital Loopback**. 0 = Disables digital loopback mode across the isolation barrier. 1 = Enables digital loopback mode across the isolation barrier.
0	SB	**Serial Digital Interface Mode**. 0 = Operation is in 15-bit mode and the LSB of the data field indicates whether a secondary frame is required. 1 = The serial port is operating in 16-bit mode and requires use of the secondary frame sync signal, FC/$\overline{\text{RGDT}}$, to initiate control data reads/writes.

Register 2. Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					AL		HBE	RXE
Type					R/W		R/W	R/W

Reset settings = 0000_0011

Bit	Name	Function
7:4	Reserved	Read returns zero.
3	AL	**Analog Loopback**. 0 = Disables analog loopback mode. 1 = Enables analog loopback mode.
2	Reserved	Read returns zero.
1	HBE	**Hybrid Enable**. 0 = Disconnects hybrid in transmit path. 1 = Connects hybrid in transmit path.
0	RXE	**Receive Enable**. 0 = Disables receive path. 1 = Enables receive path.

Register 3. Control 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = 0000_0000

Bit	Name	Function
7:0	Reserved	Read returns zero.

Register 4. Control 4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = 0000_0000

Bit	Name	Function
7:0	Reserved	Read returns zero.

Register 5. DAA Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				OPOL	ONHM	RDT	OHE	OH
Type				R/W	R/W	R	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7:5	Reserved	Read returns zero.
4	OPOL	**Off-Hook Polarity**. 0 = Off-hook pin is active low. 1 = Off-hook pin is active high.
3	ONHM	**On-Hook Line Monitor**. 0 = Normal on-hook mode. 1 = Enables low-power monitoring mode allowing the DSP to receive line activity without going off-hook. This mode is used for caller ID detection.
2	RDT	**Ring Detect**. 0 = No ring is occurring. Reset either 4.5–9 seconds after last positive ring is detected or when the system executes an off-hook. 1 = Indicates a ring is occurring.
1	OHE	**Off-Hook Pin Enable**. 0 = Off-hook pin is ignored. 1 = Enables the operation of the off-hook pin.
0	OH	**Off-Hook**. 0 = Line side chip is on-hook. 1 = Causes the line side chip to go off-hook. This bit operates independently of OHE and is a logic OR with the off-hook pin when OHE = 1.

Register 6. DAA Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CPE	ATM1	ARM1	PDL	PDN		ATM0	ARM0
Type	R/W	R/W	R/W	R/W	R/W		R/W	R/W

Reset settings = 0111_0000

Bit	Name	Function
7	CPE	**Charge Pump Enable.** 0 = Charge pump is disabled. 1 = Charge pump is enabled. (The V_A pin should not be connected to a supply. V_D = 3.3 V ± 10%.)
6,1	ATM[1:0]	**AOUT Transmit Path Level Control.** 00 = –20 dB transmit path attenuation for call progress AOUT pin only. 01 = –32 dB transmit path attenuation for call progress AOUT pin only. 10 = Mutes transmit path for call progress AOUT pin only. 11 = –26 dB transmit path attenuation for call progress AOUT pin only.
5,0	ARM[1:0]	**AOUT Receive Path Level Control.** 00 = 0 dB receive path attenuation for call progress AOUT pin only. 01 = –12 dB receive path attenuation for call progress AOUT pin only. 10 = Mutes receive path for call progress AOUT pin only. 11 = –6 dB receive path attenuation for call progress AOUT pin only.
4	PDL	**Power Down Line-Side Chip.** 0 = Normal operation. Program the clock generator before clearing this bit. 1 = Places the Si3012 in power down or reset state.
3	PDN	**Power Down.** 0 = Normal operation. 1 = Powers down the Si3021. A pulse on $\overline{\text{RESET}}$ is required to restore normal operation.
2	Reserved	Read returns zero.

Register 7. PLL1 Divide N1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N1[7:0]							
Type	R/W							

Reset settings = 0000_0000 (serial mode 0, 1, 2)

Bit	Name	Function
7:0	N1[7:0]	**N1 Divider.** Contains the (value – 1) for determining the output frequency on PLL1.

Register 8. PLL1 Multiply M1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	M1[7:0]							
Type	R/W							

Reset settings = 0000_0000 (serial mode 0, 1)

Reset settings = 0001_0011 (serial mode 2)

Bit	Name	Function
7:0	M1[7:0]	**M1 Multiplier.** Contains the (value – 1) for determining the output frequency on PLL1

Register 9. PLL2 Divide/Multiply N2/M2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N2[3:0]				M2[3:0]			
Type	R/W				R/W			

Reset settings = 0000_0000 (serial mode 0, 1, 2)

Bit	Name	Function
7:4	N2[3:0]	**N2 Divider.** Contains the (value – 1) for determining the output frequency on PLL2.
3:0	M2[3:0]	**M2 Multiplier.** Contains the (value – 1) for determining the output frequency on PLL2.

Register 10. PLL Control Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								CGM
Type								R/W

Reset settings = 0000_0000

Bit	Name	Function
7:1	Reserved	Read returns zero.
0	CGM	**Clock Generation Mode.** 0 = No additional ratio is applied to the PLL and faster lock times are possible. 1 = A 25/16 ratio is applied to the PLL allowing for a more flexible choice of MCLK frequencies while slowing down the PLL lock time.

Register 11. Chip Revision

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					REVA			
Type	R[3:0]							

Reset settings = N/A

Bit	Name	Function
7:4	Reserved	Read returns zero.
3:0	REVA[3:0]	**Chip Revision.** Four-bit value indicating the revision of the Si3021 (DSP-side) chip.

Register 12. Line Side Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLE	FDT			LCS[3:0]			
Type	R/W	R			R			

Reset settings = N/A

Bit	Name	Function
7	CLE	**Communications (ISOcap Link) Error**. 0 = ISOcap communication link between the Si3021 and the Si3012 is operating correctly. 1 = Indicates a communication problem between the Si3021 and the Si3012. A write of 0 or a reset is required to clear this bit.
6	FDT	**Frame Detect**. 0 = Indicates ISOcap link has not established frame lock. 1 = Indicates ISOcap link frame lock has been established.
5:4	Reserved	Read returns zero.
3:0	LCS[3:0]	**Loop Current Sense**. Four-bit value returning the loop current in 6 mA increments. 0 = Loop current < 0.4 mA typical. 1111 = Loop current > 155 mA typical. See “Loop Current Monitor” on page 25.

Register 13. Transmit and Receive Gain

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		CBID	REVB[3:0]				ARX	ATX
Type	R		R				R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	Reserved	Read returns zero.
6	CBID	**Chip B ID**. 0 = Indicates the line side is domestic only. 1 = Indicates the line side has international support.
5:2	REVB[3:0]	**Chip Revision**. Four-bit value indicating the revision of the Si3012 (line-side) chip.
1	ARX	**Receive Gain**. 0 = 0 dB gain is applied to the receive path. 1 = 6 dB gain is applied to the receive path. **Note:** This bit should be zero if using Register 15 to control gain.
0	ATX	**Transmit Gain**. 0 = 0 dB gain is applied to the receive path. 1 = –3 dB gain (attenuation) is applied to the transmit path. **Note:** This bit should be 0 if using Register 15 to control gain.

Register 14. Daisy-Chain Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NSLV2	NSLV1	NSLV0	SSEL1	SSEL0	FSD	RPOL	DCE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000_0010 (serial mode 0, 1)
Reset settings = 0011_1111 (serial mode 2)

Bit	Name	Function
7:5	NSLV[2:0]	**Number of Slave Devices.** 000 = 0 slaves. Simply redefines the FC/$\overline{\text{RGDT}}$ and $\overline{\text{RGDT}}$/FSD pins. 001 = 1 slave device. 010 = 2 slave devices. 011 = 3 slave devices. 100 = 4 slave devices. (For four or more slave devices, the FSD bit MUST be set.) 101 = 5 slave devices. 110 = 6 slave devices. 111 = 7 slave devices.
4:3	SSEL[1:0]	**Slave Device Select.** 00 = 16-bit SDO receive data. 01 = Reserved. 10 = 15-bit SDO receive data. LSB = 1 for the Si3035 device. 11 = 15-bit SDO receive data. LSB = 0 for the Si3035 device.
2	FSD	**Delayed Frame Sync Control.** 0 = Sets the number of SCLK periods between frame syncs to 32. 1 = Sets the number of SCLK periods between frame syncs to 16. This bit **MUST** be set when Si3035 devices are slaves. For the master Si3035, only serial mode 1 is allowed in this case.
1	RPOL	**Ring Detect Polarity.** 0 = The FC/$\overline{\text{RGDT}}$ pin (operating as ring detect) is active low. 1 = The FC/$\overline{\text{RGDT}}$ pin (operating as ring detect) is active high.
0	DCE	**Daisy-Chain Enable.** 0 = Daisy chaining disabled. 1 = Enables the Si3035 to operate with slave devices on the same serial bus. The FC/$\overline{\text{RGDT}}$ signal (pin 7) becomes the ring detect output and the $\overline{\text{RDGT}}$/FSD signal (pin 15) becomes the delayed frame sync signal. Note that **ALL** other bits in this register are ignored if DCE = 0.

Register 15.TX/RX Gain Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TXM	ATX2	ATX1	ATX0	RXM	ARX2	ARX1	ARX0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	TXM	**Transmit Mute**. 0 = Transmit signal is not muted. 1 = Mutes the transmit signal.
6:4	ATX[2:0]	**Analog Transmit Attenuation.** 000 = 0 dB attenuation. 001 = 3 dB attenuation. 010 = 6 dB attenuation. 011 = 9 dB attenuation. 1xx = 12 dB attenuation. **Note:** Register 13 ATX bit must be 0 if these bits are used.
3	RXM	**Receive Mute**. 0 = Receive signal is not muted. 1 = Mutes the receive signal.
2:0	ARX[2:0]	**Analog Receive Gain**. 000 = 0 dB gain. 001 = 3 dB gain. 010 = 6 dB gain. 011 = 9 dB gain 1xx = 12 dB gain. **Note:** Register 13 ARX bit must be 0 if these bits are used.

Register 16. IIR Filter Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	IIRE	1	0	0	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000_1000

Bit	Name	Function
7:5	Reserved	Read returns zero (must always be written with zeroes).
4	IIRE	**IIR Filter Enable.** 0 = FIR filter enabled. 1 = Transmit and receive filters are realized with an IIR filter characteristic. To enable IIR filter write 0x18; to disable IIR filter write 0x08. See Table 12 on page 11 for more details on IIR filter performance.
3:0	Reserved	Read returns 0x8 (must always be written with 0x8).

Register 17. International Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	MCAL	CALD					
Type		R/W	R/W					

Reset settings = 0000_0000

Bit	Name	Function
7	Reserved	Must be zero.
6	MCAL	**Manual Calibration.** 0 = No calibration. 1 = Initiate calibration.
5	CALD	**Auto-Calibration.** 0 = Auto-calibration enabled. 1 = Auto-calibration disabled.
4:0	Reserved	Read returns zero.

APPENDIX—UL1950 3RD EDITION

Although designs using the Si3035 comply with UL1950 3rd Edition and pass all overcurrent and overvoltage tests, there are still several issues to consider.

Figure 31 shows two designs that can pass the UL1950 overvoltage tests, as well as electromagnetic emissions. The top schematic of Figure 31 shows the configuration in which the ferrite beads (FB1, FB2) are on the unprotected side of the sidactor (RV1). For this configuration, the current rating of the ferrite beads needs to be 6 A. However, the higher current ferrite beads are less effective in reducing electromagnetic emissions.

The bottom schematic of Figure 31 shows the configuration in which the ferrite beads (FB1, FB2) are on the protected side of the sidactor (RV1). For this design, the ferrite beads can be rated at 200 mA.

In a cost optimized design, it is important to remember that compliance to UL1950 does not always require overvoltage tests. It is best to plan ahead and know which overvoltage tests will apply to your system. System-level elements in the construction, such as fire enclosure and spacing requirements, need to be considered during the design stages. Consult with your professional testing agency during the design of the product to determine which tests apply to your system.

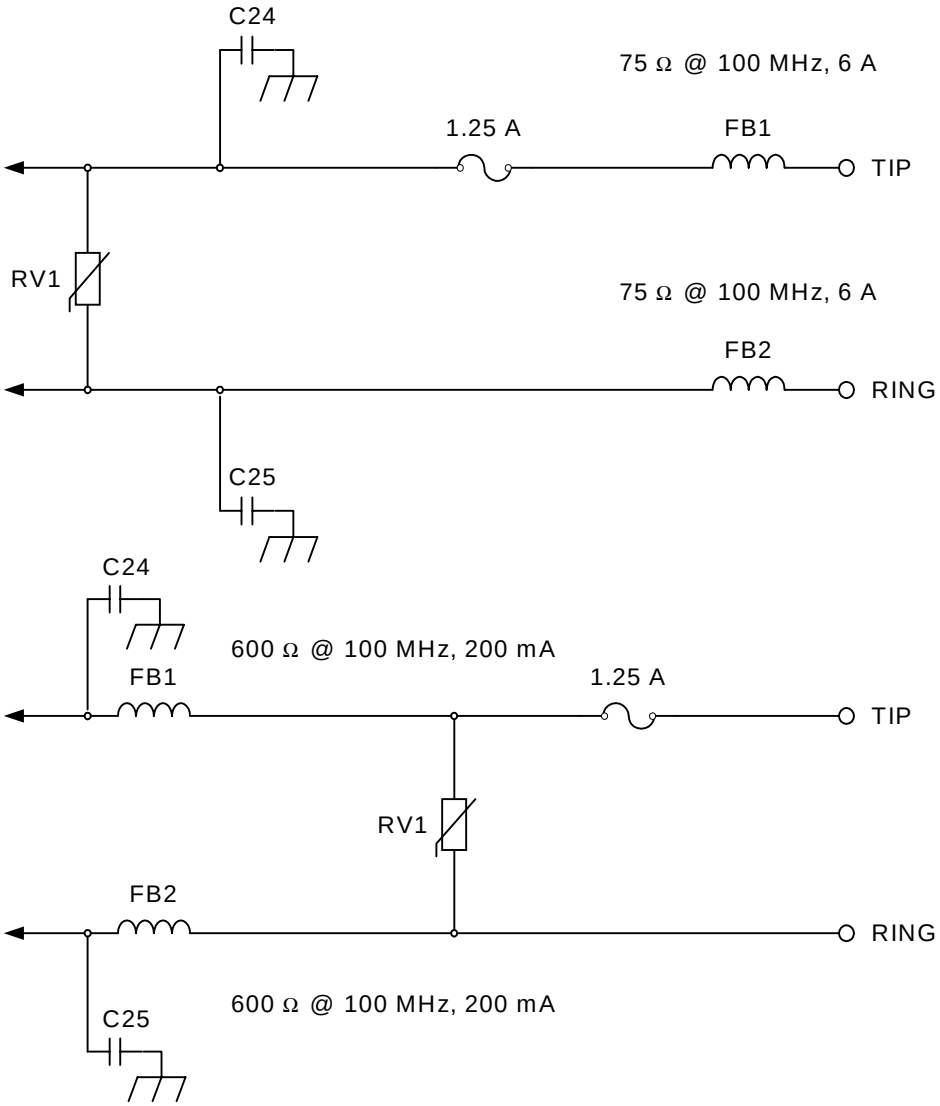
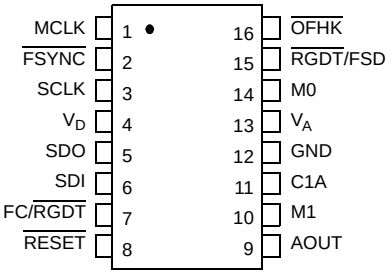


Figure 31. Circuits that Pass all UL1950 Overvoltage Tests

Pin Descriptions: Si3021

Si3021 (SOIC)



Si3021 (TSSOP)

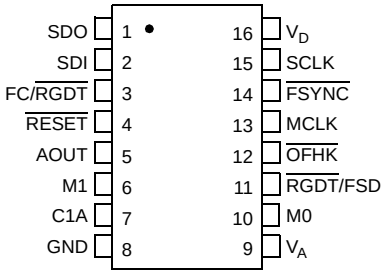


Table 21. Si3021 Pin Descriptions

SOIC Pin #	TSSOP Pin #	Pin Name	Description
1	13	MCLK	**Master Clock Input.** High speed master clock input. Generally supplied by the system crystal clock or modem/DSP.
2	14	$\overline{\text{FSYNC}}$	**Frame Sync Output.** Data framing signal that is used to indicate the start and stop of a communication/data frame.
3	15	SCLK	**Serial Port Bit Clock Output.** Controls the serial data on SDO and latches the data on SDI.
4	16	V_D	**Digital Supply Voltage.** Provides the digital supply voltage to the Si3021, nominally either 5 V or 3.3 V.
5	1	SDO	**Serial Port Data Output.** Serial communication data that is provided by the Si3021 to the modem/DSP.
6	2	SDI	**Serial Port Data Input.** Serial communication and control data that is generated by the modem/DSP and presented as an input to the Si3021.
7	3	FC/$\overline{\text{RGDT}}$	**Secondary Transfer Request Input/Ring Detect Output.** An optional signal to instruct the Si3021 that control data is being requested in a secondary frame. When daisy chain is enabled, this pin becomes the ring detect output. Produces an active low rectified version of the ring signal.
8	4	$\overline{\text{RESET}}$	**Reset Input.** An active low input that is used to reset all control registers to a defined, initialized state. Also used to bring the Si3034 out of sleep mode.
9	5	AOUT	**Analog Speaker Output.** Provides an analog output signal for driving a call progress speaker.

Table 21. Si3021 Pin Descriptions (Continued)

SOIC Pin #	TSSOP Pin #	Pin Name	Description
10	6	M1	**Mode Select 1 Input.** The second of two mode select pins that is used to select the operation of the serial port/DSP interface.
11	7	C1A	**Isolation Capacitor 1A.** Connects to one side of the isolation capacitor C1. Used to communicated with the line-side device.
12	8	GND	**Ground.** Connects to the system digital ground.
13	9	V_A	**Analog Supply Voltage.** Provides the analog supply voltage for the Si3021, nominally 5 V. This supply is typically generated internally with an on-chip charge pump set through a control register.
14	10	M0	**Mode Select 0 Input.** The first of two mode select pins that is used to select the operation of the serial port/DSP interface.
15	11	$\overline{\text{RGDT}}$/FSD	**Ring Detect/Delayed Frame Sync Output.** Output signal that indicates the status of a ring signal. Produces an active low rectified version of the ring signal. When daisy chain is enabled, this signal becomes a delayed frame sync to drive a slave device.
16	12	$\overline{\text{OFHK}}$	**Off-Hook Input.** An active low input control signal that provides a termination across TIP and RING for line seizing and pulse dialing.

Pin Descriptions: Si3012

Si3012 (SOIC or TSSOP)

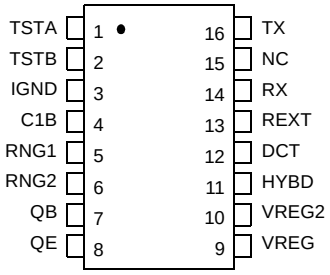


Table 22. Si3012 Pin Descriptions

(SOIC or TSSOP) Pin #	Pin Name	Description
1	TSTA	**Test Input A.** Allows access to test modes which are reserved for factory use. This pin has an internal pull-up and should be left as a no connect for normal operation.
2	TSTB	**Test Input B.** Allows access to test modes which are reserved for factory use. This pin has an internal pull-up and should be left as a no connect for normal operation.
3	IGND	**Isolated Ground.** Connects to ground on the line-side interface.
4	C1B	**Isolation Capacitor 1B.** Connects to one side of isolation capacitor C1.
5	RNG1	**Ring 1 Input.** Connects through a capacitor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the Si3035.
6	RNG2	**Ring 2 Input.** Connects through a capacitor to the RING lead of the telephone line. Provides the ring and caller ID signals to the Si3035.
7	QB	**Transistor Base.** Connects to the base of the hookswitch transistor, Q3.
8	QE	**Transistor Emitter.** Connects to the emitter of the hookswitch transistor, Q3.
9	VREG	**Voltage Regulator.** Connects to an external capacitor to provide bypassing for an internal voltage regulator.
10	VREG2	**Voltage Regulator 2.** Connects to an external capacitor to provide bypassing for an internal voltage regulator.

Table 22. Si3012 Pin Descriptions (Continued)

(SOIC or TSSOP) Pin #	Pin Name	Description
11	HYBD	**Hybrid Node Output.** Balancing capacitor connection used for JATE out-of-band noise support.
12	DCT	**DC Termination.** Provides DC termination to the telephone network.
13	REXT	**External Resistor.** Connects to an external resistor.
14	RX	**Receive Input.** Serves as the receive-side input from the telephone network.
15	NC	**No Connect.**
16	TX	**Transmit Output.** Provides the output through an AC termination impedance to the telephone network.

Ordering Guide

Table 23. Ordering Guide

Chipset	Region	Interface	Digital (SOIC)	Line (SOIC)	Digital (TSSOP)	Line (TSSOP)	Temperature
Si3034	Global	DSP Serial I/F	Si3021-KS	Si3014-KS	Si3021-KT	Si3014-KT	0°C to 70°C
Si3035	FCC/Japan	DSP Serial I/F	Si3021-KS	Si3012-KS	Si3021-KT	Si3012-KT	0°C to 70°C
Si3036	FCC/Japan	AC Link	Si3024-KS	Si3012-KS	Si3024-KT	Si3012-KT	0°C to 70°C
Si3038	Global	AC Link	Si3024-KS	Si3014-KS	Si3024-KT	Si3014-KT	0°C to 70°C
Si3044	Enhanced Global	DSP Serial I/F	Si3021-KS	Si3015-KS			0°C to 70°C
Si3044	Enhanced Global	DSP Serial I/F	Si3021-BS	Si3015-BS			–40° C to 85° C
Si3046	FCC/JATE	AC Link	Si3025-KS	Si3012-KS			0°C to 70°C
Si3048	Global	AC Link	Si3025-KS	Si3014-KS			0°C to 70°C

SOIC Outline

Figure 32 illustrates the package details for the Si3021 and Si3012. Table 24 lists the values for the dimensions shown in the illustration.

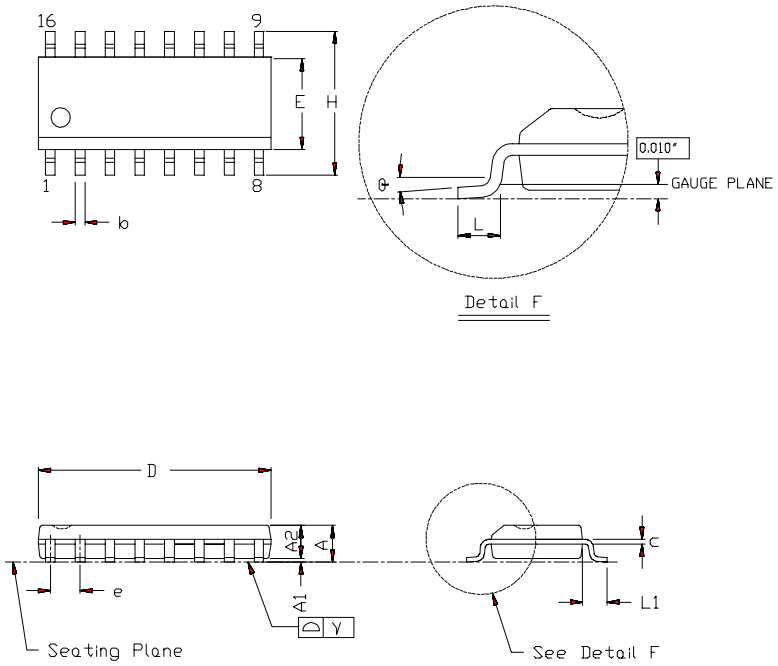


Figure 32. 16-pin Small Outline Plastic Package (SOIC)

Table 24. Package Diagram Dimensions

Controlling Dimension: mm

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	0.051	0.059	1.30	1.50
b	0.013	0.020	0.330	0.51
c	0.007	0.010	0.19	0.25
D	0.386	0.394	9.80	10.01
E	0.150	0.157	3.80	4.00
e	0.050 BSC	—	1.27 BSC	—
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
L1	0.042 BSC	—	1.07 BSC	—
γ	—	0.004	—	0.10
θ	0°	8°	0°	8°

TSSOP Outline

Figure 33 illustrates the package details for the Si3021 and Si3014. Table 25 lists the values for the dimensions shown in the illustration.

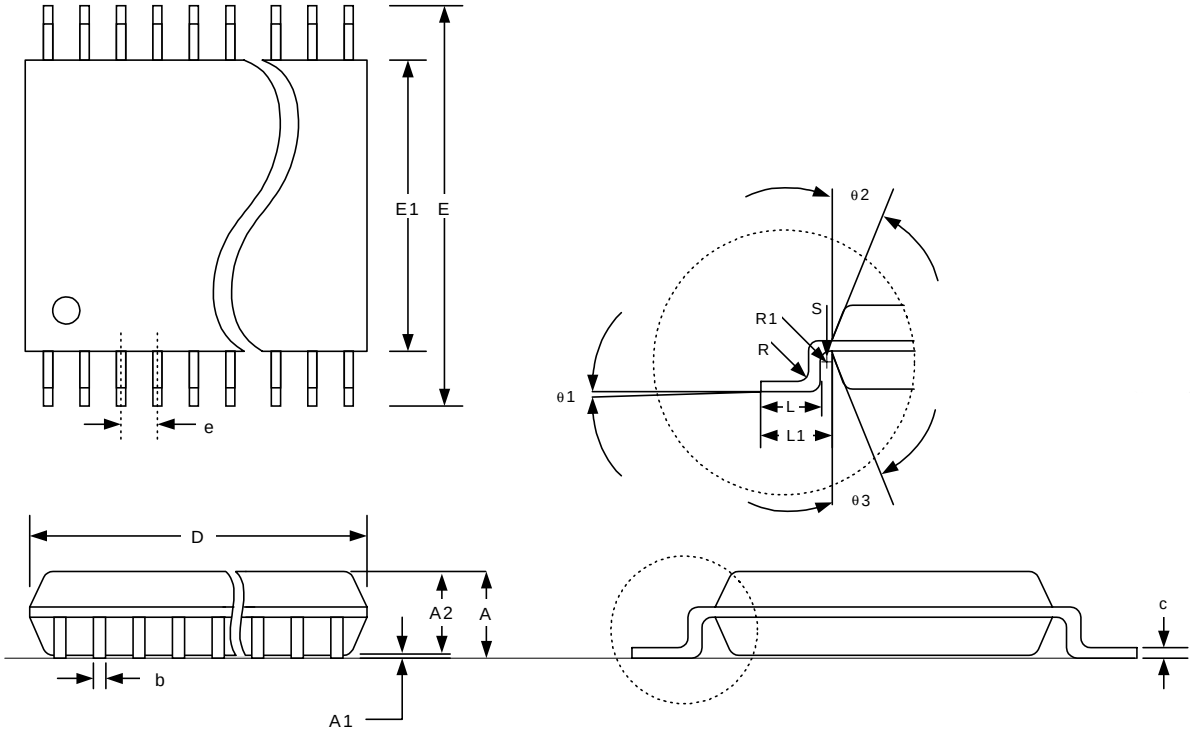


Figure 33. 16-pin Thin Small Shrink Outline Package (TSSOP)

Table 25. Package Diagram Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	—	1.10	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
c	0.09	—	0.20
D	4.85	5.00	5.15
e	0.65 BSC		
E	6.40 BSC		
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
L1	1.00 REF		
R	0.09	—	—
R1	0.09	—	—
S	0.20	—	—
θ1	0	—	8
θ2	12 REF		
θ3	12 REF		

Data Sheet Changes from Version 1.0 to Version 1.1

- Typical Application Circuit was updated.
- C24, C25 value changed from 470 pF to 1000 pF and C31, C32 were added in Table 13. The tolerance was also changed from 20% to 10%.
- Power Supply Voltage, Analog maximum changed from 4.75 V to 5.00 V in Table 4.
- Last paragraph updated in “Power Management” text section.

Data Sheet Changes from Version 1.1 to Version 1.2

- TSSOP information added.
- Total supply currents updated in Table 3 and Table 4.
- Cycle time updated in Table 7.
- Delay times updated in Table 8, Table 9, and Table 10.
- Figure 4 updated.
- Revision G values added in Table 19.
- Figure 16, “Typical Application Schematic,” on page 15 updated.
- Table 13, “Component Values—Typical Application,” on page 16 (BOM) updated.

Contact Information

Silicon Laboratories Inc.

4635 Boston Lane
Austin, TX 78735
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Email: productinfo@silabs.com
Internet: www.silabs.com