

FEATURES

- High Frequency Operation
- Wide Dynamic Range
- Low Capacitance

APPLICATIONS

- Communications
- RF Mixers

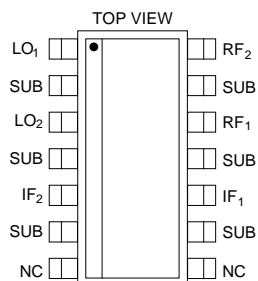
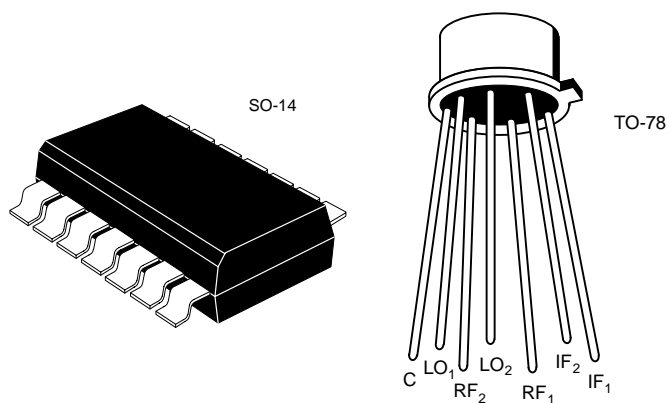
DESCRIPTION

The SD8901 is a ring demodulator/balanced mixer. Designed to utilize Calogic's ultra high speed and low capacitance lateral DMOS process. The SD8901 offers significant performance improvements over JFET and diode balanced mixers when low third order harmonic distortion has been a problem.

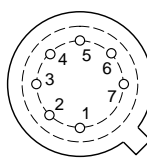
PACKAGE INFORMATION

Part	Package	Temperature Range
SD8901HD	Hermetic TO-78	-55°C to 125°C
SD8901CY	Plastic Surface Mount	-55°C to 125°C
XSD8901	Sorted Chips in Carriers	-55°C to 125°C

PIN CONFIGURATIONS



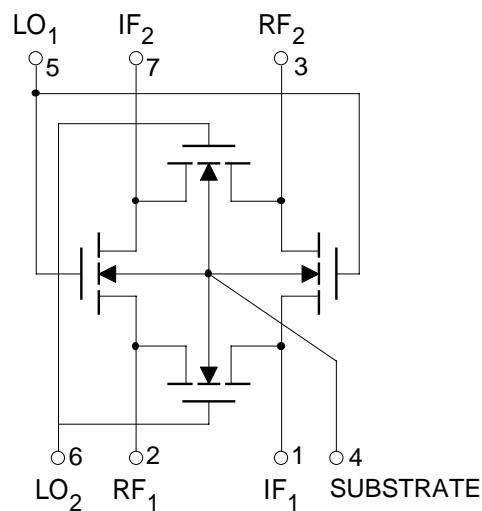
- 1 IF₁
- 2 RF₁
- 3 RF₂
- 4 CASE
- 5 LO₁
- 6 LO₂
- 7 IF₂



BOTTOM VIEW

CD4

Functional block diagram



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

V _{DS} Drain to Source	15 V	I _D Drain Current	50 mA
V _{DB} Drain to Substrate	22.5 V	Operating Temperature	-55 to 125°C
V _{SB} Source to Substrate	22.5 V	Storage Temperature	-65 to 150°C
V _{GS} Gate to Source	-22.5 V to 30 V	Power Dissipation (A Package)*	640 mW
V _{GB} Gate to Substrate	-0.3V to 30 V	* Derate 5 mW/ °C above 25°C	
V _{GD} Gate to Drain	-22.5V to 30 V		

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNIT	TEST CONDITIONS	
STATIC							
V _{(BR)DS}	Drain-Source Breakdown Voltage	15	25		V	V _{GS} = V _{SB} = -5 V I _S = 10 nA	
V _{(BR)SD}	Source-Drain Breakdown Voltage	15				V _{GD} = V _{DB} = -5 V I _D = 10 nA	
V _{(BR)DB}	Drain-Substrate Breakdown Voltage	22.5				Source Open V _{GB} = 0 V, I _D = 10 nA	
V _{(BR)SB}	Source-Substrate Breakdown Voltage	22.5				Drain Open V _{GB} = 0 V, I _D = 10 nA	
V _T	Threshold Voltage	0.1	1	2.0		V _{DS} = V _{GS} = V _T I _S = 1 μA, V _{SB} = 0V	
r _{DS(ON)}	Drain-Source "ON" Resistance		50	75	Ω	I _D = 1 mA V _{SB} = 0 V	V _{GS} = 5 V
			30				V _{GS} = 10 V
			23				V _{GS} = 15 V
			19				V _{GS} = 20 V
Δr _{DS(ON)}	Resistance Matching		3	7			
DYNAMIC							
C _{gg}	LO ₁ - LO ₂ Capacitance		4.4		pF	V _{DS} = 0 V, V _{BS} = -5.5 V V _{GS} = 4 V	
L _c	Conversion Loss		8		dB	See Figure 1, PLO = +17 dBm	
IMD ₃	Third Order Intercept		+35				
f _{MAX}	Maximum Operation Frequency		250		MHz		

Note: Guaranteed by design, not subject to production test

PERFORMANCE COMPARISON

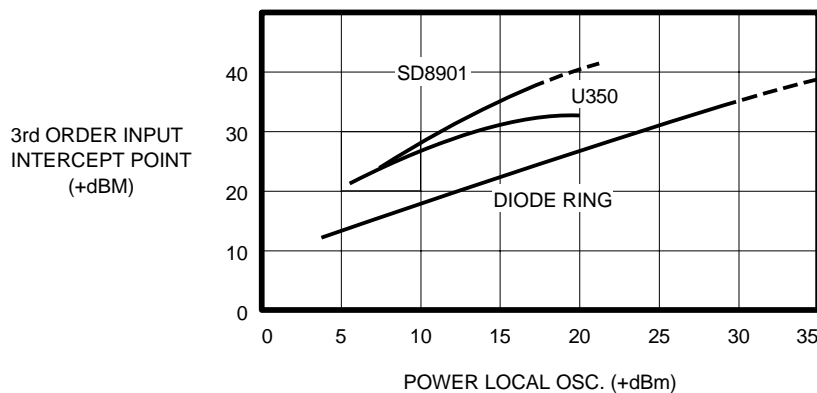


FIGURE 1.

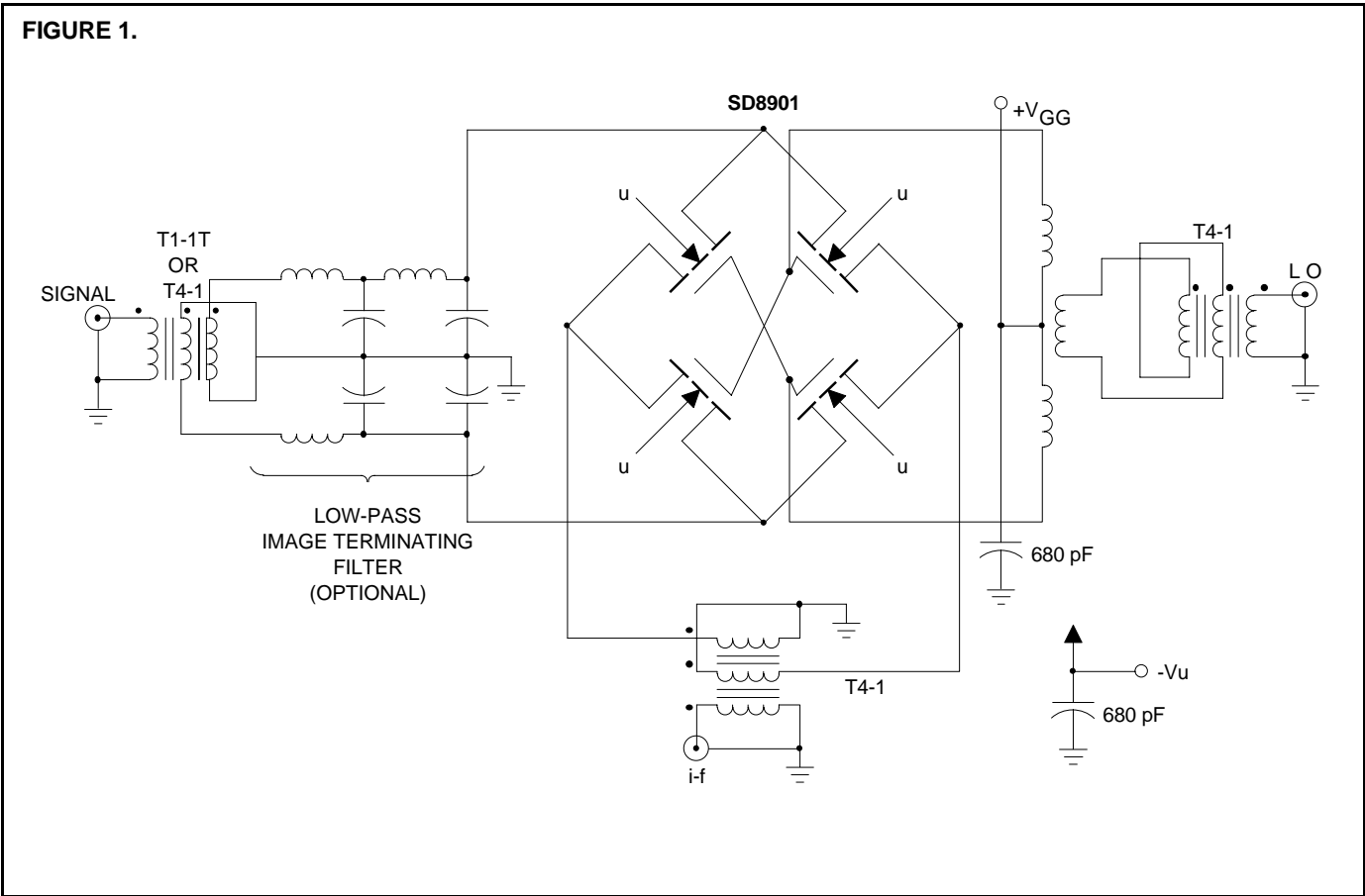


FIGURE 2. First and third Quadrant I-E Characteristic Showing Effect of Gate Voltage Leading to Large-Signal Overload Distortion.

