RJ-017

ChipBridge

FEATURES

- High performance, single chip, full remote Ethernet bridge, fully IEEE 802.3 compatible
- On chip AUI (DTE or DCE) or UTP LAN interfaces
- NRZ decoded signals for easy interface to other Ethernet chips
- 10 Mbps in half-duplex mode or 20 Mbps in full-duplex mode
- Automatic TP polarity reversal
- Multiple LAN operating modes
- Glueless connection to most LAN chips
- Up to 40 Mbps Sync WAN link
- Up to 115.2 kbps Async WAN link with internal baud rate generator
- 10,000-address LAN table
- Buffer capacity of 256 frames
- Filtering rate of 15,000 pps
- Forwarding rate of 15,000 pps
- Automatic LAN table learning and aging
- Compression type: Enhanced Tinygram
- Full on-chip support for 7 status LEDs
- Low power 0.6 micron CMOS technology
- 100-pin PQFP package

DESCRIPTION

The ChipBridge is a highly integrated ASIC that combines LAN and WAN subsystems to achieve a full Ethernet remote bridge on a single chip. It automatically learns the MAC addresses on the LAN it is connected to, and forwards only the frames destined for another LAN. It is fully compliant with the IEEE 802.3 standard.

The ChipBridge's LAN interface incorporates a Manchester encoder/decoder that allows AUI (DTE or DCE) and both half-duplex (10 Mbps) and full-duplex (20 Mbps) UTP operation modes. In addition, all LAN signals are available as NRZ decoded signals for connection to other LAN devices, such as multi-port repeaters or LAN controllers. In total, twenty-five different modes of operation can be selected by setting the LMODE input pins.

The WAN subsystem contains a sync/async HDLC controller, capable of operating at up to 40 Mbps in synchronous mode, and 115.2 kbps in asynchronous mode. Zero-bit insertion and deletion is used in synchronous mode and octet-stuffing is used in asynchronous mode for transparency. The ACCM (Async Control Character Map) can be disabled if not required (asynchronous mode only). In asynchronous mode, an external clock source may be used or the internal baud rate generator can be configured to generate standard clock frequencies between 9.6 kbps and 115.2 kbps. Enhanced Tinygram compression increases data throughput by stripping the padding bits in 64-byte frames.

The ChipBridge's LAN table can store up to 10,000 addresses and is automatically updated. The aging machine automatically deletes entries if, after 5 minutes, no frames have been received from that station. Filtering and forwarding is performed at the maximum theoretical rate of 15,000 pps. The ChipBridge buffer can hold 256 frames, with a throughput latency of 1 frame. Filtering can be disabled for those applications that require it, such as LAN extenders and segmenters.

The ChipBridge operates independently without need for a host. The only external component required is a 256k x 16 DRAM, a crystal and some resistors and capacitors. The ChipBridge contains a DRAM controller for glueless connection to the DRAM.

The ChipBridge is manufactured in low power 0.6 micron CMOS process and is available in a 100-pin PQFP package.

The ChipBridge functional block diagram is seen in Figure 1 and the connection diagram in Figure 2.

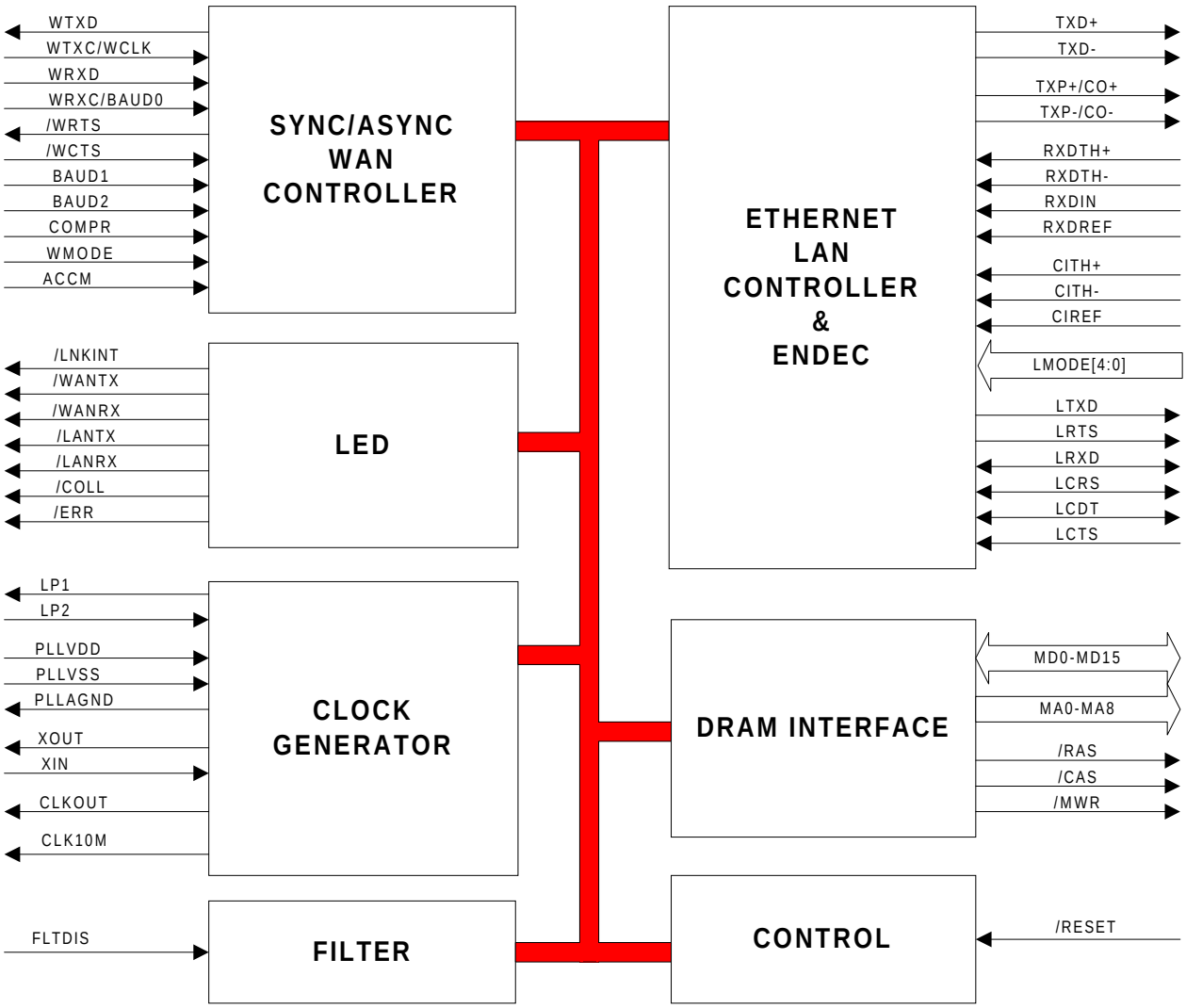


Figure 1. Functional Block Diagram

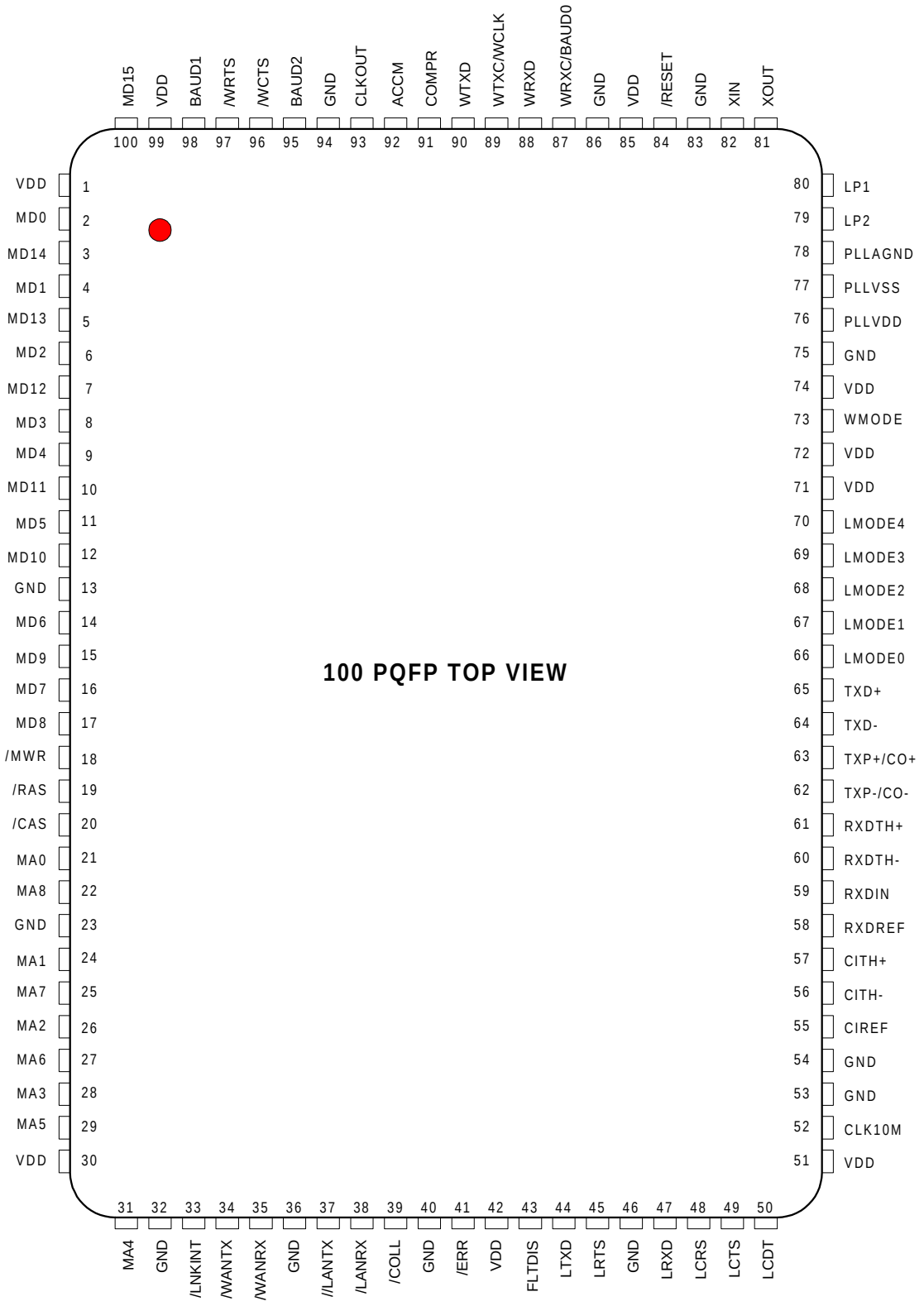


Figure 2. Connection Diagram

PIN DESCRIPTION

Table 1. Pin Description

Name	Pin No.	Type	Description
MA0-MA8	21, 22, 24, 25, 26, 27, 28, 29, 31	O	DRAM ADDRESS BUS: The DRAM address bus is multiplexed. During the first phase, it carries address bits 10-18, and during the second phase it carries address bits 1-9.
MD0 - MD15	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 14, 15, 16, 17, 100	I/O	DRAM DATA BUS: The DRAM data bus is an input while the ChipBridge is reading from the DRAM, and an output while writing to the DRAM. At all other times it is 3-state.
/RAS	19	O	DRAM ROW ADDRESS STROBE: This output drives the DRAM RAS signal. It is used to strobe address bits 10-18 into the DRAM on its falling edge, and to perform the refresh in CAS before RAS refresh cycle.
/CAS	20	O	DRAM COLUMN ADDRESS STROBE: This output drives the DRAM CAS signal. It is used to strobe address bits 1-9 into the DRAM on its falling edge, and to start a refresh in CAS before RAS refresh cycle. In an early write cycle, it is used to strobe the data into the DRAM.
/MWR	18	O	DRAM WRITE: This output is the write signal to the DRAM. It is low during a write cycle, and high at all other times.
WTXD	90	O	WAN TRANSMIT DATA: This signal has 2 modes of operation: 1. In synchronous mode, the transmitter emits a new data bit on every falling WTXC edge while WCTS is at a logic low. While WCTS is at a logic high, this pin outputs a logic high. 2. In asynchronous mode, the transmitter emits a start bit, 8 data bits and a stop bit, according to a pre-defined baud rate.
WTXC/WCLK	89	I	WAN TRANSMIT CLOCK / WAN CLOCK: This signal has 2 modes of operation: 1. In synchronous mode, it is the link clock for the transmitter at any frequency up to 40 MHz. 2. In asynchronous mode, it is the clock input to the transmitter and receiver, and is 16 times the baud rate.
WRXD	88	I	WAN RECEIVE DATA: This signal has 2 modes of operation: 1. In synchronous mode, it is sampled on every rising edge of WRXC. 2. In asynchronous mode, it is sampled at 16 times the baud rate.
WRXC/BAUD0	87	I	WAN RECEIVE CLOCK / BAUD RATE SELECT 0: This signal has 2 modes of operation: 1. In synchronous mode it is the link clock for the receiver at any frequency up to 40 MHz. 2. In asynchronous mode, this signal operates in conjunction with BAUD1 and BAUD2 to determine the baud rate or the clock source.
/WRTS	97	O	WAN REQUEST TO SEND: This signal is LOW whenever a frame is ready to be transmitted. It goes HIGH when there are no more frames to be transmitted.

Table 1. Pin Description (Cont'd)

Name	Pin No.	Type	Description
/WCTS	96	I	WAN CLEAR TO SEND: The transmitter transmits frames while this signal is LOW. In synchronous mode, if this signal goes HIGH for more than one bit-time, the frame in transmission is aborted and retransmitted in its entirety when WCTS goes low again. In asynchronous mode, if this signal goes HIGH, the current byte being transmitted is completed and transmission is suspended until /WCTS goes LOW again.
BAUD1	98	I	BAUD RATE SELECT 1: In asynchronous mode, this signal operates in conjunction with BAUD0 and BAUD2 to determine the baud rate or the clock source.
BAUD2	95	I	BAUD RATE SELECT 2: In asynchronous mode, this signal operates in conjunction with BAUD0 and BAUD1 to determine the baud rate or the clock source.
COMPR	91	I	COMPRESS ENABLE: When this signal is LOW, frames from the LAN are transmitted over the WAN as is. When this signal is HIGH, the padding bits inserted in sub-64 byte frames are stripped off (Enhanced Tinygram Compression).
WMODE	73	I	WAN MODE SELECT: When LOW, the WAN link operates in synchronous mode. When HIGH, the WAN link operates in asynchronous mode.
ACCM	92	I	ASYNC CONTROL CHARACTER MAP ENABLE: (valid in asynchronous mode only). When this input pin is LOW, the first 32 characters (up to 0x20) in asynchronous mode are transmitted as a two octet sequence consisting of the Control Escape octet (0x7d) followed by the original octet with its sixth bit complemented. When this pin is HIGH, these characters are transmitted as is.
TXD+	65	O	TRANSMIT DATA POSITIVE: This output pin is the positive Manchester encoded data transmitted onto the line. It forms the differential transmit data pair together with TXD-. The transmit data pair can contain both regular transmit data and looped-back receive data, depending on LMODE.
TXP+/CO+	63	O	DATA PRE-EMPHASIS + / COLLISION OUT+: This output has two purposes. 1. In AUI-DCE modes, it is the positive collision signal. It forms the differential collision pair with TXP-/CO-. The collision signal is a 10 MHz square wave synchronized with CLK10M. 2. In UTP mode, this pin outputs the positive pre-emphasis signal. It forms the differential pre-emphasis pair with TXP-/CO-.
TXD-	64	O	TRANSMIT DATA NEGATIVE: This output pin is the negative Manchester encoded data transmitted onto the line. It forms the differential transmit data pair together with TXD+. The transmit data pair can contain both regular transmit data and looped-back receive data, depending on LMODE.
TXP-/CO-	62	O	DATA PRE-EMPHASIS - / COLLISION OUT -: This output has two purposes. 1. In AUI-DCE mode, it is the negative collision signal. It forms the differential collision pair with TXP+/CO+. The collision signal is a 10 MHz square wave synchronized with CLK10M. 2. In UTP mode, this pin outputs the negative pre-emphasis signal. It forms the differential pre-emphasis pair with TXP+/CO+.
RXDTH+	61	I	RECEIVE DATA INPUT THRESHOLD +: This input pin is used in conjunction with RXDTH- to control the squelch function and link integrity pulse detection.
RXDTH-	60	I	RECEIVE DATA INPUT THRESHOLD -: This input pin is used in conjunction with RXDTH+ to control the squelch function and link integrity pulse detection.
RXDIN	59	I	RECEIVE DATA INPUT: This input pin receives the serial data from the network and is used by the digital PLL for data recovery.
RXDREF	58	I	RECEIVE DATA INPUT REFERENCE: This input pin is the reference voltage for the receive input signals RXDTH+, RXDTH- and RXDIN.

Table 1. Pin Description (Cont'd)

Name	Pin No.	Type	Description
CITH+	57	I	COLLISION INPUT POSITIVE THRESHOLD: This input pin is used in conjunction with CITH- to detect collisions. It is valid in AUI-DTE mode only. In other modes it should be connected to VDD.
CITH-	56	I	COLLISION INPUT NEGATIVE THRESHOLD: This input pin is used in conjunction with CITH+ to detect collisions. It is valid in AUI-DTE mode only. In other modes it should be connected to VDD.
CIREF	55	I	COLLISION INPUT REFERENCE: This input pin is the reference voltage for the collision input signals CITH+ and CITH-. It is valid in AUI-DTE mode only. In other modes it should be connected to GND.
CLK10M	52	O	10 MHz CLOCK: This is the 10 MHz clock synchronized to the LAN signals RXD, TXD, CRS, CDT, RTS. This clock is used by external logic to sample the outgoing data and control signals, and by the ChipBridge to sample the incoming data and control signals.
LTXD	44	O	LAN TRANSMIT DATA: This pin is the transmitted data from the MAC. The data on this pin is synchronized with CLK10M rising edge or falling edge depending on LMODE (see *Tables 3 and 4*)
LRXD	47	I/O	LAN RECEIVE DATA: This pin is either an input or an output depending on LMODE. 1. When this pin is an input, it is the receive data to the MAC. The data inputted should be synchronous with CLK10M rising edge or falling edge, depending on LMODE. 2. When this pin is an output, it outputs the received data from the ENDEC. This output is synchronized with CLK10M rising edge or falling edge depending on LMODE. (see *Tables 3 and 4*)
LCRS	48	I/O	LAN CARRIER SENSE: (active LOW or active HIGH, depending on LMODE) This pin is either an input or an output, depending on LMODE. 1. When this pin is an input, it acts as the CRS input to the MAC. The CRS should be synchronous with CLK10M. 2. When this pin is an output, it outputs CRS from the ENDEC. This output is synchronized with CLK10M. (see *Tables 3 and 4*)
LCDT	50	I/O	LAN COLLISION DETECT: (active LOW or active HIGH, depending on LMODE) This pin is either an input or an output, depending on LMODE. 1. When this pin is an input, it acts as the CDT input to the MAC. The CDT should be synchronous with CLK10M. 2. When this pin is an output, it outputs CDT. This output is synchronized with CLK10M. (see *Tables 3 and 4*)
LRTS	45	O	LAN REQUEST TO SEND: (active LOW or active HIGH, depending on LMODE) This pin is an output, from the MAC. It is asserted whenever the LAN is transmitting. (see *Tables 3 and 4*)
LCTS	49	I	LAN CLEAR TO SEND: (active HIGH) This pin is an input to the LAN DMAs arbiter. When this signal is asserted, the DMAs can transmit data on to the LAN. If this signal is deasserted during transmission, the current frame will be completely transmitted and then transmission will be suspended.
FLTDIS	43	I	FILTER DISABLE: When this input is HIGH, the LAN filter is disabled and all frames are passed transparently.
LMODE[4:0]	66, 67, 68, 69, 70	I	LAN MODE: These input pins select one of the 25 possible LAN operation modes, as described in Table 4.

Table 1. Pin Description (Cont'd)

Name	Pin No.	Type	Description
/LNKINT	33	OD	LINK INTEGRITY: This open drain output pin is LOW, to indicate good link integrity on the TP port during TP mode of operation.
/WANTX	34	OD	WAN TRANSMITTING: This open drain output pin is LOW, to indicate that transmission of data is taking place over the link.
/WANRX	35	OD	WAN RECEIVING: This open drain output pin is LOW, to indicate that data is being received from the link.
/LANTX	37	OD	LAN TRANSMITTING: This open drain output pin is LOW, to indicate that the LAN is transmitting.
/LANRX	38	OD	LAN RECEIVING: This open drain output pin is LOW, to indicate that the LAN is receiving data.
/COLL	39	OD	COLLISION: This open drain output pin is LOW, to indicate that a collision has occurred on the LAN.
/ERR	41	OD	ERROR: This open drain output pin is LOW, to indicate that an error has occurred in the bridge, for instance buffer overrun, FIFO overrun/underrun.
LP1	80	O	PHASE DETECTOR OUTPUT: This pin is the output from the phase detector and is connected to an external loop filter.
LP2	79	I	VCO INPUT: This pin is the input to the VCO, and it is connected to an external loop filter.
PLLVDD	76	I	PLL POWER: This pin must be connected to the board's power supply via signal traces that are kept as short as possible.
PLLVSS	77	I	PLL GROUND: This pin must be connected to the board's ground via signal traces as close as possible to the power supply.
PLLAGND	78	O	PLL ANALOG GROUND: This pin must be connected to the board's ground via signal traces as close as possible to the power supply.
XIN	82	I	CRYSTAL INPUT: A 40 MHz crystal must be connected between XIN and XOUT. Alternatively, a clock oscillator may be connected to this pin. This clock is used to drive all the ChipBridge's internal circuitry and CLKOUT output.
XOUT	81	O	CRYSTAL OUTPUT: A 40 MHz crystal must be connected between XIN and XOUT. If a clock oscillator was connected to XIN, then this pin should stay unconnected.
CLKOUT	93	O	CLOCK OUTPUT: This is the 20 MHz master clock output.
/RESET	84	I	RESET: This active low input is the ChipBridge ASIC reset input. When asserted LOW, all registers are initialized to a known state.
VDD	1, 30, 42, 51, 71, 72, 74, 85, 99	I	POSITIVE SUPPLY VOLTAGE
GND	13, 23, 32, 36, 40, 46, 53, 54, 75, 83, 86, 94	I	GROUND

FUNCTIONAL DESCRIPTION

The ChipBridge performs the bridging function at the MAC (Medium Access Control) level and is transparent to higher level protocols such as TCP/IP, DECnet and IPX, and operating systems such as NetWare and MS LAN manager. It automatically learns all the addresses of the LAN it is connected to. Only broadcasts, multicasts, or frames that are destined for another LAN are forwarded to the WAN.

Filtering and forwarding is performed at the maximum theoretical rate of 15,000 pps. Filtering can be disabled if required, by asserting the FLTDIS signal. This feature is useful for extending the physical limits of a network without incurring the penalties associated with using repeaters.

The ChipBridge's LAN table can store up to 10,000 addresses. The aging mechanism automatically deletes entries, if no frames have been received from that station for 5 minutes. The ChipBridge buffer can hold 256 frames, with a throughput latency of 1 frame.

WAN CONTROLLER

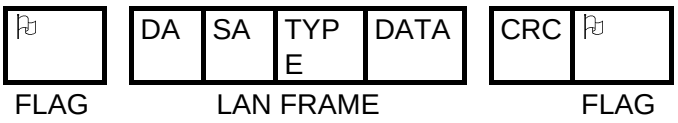
The HDLC WAN controller can be configured to operate in synchronous or asynchronous modes.

The synchronous HDLC protocol is a bit-oriented protocol, where data is transmitted in frames. Each frame starts and ends with a flag, which is the binary sequence 0111 1110 (0x7E). All frames contain a 16-bit Cyclic Redundancy Check (CRC) field. In synchronous mode, zero-bit insertion is used, to allow the contents of a frame to be transparent. Zero-bit insertion means that a binary 0 is inserted after a succession of five ones within a frame (between flags).

In asynchronous mode, HDLC-like framing is used in accordance with RFC 1662. It is an octet-oriented protocol, where each frame starts and ends with the flag sequence (0x7E). Octets are transmitted LSB first, with one start bit, eight bits of data, and one stop bit. All frames contain a 16-bit Cyclic Redundancy Check (CRC) field.

Octet stuffing is used for frame transparency in asynchronous mode. Octet stuffing is a procedure where a flag sequence, Control Escape octet (0x7D), or any octet that appears in the Async-Control-Character-Map (ACCM) is replaced by a two-octet sequence consisting of the Control Escape octet followed by the original octet XORed with 0x20. The ACCM comprises the first 32 characters (up to 0x20). It can be enabled or disabled (characters are transmitted as is) by asserting the ACCM signal.

The diagram below shows the structure of the frames transmitted over the WAN. Frame boundaries are defined by flags and all frames are transmitted with a 16-bit CRC. The 32-bit LAN CRC is not transmitted over the WAN.



Enhanced Tinygram Compression increases data throughput. Valid Ethernet frames have a minimum length of 64 bytes. Frames shorter than 64 bytes are padded. With compression enabled (by asserting the COMPR signal), these padding bytes are stripped off before being transmitted over the WAN, and repadded while being received on the other side.

The example below shows the difference between a typical Ethernet frame before and after compression.

Before compression:

	DA	SA	Type	DATA	PADDING
Bytes:	6	6	2	20	26

After compression:

	DA	SA	Type	DATA
Bytes:	6	6	2	20

In asynchronous mode, the three input lines BAUD2, BAUD1 and BAUD0 determine the internal baud rate generator frequency. This frequency can be configured to generate standard frequencies in the range 9.6 kbps to 115.2 kbps, or bypassed when using an external clock, as shown in the table below.

Table 2. Internal Baud Rate Generator Selection

BAUD RATE	BAUD2	BAUD1	BAUD0
External Clock	1	1	1
115.2 K	1	1	0
57.6 K	1	0	1
38.4 K	1	0	0
28.8 K	0	1	1
19.2 K	0	1	0
14.4 K	0	0	1
9.6 K	0	0	0

LAN CONTROLLER

The ChipBridge's CSMA/CD LAN controller fully complies with the IEEE 802.3 Ethernet standard. It integrates a Media Access Controller (MAC) and Manchester Encoder-Decoder (ENDEC) to enable a number of different physical connection schemes.

The MAC takes care of all the required functions, such as framing, preamble generation and stripping, addressing, error detection, medium allocation and contention resolution. The ENDEC incorporates the receiver, transmitter, collision, heartbeat, loopback and link integrity blocks, required to implement an IEEE 802.3 compliant AUI or 10BASE-T interface. A smart squelch function is implemented on the receive lines to ensure that noise is not mistaken for a valid signal. The complete physical media interface is achieved with only the addition of passive external components (see *Figures 16, 17 and* 18 at the end of this data sheet).

LAN interface pins are divided into two groups; Manchester encoded pins (used for the AUI and 10BASE-T interfaces) and NRZ pins.

There are 25 LAN interface modes selected via the LMODE input lines (see *Table 4*). In addition to the common modes of operation (such as AUI, UTP half duplex and UTP full duplex), non-standard modes are available for custom applications and glueless connection to most LAN chips. LAN interface modes enable either the Manchester or the NRZ pins, or combinations of the two. Certain NRZ pins can be defined either as inputs or as outputs. LAN interface modes can be grouped into three categories: AUI, UTP and NRZ.

AUI Group

The AUI group has two categories: AUI-DTE and AUI-DCE. The differences between the two categories are summarized below:

	AUI-DTE	AUI-DCE
Collision	Input	Output
Receive Data Loopback	No	Yes (if selected)
SQE Test (heartbeat)	Not applicable	Generated (if selected)

The AUI-DCE mode is used when connecting the ChipBridge directly to a station or a hub, without the need for additional interface circuitry. In this mode, the ChipBridge can draw its power from the AUI interface.

In AUI-DCE mode, the ChipBridge behaves like a MAU, in compliance with IEEE 802.3. It generates collisions, and (optionally) loops the received data back. In addition, the SQE test (heartbeat) can be enabled or disabled. SQE test is a self-test feature invoked at the end of each transmission by the DCE. It indicates to the DTE that the collision circuitry is intact and functioning and that the transmission has been recognized. SQE test should be disabled when the ChipBridge is connected to a repeater.

The AUI-DTE mode is the Attachment Unit Interface as defined by IEEE 802.3. It is typically used for connecting the ChipBridge to alternative media types, such as coax and fiber optics. External transceivers can be connected to the AUI port to support the 10BASE-2, 10BASE-5 and 10BASE-F standards.

In addition to AUI-DTE and AUI-DCE, other modes exist, that combine NRZ and Manchester signals. AUI-DTE-EXT-CDT and AUI-DCE-EXT-CDT allow NRZ control of the collision signal via the CDT input.
In AUI-DTE-EXT-RXD and AUI-DCE-EXT-RXD modes, the NRZ RXD input is the receive data input and the Manchester receive data is ignored. AUI-DCE-NLB disables the receive data loopback in DCE mode.

UTP Group

The ChipBridge contains a built-in 10BASE-T transceiver. An IEEE 802.3 compliant 10BASE-T interface is achieved with only the addition of passive external components
(see *Figure 16*). The ChipBridge also supports full-duplex mode (UTP-FDX).

UTP-EXT-CDT allows NRZ control of the collision signal via the CDT input.
In UTP-EXT-RXD mode, the NRZ RXD input is the receive data input and the Manchester receive data is ignored.

In the UTP modes, the polarity of the received signal is automatically corrected if reversed, as in the case of a wiring error.

NRZ Group

The NRZ modes are for interfacing with other Ethernet chips, such as multi-port repeaters or LAN controllers. Signals are at TTL levels. LRXD, LCRS and LCDT are either inputs or outputs, depending on the LAN mode selected (see *Table 4*). A number of NRZ modes are available for glueless connection to the most common LAN chips available, as summarized in the table 3.

Table 3. NRZ Modes Selection

Mode	Description	LAN Controller Compat-ibility	NRZ: LMODE [4..0]	NRZ-FDX: LMODE [4..0]
1	TxD, RxD: rising edge RTS, CRS, CDT: active low		01101	01111
2	TxD, RxD: rising edge RTS, CRS, CDT: active high	NATIONAL, AMD, MOTOR-OLA	11100	11111
3	TxD, RxD: falling edge RTS, CRS, CDT: active low	INTEL, AT&T	11101	10111
4	TxD, RxD: falling edge RTS, CRS, CDT: active high		01100	00111
5	TxD, RxD: falling edge RTS, CRS: active high CDT: active low	FUJITSU	11001	

Table 4. LAN Interface Operation Modes

Important Note: The polarity of the NRZ signals for modes not specified in Table 3 is as for mode 1.

LMODE [4..0]	DESCRIPTION	NRZ					MANCHESTER	
		LTXD	LRXD	LCDT	LCRS	RXD	TXD	TXP/CO
00000	AUI-DTE	tx data only	output	output	output	receive data	tx data only	not used
01000	AUI-DTE-EXT-CDT (AUI-DTE with external CDT)	tx data only	output	input	output	receive data	tx data only	not used
00010	AUI-DTE-EXT-RXD (AUI-DTE with external RxD)	tx data only	input	output	input	ignored	tx data only	not used
00011	AUI-DCE (regular AUI-DCE)	tx data only	output	output	output	receive data	tx and rx data looped back	collision generated no SQE
00100	AUI-DCE-NLB (AUI-DCE with no loopback)	tx data only	output	output	output	receive data	tx data only	collision generated no SQE
00101	AUI-DCE-EXT-CDT (AUI-DCE with external CDT)	tx data only	output	input	output	receive data	tx and rx data looped back	collision generated no SQE
00110	AUI-DCE-EXT-RXD (AUI-DCE with external RxD)	tx data only	input	output	input	ignored	tx and rx data looped back	collision generated no SQE
00001	UTP (regular 10BASE-T)	tx data only	output	output	output	receive data	tx data only	pre-emphasis only
10001	UTP-FDX (Full-duplex UTP)	tx data only	output	output	output	receive data	tx data only	pre-emphasis only
01001	UTP-EXT-CDT (UTP with external CDT)	tx data only	output	input	output	receive data	tx data only	pre-emphasis only
01011	UTP-EXT-CDT-RXD (UTP with external CDT and RXD)	tx data only	input	input	input	ignored	tx data only	pre-emphasis only
01101	NRZ (Mode 1)	tx data only	input	input	input	ignored	tx data only	not used
11100	NRZ (Mode 2)	tx data only	input	input	input	ignored	tx data only	not used
11101	NRZ (Mode 3)	tx data only	input	input	input	ignored	tx data only	not used
01100	NRZ (Mode 4)	tx data only	input	input	input	ignored	tx data only	not used

Table 4. LAN Interface Operation Modes (Cont'd)

LMODE [4..0]	DESCRIPTION	NRZ					MANCHESTER	
		LTXD	LRXD	LCDT	LCRS	RXD	TXD	TXP/CO
11001	NRZ (Mode 5	tx data only	input	input	input	ignored	tx data only	not used
01110	NRZ-LB (TTL with loopback)	tx data only	input	input	input	ignored	tx and rx data looped back	not used
01111	NRZ-FDX (Mode 1)	tx data only	input	input	input	ignored	tx data only	not used
11111	NRZ-FDX (Mode 2)	tx data only	input	input	input	ignored	tx data only	not used
10111	NRZ-FDX (Mode 3)	tx data only	input	input	input	ignored	tx data only	not used
00111	NRZ-FDX (Mode 4)	tx data only	input	input	input	ignored	tx data only	not used
10011	AUI-DCE-SQE (regular AUI-DCE with SQE enabled)	tx data only	output	output	output	receive data	tx and rx data looped back	collision generated SQE generated
10100	AUI-DCE-NLB-SQE (AUI-DCE with no loopback and SQE enabled)	tx data only	output	output	output	receive data	tx data only	collision generated SQE generated
10101	AUI-DCE-EXT-CDT-SQE (AUI-DCE with external CDT and SQE enabled)	tx data only	output	input	output	receive data	tx and rx data looped back	collision generated SQE generated
10110	AUI-DCE-EXT-RXD-SQE (AUI-DCE with external RXD and SQE enabled)	tx data only	input	output	input	ignored	tx and rx data looped back	collision generated SQE generated

DRAM

The ChipBridge has a built in DRAM controller to allow glueless connection to a 256k x 16 DRAM. It supports CAS-before-RAS and RAS-only refresh cycles and all other necessary timing required by the DRAM.

DRAM access speed should be 60 ns or faster. Any of the following DRAMS are recommended.

	Part Number	Manufacturer
1.	MT4C16257	Micron
2.	M5M44260	Mitsubishi
3.	MCM54260B	Motorola
4.	MB814260	Fujitsu

VISUAL STATUS MONITORING

Seven high drive, open drain, status signals are provided for direct connection of LEDs. These signals provide status indications of link integrity (UTP mode only), WAN and LAN activity, collisions, and system errors.

CLOCK GENERATION

The ChipBridge has a built-in crystal oscillator. The system clock can be generated by external connection of a crystal and RC network, or an external clock source. If an external clock source is used, XIN should be driven and XOUT left floating. If a crystal and RC network is used, see *Figure 15* for connection details.

PLL LOOP FILTER

For the PLL to operate properly, an external loop filter is required. See *Figure 15* for details of the external loop filter.

EVALUATION BOARD

A full featured evaluation board can be ordered separately. The evaluation board contains a complete ChipBridge system, including AUI and UTP LAN media interfaces, LAN NRZ port, an RS-232 WAN interface and status LEDs. The WAN port is also available at TTL levels for connection to physical interfaces other than RS-232.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

- **Storage Temperature**
  -65 °C to + 150 °C
- **Ambient Temperature Under Bias**
  -40 °C to +85 °C
- **Supply Voltage**
  -0.3V to + 6.0V
- **Inputs**
  -0.5V to VDD + 0.5V

OPERATING RANGE

- **Operating Temperature**
  -40 °C to +85 °C
- **Supply Voltage**
  5V +/- 5%
- **Inputs**
  VDD + 0.5V < VIN < VSS - 0.5V

Table 5. DC Characteristics (Over Operating Range)

Symbol	Parameter Description	Test Condition	Min	Type	Max	Unit
V_{IL}	Voltage Input LOW (CMOS levels) - see note 1		VSS		0.3 VDD	V
V_{IH}	Voltage Input HIGH (CMOS levels) - see note 1		0.7 VDD		VDD	V
V_T	Switching Threshold (CMOS levels) - see note 1			2.5		V
V_{IL}	Voltage Input LOW (TTL levels) - see note 2		VSS		0.8	V
V_{IH}	Voltage Input HIGH (TTL levels) - see note 2		2.0		VDD	V
V_T	Switching Threshold (TTL levels) - see note 2			1.5		V
V_{IL}	Voltage Input LOW (PECL levels) - see note 3		VSS		3.3	V
V_{IH}	Voltage Input HIGH (PECL levels) - see note 3		4.1		VDD	V
V_{T+}	Schmitt trigger positive going threshold (CMOS levels) - see note 4			1.77	2.0	V
V_{T-}	Schmitt trigger negative going threshold (CMOS levels) - see note 4		1.0	1.5		V
V_{T+}	Schmitt trigger positive going threshold (TTL levels) - see note 5			2.0	2.25	V
V_{T-}	Schmitt trigger negative going threshold (TTL levels) - see note 5		0.8	1.04		V
V_{OH}	Voltage Output High	I_{OL}= -2 mA - see note 6 I_{OL}= -4 mA - see note 7 I_{OL}= -11 mA - see note 8 I_{OL}= -12 mA - see note 9 I_{OL}= -24 mA - see note 10	2.4 2.4 2.4 2.4 2.4			V V V V V
V_{OL}	Voltage Output Low	I_{OL}= 2 mA - see note 6 I_{OL}= 4 mA - see note 7 I_{OL}= 11 mA - see note 8 I_{OL}= 12 mA - see note 9 I_{OL}= 24 mA - see note 10		0.2 0.2 0.2 0.2 0.2	0.4 0.4 0.4 0.4 0.4	V V V V V
I_{OZ}	3-state Output Leakage Current	V_{OH} = VSS or VDD	-10	+/- 1	10	uA
I_{IN}	Input Current	V_{IN} = VSS or VDD	-10	+/- 1	10	uA
I_{OS}	Output S.C. Current - see note 11	VDD=5.25V, VO=VDD VDD=5.25V, VO=VSS	37 -117	90 -75	140 -40	mA mA
I_{DD}	Supply Current	V_{IN} = VSS or VDD			150	mA
C_{IN}	Input Capacitance		2.5			pF
C_{OUT}	Output Capacitance		2.0			pF

NOTES:

1. The following signals have CMOS input levels: ACCM, BAUD1, BAUD2, COMPR, WMODE, LMODE, FLTDIS, MD
2. The following signals have TTL input levels: LRXD, LCRS, LCDT, LCTS.
3. The following signals have PECL input levels: RXDTH+, RXDTH-, RXDIN, CITH+, CITH-.
4. The following signals have CMOS Schmitt trigger inputs: /RESET.
5. The following signals have TTL Schmitt trigger inputs: WTXC, WRXD, WCTS, WRXC.
6. Valid for the following outputs: MA, MD, /MWR, WTXD, WRTS, LTXD, LRTS, LRXD, LCRS, LCDT.
7. Valid for the following outputs: /RAS, /CAS, CLCK10M, CLKOUT.
8. Valid for the following output: XOUT
9. Valid for the following outputs: /LNKINT, /WANTX, /WANRX, /LANTX, /LANRX, /COLL, /ERR.
10. Valid for the following outputs: TXD+, TXD-, TXP+/CO+, TXP-/CO-.
11. Valid for the following outputs: CLCK10M, CLKOUT.

Table 6. AC Characteristics (Over Operating Range)

Symbol	Parameter Description	Test Condition	Min	Type	Max	Unit
t1	Clock low to address valid	C_L = 20 pF	0		4	ns
t2	Clock high to /RAS low	C_L = 20 pF	0		2	ns
t3	Clock low to /RAS high	C_L = 20 pF	0		2	ns
t4	Clock high to /CAS low	C_L = 20 pF	0		3	ns
t5	Clock low to /CAS high	C_L = 20 pF	4		11	ns
t6	Data setup time	C_L = 20 pF	8			ns
t7	Data hold time	C_L = 20 pF	1			ns
t8	Clock low to /MWR low	C_L = 20 pF	0		2	ns
t9	Clock low to /MWR high	C_L = 20 pF	0		2	ns
t10	Clock low to data valid	C_L = 20 pF			5	ns
t11	Clock low to data invalid	C_L = 20 pF	0		5	ns
t12	Clock high to /CAS low (refresh)	C_L = 20 pF	0		3	ns
t13	Clock high to /CAS high (refresh)	C_L = 20 pF	4		10	ns
t15	LCTS setup time	C_L = 50 pF	18			ns
t16	Clock high to LRTS asserted	C_L = 50 pF			5	ns
t17	Clock high to LTXD valid	C_L = 50 pF			8	ns
t18	LCRS setup time	C_L = 50 pF	25			ns
t19	LCRS hold time	C_L = 50 pF	0			ns
t20	LRXD setup time	C_L = 50 pF	8			ns
t21	LRXD hold time	C_L = 50 pF	-2			ns
t23	LCDT setup time	C_L = 50 pF	18			ns
t24	LCDT hold time	C_L = 50 pF	0			ns
t25	LCTS hold time	C_L = 50 pF	0			ns
t26	Clock high to LRTS disasserted	C_L = 50 pF			7	ns
t27	Clock high to LRXD valid	C_L = 50 pF			5	ns
t28	Clock high to LCRS asserted/disasserted	C_L = 50 pF			5	ns
t29	Clock high to LCDT asserted	C_L = 50 pF			7	ns
t30	Clock high to LCDT disasserted	C_L = 50 pF			9	ns
t31	TXD+ held high from last valid transition		300		350	ns
t32	SQE test from TXD inactive			800		ns
t33	CO+ held high from last valid transition			300		ns
t34	SQE test length			700		ns
t35	TXD+ to TXD- skew				0.5	ns
t36	SQE test signal period			100		ns
t40	WTXC, WRXC clock period	C_L = 50 pF	25			ns
t41	TXC, RXC width high	C_L = 50 pF	10			ns
t44	Tx Data delay time	C_L = 50 pF			15	ns
t45	WRXD setup time	C_L = 50 pF	0			ns
t46	WRXD hold time	C_L = 50 pF	5			ns

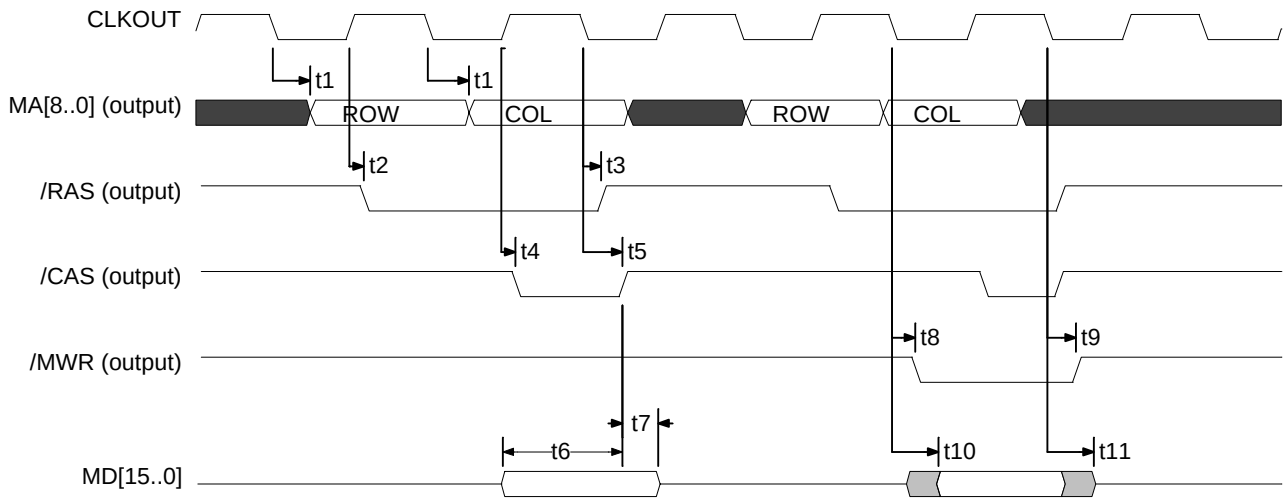


Figure 3. Single Cycle DRAM Read and Write Timing

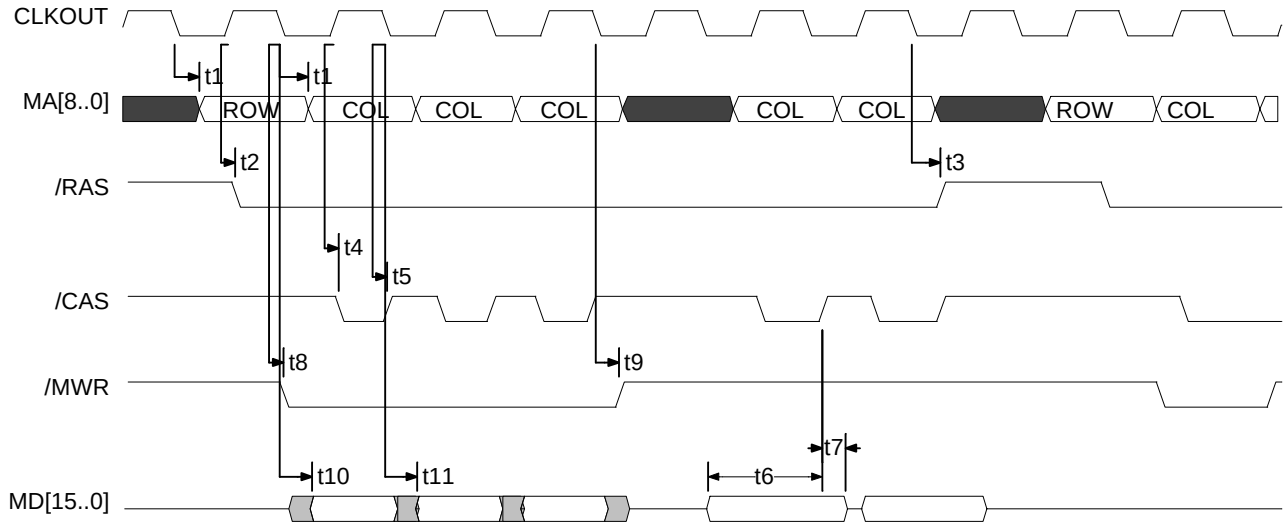


Figure 4. Burst-Mode DRAM Read and Write Timing

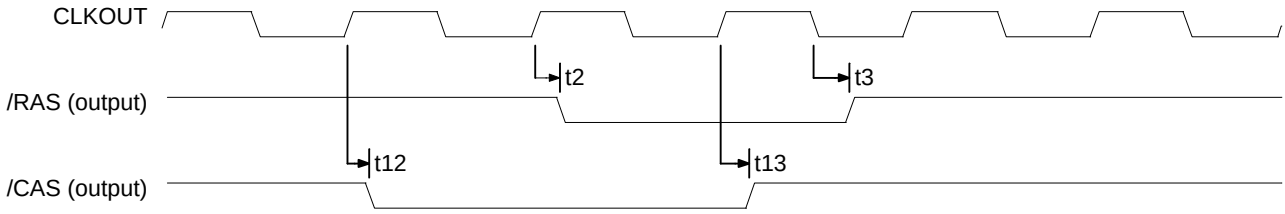


Figure 5. DRAM CAS-Before-RAS Refresh Timing

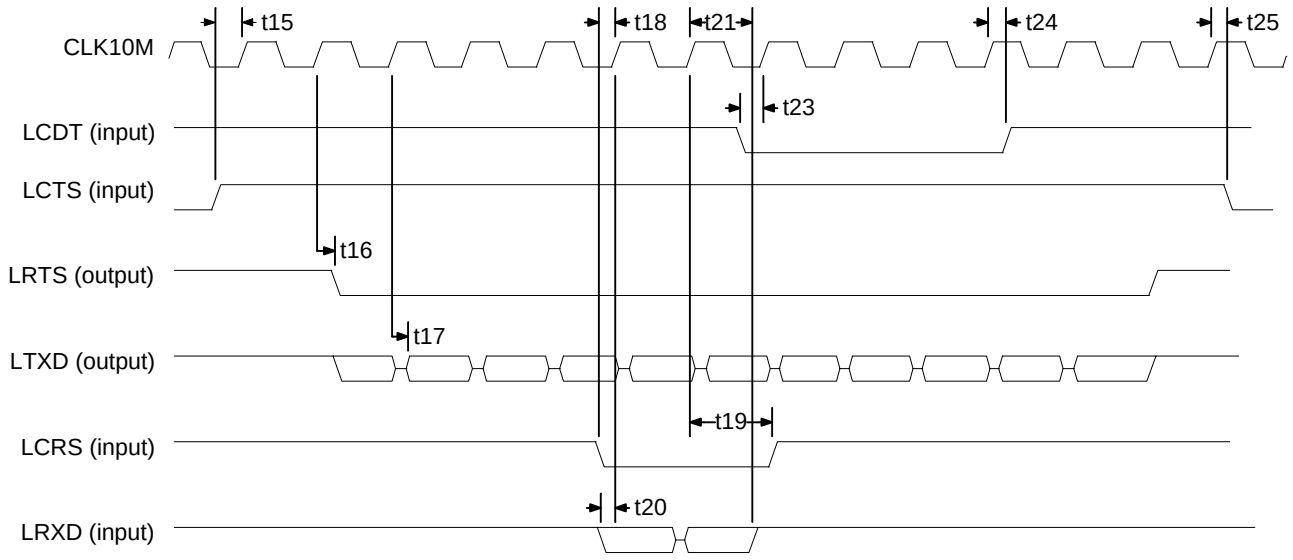


Figure 6. NRZ (Mode 1) Transmit and Receive Timing (inputs)

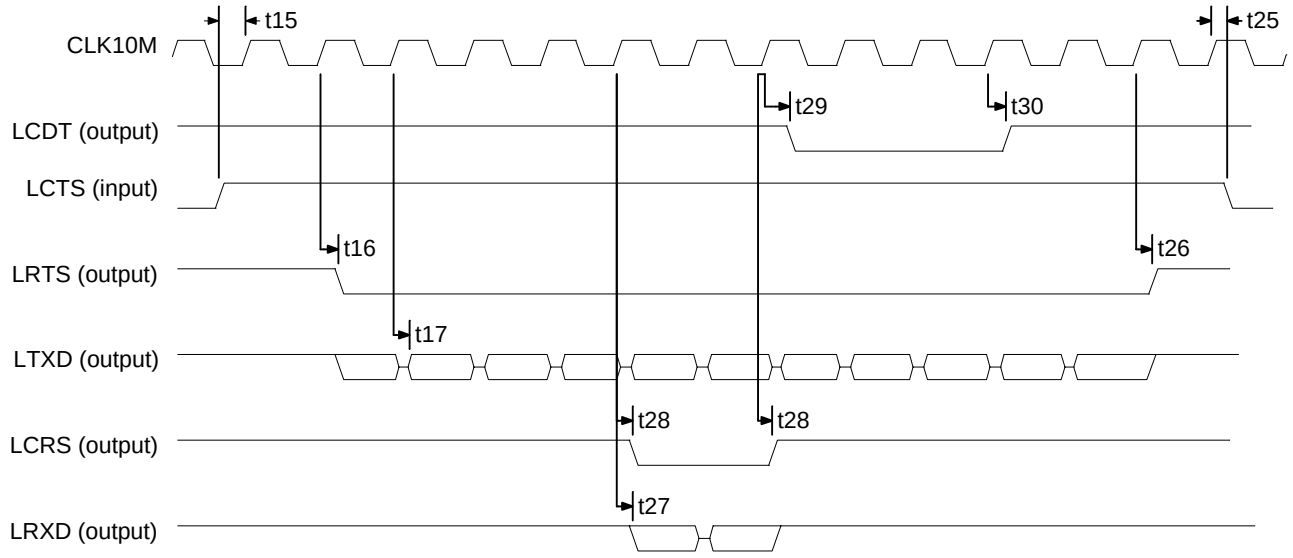


Figure 7. NRZ Transmit and Receive Timing (outputs)

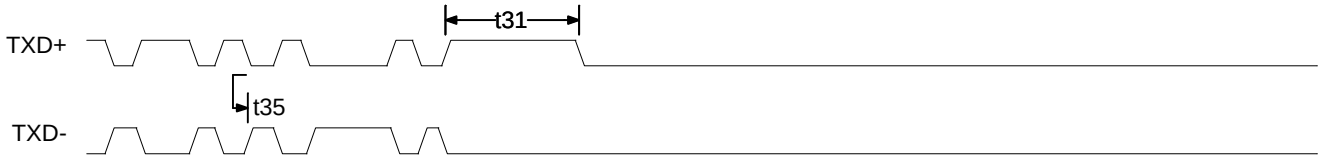


Figure 8. AUI-DTE Mode Timing

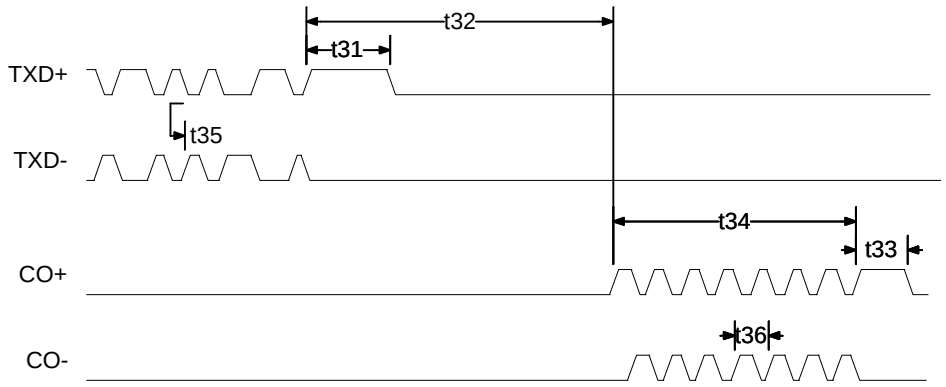


Figure 9. AUI-DCE Mode Timing

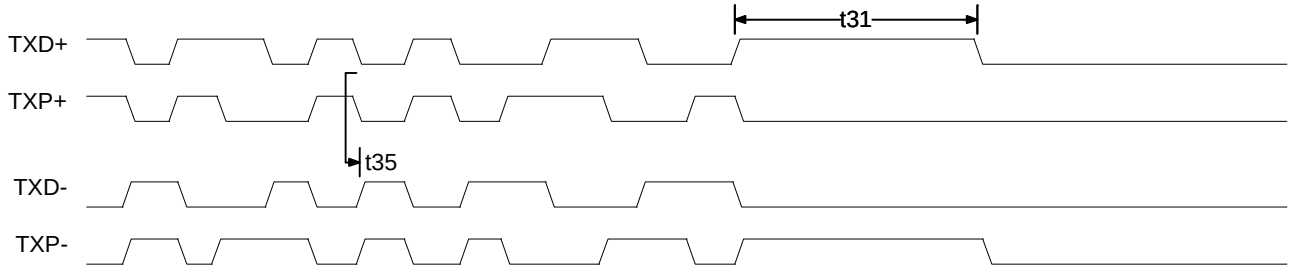


Figure 10. UTP Mode Timing

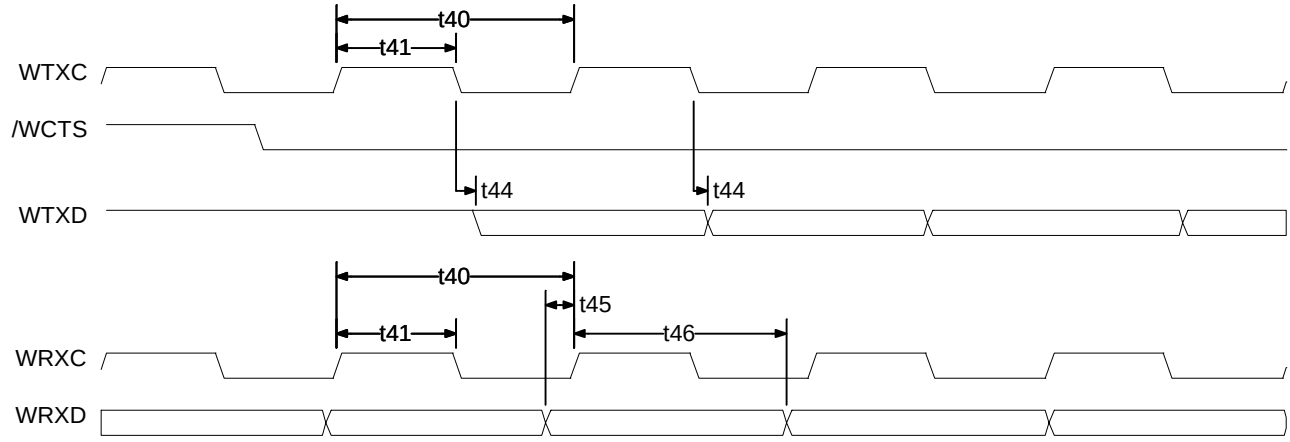
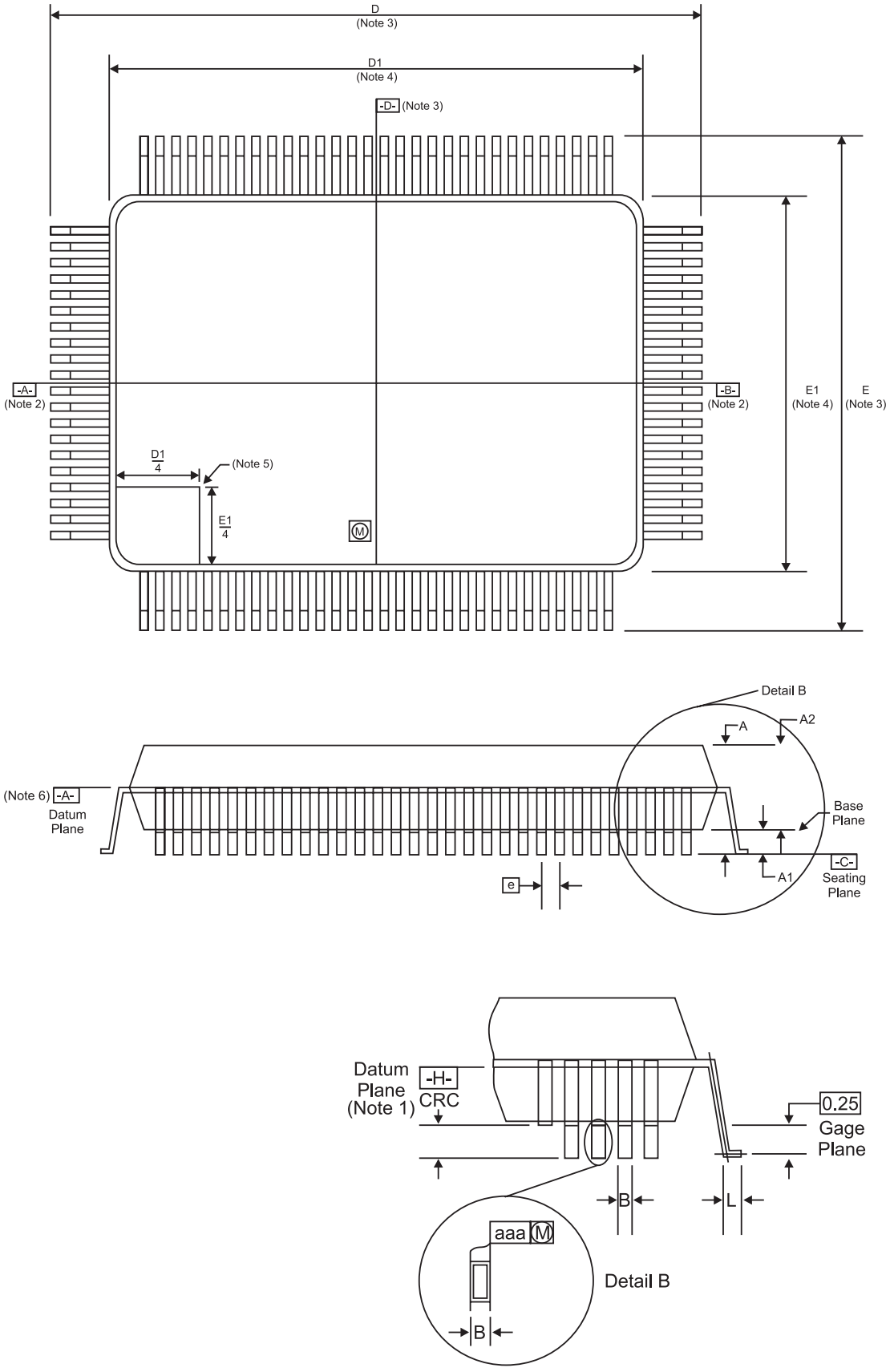


Figure 11. WAN Synchronous Mode Timing

MECHANICAL SPECIFICATIONS



Physical Dimensions

		mm	in
A	Max	3.4	(0.134)
A1	Min	0.25	(0.010)
A2	Min	2.55	(0.100)
	Max	3.05	(0.120)
B	Min	0.22	(0.009)
	Max	0.38	(0.015)
D	Min	23.65	(0.931)
	Max	24.15	(0.951)
D1	Min	19.90	(0.783)
	Max	21.10	(0.791)
e	BSC	0.65	(0.026)
E	Min	17.65	(0.695)
	Max	18.15	(0.715)
E1	Min	13.90	(0.547)
	Max	14.10	(0.555)
L	Min	0.65	(0.026)
	Max	1.15	(0.045)
aaa	Max	0.10	(0.004)
ccc	Max	0.10	(0.004)

Notes

1. Coplanarity is the difference between lead and the seating plane, -C-.
2. Datums A-B and -D- to be determined at datum plane -H-.
3. To be determined at seating plane -C-.
4. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm/0.010 in. per side. Dimensions D1 and E1 do not include mold mismatch and are determined at datum plane -H-.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.
6. Datum plane -H- is located at the mold parting line and it coincides with the bottom of the leads where the led exits the plastic body.

APPLICATIONS

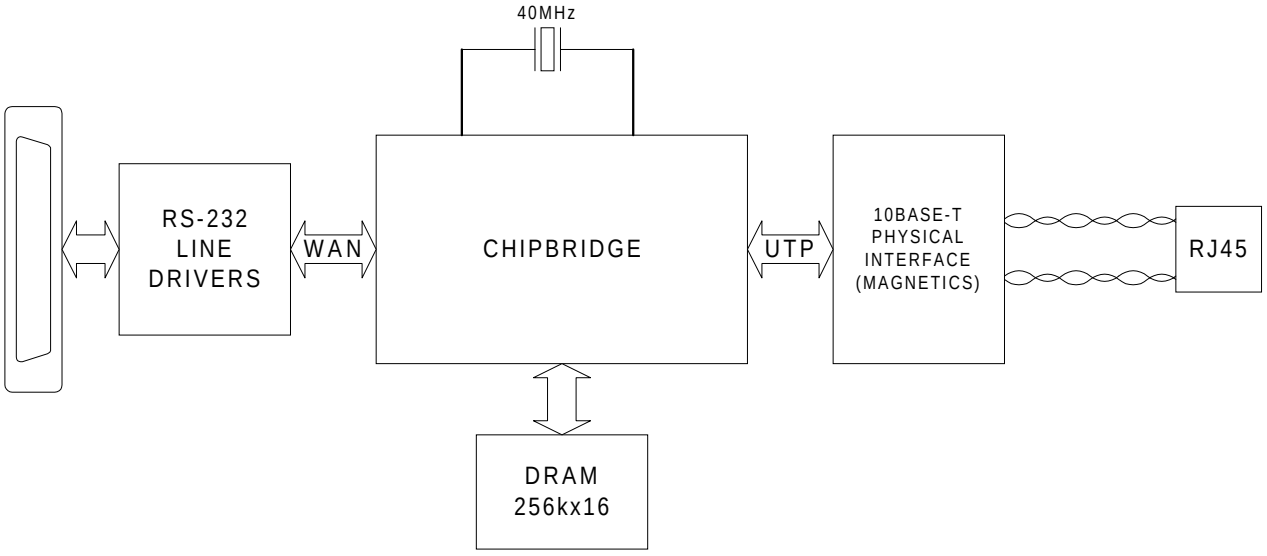


Figure 12. Remote Bridge

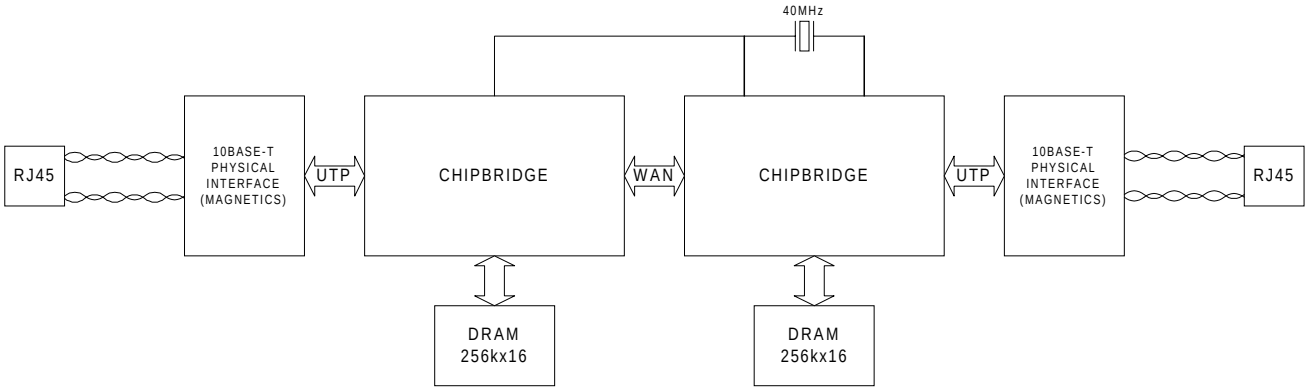


Figure 13. Local Bridge

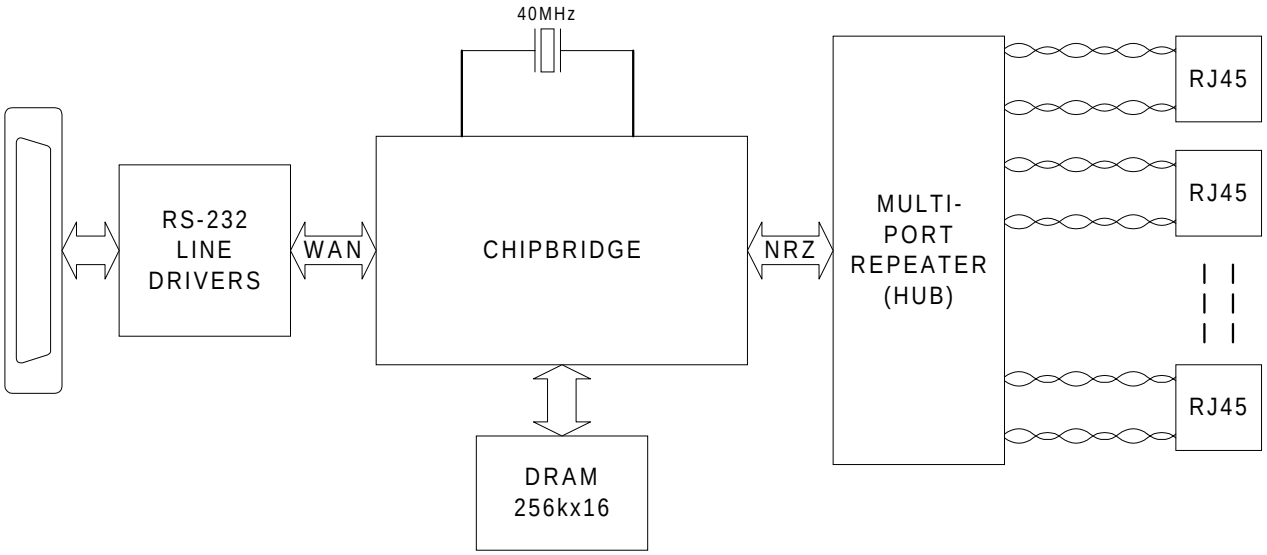


Figure 14. Connection to HUB

CHIPBRIDGE CONNECTION AND INTERFACES

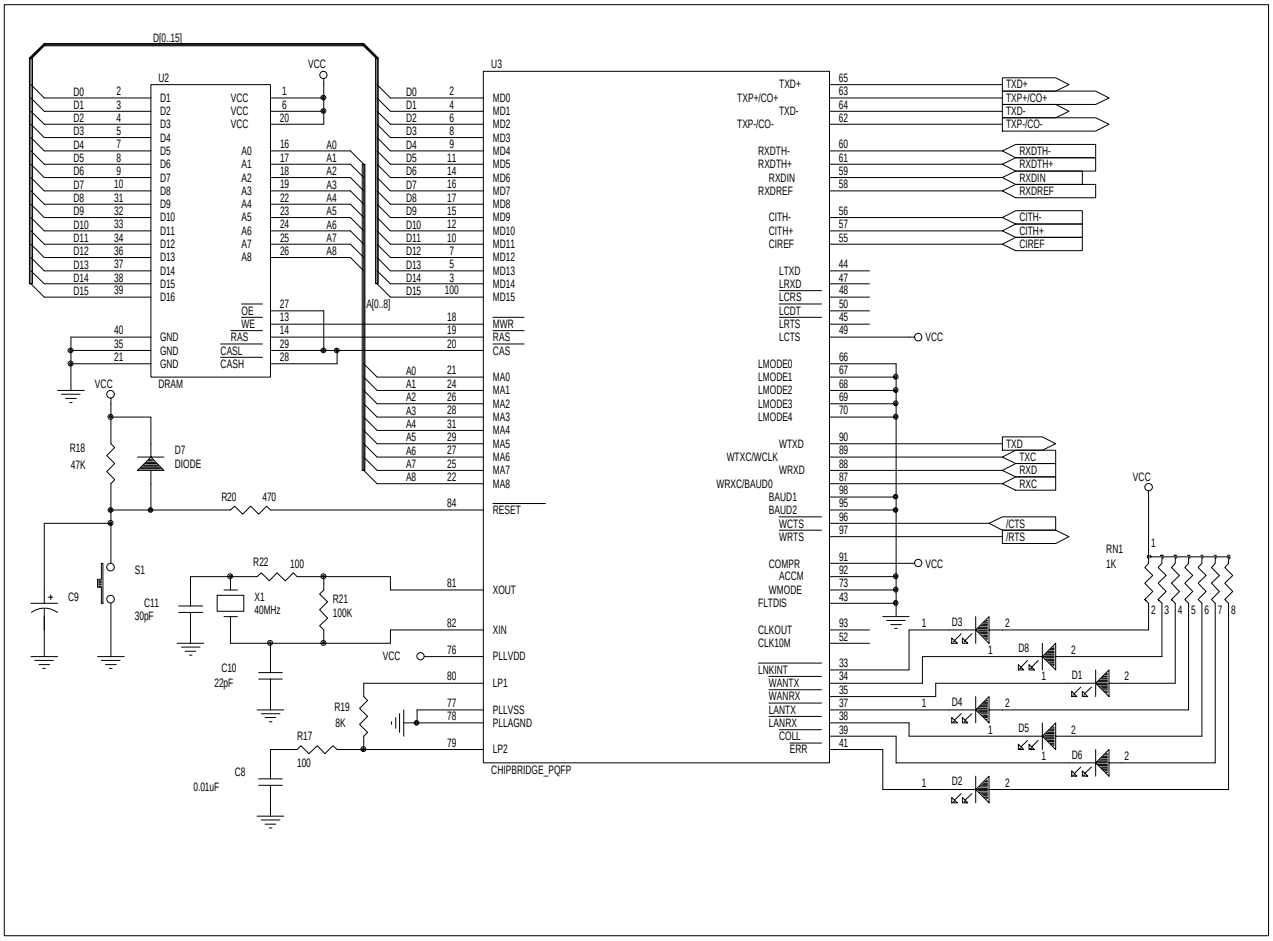


Figure 15. ChipBridge Connection

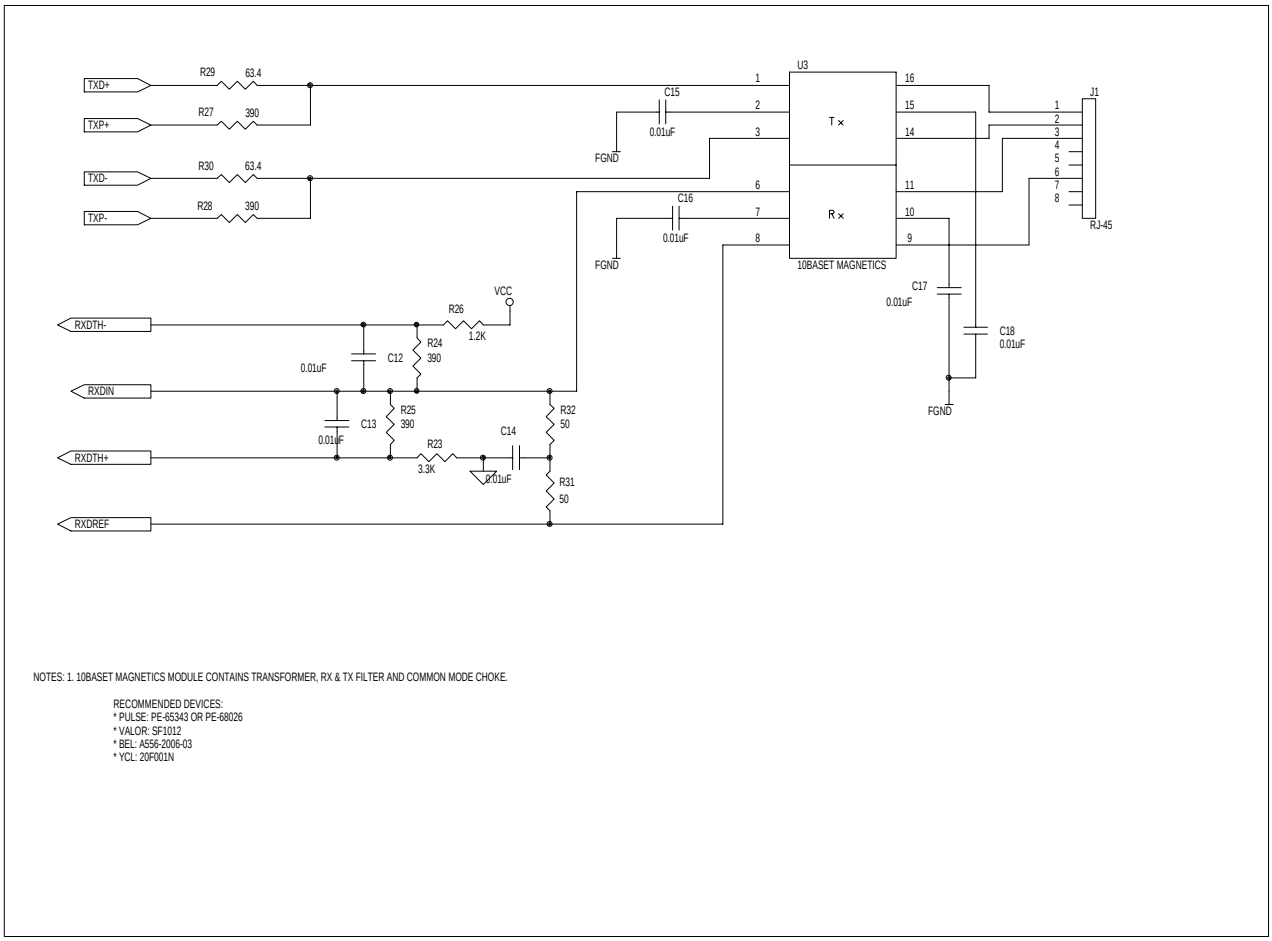


Figure 16. UTP Interface

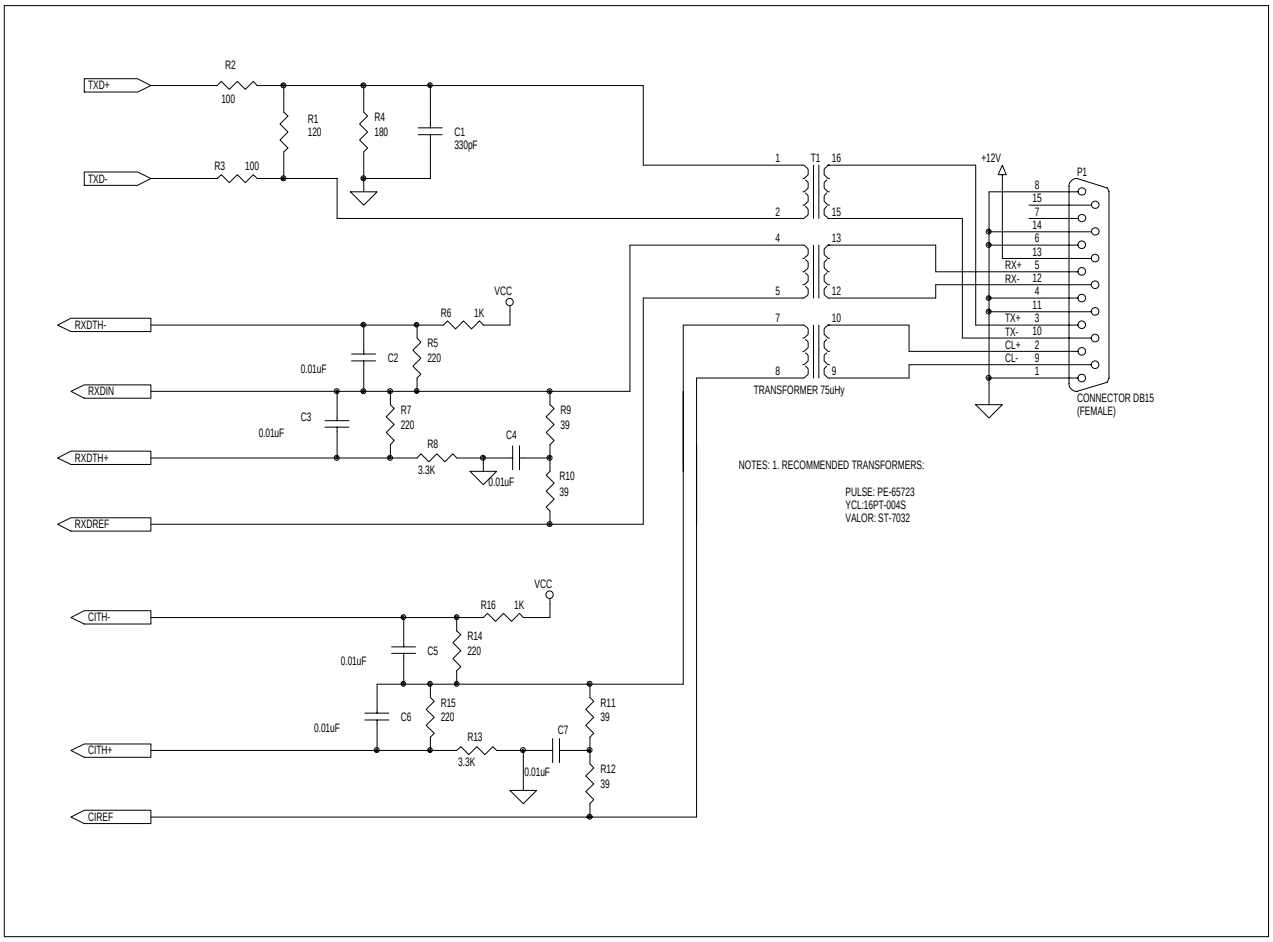


Figure 17. AUI-DTE Interface

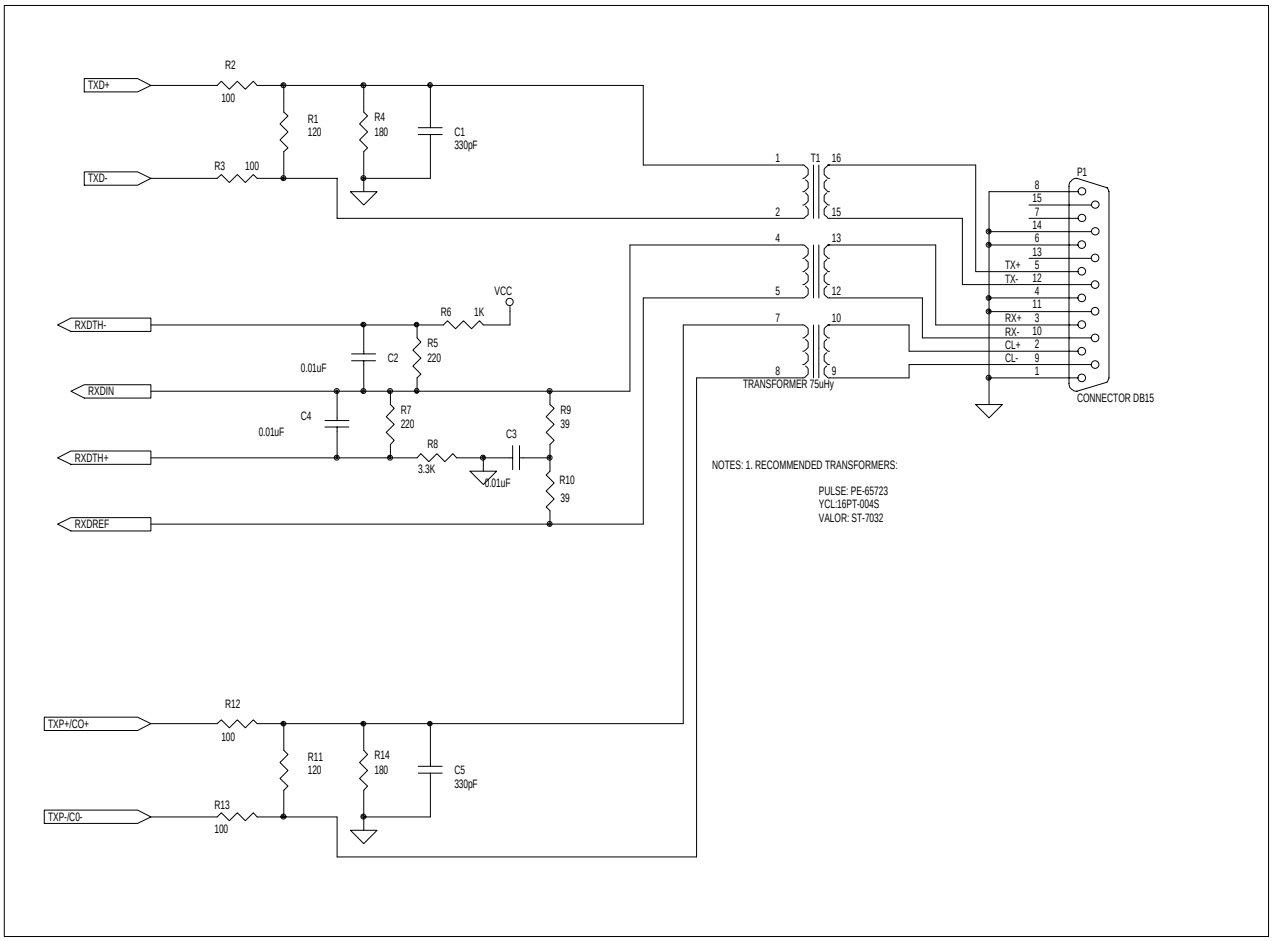


Figure 18. AUI-DCE Interface

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ORDERING

The ChipBridge is available in a 100 pin PQFP package. Use the following part numbers when ordering:

Description	Part Number
ChipBridge 100PQFP	IC-RJ017
ChipBridge Evaluation Board	RJ017-EVAL

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