

Applications

- Bluetooth™ wireless technology (Class 1)
- USB dongles
- PCMCIA, flash cards
- Access points
- 2.4GHz cordless telephone

Features

- +22.5 dBm at 45% Power Added Efficiency
- Low current 80 mA typical @ $P_{OUT} = +20$ dBm
- Temperature stability better than 1 dB over -40 °C to +85 °C
- Power-control and power-down modes
- 3.3 V single supply operation
- Small lead-free, plastic package: 6 lead QFN (1.6 mm x 3.0 mm)

Ordering Information

Part Number	Package	Remark
PA2423L	6 Pin QFN	Samples
PA2423L-R	6 Pin QFN	Tape & Reel
PA2423L-EV	Evaluation Kit	

Product Description

A monolithic, high-efficiency, silicon-germanium power amplifier IC, the PA2423L is designed for 2.4GHz wireless applications, including Bluetooth™ Class1 and 2.4 GHz cordless telephone applications. It delivers +22.5 dBm output power with 45% power-added efficiency, making it capable of overcoming insertion losses of up to 2.5 dB between amplifier output and antenna input.

The PA2423L contains an analog control input for improving PAE at reduced output power levels.

The PA2423L provides a digital control input for controlling power up and power down modes of operation.

An on-chip ramping circuit provides the turn-on/off switching of amplifier output with less than 3dB overshoot, meeting the Bluetooth™ specification 1.1.

The PA2423L operates at 3.3 V DC. At typical output power level (+22.5 dBm), its current consumption is 125 mA.

The silicon/silicon-germanium structure of the PA2423L, and its exposed die-pad package, soldered to the system PCB, provide high thermal conductivity and a subsequently low junction temperature. This device is capable of operating at a duty cycle of 100 percent.

Functional Block Diagram

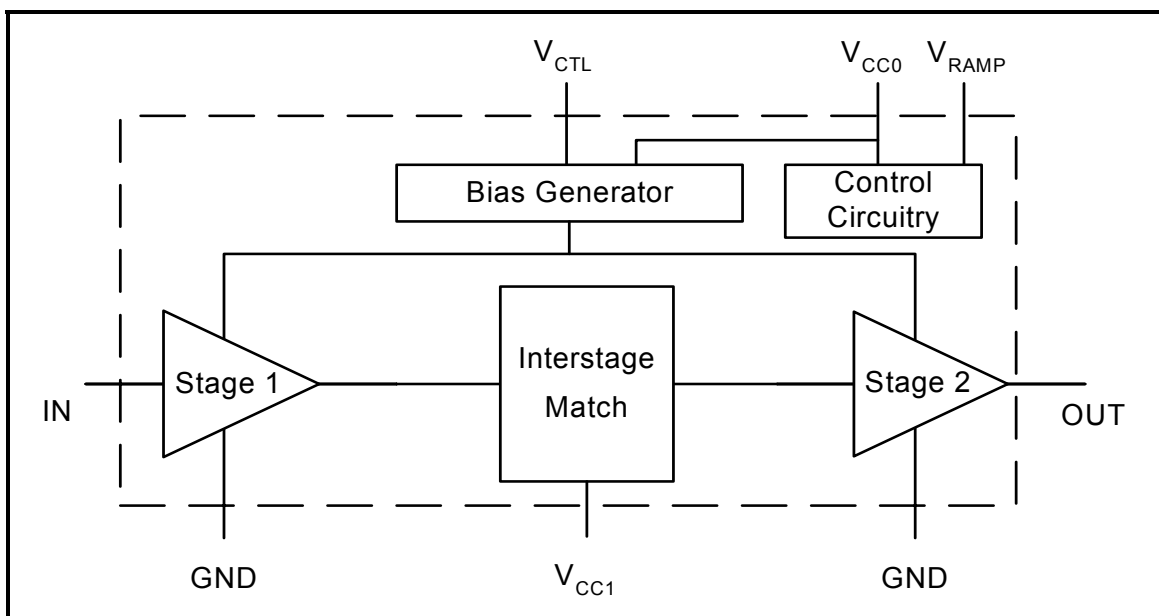


Figure 1: PA2423L Block Diagram

Pin Out Diagram

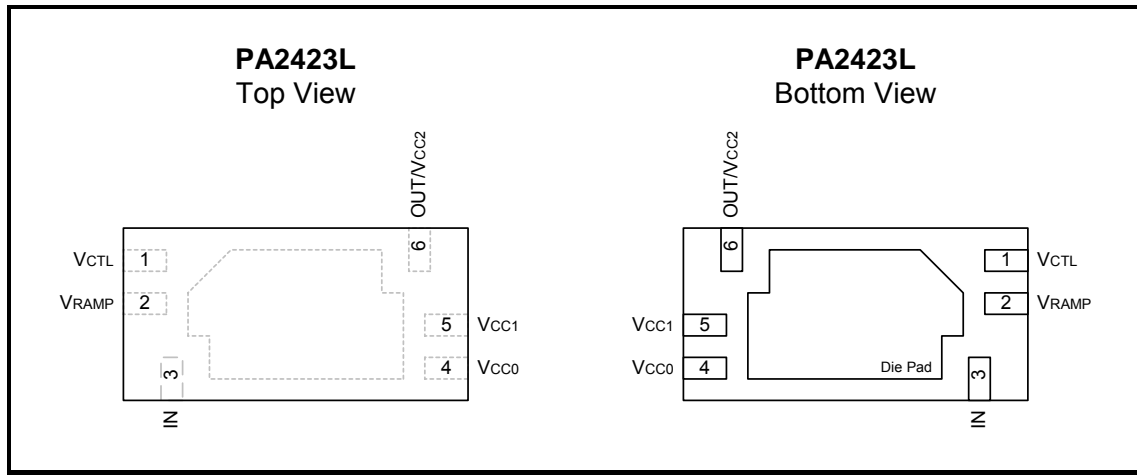


Figure 2: PA2423L Pin-Out Diagram

Pin Out Description

Pin No.	Name	Description
1	V _{CTL}	Controls the output level of the power amplifier. An analog control signal between 0V and V _{CC} varies the PA output power between minimum and maximum values
2	V _{RAMP}	Power Amplifier Enable pin. A digital control signal with logic high (power up) and logic low (power down) is used to turn the device on and off.
3	IN	Power amplifier RF input, external input matching network with DC blocking is required
4	V _{CC0}	Bias supply voltage
5	V _{CC1}	Stage 1 collector supply voltage, external inter-stage matching network is required
6	OUT/V _{CC2}	PA Output and Stage2 collector supply voltage, external output matching network with DC blocking is required
Die Pad	GND	Heatslug Die Pad is ground

Absolute Maximum Ratings

Operation in excess of any one of above Absolute Maximum Ratings may result in permanent damage. This device is a high performance RF integrated circuit with ESD rating < 600V and is ESD sensitive. Handling and assembly of this device should be at ESD protected workstations.

Symbol	Parameter	Min.	Max.	Unit
V _{CC}	Supply Voltage	-0.3	+3.6	V
V _{CTL}	Control Voltage	-0.3	V _{CC}	V
V _{RAMP}	Ramping Voltage	-0.3	V _{CC}	V
IN	RF Input Power		+8	dBm
T _A	Operating Temperature Range	-40	+85	°C
T _{STG}	Storage Temperature Range	-40	+150	°C
T _J	Maximum Junction Temperature		+150	°C

DC Electrical Characteristics

Conditions: V_{CC0} = V_{CC1} = V_{CC2} = V_{RAMP} = 3.3 V, V_{CTL} = 3.3V, P_{IN} = +2 dBm, T_A = 25 °C, f = 2.45 GHz, input and output externally matched to 50Ω unless otherwise noted.

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage		2.7	3.3	3.6	V
I _{CC}	Supply Current (I _{CC} = I _{VCC0} + I _{VCC1} + I _{VCC2}), V _{CTL} = 3.3 V	1		125	150	mA
ΔI _{CCtemp}	Supply Current variation over temperature from T _A = 25 °C (-40 °C < T _A < +85 °C)	3		25		%
V _{CTL}	PA Output Power Control Voltage Range		0		V _{CC}	V
I _{CTL}	Current sunk by V _{CTL} pin	1		200	250	μA
V _{RAMP}	Logic High Voltage	3	2.0			V
	Logic Low Voltage	3			0.8	V
I _{stdby}	Leakage Current when V _{RAMP} = 0 V, V _{CTL} = high, No RF Applied.	1		0.5	10	μA

AC Electrical Characteristics

Conditions: $V_{CC0} = V_{CC1} = V_{CC2} = V_{RAMP} = 3.3\text{ V}$, $V_{CTL} = 3.3\text{ V}$, $P_{IN} = +2\text{ dBm}$, $T_A = 25\text{ }^\circ\text{C}$, $f = 2.45\text{ GHz}$, input and output externally matched to 50Ω unless otherwise noted.

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
f_{L-U}	Frequency Range	3	2400		2500	MHz
P_{OUT}	Output Power @ $P_{IN} = +2\text{ dBm}$, $V_{CTL} = 3.3\text{ V}$	1	20	22.5		dBm
	Output Power @ $P_{IN} = +2\text{ dBm}$, $V_{CTL} = 0.4\text{ V}$	1		-20	0	dBm
ΔP_{temp}	Output Power variation over temperature ($-40\text{ }^\circ\text{C} < T_A < +85\text{ }^\circ\text{C}$)	3		1	2	dB
dP_{OUT}/dV_{CTL}	Control Voltage Sensitivity	3			120	dBm/V
PAE	Power Added Efficiency at +22.5 dBm Output Power			45		%
G	Gain @ $P_{IN} = -22\text{ dBm}$		25.5	26.5		dB
	Gain @ $P_{IN} = -10\text{ dBm}$	3	25.0	25.4		dB
	Gain @ $P_{IN} = -6\text{ dBm}$		23.5	24.0		dB
G_{VAR}	Gain Variation over band (2400-2500 MHz)	3		0.7	1.0	dB
2f,3f,4f,5f	Harmonics	3, 4		-40	-35	dBc
$IS_{21 I_{OFF}}$	Isolation in "OFF" State, $P_{IN} = +2\text{ dBm}$, $V_{RAMP} = 0\text{ V}$	2	15	20		dB
IS_{12I}	Reverse Isolation	2	32	42		dB
STAB	Stability ($P_{IN} = +2\text{ dBm}$, Load VSWR = 6:1)	2	All non-harmonically related outputs less than -50 dBc			

- Notes:**
- (1) Guaranteed by production test at $T_A = 25\text{ }^\circ\text{C}$.
 - (2) Guaranteed by design only
 - (3) Guaranteed by design and characterization
 - (4) Harmonic levels are greatly affected by topology of external matching networks.

Typical Performance Characteristics

Test Conditions: SiGe PA2423L-EV: $V_{CC0} = V_{CC1} = V_{CC2} = V_{RAMP} = 3.3$ V, $V_{CTL} = 3.3$ V, $P_{IN} = +2$ dBm, $T_A = 25$ °C, $f = 2.45$ GHz, input and output externally matched to 50Ω unless otherwise noted

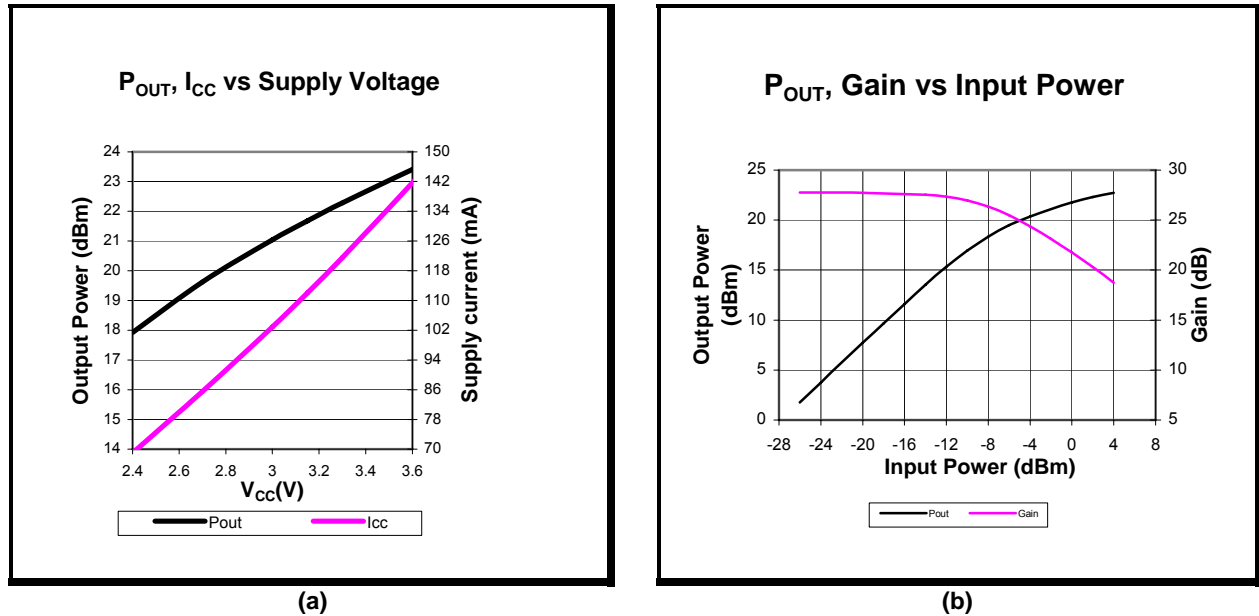


Figure 3: (a) P_{OUT}, I_{CC} vs. Supply Voltage, (b) P_{OUT}, Gain vs. Input Power

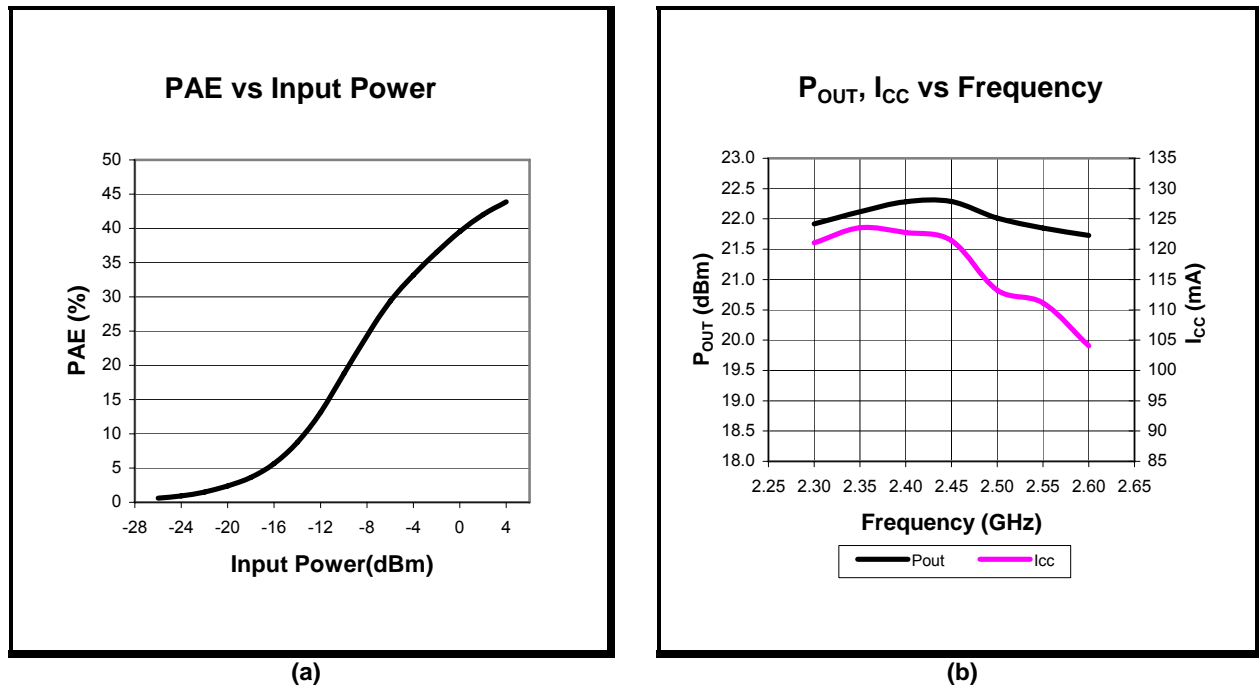


Figure 4: (a) PAE vs. Input Power, (b) P_{OUT}, I_{CC} vs. Frequency

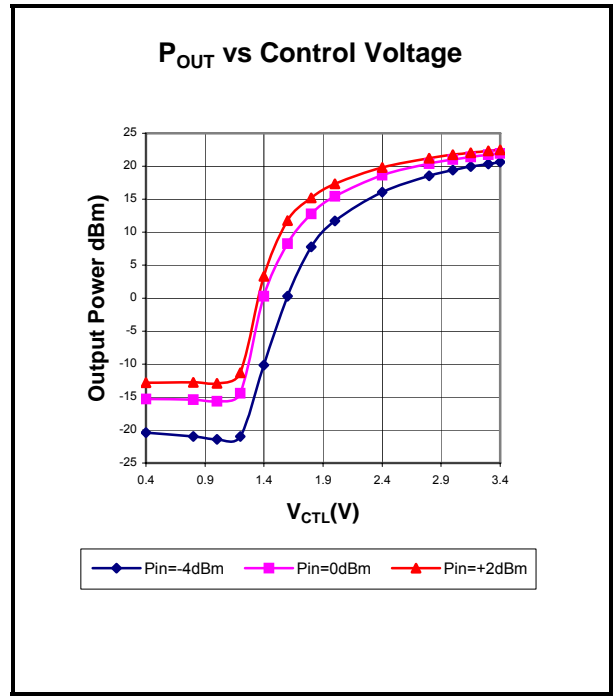
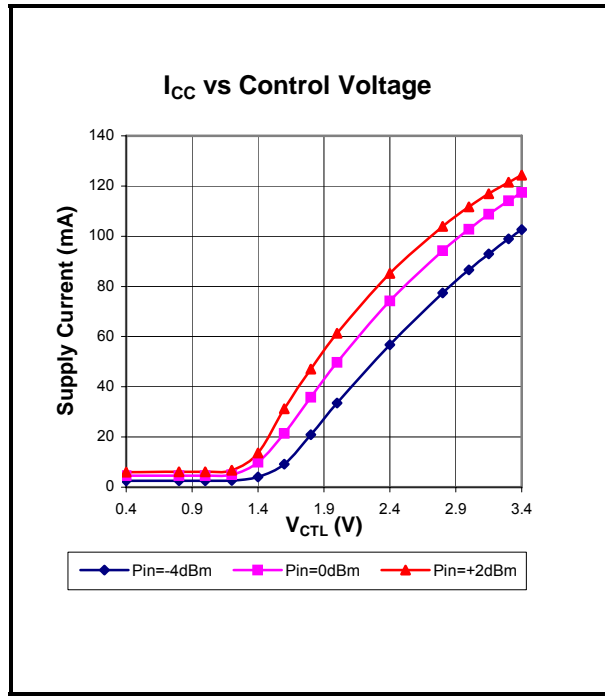


Figure 5: (a) I_{CC} vs. V_{CTL} over Input Power, (b) P_{OUT} vs. V_{CTL} over Input Power

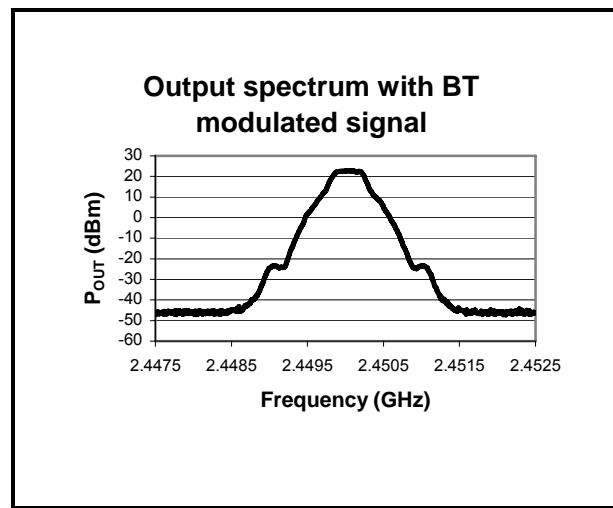
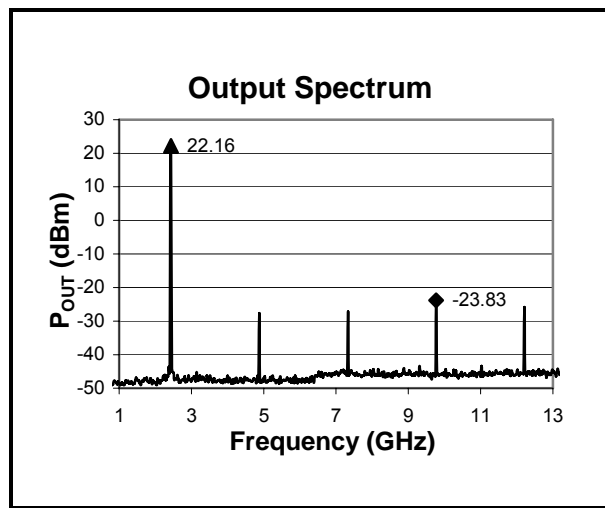


Figure 6: (a) Output Spectrum, (b) Output Spectrum with BT modulated signal

Applications Information

For test and design purposes, SiGe Semiconductor offers an evaluation board for the PA2423L. The order part number for the evaluation board is PA2423L-EV. The evaluation board is intended to simplify the testing with respect to RF performance of this power amplifier.

The application note, 13-APP-01 provides the supporting information for using the evaluation board. It contains information on the schematic, bill of materials and recommended layout for the power amplifier and the input and output matching networks. To assist in the design process, this layout is available, upon request, in gerber file format.

Using V_{RAMP}

V_{RAMP} is a digital pin used to power-up and power-down the PA2423L in Time Duplex systems such as Bluetooth™ 1.1. During receive mode, V_{RAMP} voltage is pulled down, PA2423L acts as a 25 dB isolation block between the radio and the antenna while consuming a modest 1 μ A. In transmit mode, V_{RAMP} voltage is pulled to V_{CC} and PA2423L offers 19 dB to 21 dB of large signal gain. The rise and fall time are in the order of 1-2 μ sec.

Using V_{CTL}

V_{CTL} is an analog pin that is designed to control the gain of PA2423L. Applying a voltage between 0 V and V_{CC} will adjust the gain between -15 dB and 21 dB. Used in combination with a variable drive level to PA2423L, the V_{CTL} function can greatly optimize the PAE of the system at all four Bluetooth™ transmitted power levels.

By applying approximately 1.4 V to V_{CTL} , for example, a Class1 radio can be modified to a Class2 radio with the PA2423L consuming only 15 mA.

By implementing a resistor DAC, the V_{CTL} pin can interface with Bluetooth™ transceivers offering digital and programmable outputs.

Package Dimensions

The PA2423L is packaged in a 1.6 mm x 3.0 mm 6 lead QFN package. The underside of the package is an exposed die-pad structure. This allows for direct soldering to the PCB for enhanced thermal conductivity. The package dimensions are shown in the drawing below.

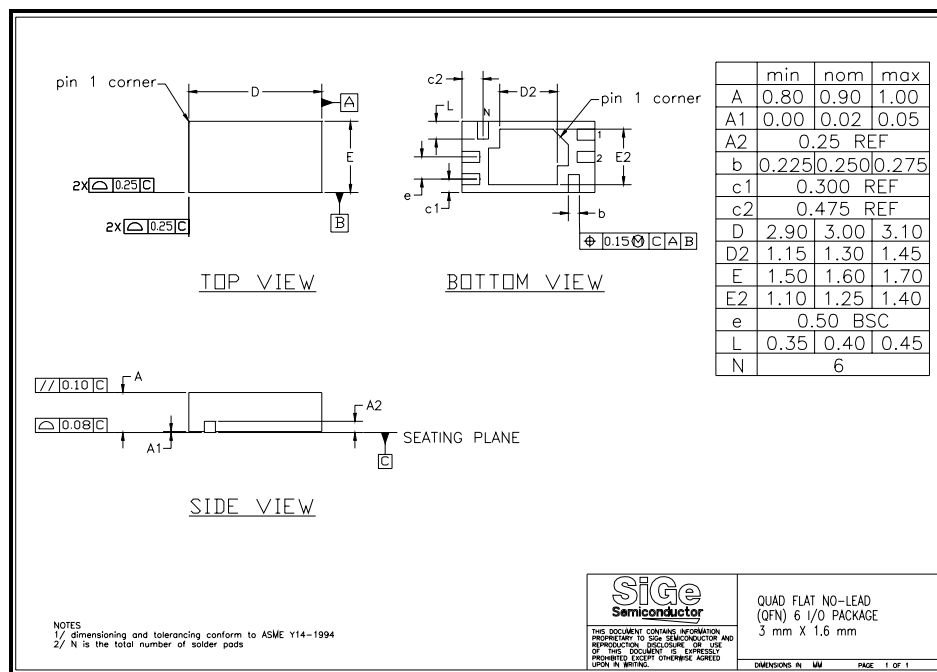


Figure 7: PA2423L Package Drawing

PA2423L 6-QFN PCB Footprint Layout

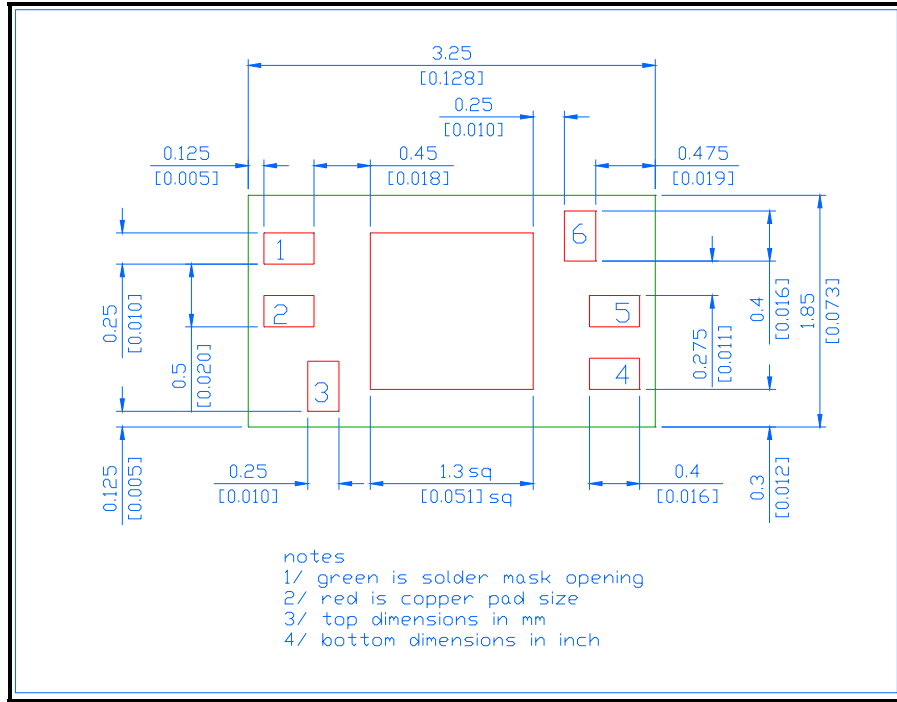


Figure 10: PA2423L PCB Footprint Layout

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Product Preview

The datasheet contains information from the product concept specification. SiGe Semiconductor, Inc. reserves the right to change information at any time without notification.

Preliminary Information

The datasheet contains information from the design target specification. SiGe Semiconductor, Inc. reserves the right to change information at any time without notification.

Production testing may not include testing of all parameters.

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