Integrated Mixed-Signal Solutions

STAC9750/51

Value-Line Two-Channel AC'97 Codecs with Headphone Drive and SPDIF Output

Data Sheet Revision 5.2

2-9750-D1-5.2-1003

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2. PRODUCT BRIEF

2.1. Features

- Full duplex stereo 18-bit ADC and 20-bit DAC
- AC'97 Rev 2.2-compliant
- High performance ΣΔ technology
- SPDIF output
- Crystal elimination circuit
- Headphone amplifier
- Independent sample rates for ADC & DACs (hardware SRCs)
- 20 or 30 dB microphone boost capability
- 90 dB SNR LINE-LINE
- 5-Wire AC-Link protocol compliance
- Digital-Ready architecture
- General purpose I/O
- +3.3V (STAC9751) and +5V (STAC9750) analog power supply options
- Pin compatible with the STAC9700/21/44/08/56/66/52
- SigmaTel Surround (SS3D) Stereo Enhancement
- Energy saving dynamic power modes
- See Register Comparision Table Below

Revision Comparison Item	CA3	CC1
Power Supply Current	3.3V Digital: 35mA 3.3V Analog: 70mA 5V Analog: 80mA	3.3V Digital: 30mA 3.3V Analog: 35mA 5V Analog: 35mA
Powerdown Power Consumption	SeeSection 3.1.3; page 10	SeeSection 3.1.3; page 10
GPIO and EAPD Control Registers	Uses Register 74h.	Uses Registers 3Eh, 4Ch, 4Eh, 50h, 52h, 54h, and 74h.

2.2. Description

SigmaTel's STAC9750/51 are general purpose 18-bit ADC, 20-bit DAC, full duplex, audio codecs conforming to the analog component specification of AC'97 (Audio Codec 97 Component Specification Rev. 2.2). The STAC9750/51 incorporate SigmaTel's proprietary ΣΔ technology to achieve a DAC SNR in excess of 90 dB. The DACs, ADCs, and mixer are integrated with analog I/Os, which include four analog line-level stereo inputs, two analog line-level mono inputs, two stereo outputs, and one mono output channel. The STAC9750/51 include digital input/output capability for support of modern PC systems with an output that supports the SPDIF format. The STAC9750/51 is a standard 2-channel stereo codec. With SigmaTel's headphone drive capability, headphones can be driven with no external amplifier. The STAC9750/51 may be used as a secondary codec, with the STAC9700/21/44/56/08/84/66 as the primary, in a multiple codec configuration conforming to the AC'97 Rev. 2.2 specification. This configuration can provide true six-channel, AC-3 playback required for DVD applications. The STAC9750/51 communicates via the five-wire AC-Link to any digital component of AC'97 providing flexibility in the audio system design. Packaged in an AC'97 compliant 48-pin TQFP, the STAC9750/51 can be placed on the motherboard, daughter boards, PCI, AMR, CNR, or ACR cards.

The STAC9750/51 block diagram is illustrated in Figure 1. It provides variable sample rate Digital-to-Analog (DA) and Analog-to-Digital (AD) conversion, mixing, and analog processing. Supported audio sample rates include 48 kHz, 44.1 kHz, 32 kHz, 22.05 kHz, 16 kHz, 11.025 kHz, and 8 kHz; additional rates are supported in the STAC9750/51 soft audio drivers. The digital interface communicates with the AC'97 controller via the five-wire AC-Link and contains the 64-word by 16-bit registers. The two DACs convert the digital stereo PCM-out content to audio. The MIXER block combines the PCM_OUT with any analog sources, to drive the LINE_OUT and HP_OUT outputs. The MONO_OUT delivers either mic only, or a mono mix of sources from the MIXER. The stereo variable sample rate ADC's provide record capability for any mix of mono or stereo sources, and deliver a digital stereo PCM-in signal back to the AC-Link. The microphone input and mono input can be recorded simultaneously, thus allowing for an all digital output in support of the digital ready initiative. All ADC's operate at 18-bit resolution and DAC’s at 20-bit resolution. For a digital ready record path, the microphone is connected to the left channel ADC while the mono output of the stereo mixer is connected to right channel ADC. Make sure the microphone input is not connected to the stereo mixer when in this mode.

The STAC9750/51 supports General Purpose Input/Output (GPIO), as well as SPDIF output. These digital I/O options provide for a number of advance architectural implementations, with volume controls and digital mixing capabilities built directly into the codec.

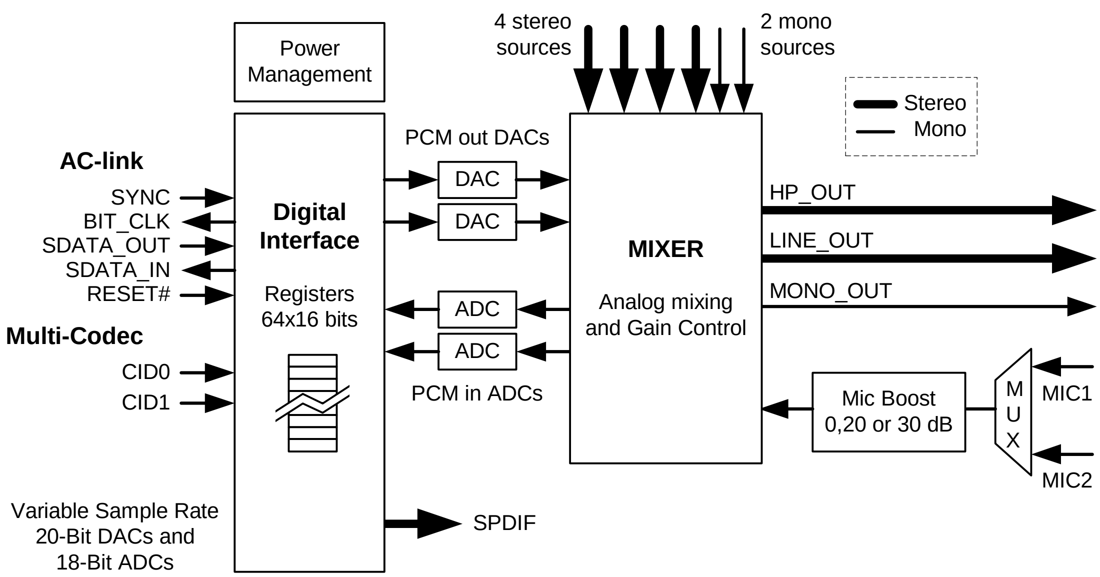
The STAC9750/51 is designed primarily to support stereo (2-speaker) audio. True AC-3 playback can be achieved for 6-speaker applications by taking advantage of the multi-codec option available in the STAC9750/51 to support multiple codecs in an AC'97 architecture. Additionally, the STAC9750/51 provides for a stereo enhancement feature, SigmaTel Surround 3D (SS3D). SS3D provides the listener with several options for improved speaker separation beyond the normal 2/4-speaker arrangements.

Together with the logic component (controller or advanced core logic chip-set) of AC'97, STAC9750/51 can be SoundBlaster® and Windows Sound System® compatible with SigmaTel’s WDM driver for WIN 98/2K/ME/XP. SoundBlaster is a registered trademark of Creative Labs. Windows is a registered trademark of Microsoft Corporation.

2.3. Ordering Information

Part Number	Package	Temp Range	Supply Range
STAC9750T	48-pin TQFP 7mm x 7mm x 1.4mm	0° C to +70° C	DVdd = 3.3V, AVdd = 5.0V
STAC9751T	48-pin TQFP 7mm x 7mm x 1.4mm	0° C to +70° C	DVdd = 3.3V, AVdd = 3.3V

2.4. STAC9750/51 Block Diagram



2.5. Key Specifications

- Analog LINE_OUT SNR: 90 dB
- Digital DAC SNR: 89 dB
- Digital ADC SNR: 85 dB
- Full-scale Total Harmonic Distortion: 0.005%
- Crosstalk between Input Channels: -70 dB
- Spurious Tone Rejection: 100 dB

2.6. Related Materials

- Product Brief
- Reference Designs for MB, AMR, CNR, and ACR applications
- Audio Precision Performance Plots

2.7. Additional Support

Additional product and company information can be obtained by going to the SigmaTel website at: www.sigmatel.com

3. CHARACTERISTICS/SPECIFICATIONS

3.1. Electrical Specifications

3.1.1. Absolute Maximum Ratings:

Voltage on any pin relative to Ground	Vss - 0.3V TO Vdd + 0.3V
Operating Temperature	0 ^{o}C TO 70 ^{o}C
Storage Temperature	-55 ^{o}C TO +125 ^{o}C
Soldering Temperature	220 ^{o}C FOR 10 SECONDS
Output Current per Pin	± 4 mA except VREFout = ± 5mA
Maximum Supply Voltage	5.5 Volts = Vdd

3.1.2. Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Power Supplies*				
+ 3.3V Digital	3.135	3.3	3.465	V
+ 5V Analog	4.75	5	5.25	V
+ 3.3V Analog	3.135	3.3	3.465	V
Ambient Temperature	0	-	70	^{o}C

Table 1. Recommended Operating Conditions.

3.1.3. Power Consumption .

Parameter	Min	Typ	Max	Unit
Digital Supply Current				
+ 3.3V Digital	-	30	-	mA
Analog Supply Current (at Reset state)				
+ 5V Analog	-	35	-	mA
+ 3.3V Analog	-	35	-	mA
Power Down Status (individually asserted) All PR measurements taken while unmuted.				
All paths unmuted +5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	- 50 44 33	-	mA
PR0 +5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	42 39 22	-	mA

Table 2. Power Consumption

The Power Consumption numbers in the table above are applicable to the STAC9750/51 CC1 revision and beyond. Revisions previous to the CC1 revision have a power consumption of 3.3V Digital: 35mA, 3.3V Analog: 70mA , and 5V Analog: 80mA.

CAUTION: ESD sensitive device. Do not open or handle except at a certified static-safe work environment. The STAC9750/51 is an ESD (Electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge without detection, electrostatic charges up to 4000 Volts. Even thought the STAC9750/51 includes ESD protection circuitry internally, proper ESD precautions should be followed to avoid damaging the functionality or performance.

Parameter	Min	Typ	Max	Unit
PR1 +5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	41 38 28	-	mA
PR2 +5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	32 29 12	-	mA
PR3 +5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	23 19 12	-	mA
PR4 +5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	50 44 0.2	-	mA
PR5 +5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	50 44 12	-	mA
PR6 +5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	38 36 33	-	mA
PR0 & PR1 +5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	- 35 35 12	-	mA
PR0, PR1, PR2, PR6 +5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	- 5 5 12	-	mA
PR0, PR1, PR2, PR3, PR6 +5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	- 0.6 0.6 12	-	mA

Table 2. Power Consumption (Continued)

The Power Consumption numbers in the table above are applicable to the STAC9750/51 CC1 revision and beyond. Revisions previous to the CC1 revision have a power consumption of 3.3V Digital: 35mA, 3.3V Analog: 70mA , and 5V Analog: 80mA.

3.1.4. Revision Comparision

	CA3			CC1			% Of Savings		
	Analog		Digital	Analog		Digital	Analog		Digital
	5V	3.3V	3.3V	5V	3.3V	3.3V	5V	3.3V	3.3V
No PR	78	69	27	50	44	33	36%	36%	-22%
PR0	62	56	23	42	39	22	32%	30%	4%
PR1	63	52	24	41	38	28	35%	27%	-17%
PR2	48	42	27	32	29	12	33%	31%	56%
PR3	40	35	21	23	19	12	43%	46%	43%
PR4	76	68	1	50	44	0.2	34%	35%	80%
PR5	75	68	7.5	50	44	12	33%	35%	-60%
PR6	97	61	27	38	36	33	61%	41%	-22%
PR bit individually asserted. All PR measurements taken while unmuted.									

3.1.5. AC-Link Static Digital Specifications

(Tambient = 25 ºC, DVdd = 3.3V ± 5%, AVss=DVss=0V; 50pF external load)

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage Range	Vin	-0.30	-	DVdd + 0.30	V
Low level input range	Vil	-	-	0.35xDVdd	V
High level input voltage	Vih	0.65xDVdd	-	-	V
High level output voltage	Voh	0.90xDVdd	-	-	V
Low level output voltage	Vol	-	-	0.1xDVdd	V
Input Leakage Current (AC-Link inputs)	-	-10	-	10	uA
Output Leakage Current (Hi-Z'd AC-Link outputs)	-	-10	-	10	uA
Output buffer drive current	-	-	4	-	mA

Table 3. AC-Link Static Specifications

3.1.6. STAC9750 Analog Performance Characteristics

($T_{ambient}$ = 25 ºC, AVdd = 5.0V ± 5%, DVdd = 3.3V ± 5%, AVss=DVss=0V; 1 kHz input sine wave; Sample Frequency = 48 kHz; 0 dB = 1 Vrms, 10KΩ//50pF load, Testbench Characterization BW: 20 Hz – 20 kHz, 0 dB settings on all gain stages)

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage:				
All Analog Inputs except Mic	-	1.0	-	Vrms
Mic Inputs (Note 1)	-	0.03	-	Vrms
Full Scale Output:				
Line Output	-	1.0	-	Vrms
PCM (DAC) to LINE_OUT	-	1.0		Vrms
MONO_OUT	-	1.0	-	Vrms
HEADPHONE_OUT (32Ω load)	-	50	-	mWpk
Analog S/N: (Note 2)				
CD to LINE_OUT	-	90	-	dB
Other to LINE_OUT	-	90	-	dB
D/A to LINE_OUT	-	89	-	dB
LINE_IN to A/D with High pass filter enabled	-	85	-	dB
Analog Frequency Response (Note 3)	20	-	20,000	Hz
Total Harmonic Distortion: (Note 4)				
CD to LINE_OUT	-	89	-	dB
Other to LINE_OUT	-	89	-	dB
D/A to LINE_OUT (full scale)	-	89	-	dB
LINE_IN to A/D with High pass filter enabled	84	-	-	dB
HEADPHONE_OUT	74	80	-	dB
A/D & D/A Digital Filter Pass Band (Note 5)	20	-	19,200	Hz
A/D & D/A Digital Filter Transition Band	19,200	-	28,800	Hz

Table 4. STAC9750 Analog Performance Characteristics

Parameter	Min	Typ	Max	Unit
A/D & D/A Digital Filter Stop Band	28,800	-	-	Hz
A/D & D/A Digital Filter Stop Band Rejection (Note 6)	100	-	-	dB
DAC Out-of-Band Rejection (Note 7)	55	-	-	dB
Group Delay (48KHz sample rate)	-		1	ms
Any Analog Input to LINE_OUT Crosstalk (10KHz Signal Frequency)	-	70	-	dB
Any Analog Input to LINE_OUT Crosstalk (1KHz Signal Frequency)	-	100	-	dB
Spurious Tone Rejection	-	100	-	dB
Attenuation, Gain Step Size	-	1.5	-	dB
Input Impedance (Note 8)	-	50	-	KΩ
Input Capacitance	-	15	-	pF
VREFout	-	0.5 X AVdd	-	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB
Interchannel Gain Mismatch DAC	-	-	0.5	dB

Table 4. STAC9750 Analog Performance Characteristics (Continued)

Note:
1. With +30 dB Boost on, 1.0Vrms with Boost off
2. Ratio of Full Scale signal to idle channel noise output is measured “A weighted” over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
3. ± 1dB limits for Line Output & 0 dB gain
4. 20 kHz BW, 48 kHz Sample Frequency
5. ± 0.25dB limits
6. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
7. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 Vrms DAC output.
8. For all inputs except PC BEEP.

3.1.7. STAC9751 Analog Performance Characteristics

($T_{ambient}$ = 25 ºC, AVdd = DVdd = 3.3V ± 5%, AVss=DVss=0V; 1 kHz input sine wave; Sample Frequency = 48 kHz; 0 dB = 1 Vrms, 10KΩ//50pF load, Testbench Characterization BW: 20 Hz – 20 kHz, 0 dB settings on all gain stages)

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage:				
All Analog Inputs except Mic	-	1.0	-	Vrms
Mic Inputs (Note 1)	-	0.03	-	Vrms
Full Scale Output:				
Line Output	-	0.5	-	Vrms
PCM (DAC) to LINE_OUT		0.5		Vrms
MONO_OUT	-	0.5	-	Vrms
HEADPHONE_OUT (32Ω load)	-	12.5	-	mWpk
Analog S/N: (Note 2)				
CD to LINE_OUT	-	90	-	dB

Table 5. STAC9751 Analog Performance Characteristics

Parameter	Min	Typ	Max	Unit
Other to LINE_OUT	-	90	-	dB
D/A to LINE_OUT	-	89	-	dB
LINE_IN to A/D with High pass filter enabled	-	85	-	dB
Analog Frequency Response (Note 3)	20	-	20,000	Hz
Total Harmonic Distortion: (Note 4)				
CD to LINE_OUT	-	89	-	dB
Other to LINE_OUT	-	89	-	dB
D/A to LINE_OUT (full scale)	-	89	-	dB
LINE_IN to A/D with High pass filter enabled	-	84	-	dB
HEADPHONE_OUT	74	80	-	dB
A/D & D/A Digital Filter Pass Band (Note 5)	20	-	19,200	Hz
A/D & D/A Digital Filter Transition Band	19,200	-	28,800	Hz
A/D & D/A Digital Filter Stop Band	28,800	-	-	Hz
A/D & D/A Digital Filter Stop Band Rejection (Note 6)	100	-	-	dB
DAC Out-of-Band Rejection (Note 7)	55	-	-	dB
Group Delay (48KHz sample rate)	-	-	1	ms
Any Analog Input to LINE_OUT Crosstalk (10KHz Signal Frequency)	-	70	-	dB
Any Analog Input to LINE_OUT Crosstalk (1KHz Signal Frequency)	-	100	-	dB
Spurious Tone Rejection	-	100	-	dB
Attenuation, Gain Step Size	-	1.5	-	dB
Input Impedance (Note 8)	-	50	-	KΩ
Input Capacitance	-	15	-	pF
VREFout	-	0.5 X AVdd	-	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB
Interchannel Gain Mismatch DAC	-	-	0.5	dB
Gain Drift	-	100	-	ppm/ºC

Table 5. STAC9751 Analog Performance Characteristics (Continued)

Note:
1. With +30 dB Boost on, 1.0Vrms with Boost off
2. Ratio of Full Scale signal to idle channel noise output is measured “A weighted” over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).0 dB gain, 20 kHz BW, 48 kHz Sample Frequency± 1 dB limits
3. ± 1dB limits for Line Output & 0 dB gain
4. 20 kHz BW, 48 kHz Sample Frequency
5. ± 0.25dB limits
6. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
7. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 Vrms DAC output.
8. For all inputs except PC BEEP.

3.2. AC Timing Characteristics

($T_{ambient}$ = 25 °C, AVdd = 3.3V or 5V ± 5%, DVdd = 3.3V ± 5%, AVss=DVss+0V; 50pF external load)

3.2.1. Cold Reset

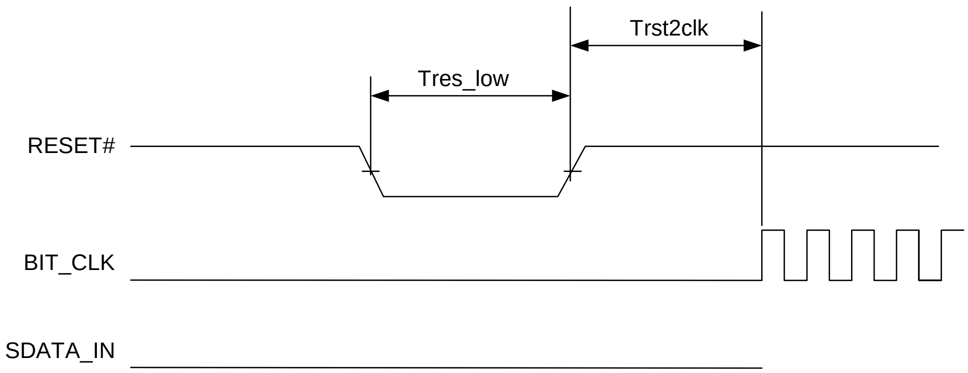


Figure 2. Cold Reset Timing

Parameter	Symbol	Min	Typ	Max	Units
RESET# active low pulse width	Tres_low	1.0	-	-	us
RESET# inactive to BIT_CLK startup delay	Trst2clk	162.8	-	-	ns

Table 6. Cold Reset Specifications

Note: BIT_CLK and SDATAIN are in a high impedance state during reset.

3.2.2. Warm Reset

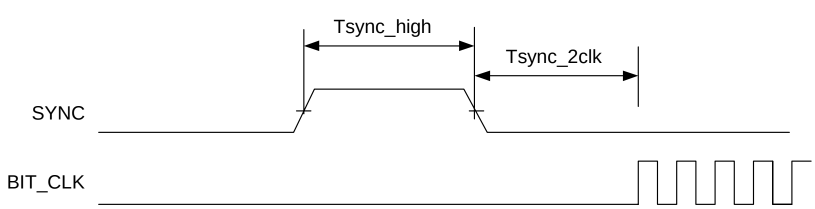


Figure 3. Warm Reset Timing

Parameter	Symbol	Min	Typ	Max	Units
SYNC active high pulse width	Tsync_high	1.0	1.3	-	us
SYNC inactive to BIT_CLK startup delay	Tsync2clk	162.8	-	-	ns

Table 7. Warm Reset Specifications

3.2.3. Clocks

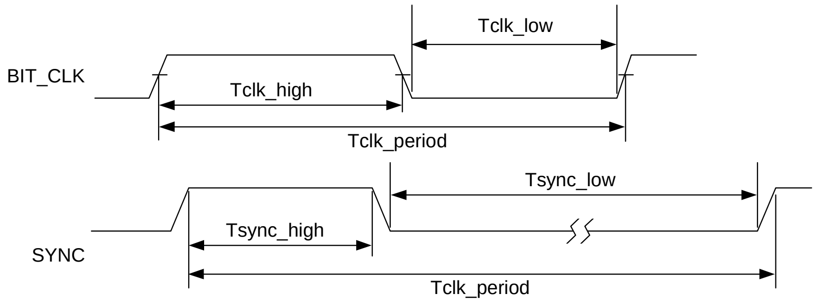


Figure 4. Clocks Timing

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	Tclk_period	-	81.4	-	ns
BIT_CLK output jitter		-	750	-	ps
BLT_CLK high pulsewidth (Note 1)	Tclk_high	36	40.7	45	ns
BIT_CLK low pulse width (Note 1)	Tclk_low	36	40.7	45	ns
SYNC frequency		-	48.0	-	kHz
SYNC period	Tsync_period	-	20.8	-	us
SYNC high pulse width	Tsync_high	-	1.3	-	us
SYNC low_pulse width	Tsync_low	-	19.5	-	us

Note: 1. Worst case duty cycle restricted to 45/55.

Table 8. Clocks Specifications

The 9750/9751 supports several clock frequency inputs as described in the following table. In general, when a 24.576MHz clock xtal is not used, the xtalout pin should be tied to ground. This short to ground configures the part into an alternate clock mode and enables an on board PLL.

XTL_OUT pin config	CID1 pin config	CID0 pin config	clock source input	Codec mode	codec ID
xtal	float	float	24.576Mhz xtal	P	0
XTAL or open	float	pulldown	12.288Mhz bit clk	S	1
XTAL or open	pulldown	float	12.288Mhz bit clk	S	2
XTAL or open	pulldown	pulldown	12.288Mhz bit clk	S	3
short to ground	float	float	14.31818Mhz source[1]	P	0
short to ground	float	pulldown	27MHz source	P	0
short to ground	pulldown	float	48MHz source[2]	P	0
short to ground	pulldown	pulldown	24.576Mhz source	P	0

Table 9. Clock mode configuration

Note:1. In the CA1 and CA2 revisions, this clock source input is 48Mhz.

Note: 2. In the CA1 and CA2 revisions, this clock source input is 14.3181 MHz.

3.2.4. Data Setup and Hold

(47.5-75pF external load)

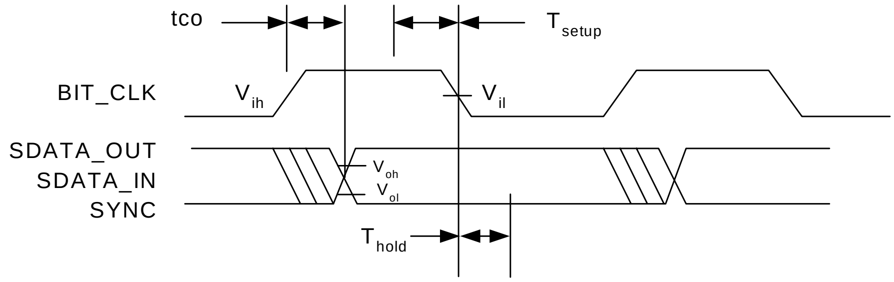


Figure 5. Data Setup and Hold Timing

Parameter	Symbol	Min	Typ	Max	Units
Setup to falling edge of BIT_CLK	Tsetup	10	-	-	ns
Hold from falling edge of BIT_CLK	Thold	10	-	-	ns

Note: Setup and hold time parameters for SDATA_IN are with respect to the AC'97 controller.

Table 10. Data Setup and Hold Specifications

3.2.5. Signal Rise and Fall Times

(75pF external load; from 10% to 90% of Vdd)

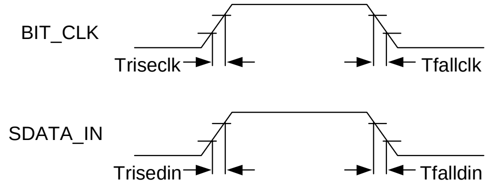


Figure 6. Signal Rise and Fall Times Timing

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK rise time	Triseclk	-	-	6	ns
BIT_CLK fall time	Tfallclk	-	-	6	ns
SDATA_IN rise time	Trisedin	-	-	6	ns
SDATA_IN fall time	Tfalldin	-	-	6	ns

Table 11. Signal Rise and Fall Times Specifications

3.2.6. AC-Link Low Power Mode Timing

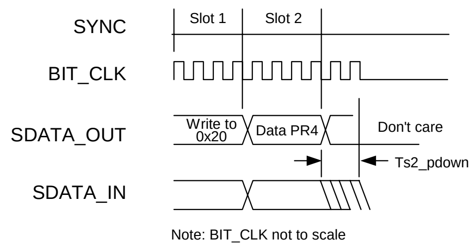


Figure 7. AC-Link Low Power Mode Timing

Parameter	Symbol	Min	Typ	Max	Units
End of Slot 2 to BIT_CLK, SDATA_IN low	Ts2_pdown	-	-	1.0	us

Table 12. AC-Link Low Power Mode Timing Specifications

3.2.7. ATE Test Mode

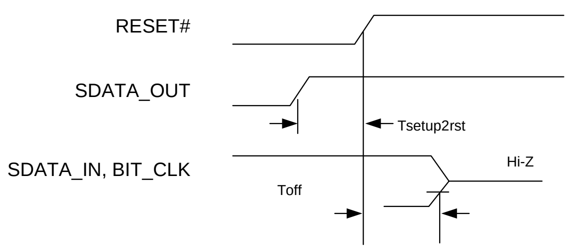


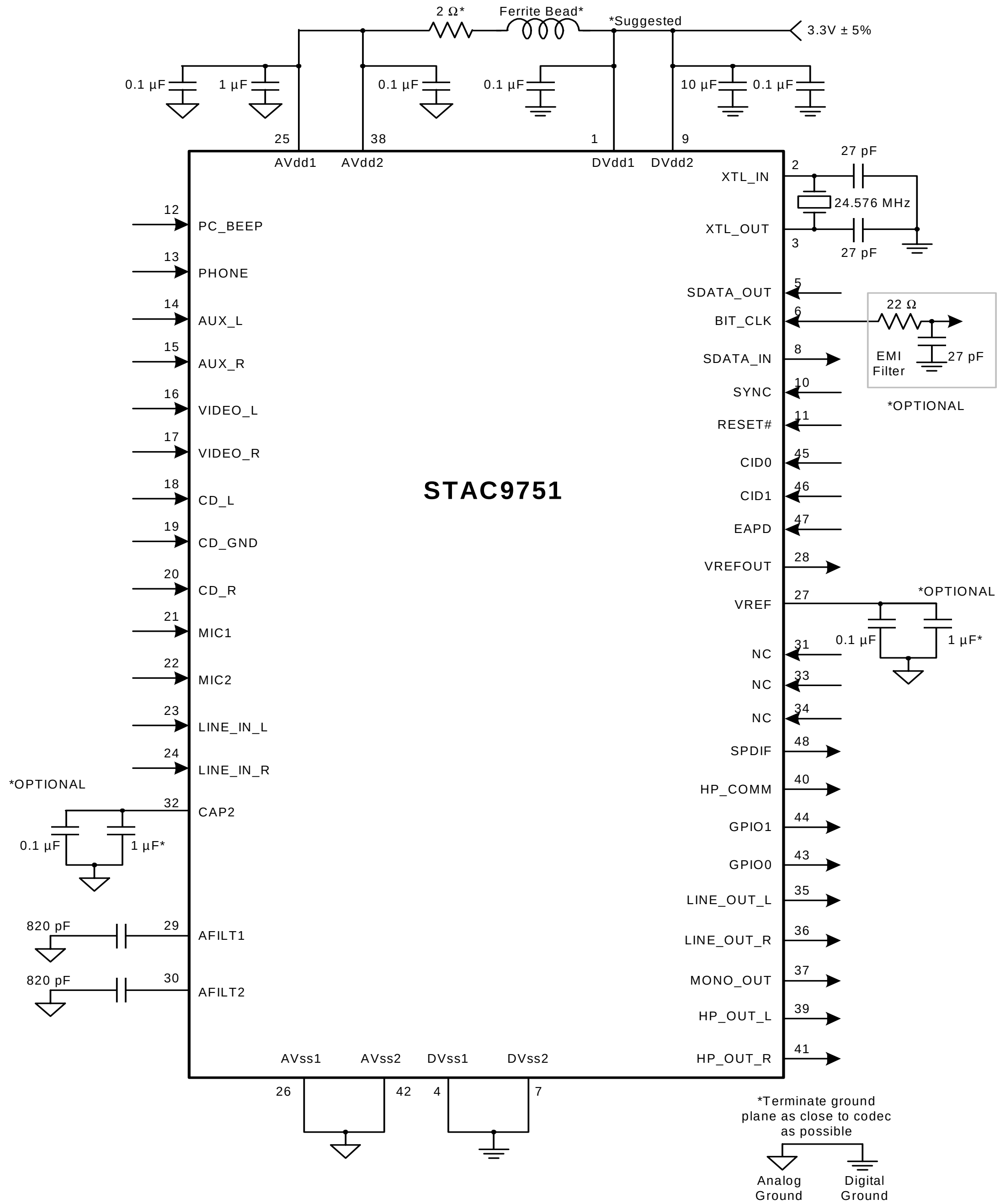
Figure 8. ATE Test Mode Timing

Parameter	Symbol	Min	Typ	Max	Units
Setup to trailing edge of RESET# (also applies to SYNC)	Tsetup2rst	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	Toff	-	-	25.0	ns

Table 13. ATE Test Mode Specifications

Note:
1. All AC-Link signals are normally low through the trailing edge of RESET#. Bringing SDATA_OUT high for the trailing edge of RESET# causes STAC9750/51 AC-Link outputs to go high impedance which is suitable for ATE in circuit testing.
2. Once the test mode has been entered, the STAC9750/51 must be issued another RESET# with all AC-Link signals low to return to the normal operating mode.
3. # denotes active low.

4. TYPICAL CONNECTION DIAGRAM



Note:

1. See Appendix A for specific connection requirements prior to operation.
2. See Figure 23 on page 65 for split supply connections.
3. Pin 48: To Enable SPDIF, use an 1K-10K external pulldown. To Disable SPDIF, use an 1K-10K external pullup. Do Not leave Pin 48 floating.
4. The CD_GND signal is an AC signal return for the two CD input channels. It is normally biased at about 2.5V. The name of the pin in the AC97 specification is CD_GND, and this has confused many designers. It should not have any DC path to GND. Connecting the CD_GND signal directly to ground will change the internal bias of the entire codec, and cause bad distortion. If there is no analog CD input, then this pin can be No-Connect

5. AC-LINK

Figure 10 shows the AC-Link point to point serial interconnect between the STAC9750/51 and its companion controller. All digital audio streams and command/status information are communicated over this AC-Link. See “Digital Interface” on page 21 for details.

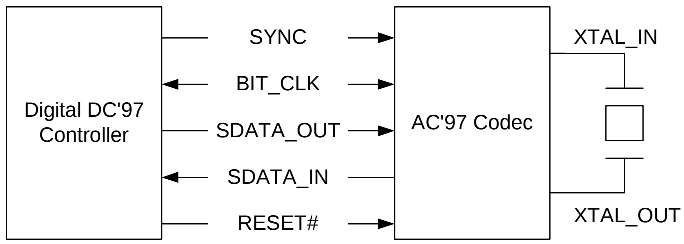


Figure 10. AC-Link to its Companion Controller

5.1. Clocking

STAC9750/51 derives its clock internally from an externally connected 24.576 MHz crystal or an oscillator through the XTAL_IN pin. Synchronization with the AC'97 controller is achieved through the BIT_CLK pin at 12.288 MHz.

The beginning of all audio sample packets, or “Audio Frames”, transferred over AC-Link is synchronized to the rising edge of the “SYNC” signal driven by the AC'97 controller. Data is transitioned on AC-Link on every rising edge of BIT_CLK, and subsequently sampled by the receiving side on each immediately following falling edge of BIT_CLK.

5.2. Reset

There are 3 types of resets:

1. a “cold” reset where all STAC9750/51 logic and registers are initialized to their default state
2. a “warm” reset where the contents of the STAC9750/51 register set are left unaltered
3. a “register” reset which only initializes the STAC9750/51 registers to their default states

After signaling a reset to the STAC9750/51**,** the AC'97 controller should not attempt to play or capture audio data until it has sampled a “Codec Ready” indication via register 26h from the STAC9750/51**.**

For proper reset operation SDATA_OUT should be “0” during “cold” reset.

6. DIGITAL INTERFACE

6.1. AC-Link Digital Serial Interface Protocol

The STAC9750/51 communicates to the AC'97 controller via a 5-pin digital serial AC-Link interface, which is a bi-directional, fixed rate, serial PCM digital stream. All digital audio streams, commands and status information are communicated over this point-to-point serial interconnect. The AC-Link handles multiple inputs, and output audio streams, as well as control register accesses using a time division multiplexed (TDM) scheme. The AC'97 controller synchronizes all AC-Link data transaction. Table 14 shows the data streams available on the STAC9750/51**:**

PCM Playback	2 output slots	2 Channel composite PCM output stream
PCM Record data	2 input slots	2 Channel composite PCM input stream
Control	2 output slots	Control register write port
Status	2 input slots	Control register read port

Table 14. STAC9750/51 Available Data Streams

Synchronization of all AC-Link data transactions is handled by the AC'97 controller. The STAC9750/51 drives the serial bit clock onto AC-Link. The AC'97 controller then qualifies with a synchronization signal to construct audio frames.

SYNC, fixed at 48 kHz, is derived by dividing down the serial bit clock (BIT_CLK). BIT_CLK, fixed at 12.288 MHz, provides the necessary clocking granularity to support 12, 20-bit outgoing and incoming time slots. AC-Link serial data is transitioned on each rising edge of BIT_CLK. The receiver of AC-Link data, STAC9750/51 for outgoing data and AC'97 controller for incoming data, samples each serial bit on the falling edges of BIT_CLK.

The AC-Link protocol provides for a special 16-bit (13-bits defined, with 3 reserved trailing bit positions) time slot (Slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A “1” in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data. If a slot is “tagged” invalid, it is the responsibility of the source of the data, (STAC9750/51 for the input stream, AC'97 controller for the output stream), to stuff all bit positions with 0’s during that slot’s active time.

SYNC remains high for a total duration of 16 BIT_CLKs at the beginning of each audio frame. The portion of the audio frame where SYNC is high is defined as the “Tag Phase”. The remainder of the audio frame where SYNC is low is defined as the “Data Phase”.

Additionally, for power savings, all clock, sync, and data signals may be halted by the controller.

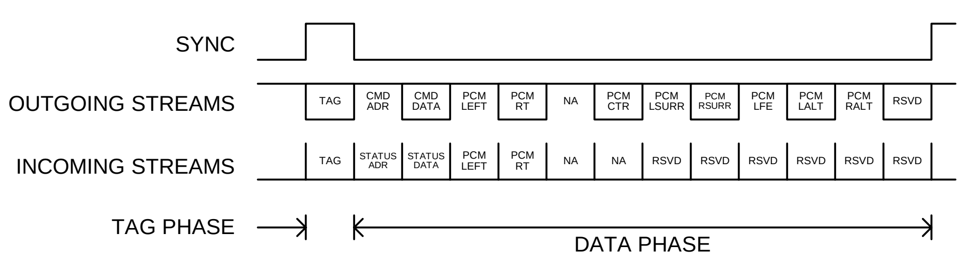


Figure 11. AC'97 Standard Bi-directional Audio Frame

6.1.1. AC-Link Audio Output Frame (SDATA_OUT)

The audio output frame data streams correspond to the multiplexed bundles of all digital output data targeting the STAC9750/51 DAC inputs, and control registers. Each audio output frame supports up to twelve 20-bit outgoing data time slots. Slot 0 is a special reserved time slot containing 16 bits that are used for AC-Link protocol infrastructure.

Within slot 0, the first bit is a global bit (SDATA_OUT slot 0, bit 15) which flags the validity for the entire audio frame. If the “Valid Frame” bit is a 1, this indicates that the current audio frame contains at least one slot time of valid data. The next 12 bit positions sampled by the STAC9750/51 indicate which of the corresponding 12 times slots contain valid data. In this way data streams of differing sample rates can be transmitted across AC-Link at its fixed 48kHz audio frame rate. The following diagram illustrates the time slot based AC-Link protocol.

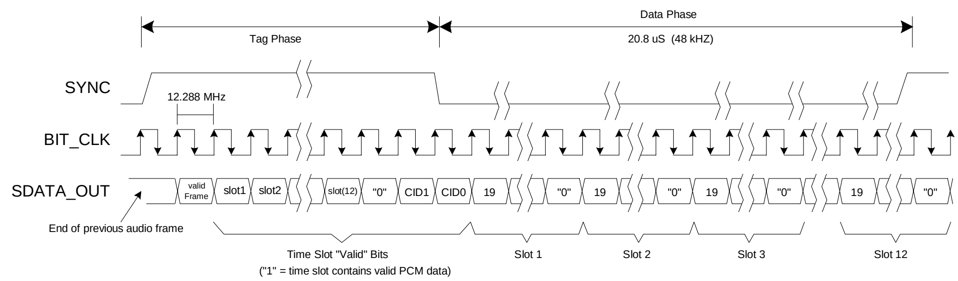


Figure 12. AC-Link Audio Output Frame

A new audio output frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the STAC9750/51 samples the assertion of SYNC. This following edge marks the time when both sides of AC-Link are aware of the start of a new audio frame. On the next rising edge of BIT_CLK, the AC'97 controller transitions SDATA_OUT into the first bit position of slot 0 (Valid Frame bit). Each new bit position is presented to AC-Link on a rising edge of BIT_CLK, and subsequently sampled by the STAC9750/51 on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.

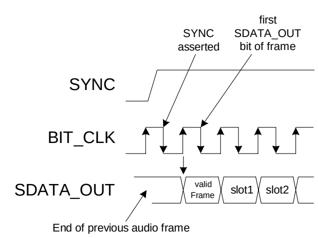


Figure 13. Start of an Audio Output Frame

SDATA_OUT’s composite stream is MSB justified (MSB first) with all non-valid slots’ bit positions stuffed with 0’s by the AC'97 controller.

When mono audio sample streams are sent from the AC'97 controller, it is necessary that BOTH left and right sample stream time slots be filled with the same data.

6.1.1.1. Slot 1: Command Address Port

The command port is used to control features, and monitor status (see Audio Input Frame Slots 1 and 2) of the STAC9750/51 functions including, but not limited to, mixer settings, and power management (refer to the control register section of this specification).

The control interface architecture supports up to sixty-four 16-bit read/write registers, addressable on even byte boundaries. Only the even registers (00h, 02h, etc.) are valid. Odd accesses are considered invalid and return 0 0 0 0.

Audio output frame slot 1 communicates control register address, and write/read command information to the STAC9750/51.

Bit	Description	Comments
19	Read/Write command	1= read, 0=write
18:12	Control Register Index	sixty-four 16-bit locations, addressed on even byte boundaries
11:0	Reserved	Stuffed with 0's

Table 15. Command Address Port Bit Assignments

The first bit (MSB) sampled by STAC9750/51 indicates whether the current control transaction is a read or a write operation. The following 7 bit positions communicate the targeted control register address. The trailing 12 bit positions within the slot are reserved and must be stuffed with 0's by the AC'97 controller.

6.1.1.2. Slot 2: Command Data Port

The command data port is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle (as indicated by Slot 1, bit 19).

Bit	Description	Comments
19:4	Control Register Write Data	Stuffed with 0's if current operation is a read
3:0	Reserved	Stuffed with 0's

Table 16. Command Data Port Bit Assignments

If the current command port operation is a read then the entire slot time must be stuffed with 0's by the AC'97 controller.

6.1.1.3. Slot 3: PCM Playback Left Channel

Audio output frame slot 3 is the composite digital audio left playback stream. In a typical “Games Compatible” PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC'97 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC'97 controller must stuff all trailing non-valid bit positions within this time slot with 0's.

6.1.1.4. Slot 4: PCM Playback Right Channel

Audio output frame slot 4 is the composite digital audio right playback stream. In a typical “Games Compatible” PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC'97 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC'97 controller must stuff all trailing non-valid bit positions within this time slot with 0's.

6.1.1.5. Slot 5: Reserved

Audio output frame slot 5 is reserved for modem operation and is not used by the STAC9750/51.

6.1.1.6. Slot 6: PCM Center Channel

Audio output frame slot 6 is the composite digital audio center stream used in a multi-channel application where the STAC9750/51 is programmed to accept the primary DAC PCM data from slots 6 and 9. Please refer to the register programming section for details on the multi-channel programming options.

6.1.1.7. Slot 7: PCM Left Surround Channel

Audio output frame slot 7 is the composite digital audio left surround stream. In the default state, the STAC9750/51 accepts PCM data from slots 7 and 8 for the surround DACs, for output to the DAC_OUT pins. As a programming option, PCM data from slots 7 and 8 may be used to supply data to the primary DACs when slots 6 and 9 are used to drive the surround DACs. Please refer to the register programming section for details on the multi-channel programming options.

6.1.1.8. Slot 8: PCM Right Surround Channel

Audio output frame slot 8 is the composite digital audio right surround stream. As a programming option, PCM data from slots 7 and 8 may be used to supply data to the primary DACs. Please refer to the register programming section for details on the multi-channel programming options.

6.1.1.9. Slot 9: PCM Low Frequency Channel

Audio output frame slot 9 is the composite digital audio low frequency stream used in a multi-channel application where the STAC9750/51 is programmed to accept the primary DAC PCM data from slots 6 and 9. Please refer to the register programming section for details on the multi-channel programming options.

6.1.1.10. Slot 10: PCM Alternate Left

Audio output frame slot 10 is the composite digital audio alternate left stream used in a multi-channel applications. Please refer to the register programming section for details on the multi channel programming options.

6.1.1.11. Slot 11: PCM Alternate Right

Audio output frame slot 11 is the composite digital audio alternate right stream used in a multi-channel applications. Please refer to the register programming section for details on the multi channel programming options.

6.1.1.12. Slot 12: Reserved

Audio output frame slot 12 is reserved for modem operations and is not used by the STAC9750/51.

6.1.2. AC-Link Audio Input Frame (SDATA_IN)

The audio input frame data streams correspond to the multiplexed bundles of all digital input data targeting the AC'97 controller. As is the case for audio output frame, each AC-Link audio input frame consists of 12, 20-bit time slots. Slot 0 is a special reserved time slot containing 16 bits that are used for AC-Link protocol infrastructure.

Within slot 0 the first bit is a global bit (SDATA_IN slot 0, bit 15) which flags whether the STAC9750/51 is in the “Codec Ready” state or not. If the “Codec Ready” bit is a 0, this indicates that STAC9750/51 is not ready for normal operation. This condition is normal following the de-assertion of power on reset, for example, while STAC9750/51’s voltage references settle. When the AC-Link “Codec Ready” indicator bit is a 1, it indicates that the AC-Link and STAC9750/51 control/status registers are in a fully operational state. The AC'97 controller must further probe the Power-down Control Status Register (refer to Mixer Register section) to determine exactly which subsections, if any, are ready.

Prior to any attempts at putting STAC9750/51 into operation the AC'97 controller should poll the first bit in the audio input frame (SDATA_IN slot 0, bit 15) for an indication that STAC9750/51 has become “Codec Ready”. Once the STAC9750/51 is sampled “Codec Ready”, the next 12 bit positions sampled by the AC'97 controller indicate which of the corresponding 12 time slots are assigned to input data streams, and that they contain valid data. The following diagram illustrates the time slot based AC-Link protocol.

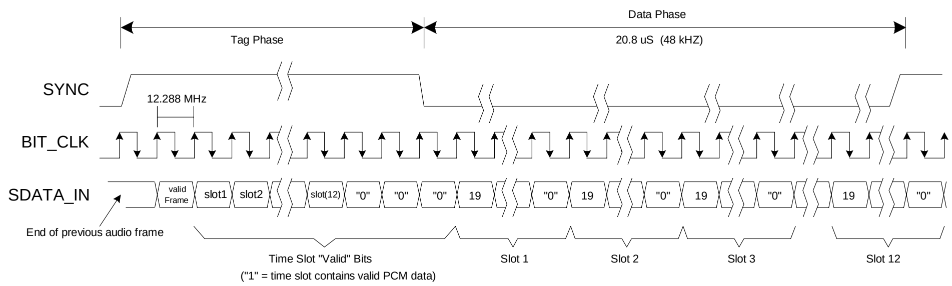


Figure 14. STAC9750/51 Audio Input Frame

A new audio input frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. Immediately following the falling edge of BIT_CLK, the STAC9750/51 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-Link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the STAC9750/51 transitions SDATA_IN into the first bit position of slot 0 (“Codec Ready” bit). Each new bit position is presented to AC-Link on a rising edge of BIT_CLK and subsequently sampled by the AC'97 controller on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.

SDATA_IN's composite stream is MSB justified (MSB first) with all non-valid bit positions (for assigned and/or unassigned time slots) stuffed with 0's by STAC9750/51. SDATA_IN data is sampled on the falling edges of BIT_CLK.

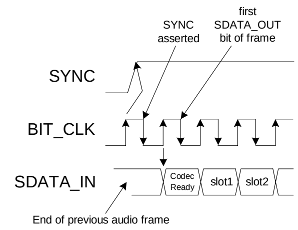


Figure 15. Start of an Audio Input Frame

6.1.2.1. Slot 1: Status Address Port

The status port is used to monitor status for STAC9750/51 functions including, but not limited to, mixer settings, and power management.

Audio input frame slot 1's stream echoes the control register index, for historical reference, for the data to be returned in slot 2. (Assuming that slots 1 and 2 had been tagged "valid" by STAC9750/51 during slot 0)

Bit	Description	Comments
19	Reserved	Stuffed with 0's
18:12	Control Register Index	Echo of register index for which data is being returned
11:2	Slot Request	see sections below
1:0	Reserved	Stuffed with 0's

Table 17. Status Address Port Bit Assignments

The first bit (MSB) generated by STAC9750/51 is always stuffed with a 0. The following 7 bit positions communicate the associated control register address, and the trailing 12 bit positions are stuffed with 0's by STAC9750/51.

6.1.2.2. Slot 2: Status Data Port

The status data port delivers 16-bit control register read data.

Bit	Description	Comments
19:4	Control Register Read Data	Stuffed with 0's if tagged "invalid"
3:0	Reserved	Stuffed with 0's

Table 18. Status Data Port Bit Assignments

If Slot 2 is tagged "invalid" by STAC9750/51**,** then the entire slot will be stuffed with 0's.

6.1.2.3. Slot 3: PCM Record Left Channel

Audio input frame slot 3 is the left channel output of STAC9750/51 input MUX, post-ADC.

STAC9750/51 ADCs are implemented to support 18-bit resolution.

STAC9750/51 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0's to fill out its 20-bit time slot.

6.1.2.4. Slot 4: PCM Record Right Channel

Audio input frame slot 4 is the right channel output of STAC9750/51 input MUX, post-ADC.

STAC9750/51 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0's to fill out its 20-bit time slot.

6.1.2.5. Slot 5: Reserved

Audio input frame slot 5 is reserved for modem operation and is not used by the STAC9750/51. This slot is always stuffed with 0's.

6.1.2.6. Slot 6: PCM Left Record Channel

Audio input frame slot 6 is the left channel output of STAC9750/51 input MUX, post-ADC.

STAC9750/51 ADCs are implemented to support 18-bit resolution.

STAC9750/51 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0's to fill out its 20-bit time slot.

See section 7.5.25; page 49 for slot configurations and register settings.

6.1.2.7. Slot 7: PCM Left Record Channel

Audio input frame slot 7 is the left channel output of STAC9750/51 input MUX, post-ADC.

STAC9750/51 ADCs are implemented to support 18-bit resolution.

STAC9750/51 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0's to fill out its 20-bit time slot.

See section 7.5.25; page 49 for slot configurations and register settings.

6.1.2.8. Slot 8: PCM Right Record Channel

Audio input frame slot 8 is the right channel output of STAC9750/51 input MUX, post-ADC.

STAC9750/51 ADCs are implemented to support 18-bit resolution.

STAC9750/51 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0's to fill out its 20-bit time slot.

See section 7.5.25; page 49 for slot configurations and register settings.

6.1.2.9. Slot 9: PCM Right Record Channel

Audio input frame slot 9 is the right channel output of STAC9750/51 input MUX, post-ADC.

STAC9750/51 ADCs are implemented to support 18-bit resolution.

STAC9750/51 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0's to fill out its 20-bit time slot.

See section 7.5.25; page 49 for slot configurations and register settings.

6.1.2.10. Slot 10: PCM Left Record Channel

Audio input frame slot 10 is the left channel output of STAC9750/51 input MUX, post-ADC.

STAC9750/51 ADCs are implemented to support 18-bit resolution.

STAC9750/51 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0's to fill out its 20-bit time slot.

See section 7.5.25; page 49 for slot configurations and register settings.

6.1.2.11. Slot 11: PCM Right Record Channel

Audio input frame slot 11 is the right channel output of STAC9750/51 input MUX, post-ADC.

STAC9750/51 ADCs are implemented to support 18-bit resolution.

STAC9750/51 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0's to fill out its 20-bit time slot.

See section 7.5.25; page 49 for slot configurations and register settings.

6.1.2.12. Slot 12: Reserved

Audio input frame slot 12 is reserved for modem operation and is not used by the STAC9750/51. This slot is always stuffed with 0's.

6.2. AC-Link Low Power Mode

The **STAC9750/51** AC-Link can be placed in the low power mode by programming register 26h to the appropriate value. Both BIT_CLK and SDATA_IN will be brought to, and held at a logic low voltage level. The AC'97 controller can wake up the **STAC9750/51** by providing the appropriate reset signals.

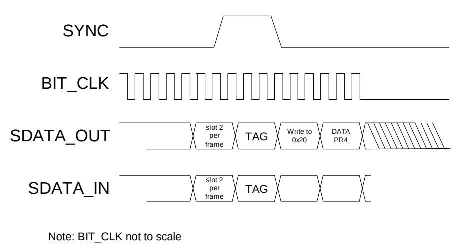


Figure 16. STAC9750/51 Powerdown Timing

BIT_CLK and SDATA_IN are transitioned low immediately (within the maximum specified time) following the decode of the write to the Powerdown Register (26h) with PR4. When the AC'97 controller driver is at the point where it is ready to program the AC-Link into its low power mode, slots (1 and 2) are assumed to be the only valid stream in the audio output frame (all sources of audio input have been neutralized).

The AC'97 controller should also drive SYNC, and SDATA_OUT low after programming the **STAC9750/51** to this low power mode.

6.3. Waking up the AC-Link

Once the STAC9750/51 has halted BIT_CLK, there are only two ways to “wake up” the AC-Link. Both methods must be activated by the AC'97 controller. The AC-Link protocol provides for a “Cold AC'97 Reset”, and a “Warm AC'97 Reset”. The current power down state would ultimately dictate which form of reset is appropriate. Unless a “cold” or “register” reset (a write to the Reset register) is performed, wherein the AC'97 registers are initialized to their default values, registers are required to keep state during all power down modes. Once powered down, re-activation of the AC-Link via re-assertion of the SYNC signal must not occur for a minimum of 4 audio frame times following the frame in which the power down was triggered. When AC-Link powers up it indicates readiness via the Codec Ready bit (input slot 0, bit 15).

Cold Reset - a cold reset is achieved by asserting RESET# for the minimum specified time, and then bringing RESET# back HIGH. The reset occurs on the rising edge when RESET# is deasserted. By asserting and deasserting RESET#, BIT_CLK and SDATA_IN will be activated, or re-activated as the case may be, and all STAC9750/51 control registers will be initialized to their default power on reset values.

Note: RESET# is an asynchronous input. (# denotes active low)

Warm Reset - a warm reset will re-activate the AC-Link without altering the current STAC9750/51 register values. A warm reset is signaled by driving SYNC high for a minimum of 1us in the absence of BIT_CLK.

Note: Within normal audio frames, SYNC is a synchronous input. However, in the absence of BIT_CLK, SYNC is treated as an asynchronous input used in the generation of a warm reset to the STAC9750/51.

7. STAC9750/51 MIXER

The STAC9750/51 includes analog and digital mixers for maximum flexibility. The analog mixer is designed to the AC'97 specification to manage the playback and record of all digital and analog audio sources in the PC environment. The analog mixer also includes several extensions of the AC'97 specification to support "all analog record" capability as well as "POP BYPASS" mode for all digital playback. The analog sources include:

- **System Audio**: digital PCM input and output for business, games and multimedia
- **CD/DVD**: analog CD/DVD-ROM audio with internal connections to Codec mixer
- **Mono microphone**: choice of desktop mic, with programmable boost and gain
- **Speakerphone**: use of system mic and speakers for telephone, DSVD, and video conferencing
- **Video**: TV tuner or video capture card with internal connections to Codec mixer
- **AUX/synth**: analog FM or wavetable synthesizer, or other internal source

The digital mixer includes inputs for the PCM DAC and the recorded ADC output.

Source	Function	Connection
PC_BEEP	PC BEEP pass through to LINE_OUT	from PC_BEEP output
PHONE	MONO input	from telephony subsystem
MIC1	desktop microphone	from mic jack
MIC2	second microphone	from second mic jack
LINE_IN	external audio source	from line-in jack
CD	audio from CD-ROM	cable from CD-ROM
VIDEO	audio from TV tuner or video camera	cable from TV or VidCap card
AUX	upgrade synth or other external source	internal connector
PCM out	digital audio output from AC'97 Controller	AC-Link

Destination	Function	Connection
HP_OUT	stereo mix of all sources	To headphone out jack
LINE_OUT	stereo mix of all sources	To output jack
MONO_OUT	mic or MONO Analog mixer output	to telephony subsystem
PCM in	digital data from the codec to the AC'97 Controller	AC-Link
SPDIF	SPDIF digital audio output	To SPDIF output connector

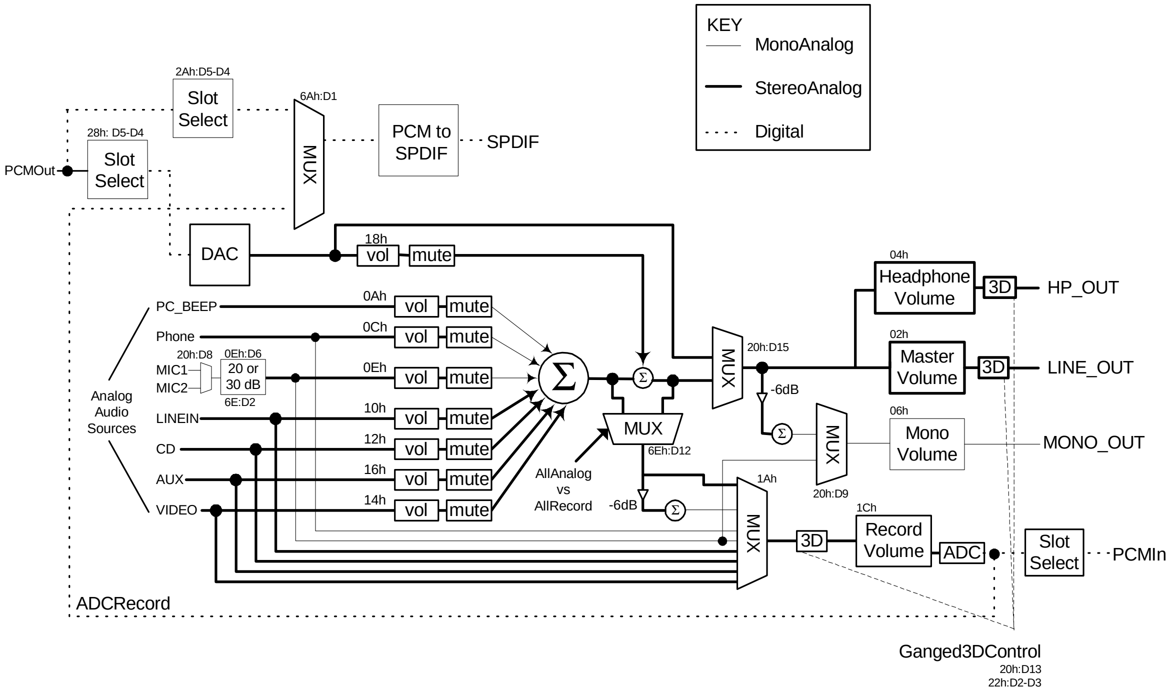


Figure 17. STAC9750 2-Channel Mixer Functional Diagram

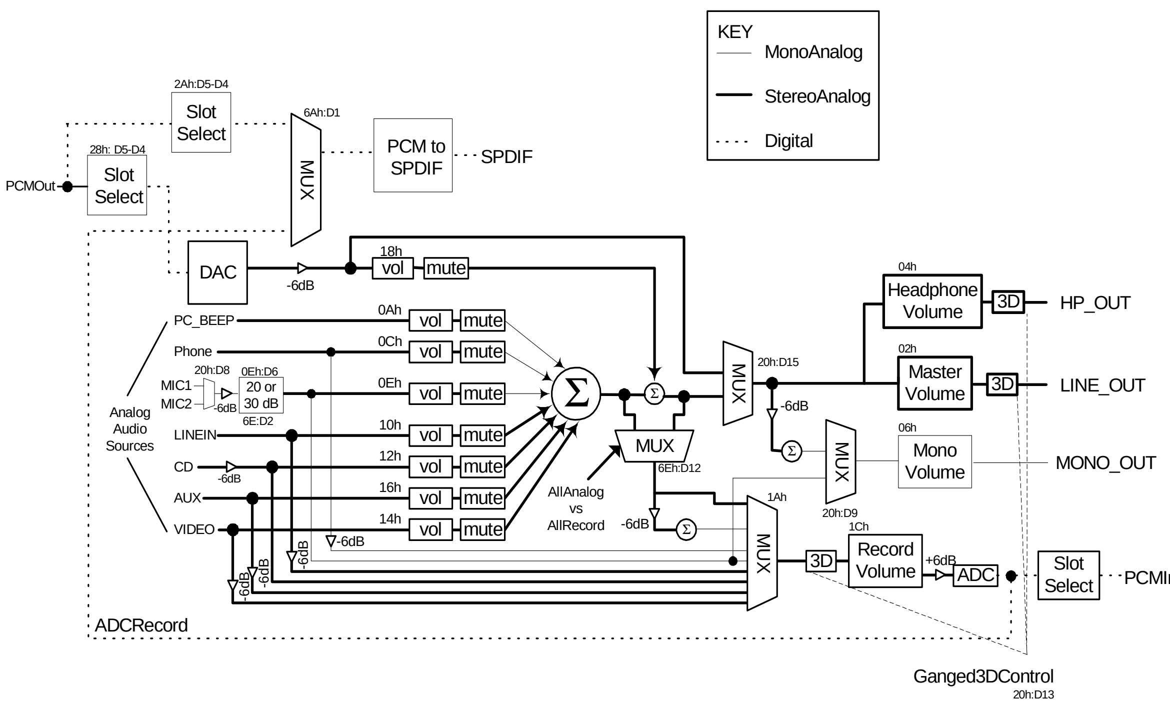


Figure 18. STAC9751 2-Channel Mixer Functional Diagram

7.1. Analog Mixer Input

The mixer provides recording and playback of any audio sources or output mix of all sources. The STAC9750/51 supports the following input sources:

- any mono or stereo source
- mono or stereo mix of all sources
- 2-channel input w/mono output reference (mic + stereo mix)

Note: All unused inputs should be tied together and have a capacitor (0.1 µF suggested) to ground.

7.2. Analog Mixer Output

The mixer generates three distinct outputs:

- a stereo mix of all sources for output to the LINE_OUT and HP_OUT
- a stereo mix of all analog sources for recording
- mic only or mono mix of all sources for MONO_OUT

Note:Mono output of stereo mix is attenuated by -6 dB.

7.3. SPDIF Digital Mux

The STAC9750/51 incorporates a digital output that supports SPDIF formats. A multiplexer determines which of two digital input streams are used for the digital output conversion process. These two streams include the PCM OUT data from the audio controller and the ADC recorded output. The normal analog LINE_OUT signal can be converted to the SPDIF formats by using the internal ADC to record the 'MIX" output, which is the combination of all analog and all digital sources. In the case of digital controllers with support for 4 or more channels, the SPDIF output mode can be used to support compressed 6-channel output streams for delivery to home theater systems. These can be routed on alternate AC-Link slots to the SPDIF output, while the standard 2-channel output is delivered as selected by bits D5 and D4 in Register 6E. If the digital controller supports 6 channels, a SPDIF output with 4 analog channels can also be configured (in a multi-codec setup). For more information for SPDIF please see 7.5.12.2; page 43.

Pin 48: To Enable SPDIF, use an 1K-10K external pulldown. To Disable SPDIF, use an 1K-10K external pullup. Do Not leave Pin 48 floating.

7.4. PC Beep Implementation

PC Beep is active on power up and defaults to an un-muted state. The PC-BEEP input is routed directly to the MONO_OUT, LINE_OUT and HP_OUT pins of the codec. Because the PC_BEEP input drive is often a full scale digital signal, some resistive attenuation of the PC_BEEP input is recommended to keep the beep tone within reasonable volume levels. The user should mute this input before using any other mixer input because the PC Beep input can contribute noise to the lineout during normal operation. This style of PC Beep is related to the AC'97 Specification Rev 2.2. To use the analog PC Beep,a value of 00h to bits F[7:0](D[12:5]) disables the Digital PC Beep generation. PV[3:0] (D[4:1]) controls the volume level from 0 to 45dB of attenuation in 3dB steps.

7.5. Programming Registers

Address	Name	Default	Location
00h	Reset	6990h	7.5.1; page 34
02h	Master Volume	8000h	7.5.2.1; page 34
04h	HP_OUT Mixer Volume	8000h	7.5.2.2; page 34 and 35
06h	Master Volume MONO	8000h	7.5.2.3; page 35
0Ah	PC Beep Mixer Volume	0000h	7.5.3; page 35
0Ch	Phone Mixer Volume	8008h	7.5.4.1; page 36
0Eh	Mic Mixer Volume	8008h	7.5.4.2; page 36
10h	Line In Mixer Volume	8808h	7.5.4.3; page 36
12h	CD Mixer Volume	8808h	7.5.4.4; page 36
14h	Video Mixer Volume	8808h	7.5.4.5; page 37
16h	Aux Mixer Volume	8808h	7.5.4.6; page 37
18h	PCM Out Mixer Volume	8808h	7.5.4.7; page 37
1Ah	Record Select	0000h	7.5.5; page 37
1Ch	Record Gain	8000h	7.5.6; page 38
20h	General Purpose	0000h	7.5.7; page 38
22h	3D Control	0000h	7.5.8; page 39
24h **	Audio Interrupt	0000h	7.5.9; page 39
26h	Powerdown Ctrl/Stat	000Fh	7.5.10; page 40
28h	Extended Audio ID	0205h	7.5.11; page 41
2Ah	Extended Audio Control/Status	0400h	7.5.12; page 42
2Ch	PCM DAC Rate	BB80h	7.5.14; page 44
32h	PCM LR ADC Rate	BB80h	7.5.15; page 44
3Ah	SPDIF Control	2A00h	7.5.16; page 45
3Eh**	Extended Modem Stat/Ctl	0100h	7.5.17; page 46
4Ch**	GPIO Pin Configuration	0003h	7.5.18; page 46
4Eh**	GPIO Pin Polarity/Type	FFFFh	7.5.19; page 46
50h**	GPIO Pin Sticky	0000h	7.5.20; page 47
52h**	GPIO Wake-up	0000h	7.5.21; page 47
54h**	GPIO Pin Status	0000h	7.5.22; page 48
6Ah	Digital Audio Control	0000h	7.5.16; page 45
6Ch	Revision Code	00xxh	7.5.24; page 49
6Eh	Analog Special	0000h	7.5.25; page 49
70h	72h Enable	0000h	7.5.25.6; page 50
72h	Analog Current Adjust	0000h	7.5.25.7; page 51
74h*	GPIO Current Access	0000h	7.5.26; page 52
76h	78h Enable	0000h	7.5.27.1; page 52
78h	Clock Access	0000h	7.5.27.2; page 53
7Ch	Vendor ID1	8384h	7.5.28.1; page 53
7Eh	Vendor ID2	76xxh	7.5.28.2; page 53

Table 19. Programming Registers

1. Register 74h is used for GPIO control in revision CA3.
2. **Registers used in revision CC1 and beyond for GPIO. EAPD is still controled by Register 74.

7.5.1. Reset (00h)

Default: 6990h

D15	D14	D13	D12	D11	D10	D9	D8
RSRVD4	SE4	SE3	SE2	SE1	SE0	ID9	ID8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Writing any value to this register performs a register reset, which causes all registers to revert to their default values. Reading this register returns the ID code of the part.

7.5.2. Play Master Volume Registers (Index 02h, 04h, and 06h)

These registers manage the output signal volumes. Register 02h controls the stereo LINE_OUT master volume (both right and left channels), register 04h controls the Headphone Out master volume, and register 06h controls the MONO volume output. Each step corresponds to 1.5 dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB. ML5 through ML0 is for left channel level, MR5 through MR0 is for the right channel and MM5 through MM0 is for the mono out channel. When bits D5 and D13 are set in any of these registers it automatically writes all 1's to the next lower 5-bits.

The default value is 8000h for registers 02h, 04h, and 06h, which corresponds to 0 dB attenuation with mute on.

Mute	Mx5...Mx0	Function	Range
0	00 0000	0dB Attenuation	Req.
0	01 1111	46.5 Attenuation	Req.
1	xx xxxx	∞ dB Attenuation	Req.

Table 20. Play Master Volume Register

7.5.2.1. Master Volume (02h)

Default: 8000h

Note: If optional bits D13, D5 of register 02h are set to 1, then the corresponding attenuation is set to 46dB and the register reads will produce 1Fh as a value for this attenuation/gain block.

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RSRVD	ML5	ML4	ML3	ML2	ML1	ML0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED		MR5	MR4	MR3	MR2	MR1	MR0

7.5.2.2. Headphone Out Volume (04h)

Default: 8000h

If optional bits D13, D5 of register 04h are set to 1, then the corresponding attenuation is set to 46dB and the register reads will produce 1Fh as a value for this attenuation/gain block.

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RSRVD	HPL5	HPL4	HPL3	HPL2	HPL1	HPL0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED		HPR5	HPR4	HPR3	HPR2	HPR1	HPR0

7.5.2.3. Master Volume MONO (06h)

Default: 8000h

Note: If optional bits D5 of register 06h is set to 1, then the corresponding attenuation is set to 46dB and the register reads will produce 1Fh as a value for this attenuation/gain block.

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED						
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED		MM5	MM4	MM3	MM2	MM1	MM0

7.5.3. PC Beep Mixer Volume (Index 0Ah)

Default: 0000h

Note: PC_BEEP default to 0000h, mute off.

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED						
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED			PV3	PV2	PV1	PV0	RSRVD

This register controls the level for the PC Beep input. Each step corresponds to approximately 3 dB of attenuation. The MSB of the register is the mute bit. When this bit is set to 1, the level for that channel is set at -∞ dB. PC_BEEP supports motherboard implementations. The intention of routing PC_BEEP through the STAC9750/51 mixer is to eliminate the requirement for an onboard speaker by guaranteeing a connection to speakers connected via the output jack. In order for this to be viable the PC_BEEP signal needs to reach the output jack at all times. NOTE: the PC_BEEP is routed to the mono outputs when the STAC9750/51 is in a RESET state. This is so that Power On Self Test (POST) codes can be heard by the user in case of a hardware problem with the PC. For further PC_BEEP implementation details please refer to the AC'97 Technical FAQ sheet. The default value is 0000h, which corresponds to 0 dB attenuation with mute off.

Mute	PV3…PV0	Function
0	0000	0 dB Attenuation
0	1111	45 dB Attenuation
1	xxxx	∞ dB Attenuation

Table 21. PC_BEEP Register

7.5.4. Analog Mixer Input Gain Registers (Index 0Ch - 18h)

These registers control the gain/attenuation for each of the analog inputs. Each step corresponds to approximately 1.5 dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB.

The default value for stereo registers is 8808h, corresponding to 0 dB gain with mute on.

Mute	Gx4…Gx0	Function
0	00000	+12 dB gain
0	01000	0 dB gain
0	11111	-34.5 dB gain

Table 22. Analog Mixer Input Gain Register

7.5.4.1. Phone Mixer Volume (0Ch)

Default: 8008h

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED						
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED			GN4	GN3	GN2	GN1	GN0

7.5.4.2. Mic Mixer Volume (0Eh)

Default: 8008h

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED						
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RSRVD	BOOST_EN	RSRVD	GN4	GN3	GN2	GN1	GN0

Register 0Eh (Mic Volume Register) Bit D6 is the Mic boost enable. To select between 20db or 30db Mic Boost, see register 6Eh, D2 in section 7.5.25; page 49.

7.5.4.3. Line In Mixer Volume (10h)

Default: 8808h

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED		GL4	GL3	GL2	GL1	GL0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED			GR4	GR3	GR2	GR1	GR0

7.5.4.4. CD Mixer Volume (12h)

Default: 8808h

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED		GL4	GL3	GL2	GL1	GL0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED			GR4	GR3	GR2	GR1	GR0

7.5.4.5. Video Mixer Volume (14h)

Default: 8808h

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED		GL4	GL3	GL2	GL1	GL0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED			GR4	GR3	GR2	GR1	GR0

7.5.4.6. AUX Mixer Volume (16h)

Default: 8808h

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED		GL4	GL3	GL2	GL1	GL0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED			GR4	GR3	GR2	GR1	GR0

7.5.4.7. PCM Out Mixer Volume (18h)

Default: 8808h

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED		GL4	GL3	GL2	GL1	GL0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED			GR4	GR3	GR2	GR1	GR0

7.5.5. Record Select (1Ah)

Default: 0000h (corresponding to Mic in)

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED					SL2	SL1	SL0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED					SR2	SR1	SR0

Used to select the record source independently for right and left.

Bit(s)	Reset	Name	Description
15:11	0	RESERVED	BITS NOT USED, SHOULD READ BACK 0
10:8	0	SL2:SL0	LEFT CHANNEL INPUT SELECT 000 = Mic 100 = Line In (left) 001 = CD In (left) 101 = Stereo Mix (left) 010 = Video In (left) 110 = Mono Mix 011 = Aux In (left) 111 = Phone
7:3	0	RESERVED	BITS NOT USED, SHOULD READ BACK 0
2:0	0	SR2:SR0	RIGHT CHANNEL INPUT SELECT 000 = Mic 100 = Line In (right) 001 = CD In (right) 101 = Stereo Mix (right) 010 = Video In (right) 110 = Mono Mix 011 = Aux In (right) 111 = Phone

Table 23. Record Select Control Registers

7.5.6. Record Gain (1Ch)

Default: 8000h (corresponding to 0 dB gain with mute on)

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED			GL3	GL2	GL1	GL0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED				GR3	GR2	GR1	GR0

The 1Ch register adjusts the stereo input record gain. Each step corresponds to 1.5 dB. 22.5 dB corresponds to 0F0Fh. The MSB of the register is the mute bit. When this bit is set to 1, the level for that channel(s) is set at -∞ dB.

Mute	Gx3… Gx0	Function
0	1111	+22.5 dB gain
0	0000	0 dB gain
1	xxxx	-∞ gain

Table 24. Record Gain Registers

7.5.7. General Purpose (20h)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
POP BYP	RSRVD	3D	RESERVED			MIX	MS
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
LPBK	RESERVED						

This register is used to control some miscellaneous functions. Below is a summary of each bit and its function. The MS bit controls the mic selector. The LPBK bit enables loopback of the ADC output to the DAC input without involving the AC-Link, allowing for full system performance measurements.

Bit	Function
3D	3D Stereo Enhancement on/off 1 = on
MIX	Mono output select 0 = Mix, 1= Mic
MS	Mic select 0 = Mic1, 1 = Mic2
POP BYP	DAC bypasses mixer and connects directly to Line Out
LPBK	ADC/DAC loopback mode

Table 25. General Purpose Register

7.5.8. 3D Control (22h)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED				DP3	DP2	RESERVED	

This register is used to control the 3D stereo enhancement function, ***Sigmatel Surround 3D (SS3D),*** built into the AC'97 component. Note that register bits DP3-DP2 are used to control the separation ratios in the 3D control for LINE_OUT. ***SS3D*** provides for a wider soundstage extending beyond the normal 2-speaker arrangement. Note that the 3D bit in the general purpose register (20h) must be set to 1 to enable SS3D functionality and for the bits in 22h to take effect.

DP3, DP2	LINE_OUT SEPARATION RATIO
0 0	0 (Off)
0 1	3 (Low)
1 0	4.5 (Med)
1 1	6 (High)

Table 26. 3D Control Registers

The three separation ratios are implemented as shown in Table 26. The separation ratio defines a series of equations that determine the amount of depth difference (High, Medium, and Low) perceived during two-channel playback. The ratios provide for options to narrow or widen the soundstage.

7.5.9. Audio Interrupt (24h)

For use with Revsion CC1 GPIO interrupts.

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
I4	I3	RESERVED		I0	RESERVED		
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED							

Bit(s)	Reset Value	R/W	Name	Description
15	0	RW	I4	0=Interrupt is clear 1=interrupt is set Interrupt event is cleared by writing a “1” to this bit. The interrupt bit will change regardless of condition of interrupt enable (I0) status. An interrupt in the GPI in slot 12 in the ACLink will follow this bit change when interrupt enable (I0) is unmasked.
14	0	RO	I3	Interrupt Cause 0 = No Interrupt Caused 1 = Change in GPIO input status These bits will reflect the general cause of the first interrupt event generated. It should be read after interrupt status has been confirmed as interrupting. The information should be used to scan possible interrupting events in proper pages.

Bit(s)	Reset Value	R/W	Name	Description
13-12	0	RW	RESERVED	BITS NOT USED, SHOULD READ BACK 0
11	0	RW	I0	Interrupt Enable 0 = Interrupt generation is masked. 1 = Interrupt generation is un-masked. The driver should not un-mask the interrupt unless ensured by the AC '97 controller that no conflict is possible with modem slot 12 - GPI functionality. Some AC'97 2.2 compliant controllers will not likely support audio codec interrupt infrastructure. In either case, S/W should poll the interrupt status after initiating a sense cycle and wait for Sense Cycle Max Delay to determine if an interrupting event has occurred.
10:0	0	RO	RESERVED	BITS NOT USED, SHOULD READ BACK 0

7.5.10. Powerdown Ctrl/Stat (26h)

Default: 000Fh

D15	D14	D13	D12	D11	D10	D9	D8
EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED				REF	ANL	DAC	ADC

This read/write register is used to program powerdown states and monitor subsystem readiness. The EAPD external control is also supported through this register.

Bit	Function
EAPD	External Amplifier Power Down
REF	VREF's up to nominal level
ANL	Analog mixers, etc. ready
DAC	DAC section ready to playback data
ADC	ADC section ready to playback data

Table 27. Powerdown Status Registers

7.5.10.1. Ready Status

The lower half of this register is read only status, a "1" indicating that the subsection is "ready". Ready is defined as the subsection's ability to perform in its nominal state. When this register is written, the bit values that come in on AC-Link will have no effect on read only bits 0-7.

When the AC-Link "Codec Ready" indicator bit (SDATA_IN slot 0, bit 15) is a 1, it indicates that the AC-Link and AC'97 control and status registers are in a fully operational state. The AC'97 controller must further probe this Powerdown Control/Status Register to determine exactly which subsections, if any are ready. When this register is written, the bit values that come in on AC-Link will have no effect on read only bits 0-7.

7.5.10.2. Powerdown Controls

The STAC9750/51 is capable of operating at reduced power when no activity is required. The state of power down is controlled by the Powerdown Register (26h). See the section “Low Power Modes” for more information.

7.5.10.3. External Amplifier Power Down Control

The EAPD bit 15 of the Powerdown Control/Status Register (Index 26h) directly controls the output of the EAPD output, pin 45, and produces a logical “1” when this bit is set to logic high. This function is used to control an external audio amplifier power down. EAPD = 0 places approximately 0V on the output pin, enabling an external audio amplifier. EAPD = 1 places approximately DVdd on the output pin, disabling the external audio amplifier. Audio amplifiers that operate with reverse polarity will likely require an external inverter to maintain software driver compatibility.

7.5.11. Extended Audio ID (28h)

Default: 0605h

D15	D14	D13	D12	D11	D10	D9	D8
ID1	ID0	RESERVED		REV1	REV0	AMAP	LDAC
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
SDAC	CDAC	DSA1	DSA0	VRM	SPDIF	DRA	VRA

The Extended Audio ID register is a read only register, except for Bits D5:D4. ID1 and ID0 echo the configuration of the codec as defined by the programming of pins 45 and 46 externally. “00” returned defines the codec as the primary codec, while any other code identifies the codec as one of three secondary codec possibilities. SDAC=0 tells the controller that the STAC9750/51 is a two-channel codec as defined by the Intel spec. The AMAP bit, D9, will return a 1 indicating that the codec supports the optional “AC’97 2.2 compliant AC-link slot to audio DAC mappings”. The default condition assumes that 0, 0 are loaded in the DSA0 and DSA1 bits of the Extended Audio ID (Index 28h). With 0s in the DSAx bits, the codec slot assignments are as per the AC’97 specification recommendations. If the DSAx bits do not contain 0s, the slot assignments are as per the table in the section describing the Extended Audio ID (Index 28h). The VRA bit, D0, will return a 1 indicating that the codec supports the optional variable sample rate conversion as defined by the AC’97 specification.

Bit	Name	Access	Reset Value	Function
15:14	ID [1,0]	Read only	variable	0,0=XTAL_OUT grounded **(note 1)** CID1#,CID0#=XTAL_OUT crystal or floating
13:12	Reserved	Read only	00	Reserved
11:10	Rev[1:0]	Read only	01	Indicates codec is AC'97 Rev 2.2 compliant
9	AMAP	Read only	1	Multi-channel slot support (Always = 1)
8	LDAC	Read only	0	Low Frequency Effect, not supported (Always=0)
7	SDAC	Read only	0	Surround DAC, not supported (Always = 0)
6	CDAC	Read only	0	Center channel, not supported (Always = 0)
5:4	DSA [1,0]	Read/Write	00	DAC slot assignment If CID[1:0]=00 then DSA[1:0] resets to 00 If CID[1:0]=01 then DSA[1:0] resets to 01 If CID[1:0]=10 then DSA[1:0] resets to 01 If CID[1:0]=11 then DSA[1:0] resets to 10 00 = left slot 3, right slot 4 01 = left slot 7, right slot 8 10 = left slot 6, right slot 9 11 = left slot 10, right slot 11
3	VRM	Read only	0	Variable Sample Rate Mic, not supported (Always = 0)
2	SPDIF	Read only	1	0=SPDIF pulled high on reset, SPDIF disabled 1=default, SPDIF enabled **(Note 2)**
1	DRA	Read only	0	Double Rate Audio,not supported (always = 0)
0	VRA	Read only	1	Variable sample rates supported (Always = 1)

Table 28. Extended Audio ID

1. External CID pin status (from analog) these bits are the logical inversion of the pin polarity (pin 45-46). These bits are zero if XTAL_OUT is grounded with an alternate external clock source in primary mode only. Secondary mode can either be through BIT CLK driven or 24MHz clock driver with XTAL_OUT floating/shorted.
2. If pin 48 is held high at powerup, this bit will be held to zero, to indicate the SPDIF is not available. Pin 48: To Enable SPDIF, use an 1K-10K external pulldown. To Disable SPDIF, use an 1K-10K external pullup. Do Not leave Pin 48 floating.

7.5.12. Extended Audio Control/Status (2Ah)

Default: 0400h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED					SPCV	RESERVED	

D7	D6	D5	D4	D3	D2	D1	D0
RESERVED		SPSA1	SPSA0	RSRVD	SPDIF	RSRVD	VRA enable

7.5.12.1. Variable Rate Sampling Enable

The Extended Audio Status Control register also contains one active bit to enable or disable the Variable Sampling Rate capabilities of the DACs and ADCs. If the VRA, bit D0, is 1 the variable sample rate control registers (2Ch and 32h) are active, and “on-demand” slot data required transfers are allowed. If the VRA bit is 0, the DACs and ADCs will operate at the default 48 kHz data rate.

The **STAC9750/51** supports “on-demand” slot request flags. These flags are passed from the codec to the AC’97 controller in every audio input frame. Each time a slot request flag is set (active low) in a given audio frame, the controller will pass the next PCM sample for the corresponding slot in the audio frame that immediately follows. The VRA enable bit must be set to 1 to enable “on-demand” data transfers. If the VRA enable bit is not set, the codec will default to 48 kHz transfers and every audio frame will include an active slot request flag and data is transferred every frame.

For variable sample rate output, the codec examines its sample rate control registers, the state of the FIFOs, and the incoming SDATA_OUT tag bits at the beginning of each audio output frame to determine which SLOTREQ bits to set active (low). SLOTREQ bits are asserted during the current audio input frame for active output slots, which will require data in the next audio output frame.

For variable sample rate input, the tag bit for each input slot indicates whether valid data is present or not. Thus, even in variable sample rate mode, the codec is always the master: for SDATA_IN (codec to controller), the codec sets the TAG bit; for SDATA_OUT (controller to codec), the codec sets the SLOTREQ bit and then checks for the TAG bit in the next frame. Whenever VRA is set to 0 the PCM rate registers (2Ch and 32h) are overwritten with BB80h (48 kHz).

7.5.12.2. SPDIF

The SPDIF bit in the Extended Audio Status Control Register is used to enable and disable the SPDIF functionality within the STAC9750/51. If the SPDIF is set to a 1, then the function is enabled and when set to a 0 it is disabled.

7.5.12.3. SPCV (SPDIF Configuration Valid)

The SPCV bit is read only and indicates whether or not the SPDIF system is set up correctly. When SPCV is a 0, it indicates the system configuration is invalid and valid if it is a 1.

7.5.12.4. SPSA1, SPSA0 (SPDIF Slot Assignment)

SPSA1 and SPSA0 combine to provide the slot assignments for the SPDIF data. The following details the slot assignment relationship between SPSA1 and SPSA0.

SPSA[1,0]	Slot Assignment	Comments
00	3 & 4	SPDIF source data slot assignment
01	7 & 8	2-ch codec primary default
10	6 & 9	4-ch codec primary default
11	10 & 11	6-ch codec primary default

Table 29. Slot assignment relationship between SPSA1 and SPSA0

The STAC9750/51 are AMAP compliant with the following table.

Codec ID	Function	SPSA = 00	SPSA = 01	SPSA = 10	SPSA = 11
00	2-ch Primary w/SPDIF	3 & 4	7 & 8*	6 & 9	10 & 11
01	2-ch Dock Codec w/SPDIF	3 & 4	7 & 8	6 & 9*	10 & 11
10	+2-ch Surr w/ SPDIF	3 & 4	7 & 8	6 & 9*	10 & 11
11	+2-ch Cntr/LFE w/ SPDIF	3 & 4	7 & 8	6 & 9	10 & 11*

Note:* is the default slot assignment

Table 30. STAC9750/51 AMAP compliant

7.5.13. PCM DAC Rate Registers (2Ch and 32h)

The internal sample rate for the DACs and ADCs are controlled by the value in these read/write registers that contain a 16-bit unsigned value between 0 and 65535 representing the conversion rate in Hz. In VRA mode (register 2Ah bit D0 = 1), if the value written to these registers is supported that value will be echoed back when read, otherwise the closest (higher in the case of a tie) sample rate is supported and returned. Per PC 99 / PC 2001 specification, independent sample rates are supported for record and playback. Whenever VRA is set to 0 the PCM rate registers (2Ch and 32h) will readback with BB80h (48 kHz).

Sample Rate	SR15-SR0 Value
8 kHz	1F40h
11.025 kHz	2B11h
16 kHz	3E80h
22.05 kHz	5622h
32 kHz	7D00h
44.1 kHz	AC44h
48 kHz	BB80h

Table 31. Hardware Supported Sample Rates

7.5.14. PCM DAC Rate (2Ch)

Default: BB80h

D15	D14	D13	D12	D11	D10	D9	D8
SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0

7.5.15. PCM LR ADC Rate (32h)

Default: BB80h

D15	D14	D13	D12	D11	D10	D9	D8
SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0

7.5.16. SPDIF Control (3Ah)

Default: 2A00h

D15	D14	D13	D12	D11	D10	D9	D8
#V	DRS	SPSR1	SPSR2	L	CC6	CC5	CC4
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
CC3	CC2	CC1	CC0	PRE	COPY	#PCM/AUDIO	PRO

Register 3Ah is a read/write register that controls SPDIF functionality and manages bit fields propagated as channel status (or sub-frame in the V case). With exception of V, this register should only be written to when the SPDIF transmitter is disabled (SPDIF bit register 2 Ah is “0”). This ensures that control and status information start up correctly at the beginning of SPDIF transmission. The default is 2A00h which sets the SPDIF output sample rate at 48kHz and the normal SPDIF expectations.

Bit(s)	Reset	Access	Name	Description (note 1-2)
15	0	Read & Write	#V	Validity bit is set indicating each sub-frame's samples are invalid. If #V is 0, then it indicates that each sub-frame was transmitted and received correctly by the interface.
14	0	Read Only	DRS	1 = Double Rate SPDIF support (always = 0)
13:12	10	Read & Write	SPSR[1,0]	SPDIF Sample Rate. 00 44.1 kHz Rate 01 Reserved 10 48 kHz Rate (default) 11 32 kHz Rate
11	0	Read & Write	L	Generation Level is defined by the IEC standard, or as appropriate. (Always = 1)
10:4	0	Read & Write	CC[6, 0]	Category Code is defined by the IEC standard or as appropriate by media.
3	0	Read & Write	PRE	0 = 0 usec Pre-emphasis 1 = Pre-emphasis is 50/15 usec
2	0	Read & Write	COPY	0 = Copyright not asserted 1 = Copyright is asserted
1	0	Read & Write	/AUDIO	0 = PCM data 1 = Non-Audio or non-PCM format
0	0	Read & Write	PRO	0 = Consumer use of the channel 1 = Professional use of the channel

Table 32. SPDIF Control

1. If pin 48 is held high at powerup, 28h D2 will be low indicating no SPDIF available and the register 3Ah will then read back 0000h. Pin 48: To Enable SPDIF, use an 1K-10K external pulldown. To Disable SPDIF, use an 1K-10K external pullup. Do Not leave Pin 48 floating.
2. Bits D15,D13-D00 of this register cannot be written to without first setting Reg 2Ah bit D2=0 (SPDIF disabled) and Register 28h bit D2=1 (SPDIF avaliable).

7.5.17. Extended Modem Status and Control Register (3Eh) (Used in Revision CC1 and beyond)

Default: 0100h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED							PRA
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED							GPIO

Bit(s)	Access	Reset Value	Name	Description
15:9	Read Only	0	RESERVED	BIT NOT USED, SHOULD READ BACK 0
8	Read / Write	1	PRA	0=GPIO powered up / enabled 1=GPIO powered down / disabled
7:1	Read Only	0	RESERVED	BIT NOT USED, SHOULD READ BACK 0
0	Read Only	0	GPIO	0 = GPIO not ready (powered down) 1 = GPIO ready (powered up)

Table 33. Extended Moden Status and Control

7.5.18. GPIO Pin Configuration Register (4Ch) (Used in Revision CC1 and beyond)

Default: 0003h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED						GC1 (GPIO1)	GC0 (GPIO0)

Bit(s)	Access	Reset Value	Name	Description
15:2	Read Only	0	RESERVED	BIT NOT USED, SHOULD READ BACK 0
1	Read / Write	1	GC1	0 = GPIO1 configured as output 1 = GPIO1 configured as input
0	Read / Write	1	GC0	0 = GPIO0 configured as output 1 = GPIO0 configured as input

Table 34. GPIO Pin Configuration Register

7.5.19. GPIO Pin Polarity/Type Register (4Eh)(Used in Revision CC1 and beyond)

Default: FFFFh

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED						GP1 (GPIO1)	GP0 (GPIO0)

Bit(s)	Access	Reset Value	Name	Description
15:2	Read Only	0	RESERVED	BIT NOT USED, SHOULD READ BACK 0
1	Read / Write	1	GP1	0 = GPIO1 Input Polarity Inverted, CMOS output drive. 1 = GPIO1 Input Polarity Non-inverted, Open-Drain output drive.
0	Read / Write	1	GP0	0 = GPIO0 Input Polarity Inverted, CMOS output drive. 1 = GPIO0 Input Polarity Non-inverted, Open-Drain output drive.

Table 35. GPIO Pin Polarity/Type Register

7.5.20. GPIO Pin Sticky Register (50h) (Used in Revision CC1 and beyond)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED						GS1 (GPIO1)	GS0 (GPIO0)

Bit(s)	Access	Reset Value	Name	Description
15:2	Read Only	0	RESERVED	BIT NOT USED, SHOULD READ BACK 0
1	Read / Write	0	GS1	0 = GPIO1 Non Sticky configuration. 1 = GPIO1 Sticky configuration.
0	Read / Write	0	GS0	0 = GPIO0 Non Sticky configuration. 1 = GPIO0 Sticky configuration.

Table 36. GPIO Pin Sticky Register

7.5.21. GPIO Pin Mask Register (52h)(Used in Revision CC1 and beyond)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED						GW1 (GPIO1)	GW0 (GPIO0)

Bit(s)	Access	Reset Value	Name	Description
15:2	Read Only	0	RESERVED	BIT NOT USED, SHOULD READ BACK 0
1	Read / Write	0	GW1	0 = GPIO1 interrupt not passed to GPIO_INT slot 12. 1 = GPIO1 interrupt is passed to GPIO_INT slot 12.
0	Read / Write	0	GW0	0 = GPIO0 interrupt not passed to GPIO_INT slot 12. 1 = GPIO0 interrupt is passed to GPIO_INT slot 12.

Table 37. GPIO Pin Mask Register

7.5.22. GPIO Pin Status Register (54h) (Used in Revision CC1 and beyond)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED						GI1 (GPIO1)	GI0 (GPIO0)

Bit(s)	Access	Reset Value	Name	Description
15:2	Read Only	0	RESERVED	BIT NOT USED, SHOULD READ BACK 0
1	Read / Write	x	GI1	When GPIO1 is configured as output and Register h74 bit[0] = 0 (default), the value of this register will be placed on the GPIO1 pad. When GPIO1 is configured as output and Register h74 bit[0] =1, the GPIO1 pad will get its value from slot12. When GPIO1 is configured as input and configured as a sticky writing a 1 does nothing, writing a 0 clears this bit. When GPIO1 is configured as input this register reflects the value on the GPIO1 pad after interpretation of the polarity and sticky configurations.
0	Read / Write	x	GI0	When GPIO0 is configured as output and Register h74 bit[0] = 0 (default), the value of this register will be placed on the GPIO0 pad. When GPIO0 is configured as output and Register h74 bit[0] =1, the GPIO0 pad will get its value from slot12. When GPIO0 is configured as input and configured as a sticky writing a 1 does nothing, writing a 0 clears this bit. When GPIO0 is configured as input this register reflects the value on the GPIO0 pad after interpretation of the polarity and sticky configurations.

Table 38. GPIO Pin Status Register

7.5.23. Digital Audio Control (6Ah)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED						DO1	DO0

Bit(s)	Reset	Name	Description
15:2	0	RESERVED	BITS NOT USED, SHOULD READ BACK 0
1	0	DO1	**SPDIF Digital Output Source Selection:** DO1 = 0; PCM data from the AC-Link to SPDIF DO1 = 1; ADC record data to SPDIF
0	0	DO0	Always reads zero

Table 39. Digital Audio Control Register

This read/write register is used to program the digital mixer input status. In the default state, the PCM DAC path is enabled and the ADC record inputs are disabled.

The DO1 and DO0 bits control the input source for the PCM to digital output converters. The table describes the available options.

7.5.24. Revision Code (6Ch)

Default: 00xxh

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	0	0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0

The device Revision register (index 6Ch) contains a software readable revision-specific code used to identify performance, architectural, or software differences between various device revisions. Bits 7:0 of the Revision register are user readable; bits 15:8 are not used at this time and will return zeros when read. This value can be used by the audio driver, or miniport driver in the case of WIN98® WDM approaches, to adjust software functionality to match the feature-set of the STAC9750/51. This will allow the software driver to identify any required operational differences between the existing STAC9750/51 and any future versions.

7.5.25. Analog Special (6Eh)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED			AC97 ALL MIX	RESERVED			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RSVD	MUTE FIX DISABLE	ADCSLT1	ADCSLT0	RESERVED	20/30 SEL	SPLYOVR EN	SPLYOVR VAL

The Analog Special Register has several bits used to control various functions specific to the STAC9750/51.

7.5.25.1. ALL MIX

The AC'97 ALL MIX, bit D12 of register 6Eh, controls the record source when the Stereo Mix option is selected for recording. If the AC97 mode is default logic 1, the Stereo Mix Record option will include the sum of the analog sources with or without 3D enhancement, and the main PCM DAC output. If the “ALL Analog Record” option is selected, the Stereo Mix Record option will include the sum of the analog sources only, with or without 3D enhancement. The “AC'97 mode” is useful for recording all sound sources. The “ALL Analog” mode is useful in conjunction with the POP BYPASS mode for recording all analog sources, which are often further processed and combined with other PCM data to be output directly to the DAC outputs which are configured in POP_BYPASS mode using the General Purpose register (index 20h).

7.5.25.2. ADC Data on AC LINK

Bits D5-D4 select slots for ADC data on ACLINK.

Value	Function
00	left slot 3, right slot 4
01	left slot 7, right slot 8
10	left slot 6, right slot 9
11	left slot 10, right slot 11

Table 40. ADC data on AC LINK

7.5.25.3. MuteFix Disable ***(Used in Revision CC1 and beyond)***

Bit D6 controls the enable and disable of the MuteFix functions.

0 = MUTE FIX Enabled

1 = MUTE FIX Disabled

When this bit is zero, and either channel is set to -46.5dB attenuation, 1Fh, then that channel is fully muted. When this bit is one, then operation is per AC'97 specificaiton.

This bit is RESERVED in revisions prior to CC1.

7.5.25.4. Mic Boost Select

The Mic boost value can be selected with Bit D2, which in enabled by Register 0Eh, bit D6. Writing a zero to Bit 2 will provide 20dB of Mic Boost. Writing a one will provide 30dB of Mic Boost.

Value	Function
0	**20dB**
1	**30dB**

Table 41. Mic Boost Select

7.5.25.5. Supply Override Select

The Supply Override bit, D1, allows override of the supply detect. Writing a zero disables the override on supply detect. Writing a one, overrides supply detect with Bit D0. Bit D0 provides the supply override value. A zero forces 3.3V analog operation and one forces 5V analog operation.

7.5.25.6. 72h Enable (70h)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
EN15	EN14	EN13	EN12	EN11	EN10	EN9	EN8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0

7.5.25.7. Analog Current Adjust (72h)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
INT APOP	RESERVED				IBIAS1	IBIAS0	RSVD

The Analog Current Adjust register (index 72h) is a locked register and can only be properly written and read from when ABBAh has been written into register 70h. The BIASx bits allow the analog current to be adjusted with minimal reduction in performance. A lower analog current setting is NOT recommended when a 5V analog supply is used. A lower setting for 3.3V supplies is recommended to reduce power consumption for notebook computers to its lowest level.

IBIAS1	IBIAS0	Analog Current
0	0	Normal Current
0	1	80% of nominal Analog Current
1	0	120% of nominal Analog Current
1	1	140% of nominal Analog Current

Table 42. Analog Current Adjust

7.5.25.8. Internal Power-On/Off Anti-Pop Circuit

The STAC9750/51 includes an internal power supply anti-pop circuit that prevents audible clicks and pops from being heard when the codec is powered on and off. This function is accomplished by delaying the charge/discharge of the VREF capacitor (Pin 27). C_{VREF} value of 1uF will cause a turn-on delay of roughly 3 seconds, which will allow the power supplies to stabilize before the codec outputs are enabled. The delay will be extended to 30 seconds if a value of C_{VREF} value of 10uF is used. The codec outputs are also kept stable for the same amount of time at power-off to allow the system to be gracefully turned off. The INT_APOP bit D7 of register 72h allows this delay circuit to be bypassed for rapid production testing. Any external component anti-pop circuit is unaffected by the internal circuit.

7.5.26. GPIO Access Register (74h) (Used only in CA3 revision for GPIO)

EAPD Access for ALL revisions is Register 74h.

Default: 0800h

D15	D14	D13	D12	D11	D10	D9	D8
EAPD	RESERVED	GPIO1	GPIO0	EAPD_OEN	RESERVED	GPIO1_OEN	GPIO0_OEN
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED							

Bit(s)	Reset Value	Name	Description
15	0	EAPD	EAPD data output on EAPD when bit D11=1 EAPD data input from pin when bit D11=0
14	0	RESERVED	RESERVED
13	0	GPIO1	GPIO1 data output on GPIO1 when bit D9=1 GPIO1 data input from pin when bit D9=0
12	0	GPIO0	GPIO0 data output on GPIO0 when bit D8=1 GPIO0 data input from pin when bit D8=0
11	1	EAPD_OEN	0 = EAPD data out disabled 1 = EAPD data output enabled
10	0	RESERVED	RESERVED
9	0	GPIO1_OEN	0 = GPIO1 data out disabled 1 = GPIO1 data output enabled
8	0	GPIO0_OEN	0 = GPIO0 data out disabled 1 = GPIO0 data output enabled
7:0	0	RESERVED	RESERVED

Table 43. GPIO Access Registers (74h)

The GPIO Access Register requires the output enable bits (D11, D9 and D8) be used in conjunction with the data source selection (input or output) for the EAPD, GPIO0 and GPIO1 (pins 47, 43 and 44 respectively) . For example, to use GPIO1 as an output, set D9=1 to enable the output, and use D13 to write the output value desired. To use GPIO1 as an input, set D9=0 to disable the output, and use D13 to read the input value.

7.5.27. High Pass Filter Bypass (Index 76h and 78h)

The High Pass Filter Bypass register (index 78h) is a locked register and can only be properly written and read from when ABBAh has been written into register 76h. Bit D0 controls the High Pass Filter Bypass. Default is zero which provides for normal operation where the high pass filter is active. Writing a one, will disable, or bypass the ADC high pass filter.

7.5.27.1. 78h Enable (76h)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
EN15	EN14	EN13	EN12	EN11	EN10	EN9	EN8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0

7.5.27.2. ADC High Pass FIlter Bypass(78h)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED							ADC HPF BYP

7.5.28. Vendor ID1 and ID2 (Index 7Ch and 7Eh)

These two registers contain four 8-bit ID codes. The first three codes have been assigned by Microsoft using their Plug and Play Vendor ID methodology. The fourth code is a SigmaTel, Inc. assigned code identifying the STAC9750/51. The ID1 register (index 7Ch) contains the value 8384h, which is the first (83h) and second (84h) characters of the Microsoft ID code. The ID2 register (index 7Eh) contains the value 7650h, which is the third (76h) of the Microsoft ID code, and 50h which is the STAC9750/51 ID code.

Note: The lower half of the Vendor ID2 register (index 7Eh) currently contains the value xxh identifying the STAC9750/51. This value can be used by the audio driver, or miniport driver in the case of WIN98®, to adjust software functionality to match the feature-set of the STAC9750/51. This portion of the register will likely contain different values if the software profile of the STAC9750/51 changes, as in the case of silicon level device modifications. This will allow the software driver to identify any required operational differences between the existing STAC9750/51 and any future versions.

7.5.28.1. Vendor ID1 (7Ch)

Default: 8384h

D15	D14	D13	D12	D11	D10	D9	D8
1	0	0	0	0	0	1	1
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	0	0	0	0	1	0	0

7.5.28.2. Vendor ID2 76xx (7Eh)

Default: 7650h

D15	D14	D13	D12	D11	D10	D9	D8
0	1	1	1	0	1	1	0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	0	0	0	0

8. LOW POWER MODES

The STAC9750/51 is capable of operating at reduced power when no activity is required. The state of power down is controlled by the Powerdown Register (26h). There are 7 commands of separate power down. The power down options are listed in Table 44. The first three bits, PR0..PR2, can be used individually or in combination with each other, and control power distribution to the ADC's, DAC's and Mixer. The last analog power control bit, PR3, affects analog bias and reference voltages, and can only be used in combination with PR1, PR2, and PR3. PR3 essentially removes power from all analog sections of the codec, and is generally only asserted when the codec will not be needed for long periods. PR0 and PR1 control the PCM ADC's and DAC's only. PR2 and PR3 do not need to be "set" before a PR4, but PR0 and PR1 must be "set" before PR4. PR5 disables the internal codec clock and requires an external cold reset for recovery. PR6 disables the headphone driver amplifier for additional analog power saving.

GRP Bits	Function
PR0	PCM in ADC's & Input Mux Powerdown
PR1	PCM out DACs Powerdown
PR2	Analog Mixer powerdown (VREF still on)
PR3	Analog Mixer powerdown (VREF off)
PR4	Digital Interface (AC-Link) powerdown (extnl clk off)
PR5	Internal Clk disable
PR6	Powerdown HEADPHONE_OUT

Table 44. Low Power Modes

The Figure 19 illustrates one example procedure to do a complete powerdown of STAC9750/51. From normal operation, sequential writes to the Powerdown Register are performed to power down STAC9750/51 a piece at a time. After everything has been shut off, a final write (of PR4) can be executed to shut down the AC-Link. The part will remain in sleep mode with all its registers holding their static values. To wake up, the AC'97 controller will send an extended pulse on the sync line, issuing a warm reset. This will restart the AC-Link (resetting PR4 to zero). The STAC9750/51 can also be woken up with a cold reset. A cold reset will reset all of the registers to their default states. When a section is powered back on, the Powerdown Control/Status register (index 26h) should be read to verify that the section is ready (stable) before attempting any operation that requires it.

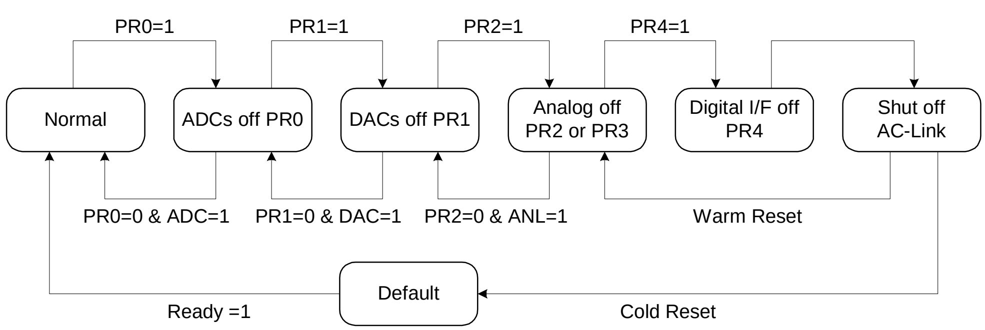


Figure 19. Example of STAC9750/51 Powerdown/Powerup flow

Figure 20 illustrates a state when all the mixers should work with the static volume settings that are contained in their associated registers. This configuration can be used when playing a CD (or external LINE_IN source) through STAC9750/51 to the speakers, while most of the system in low power mode. The procedure for this follows the previous except that the analog mixer is never shut down.

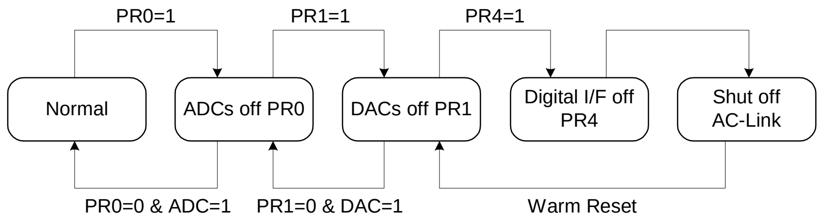


Figure 20. STAC9750/51 Powerdown/Powerup flow with analog still alive

9. MULTIPLE CODEC SUPPORT

The STAC9750/51 provides support for the multi-codec option according to the Intel AC'97, rev 2.2 specification. By definition there can be only one Primary Codec (Codec ID 00) and up to three Secondary Codecs (Codec IDs 01,10, and 11). The Codec ID functions as a chip select. Secondary devices therefore have completely orthogonal register sets; each is individually accessible and they do not share registers.

9.1. Primary/Secondary Codec Selection

In a multi-codec environment the codec ID is provided by external programming of pins 45 and 46 (CID0 and CID1). The CID pin electrical function is logically inverted from the codec ID designation. The corresponding pin state and its associated codec ID are listed in the “Codec ID Selection” table. Also see slot assignment discussion, “Multi-Channel Programming Register (Index 74)”.

CID1 State	CID0 State	Codec ID	Codec Status
Dvdd or floating	Dvdd or floating	00	Primary
Dvdd or floating	0V	01	Secondary
0V	Dvdd or floating	10	Secondary
0V	0V	11	Secondary

Table 45. Codec ID Selection

9.1.1. Primary Codec Operation

As a Primary device the STAC9750/51 is completely compatible with existing AC'97 definitions and extensions. Primary Codec registers are accessed exactly as defined in the AC'97 Component Specification and AC'97 Extensions. The STAC9750/51 operates as Primary by default, and the external ID pins (45 and 46), have internal pull-ups so that these pins may be left as no-connects for primary operation.

When used as the Primary Codec, the STAC9750/51 generates the master AC-Link BIT_CLK for both the AC'97 Digital Controller and any Secondary Codecs. The STAC9750/51 can support up to 4, 10 KΩ 50 pF loads on the BIT_CLK. This is to insure that up to 4 Codec implementations will not load down the clock output.

9.1.2. Secondary Codec Operation

When the STAC9750/51 is configured as a Secondary device the BIT_CLK pin is configured as an input at power up. Using the BIT_CLK provided by the Primary Codec insures that everything on the AC-Link will be synchronous. As a Secondary device it can be defined as Codec ID 01, 10, or 11 in the two-bit field(s) of the Extended Audio and/or Extended Modem ID Register(s).

9.2. Secondary Codec Register Access Definitions

The AC'97 Digital Controller can independently access Primary and Secondary Codec registers by using a 2-bit Codec ID field (chip select) which is defined as the LSBs of Output Slot 0. For Secondary Codec access, the AC'97 Digital Controller must *invalidate* the tag bits for Slot 1 and 2 Command Address and Data (Slot 0, bits 14 and 13) and place a *non-zero* value (01, 10, or 11) into the Codec ID field (Slot 0, bits 1 and 0).

As a Secondary Codec, the STAC9750/51 will disregard the Command Address and Command Data (Slot 0, bits 14 and 13) tag bits when it sees a 2-bit Codec ID value (Slot 0, bits 1 and 0) that matches its configuration. In a sense the Secondary Codec ID field functions as an alternative Valid Command Address (for Secondary reads and writes) and Command Data (for Secondary writes) tag indicator.

Secondary Codecs must monitor the Frame Valid bit, and ignore the frame (regardless of the state of the Secondary Codec ID bits) if it is not valid. AC'97 Digital Controllers should set the frame valid bit for a frame with a secondary register access, even if no other bits in the output tag slot except the Secondary Codec ID bits are set.

This method is designed to be backward compatible with existing AC'97 controllers and Codecs. There is no change to output Slot 1 or 2 definitions.

Output Tag Slot (16-bits)	
Bit	**Description**
15	Frame Valid
14	Slot 1 Valid Command Address bit (†Primary Codec only)
13	Slot 2 Valid Command Data bit (†Primary Codec only)
12-3	Slot 3-12 Valid bits as defined by AC'97
2	Reserved (Set to “0”)
†1-0	2-bit Codec ID field (00 reserved for Primary; 01, 10, 11 indicate Secondary)

Note: † New definitions for Secondary Codec Register Access

Table 46. Secondary Codec Register Access Slot 0 Bit Definitions

10. TESTABILITY

The STAC9750/51 has two test modes. One is for ATE in-circuit test and the other is restricted for SigmaTel's internal use. STAC9750/51 enters the ATE in circuit test mode if SDATA_OUT is sampled high at the trailing edge of RESET#. Once in the ATE test mode, the digital AC-Link outputs (BIT_CLK and SDATA_IN) are driven to a high impedance state. This allows ATE in-circuit testing of the AC'97 controller. Use of the ATE test mode is the recommended means of removing the codec from the AC-Link when another codec is to be used as the primary. This case will never occur during standard operating conditions. Once either of the two test modes have been entered, the STAC9750/51 must be issued another RESET# with all AC-link signals held low to return to the normal operating mode.

11. PIN DESCRIPTION

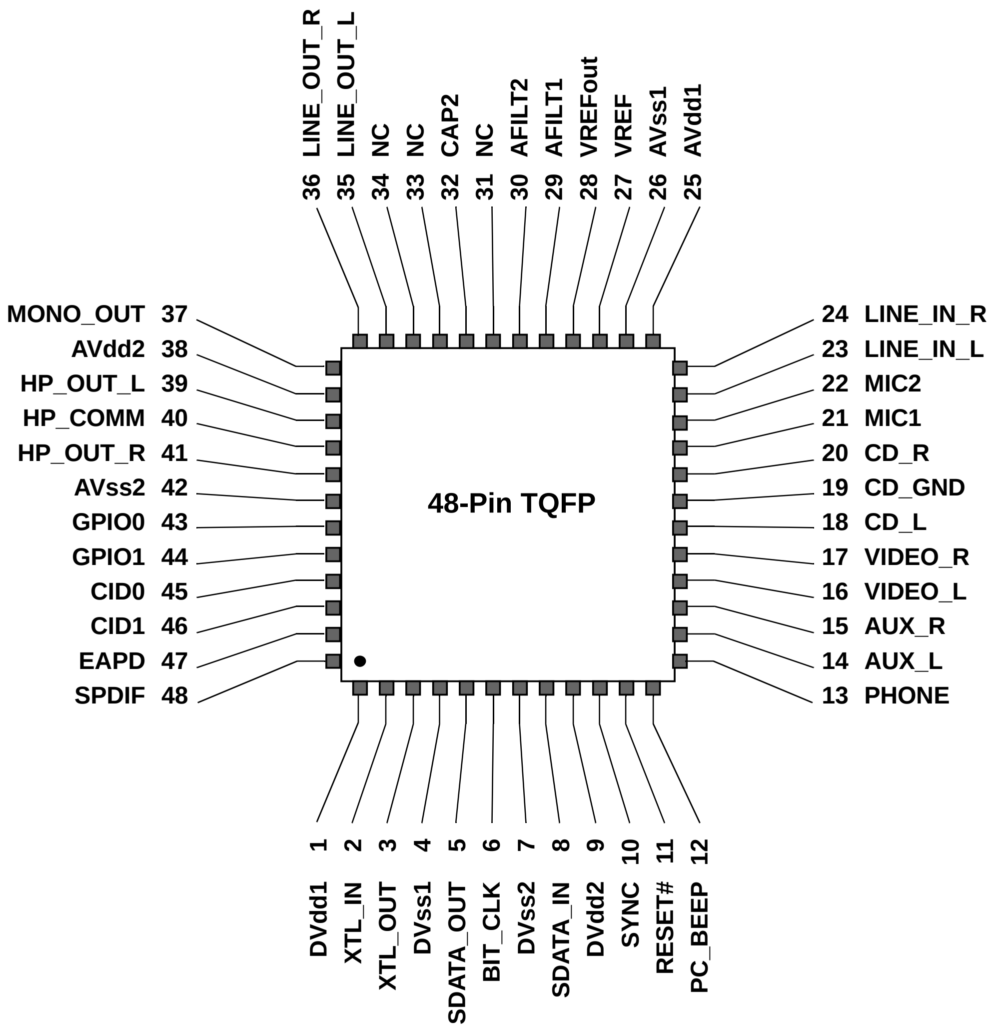


Figure 21. STAC9750/51 Pin Description Drawing

Pin 48: To Enable SPDIF, use an 1K-10K external pulldown. To Disable SPDIF, use an 1K-10K external pullup. Do Not leave Pin 48 floating.

The CD_GND signal is an AC signal return for the two CD input channels. It is normally biased at about 2.5V. The name of the pin in the AC97 specification is CD_GND, and this has confused many designers. It should not have any DC path to GND. Connecting the CD_GND signal directly to ground will change the internal bias of the entire codec, and cause bad distortion. If there is no analog CD input, then this pin can be No-Connect

11.1. Digital I/O

These signals connect the STAC9750/51 to its AC'97 controller counterpart, an external crystal, multi-codec selection and external audio amplifier.

Pin Name	Pin #	Type	Description
XTL_IN	2	I	24.576 MHz Crystal or External Clock Source
XTL_OUT	3	I/O	24.576 MHz Crystal or ground if external clock source connected to XTAL_IN
SDATA_OUT	5	I	Serial, time division multiplexed, AC'97 input stream
BIT_CLK	6	I/O	12.288 MHz serial data clock
SDATA__IN	8	O	Serial, time division multiplexed, AC'97 output stream
SYNC	10	I	48 kHz fixed rate sample sync
RESET#	11	I	AC'97 Master H/W Reset
NC	31	I/O	No Connect
NC	33	I/O	No Connect
NC	34	I/O	No Connect
GPIO0	43	I/O	General Purpose I/O
GPIO1	44	I/O	General Purpose I/O
CID0	45	I	Multi-Codec ID select – bit 0
CID1	46	I	Multi-Codec ID select – bit 1
EAPD	47	I/O	External Amplifier Power Down
SPDIF	48	O	SPDIF digital output Pin 48: To Enable SPDIF, use an 1K-10K external pulldown. To Disable SPDIF, use an 1K-10K external pullup. Do Not leave Pin 48 floating.

Table 47. Digital Connection Signals

11.2. Analog I/O

These signals connect the STAC9750/51 to analog sources and sinks, including microphones and speakers.

Pin Name	Pin #	Type	Description
PC-BEEP	12	I*	PC Speaker beep pass-through
PHONE	13	I*	From telephony subsystem speakerphone (or DLP:Down Line Phone)
AUX_L	14	I*	Aux Left Channel
AUX_R	15	I*	Aux Right Channel
VIDEO_L	16	I*	Video Audio Left Channel
VIDEO_R	17	I*	Video Audio Right Channel
CD_L	18	I*	CD Audio Left Channel
CD_GND	19	I*	CD Audio analog ground
CD_R	20	I*	CD Audio Right Channel
MIC1	21	I*	Desktop Microphone Input
MIC2	22	I*	Second Microphone Input
LINE_IN_L	23	I*	Line In Left Channel
LINE_IN_R	24	I*	Line In Right Channel
LINE_OUT_L	35	O	Line Out Left Channel
LINE_OUT_R	36	O	Line Out Right Channel
MONO_OUT	37	O	To telephony subsystem speakerphone(or DLP – Down Line Phone)
HP_OUT_L	39	O	Headphone Out Left Channel
HP_COMM	40	O	Headphone Ground Return
HP_OUT_R	41	O	Headphone Out Right Channel

Table 48. Analog Connection Signals

Note: * any unused input pins should be tied together through a capacitor (0.1 µF suggested) to ground, except the MIC inputs which should have their own capacitor to ground if not used.

The CD_GND signal is an AC signal return for the two CD input channels. It is normally biased at about 2.5V. The name of the pin in the AC97 specification is CD_GND, and this has confused many designers. It should not have any DC path to GND. Connecting the CD_GND signal directly to ground will change the internal bias of the entire codec, and cause bad distortion. If there is no analog CD input, then this pin can be No-Connect

11.3. Filter/References/GPIO

These signals are connected to resistors, capacitors, specific voltages, or provide general purpose I/O.

Signal Name	Pin Number	Type	Description
VREF	27	O	Analog ground (.45*vdd, at 5V; .41*vdd at 3V)
VREFOUT	28	O	Reference Voltage out 5mA drive (intended for mic bias) (~vdd/2)
AFILT1	29	O	Anti-Aliasing Filter Cap - ADC left channel
AFILT2	30	O	Anti-Aliasing Filter Cap - ADC right channel
CAP2	32	O	ADC reference Cap

Table 49. Filtering and Voltage References

11.4. Power and Ground Signals

Pin Name	Pin #	Type	Description
AVdd1	25	I	Analog Vdd = 5.0V or 3.3V
AVdd2	38	I	Analog Vdd = 5.0V or 3.3V (headphone power source)
AVss1	26	I	Analog Gnd
AVss2	42	I	Analog Gnd
DVdd1	1	I	Digital Vdd = 3.3V
DVdd2	9	I	Digital Vdd = 3.3V
DVss1	4	I	Digital Gnd
DVss2	7	I	Digital Gnd

Table 50. Power and Ground Signals

12. PACKAGE DRAWING

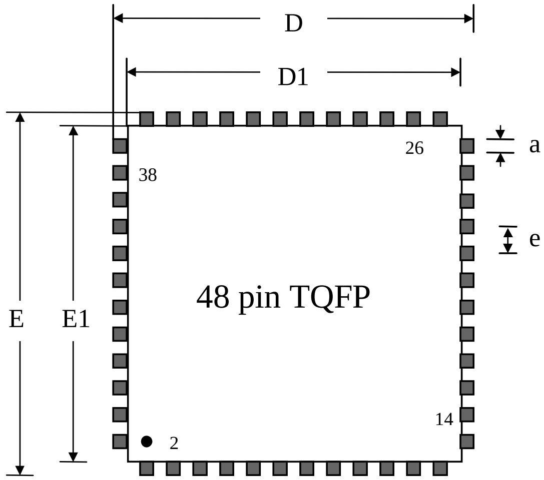


Figure 22. 48-Pin TQFP Package Drawing

Key	TQFP Dimensions
D	9.00 mm
D1	7.00 mm
E	9.00 mm
E1	7.00 mm
a (lead width)	0.20 mm
e (pitch)	0.50 mm
thickness	1.4 mm

Table 51. 48-Pin TQFP Package Dimensions

13. APPENDIX A: SPLIT INDEPENDENT POWER SUPPLY OPERATION

In PC applications, one power supply input to the STAC9750/51 may be derived from a supply regulator (as shown in Figure 23) and the other directly from the PCI power supply bus. When power is applied to the PC, the regulated supply input to the IC will be applied some time delay after the PCI power supply. Without proper on-chip partitioning of the analog and digital circuitry, some manufacturer's codecs would be subject to on-chip SCR type latch-up.

SigmaTel's STAC9750/51 specifically allows power-up sequencing delays between the analog (AVddx) and digital (VDddx) supply pins. These two power supplies can power-up independently and at different rates with no adverse effects to the codec. The IC is designed with independent analog and digital circuitry that prevents on-chip SCR type latch-up.

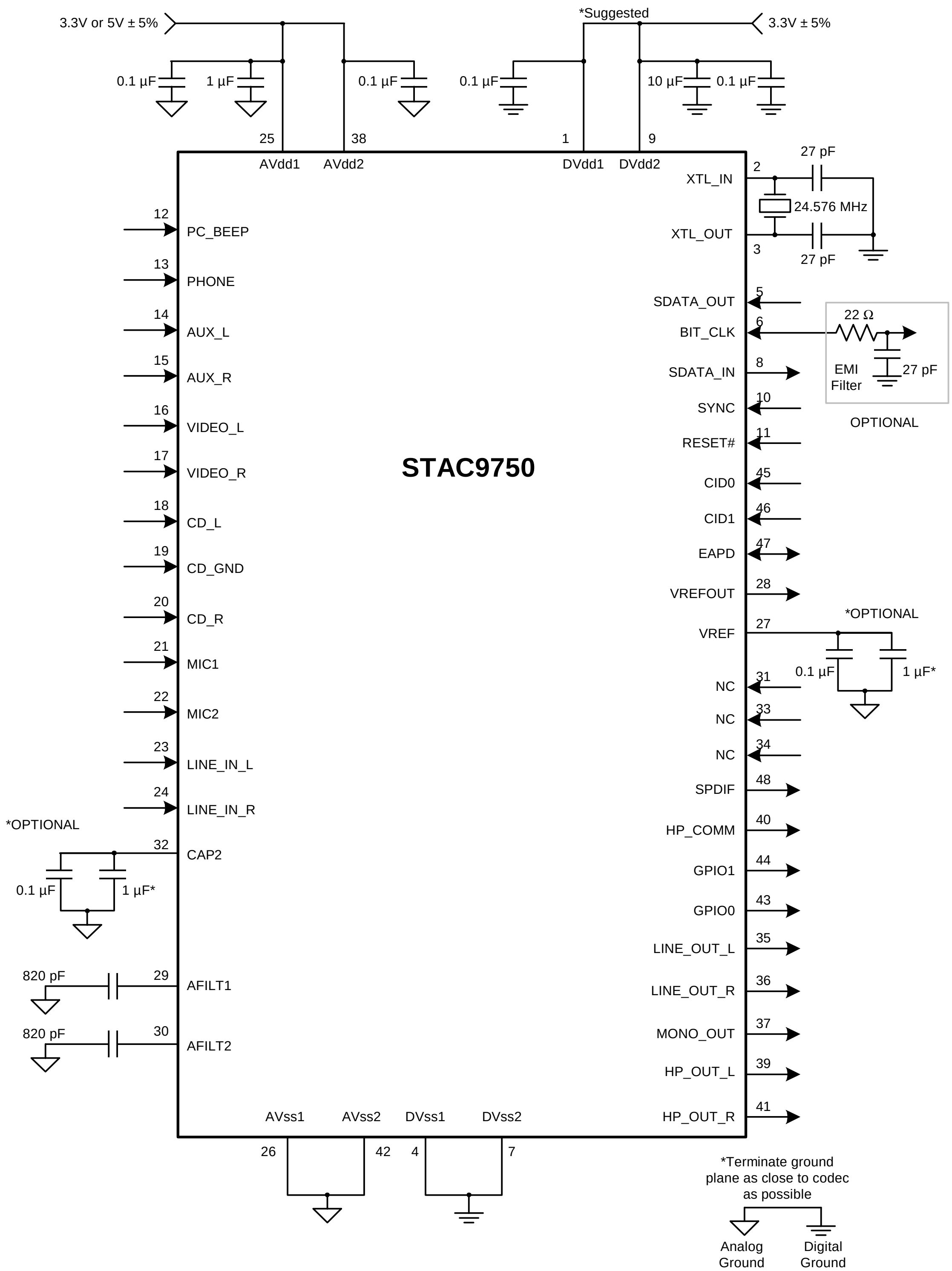


Figure 23. STAC9750/51 Split Independent Power Supply Operation Typical Connection Diagram

Pin 48: To Enable SPDIF, use an 1K-10K external pulldown. To Disable SPDIF, use an 1K-10K external pullup. Do Not leave Pin 48 floating.

14. APPENDIX B: PROGRAMMING REGISTERS

<table>
<tr><th>Reg #</th><th>Name</th><th>D15</th><th>D14</th><th>D13</th><th>D12</th><th>D11</th><th>D10</th><th>D9</th><th>D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>00h</td><td>Reset</td><td>RSRVD</td><td>SE4</td><td>SE3</td><td>SE2</td><td>SE1</td><td>SE0</td><td>ID9</td><td>ID8</td><td>ID7</td><td>ID6</td><td>ID5</td><td>ID4</td><td>ID3</td><td>ID2</td><td>ID1</td><td>ID0</td><td>6990h</td></tr>
<tr><td>02h</td><td>Master Volume</td><td>Mute</td><td>RSRVD</td><td>ML5</td><td>ML4</td><td>ML3</td><td>ML2</td><td>ML1</td><td>ML0</td><td colspan="2">RESERVED</td><td>MR5</td><td>MR4</td><td>MR3</td><td>MR2</td><td>MR1</td><td>MR0</td><td>8000h</td></tr>
<tr><td>04h</td><td>HP_OUT Mixer Volume</td><td>Mute</td><td>RSRVD</td><td>HPL5</td><td>HPL4</td><td>HPL3</td><td>HPL2</td><td>HPL1</td><td>HPL0</td><td colspan="2">RESERVED</td><td>HPR5</td><td>HPR4</td><td>HPR3</td><td>HPR2</td><td>HPR1</td><td>HPR0</td><td>8000h</td></tr>
<tr><td>06h</td><td>Master Volume Mono</td><td>Mute</td><td colspan="9">RESERVED</td><td>MM5</td><td>MM4</td><td>MM3</td><td>MM2</td><td>MM1</td><td>MM0</td><td>8000h</td></tr>
<tr><td>0Ah</td><td>PC_BEEP Volume</td><td>Mute</td><td colspan="10">RESERVED</td><td>PV3</td><td>PV2</td><td>PV1</td><td>PV0</td><td>RSRVD</td><td>0000h</td></tr>
<tr><td>0Ch</td><td>Phone Volume</td><td>Mute</td><td colspan="10">RESERVED</td><td>GN4</td><td>GN3</td><td>GN2</td><td>GN1</td><td>GN0</td><td>8008h</td></tr>
<tr><td>0Eh</td><td>Mic Volume</td><td>Mute</td><td colspan="8">RESERVED</td><td>boosted</td><td>RSRVD</td><td>GN4</td><td>GN3</td><td>GN2</td><td>GN1</td><td>GN0</td><td>8008h</td></tr>
<tr><td>10h</td><td>Line In Volume</td><td>Mute</td><td colspan="2">RESERVED</td><td>GL4</td><td>GL3</td><td>GL2</td><td>GL1</td><td>GL0</td><td colspan="3">RESERVED</td><td>GR4</td><td>GR3</td><td>GR2</td><td>GR1</td><td>GR0</td><td>8808h</td></tr>
<tr><td>12h</td><td>CD Volume</td><td>Mute</td><td colspan="2">RESERVED</td><td>GL4</td><td>GL3</td><td>GL2</td><td>GL1</td><td>GL0</td><td colspan="3">RESERVED</td><td>GR4</td><td>GR3</td><td>GR2</td><td>GR1</td><td>GR0</td><td>8808h</td></tr>
<tr><td>14h</td><td>Video Volume</td><td>Mute</td><td colspan="2">RESERVED</td><td>GL4</td><td>GL3</td><td>GL2</td><td>GL1</td><td>GL0</td><td colspan="3">RESERVED</td><td>GR4</td><td>GR3</td><td>GR2</td><td>GR1</td><td>GR0</td><td>8808h</td></tr>
<tr><td>16h</td><td>AUX Volume</td><td>Mute</td><td colspan="2">RESERVED</td><td>GL4</td><td>GL3</td><td>GL2</td><td>GL1</td><td>GL0</td><td colspan="3">RESERVED</td><td>GR4</td><td>GR3</td><td>GR2</td><td>GR1</td><td>GR0</td><td>8808h</td></tr>
<tr><td>18h</td><td>PCM Out Volume</td><td>Mute</td><td colspan="2">RESERVED</td><td>GL4</td><td>GL3</td><td>GL2</td><td>GL1</td><td>GL0</td><td colspan="3">RESERVED</td><td>GR4</td><td>GR3</td><td>GR2</td><td>GR1</td><td>GR0</td><td>8808h</td></tr>
<tr><td>1Ah</td><td>Record Select</td><td colspan="5">RESERVED</td><td>SL2</td><td>SL1</td><td>SL0</td><td colspan="5">RESERVED</td><td>SR2</td><td>SR1</td><td>SR0</td><td>0000h</td></tr>
<tr><td>1Ch</td><td>Record Gain</td><td>Mute</td><td colspan="3">RESERVED</td><td>GL3</td><td>GL2</td><td>GL1</td><td>GL0</td><td colspan="4">RESERVED</td><td>GR3</td><td>GR2</td><td>GR1</td><td>GR0</td><td>8000h</td></tr>
<tr><td>20h</td><td>General Purpose</td><td>POP BYP</td><td>RSRVD</td><td>3D</td><td colspan="3">RESERVED</td><td>MIX</td><td>MS</td><td>LPBK</td><td colspan="7">RESERVED</td><td>0000h</td></tr>
<tr><td>22h</td><td>3D Control</td><td colspan="12">RESERVED</td><td>DP3</td><td>DP2</td><td colspan="2">RESERVED</td><td>0000h</td></tr>
<tr><td>24h**</td><td>Audio Interrupt</td><td>I4</td><td>I3</td><td colspan="2">RESERVED</td><td>I0</td><td colspan="11">RESERVED</td><td>0000h</td></tr>
<tr><td>26h</td><td>Powerdown Ctrl/Stat</td><td>EAPD</td><td>PR6</td><td>PR5</td><td>PR4</td><td>PR3</td><td>PR2</td><td>PR1</td><td>PR0</td><td colspan="4">RESERVED</td><td>REF</td><td>ANL</td><td>DAC</td><td>ADC</td><td>000Fh</td></tr>
<tr><td>28h</td><td>Extended Audio ID</td><td>ID1</td><td>ID0</td><td colspan="2">RESERVED</td><td>REV1 (0)</td><td>REV0 (1)</td><td>AMAP</td><td>LDAC</td><td>SDAC</td><td>CDAC</td><td>DSA1</td><td>DSA0</td><td>RSVD</td><td>SPDIF</td><td>DRA</td><td>VRA</td><td>0605h</td></tr>
<tr><td>2Ah</td><td>Extended Audio Control/ Status</td><td colspan="5">RESERVED</td><td>SPCV</td><td colspan="4">RSRVD</td><td>SPSA1</td><td>SPSA0</td><td>RSRVD</td><td>SPDIF</td><td>RSRVD</td><td>VRA enable</td><td>0400h</td></tr>
<tr><td>2Ch</td><td>PCM DAC Rate</td><td>SR15</td><td>SR14</td><td>SR13</td><td>SR12</td><td>SR11</td><td>SR10</td><td>SR9</td><td>SR8</td><td>SR7</td><td>SR6</td><td>SR5</td><td>SR4</td><td>SR3</td><td>SR2</td><td>SR1</td><td>SR0</td><td>BB80h</td></tr>
<tr><td>32h</td><td>PCM LR ADC Rate</td><td>SR15</td><td>SR14</td><td>SR13</td><td>SR12</td><td>SR11</td><td>SR10</td><td>SR9</td><td>SR8</td><td>SR7</td><td>SR6</td><td>SR5</td><td>SR4</td><td>SR3</td><td>SR2</td><td>SR1</td><td>SR0</td><td>BB80h</td></tr>
<tr><td>3Ah</td><td>SPDIF Control</td><td>#V</td><td>DRS</td><td>SPSR1</td><td>SPSR2</td><td>L</td><td>CC6</td><td>CC5</td><td>CC4</td><td>CC3</td><td>CC2</td><td>CC1</td><td>CC0</td><td>PRE</td><td>COPY</td><td>#PCM/ AUDIO</td><td>PRO</td><td>2A00h</td></tr>
<tr><td>3Eh**</td><td>Extended Modem Status</td><td colspan="7">RESERVED</td><td>PRA</td><td colspan="7">RESERVED</td><td>GPIO</td><td>0100h</td></tr>
<tr><td>4Ch**</td><td>GPIO Pin Config</td><td colspan="14">RESERVED</td><td>GC1 (GPIO1)</td><td>GC0 (GPIO0)</td><td>0300h</td></tr>
<tr><td>4Eh**</td><td>GPIO Pin Polarity/Type</td><td colspan="14">RESERVED</td><td>GP1 (GPIO1)</td><td>GP0 (GPIO0)</td><td>FFFFh</td></tr>
<tr><td>50h**</td><td>GPIO Pin Sticky</td><td colspan="14">RESERVED</td><td>GS1 (GPIO1)</td><td>GS0 (GPIO0)</td><td>0000h</td></tr>
<tr><td>52h**</td><td>GPIO Pin Mask</td><td colspan="14">RESERVED</td><td>GW1 (GPIO1)</td><td>GW0 (GPIO0)</td><td>0000h</td></tr>
<tr><td>54h**</td><td>GPIO Pin Status</td><td colspan="14">RESERVED</td><td>GI1 (GPIO1)</td><td>GI0 (GPIO0)</td><td>0000h</td></tr>
<tr><td>60h</td><td>Z_DATA Volume</td><td>Mute</td><td colspan="2">RESERVED</td><td>GL4</td><td>GL3</td><td>GL2</td><td>GL1</td><td>GL0</td><td colspan="3">RESERVED</td><td>GR4</td><td>GR3</td><td>GR2</td><td>GR1</td><td>GR0</td><td>8808h</td></tr>
<tr><td>6Ah</td><td>Digital Audio Control</td><td colspan="14">RESERVED</td><td>DO1</td><td>DO0</td><td>0000h</td></tr>
<tr><td>6Ch</td><td>Revision Code</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00xxh</td></tr>
<tr><td>6Eh</td><td>Analog Special</td><td colspan="3">RESERVED</td><td>AC97 ALL MIX</td><td colspan="5">RESERVED</td><td>MUTE FIX DISBLE</td><td>ADCslot 1</td><td>ADCslot 0</td><td>RSVD</td><td>MIC GAIN VALUE</td><td>SPLY OVR EN</td><td>SPLY OVR VAL</td><td>1000h</td></tr>
<tr><td>70h</td><td>72h Enable</td><td>EN15</td><td>EN14</td><td>EN13</td><td>EN12</td><td>EN11</td><td>EN10</td><td>EN9</td><td>EN8</td><td>EN7</td><td>EN6</td><td>EN5</td><td>EN4</td><td>EN3</td><td>EN2</td><td>EN1</td><td>EN0</td><td>0000h</td></tr>
<tr><td>72h</td><td>Analog Current Adjust</td><td colspan="8">RESERVED</td><td>INT APOP</td><td colspan="4">RESERVED</td><td colspan="2">IBIAS<1:0></td><td>RSVD</td><td>0000h</td></tr>
<tr><td>74h*</td><td>GPIO Access</td><td>EAPD</td><td>RSVD</td><td>GPIO1</td><td>GPIO0</td><td>EAPD_ OEN</td><td>RESER VED</td><td>GPIO1_ OEN</td><td>GPIO0_ OEN</td><td colspan="8">RESERVED</td><td>0000h</td></tr>
<tr><td>76h</td><td>78h Enable</td><td>EN15</td><td>EN14</td><td>EN13</td><td>EN12</td><td>EN11</td><td>EN10</td><td>EN9</td><td>EN8</td><td>EN7</td><td>EN6</td><td>EN5</td><td>EN4</td><td>EN3</td><td>EN2</td><td>EN1</td><td>EN0</td><td>0000h</td></tr>
<tr><td>78h</td><td>High Pass Filter Bypass</td><td colspan="15">RSESERVED</td><td>ADC HPF BYP</td><td>0000h</td></tr>
<tr><td>7Ch</td><td>Vendor ID1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>8384h</td></tr>
<tr><td>7Eh</td><td>Vendor ID2 9750</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>7650h</td></tr>
</table>

Note: 1. All registers not shown and those labeled “RESERVED” can be written to but are don’t care upon read back.
2. PC_BEEP default to 0000h, mute off
3. Register 74h is used for GPIO control in revision CA3.
4. **Registers used in revision CC1 and beyond for GPIO. EAPD is still controled by Register 74.

15. DOCUMENT HISTORY

Prior to Rev 5.1 -- History not included in Datasheet

Rev 5.2 (October 2003)

1. Corrected error on page 26: Slot 1 Status Address Port, bit D2 is a SLot Request not reserved as stated in rev 5.1
2. Added CD_GND elaboration note on connection diagram, pin list and pin out diagrams:

   The CD_GND signal is an AC signal return for the two CD input channels. It is normally biased at about 2.5V. The name of the pin in the AC97 specification is CD_GND, and this has confused many designers. It should not have any DC path to GND. Connecting the CD_GND signal directly to ground will change the internal bias of the entire codec, and cause bad distortion. If there is no analog CD input, then this pin can be No-Connect.