DATA SHEET

SUNPLUS

SPHE8281D

DVD Single Chip MPEG A/V Processor

Preliminary

MAY 19, 2005

Version 0.1

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DVD SINGLE CHIP MPEG A/V PROCESSOR

1.GENERAL DESCRIPTION

SPHE8281D A/V decoder is a single-chip integrated DVD A/V decoder. It is designed to maximize system performance with minimum cost. It integrates DVD/CD controller, host processor, A/V decoding hardware, audio quality DAC and a 6-channel multi-format TV-encoder.

SPHE8281D supports DVD and CD physical formats. For logical formats it supports DVD-Video, Super Video CD, Video CD, CD-DA, OKO, and CD-ROM discs.

SPHE8281D performs real-time decoding and playback of ISO/IEC 11172 MPEG1, 13818 MPEG2 sources. Besides MPEG A/V decoding, it supports Dolby Digital and MPEGI/II Layer1/2, PCM, LPCM audio playback.

SPHE8281D also combines all the functions required for a high-performance progressive-scan DVD system. Built-in de-interlacing hardware allows high quality DVD playback. The embedded digital audio decoder is able to support key control and audio sound effects for Karaoke.

Development tools of SPHE8281D include complete compiler tools, programming guide and system application libraries.

Application utilizing the SPHE8281D is presented below:

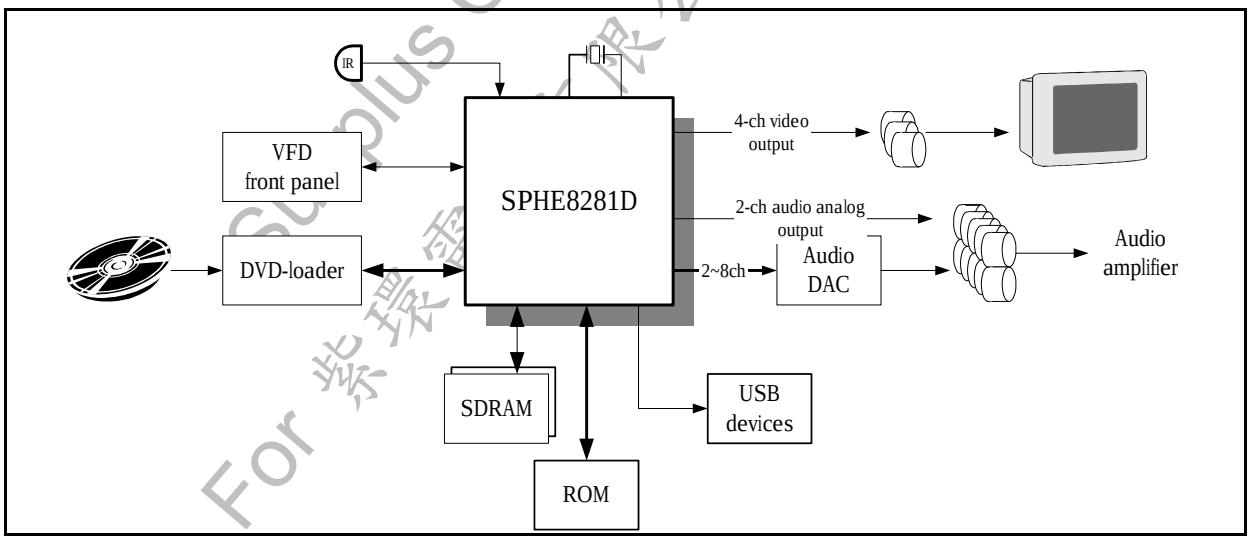

Figure 1-1 Sample SPHE8281D application

2.FEATURE

- Single Chip Integrated DVD Servo and A/V Decoder
- Integrated DVD/CD Servo Controller
  - Support 1x ~ 2x DVD format reading
  - Support 1x ~ 8x CD format reading
- Embedded 32-bit RISC Processor without external host controller
- Embedded Audio Processor supports multiple audio standards
- Embedded 8-bit I/O processor supports programmable interface control
- Embedded TV encoder with multi-channel built-in high-speed video DAC supports various display standards
- Embedded 2-channel 24-bit audio DAC
- Built-in system PLL and audio PLL generate all clock sources required from single 27MHz crystal input
- Support following disc format:
  - DVD Navigation 1.0
  - SVCD (Chaoji VCD)
  - OKO disc
  - VCD 2.0/1.1/1.0
  - CDDA / HDCD
  - CDROM (game, WMA and JPEG disc)
- CSS/CPPM hardware
  - Built-in CSS hardware
  - Built-in CPPM C2_DCBC and C2_D/C2_E function
- Video Decoder
  - Real time MPEG2 MP@ML decoding
  - Real time MPEG4 ASP D1 resolution decoding
  - Real time MPEG1 D1 (720x480x30 /720x576x25) decoding
  - DivX 3.11, 4.0 and 5.x version compatible
  - Hardware accelerated JPEG decoding
  - Advanced decoding and display control
- Sub-picture Decoder
  - Advanced Sub-Picture Decoder for DVD SVCD and OKO
  - Support hardware vertical scaling
- Audio Decoder
  - Flexible Programmable DSP Architecture
  - Support CDDA
  - Support LPCM, PCM, and WMA™ [1] playback
  - Support MPEGI/II layer 1/2 and MPEG 2.5 playback (with optional down-mixing)
  - Support Dolby™ [2] Digital AC3 playback
  - Support Key Shift of 2 channels
  - Support equalization, reverb and special sound field
- SDRAM controller
  - High Performance SDRAM controller
  - Support 16 or 32 bit operation
  - Support up to 2 SDRAM devices
  - Support 16M/64M SDRAM devices
- Video Display
  - De-interlacing of interlaced video source
  - Flexible vertical interpolation
  - Flexible horizontal interpolation with optional CIF filter
  - Powerful cropping and panning effect
  - Support YUV422, 8-bit indexed color format
- OSD
  - Multiple OSD regions with different formats
  - Support 2/4/16 indexed color
  - Support 16/24-bit direct color
- Embedded TV encoder
  - Simultaneous multi-channel output
  - Support 480i/480p/576i/576p format
  - Support CVBS and S-Video output
  - Support Component (YUV / YPbPr) or SCART-RGB output
  - Support WSS and CGMS/A
  - Macrovision™ [3] 7.1.D1 and Macrovision AGC v1.03 analog copy protection
- Interface
  - 27MHz crystal driver
  - 16/32-bit SDRAM interface
  - 8-bit ROM/FLASH/SRAM interface
  - One UART port
  - IR and VFD support
  - 4-channel 12-bit video DAC analog output
  - Simultaneous 8-channel audio DAC output
  - IEC958/SPDIF digital input / output
  - 2-channel 24-bit audio DAC analog output
  - External ADC digital input interface (optional)
  - Optional ATAPI and I2S interface support
  - Optional Parallel Port interface support
- Low power
  - Advanced low power design
  - Selective standby mode
  - Programmable low speed operation
- Technology
  - Advanced CMOS technology
  - 216-pin LQFP package
  - 3v (I/O) and 1.8v (kernel) power supplies
  - 5v I/O tolerance

[1] WMA is a trademark of Microsoft Corporation

[2] Dolby is a trademark of the Dolby Laboratories

[3] Macrovision is a trademark of Macrovision Corporation

■ **Licensing Notice**

- **In order to take care of different royalties, Sunplus SPHE8281D series have different combinations for different royalties. For detail information, please contact with Sunplus Sales.**
- **Supply of the implementation of Dolby, WMA, Macrovision … technologies do not imply of a right or convey a license under any patent, or any Intellectual Property Right of each respective company. Companies plan to use the implementations MUST obtain respective license from respective licensor. Additional royalties may be required and are to be paid by purchaser to each respective licensor**
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- **WMA is a trademark of Microsoft Corporation. "This product includes technology owned by Microsoft Corporation cannot be used or further distributed without a license from Microsoft."**
- **DivX is a trademark of the DivXNetworks Inc. "This product includes technology owned by DivXNetworks Inc. cannot be used or further distributed without a license from DivXNetworks Inc."**
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- **All other trademarks are owned and trademarks of their respective holders and companies, which are used for identification purposed only**

3.BLOCK DIAGRAM

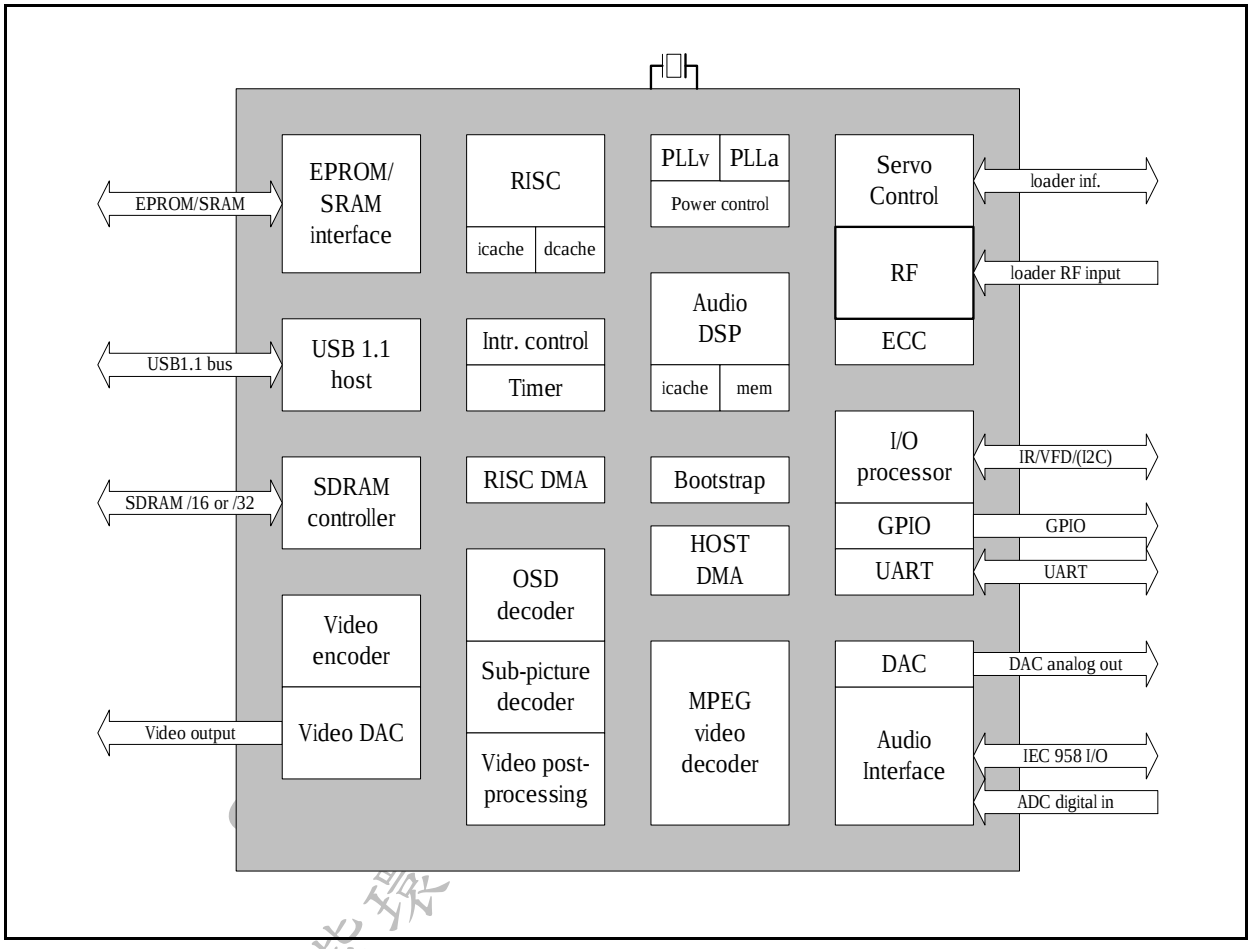

Figure 3-1 SPHE8281D block diagram

4.SIGNAL DESCRIPTION

4.1. Pin Map

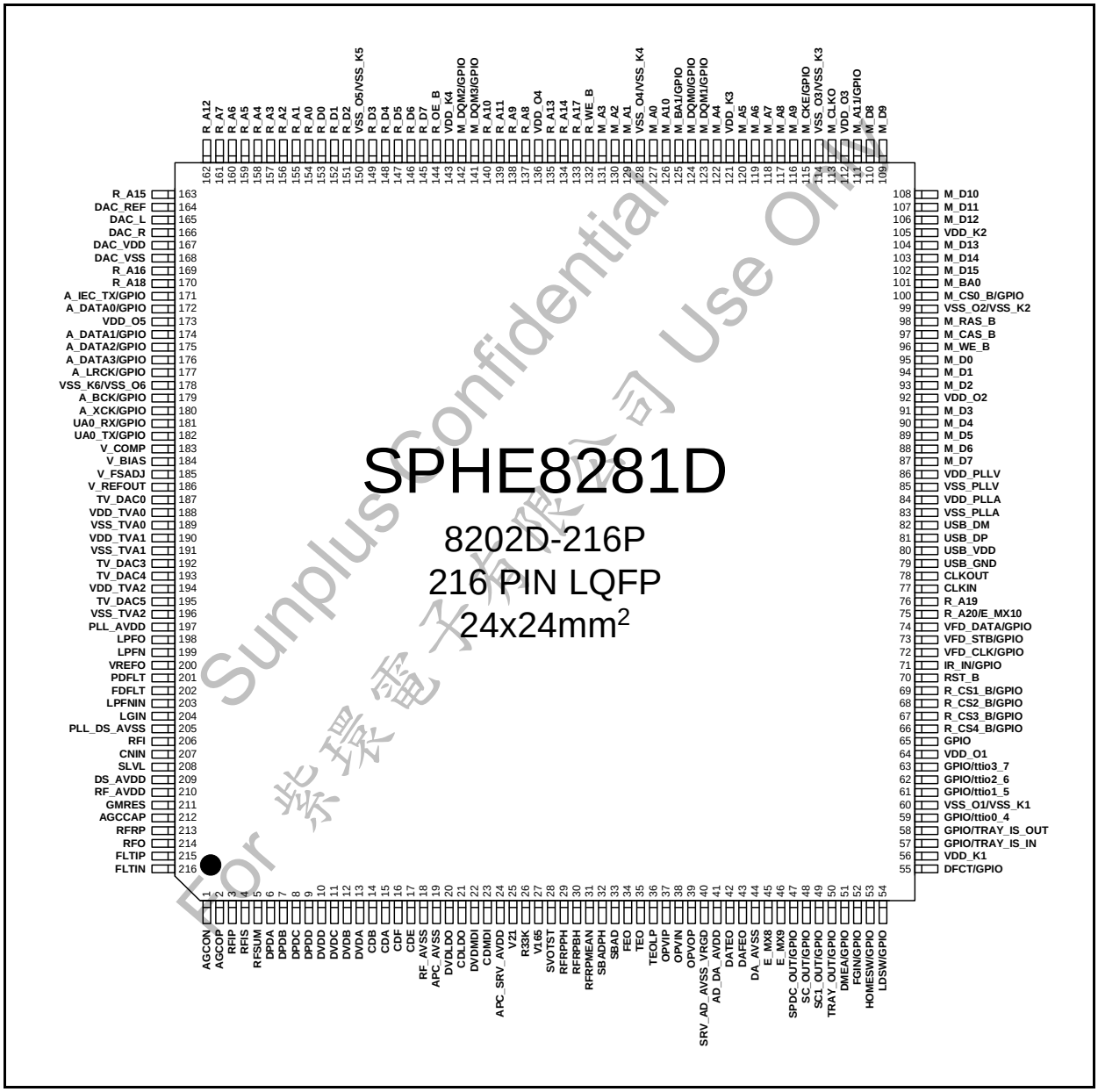

Figure 4-1 SPHE8281D pin

4.2. Group Map

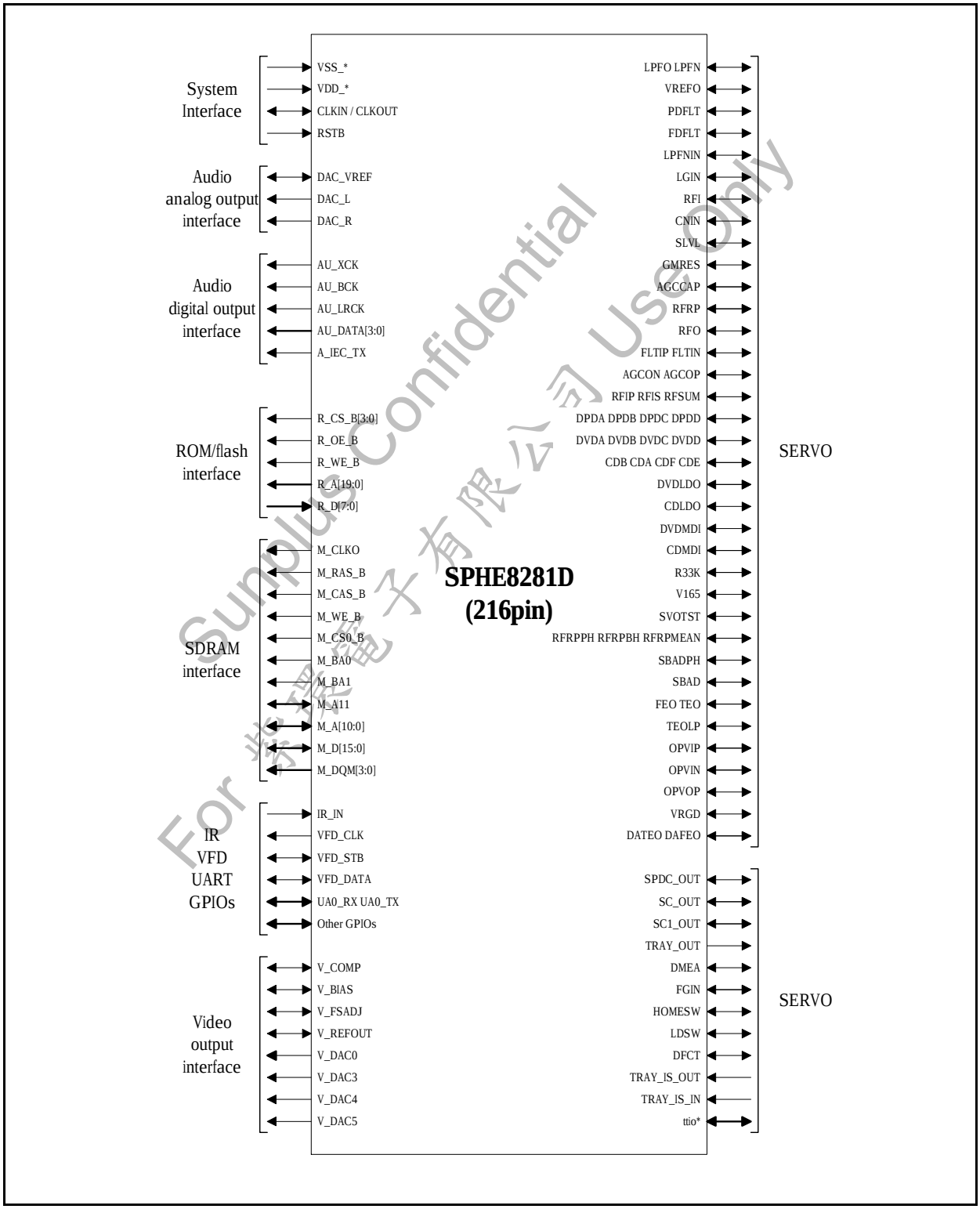

Figure 4-2 SPHE8281D pin groups

4.3. Pin Description

Symbol	Pin No.	I/O	Description
AGCON	1	O	Differential AGC output #N
AGCOP	2	O	Differential AGC output #P
RFIP	3	I	Differential RF signal input #P
RFIS	4	I	Single-ended RF equalizer input.
RFSUM	5	O	RF summing amplified output.
DPDA	6	I	AC coupled RF inputs for the DPD #A, from the main beam photo detector.
DPDB	7	I	AC coupled RF inputs for the DPD #B, from the main beam photo detector.
DPDC	8	I	AC coupled RF inputs for the DPD #C, from the main beam photo detector.
DPDD	9	I	AC coupled RF inputs for the DPD #D, from the main beam photo detector.
DVDD	10	I	DVD RF inputs #A, from the main beam photo detector.
DVDC	11	I	DVD RF inputs #B, from the main beam photo detector.
DVDB	12	I	DVD RF inputs #C, from the main beam photo detector.
DVDA	13	I	DVD RF inputs #D, from the main beam photo detector.
CDB	14	I	CD RF inputs #B, from the main beam photo detector.
CDA	15	I	CD RF inputs #A, from the main beam photo detector.
CDF	16	I	CD tracking error inputs #F, from the sub-beam photo detector.
CDE	17	I	CD tracking error inputs #E, from the sub-beam photo detector.
RF_AVSS	18	S	Servo RF ground
APC_AVSS	19	S	Servo APC ground
DVDLDO	20	O	DVD APC output.
CDLDO	21	O	CD APC output.
DVDMDI	22	I	DVD APC input from monitor photo diode.
CDMDI	23	I	CD APC input from monitor photo diode.
APC_SRV_AVDD	24	S	Servo APC and analog 3.3V power (216pin only)
V21	25	-	Reference DC bias voltage.
R33K	26	-	External reference resistor input.
V165	27	-	Reference DC bias voltage.
SVOTST	28	O	RF peak hold external capacitor
RFRPPH	29	O	RFRP peak hold signal output.
RFRPBH	30	O	RFRP bottom hold signal output.
RFRPMEAN	31	O	RFRP mean signal output.
SBADPH	32	O	Sub-beam adds peak hold signal output.
SBAD	33	O	Sub-beam adds signal output.
FEO	34	O	Focus error signal output.
TEO	35	O	Tracking error signal output.
TEOLP	36	A	
OPVIP	37	I	Op-amp 1 positive input.
OPVIN	38	I	Op-amp 1 negative input.
OPVOP	39	O	Op-amp output.
SRV_AD_VRGD_AVSS	40	S	Servo/ADC analog ground
AD_DA_AVDD	41	S	Servo ADC/DAC 3.3V power
DATEO	42	A	
DAFEO	43	A	

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>I/O</th><th>Description</th></tr>
<tr><td>DA_AVSS</td><td>44</td><td>S</td><td>Servo DAC ground</td></tr>
<tr><td>E_MX8</td><td>45</td><td>I/O</td><td>GPIO [70]
<table>
<tr><th>Priority selection</th><th>Function</th><th>Dir</th></tr>
<tr><td>sft_cfg2[5:4] =2'b01</td><td>UA1_RXD</td><td>I</td></tr>
<tr><td>sft_cfg7[5:4]=2'b11</td><td>656_DATA[0]</td><td>O</td></tr>
<tr><td>sft_cfg1[11:9]=3'b110</td><td>RISC_INT1_11</td><td>I</td></tr>
<tr><td>sft_cfg7[1]= 1'b 0,
sft_cfg0[11]= 1'b 1,
fm_gpio_len[3:0]>8</td><td>FM_GPIOB [12]</td><td>I/O</td></tr>
<tr><td>sft_cfg0[11]= 1'b 0,
fm_gpio_len[3:0]=4'b1100</td><td>FM_GPIOB [29]</td><td>I/O</td></tr>
<tr><td>Sft_cfg8[5]= 1'b 1</td><td>TV_EXT_DATA_Cr[7]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[70](default)</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>E_MX9</td><td>46</td><td>I/O</td><td>GPIO[71]
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[5:4] =2'b01</td><td>UA1_TXD</td><td>O</td></tr>
<tr><td>sft_cfg7[5:4]=2'b11</td><td>656_DATA[1]</td><td>O</td></tr>
<tr><td>sft_cfg1[11:9]=3'b110</td><td>RISC_INT1_12</td><td>I</td></tr>
<tr><td>sft_cfg7[1]= 1'b 0,
sft_cfg0[11]= 1'b 1,
fm_gpio_len[3:0]>8</td><td>FM_GPIOB [13]</td><td>I/O</td></tr>
<tr><td>sft_cfg0[11]= 1'b 0,
fm_gpio_len[3:0]=4'b1100</td><td>FM_GPIOB [30]</td><td>I/O</td></tr>
<tr><td>Sft_cfg8[5]= 1'b 1</td><td>TV_EXT_DATA_Cr[6]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[71](default)</td><td>I/O</td></tr>
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<tr><td>SPDC_OUT/GPIO</td><td>47</td><td>I/O</td><td>Servo SPDC_OUT
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[11:10]=2'b01,2'b10</td><td>AT_RESET_B</td><td>O</td></tr>
<tr><td>sft_cfg4[0]=1'b1</td><td>SPDC_OUT (default)</td><td>I/O</td></tr>
<tr><td>Sft_cfg8[9]=1'b1</td><td>DAC_PDF</td><td>I</td></tr>
<tr><td>sft_cfg8[8]=1'b1</td><td>OTP_TEST_ADDR[0]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[0]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>SC_OUT/GPIO</td><td>48</td><td>I/O</td><td>Servo SC_OUT
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[11:10]=2'b01,2'b10</td><td>AT_DIOR_B</td><td>O</td></tr>
<tr><td>sft_cfg4[1]=1'b1</td><td>SC_OUT (default)</td><td>I/O</td></tr>
<tr><td>Sft_cfg8[9]=1'b1</td><td>DAC_PDE</td><td>I</td></tr>
<tr><td>sft_cfg8[8]=1'b1</td><td>OTP_TEST_ADDR[1]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[1]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>SC1_OUT/GPIO</td><td>49</td><td>I/O</td><td>Servo SC1_OUT
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[11:10]=2'b01,2'b10</td><td>AT_DIOW_B</td><td>O</td></tr>
<tr><td>sft_cfg4[2]=1'b1</td><td>SC1_OUT (default)</td><td>I/O</td></tr>
<tr><td>Sft_cfg8[9]=1'b1</td><td>DAC_PDD</td><td>I</td></tr>
<tr><td>sft_cfg8[8]=1'b1</td><td>OTP_TEST_ADDR[2]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[2]</td><td>I/O</td></tr>
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<table>
<tr><th>Symbol</th><th>Pin No.</th><th>I/O</th><th>Description</th></tr>
<tr><td>TRAY_OUT/GPIO</td><td>50</td><td>I/O</td><td>Servo TRAY_OUT
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[11:10]=2’b01,2’b10</td><td>AT_IORDY</td><td>I</td></tr>
<tr><td>sft_cfg4[3]=1’b1</td><td>TRAY_OUT (default)</td><td>I/O</td></tr>
<tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_PDC</td><td>I</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>OTP_TEST_ADDR[3]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[3]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>DMEA_OUT/GPIO</td><td>51</td><td>I/O</td><td>Servo DMEA
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[11:10]=2’b01,2’b10</td><td>AT_DMACK</td><td>O</td></tr>
<tr><td>sft_cfg4[4]=1’b1</td><td>DMEA_OUT (default)</td><td>O</td></tr>
<tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_PDB</td><td>I</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>OTP_TEST_ADDR[4]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[4]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>FGIN/GPIO</td><td>52</td><td>I/O</td><td>Servo FGIN
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<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[11:10]=2’b01,2’b10</td><td>AT_DMARQ</td><td>I</td></tr>
<tr><td>sft_cfg4[5]=1’b1</td><td>FGIN (default)</td><td>I</td></tr>
<tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_PDA</td><td>I</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>OTP_TEST_PGM</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[5]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>HOMESW/GPIO</td><td>53</td><td>IO</td><td>Servo HOMESW
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[3:2]=2’b10</td><td>UA0_RXD</td><td>I</td></tr>
<tr><td>sft_cfg1[8:6]=3’b010</td><td>R_CSALL_B</td><td>O</td></tr>
<tr><td>sft_cfg7[7:6]=2’b11</td><td>PCMCIA_IOW_B</td><td>O</td></tr>
<tr><td>Sft_cfg8[1]=1’b1</td><td>DSP_FL0</td><td>O</td></tr>
<tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_DATA_F[9]</td><td>I</td></tr>
<tr><td>sft_cfg9[14:13]=2’b01</td><td>EXT_CLK48</td><td>I</td></tr>
<tr><td>sft_cfg6[4]=1’b1</td><td>DELAY_CHAIN1</td><td>O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>OTP_TEST_DATA</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[6] (default)</td><td>I/O</td></tr>
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<tr><td>LDSW/GPIO</td><td>54</td><td>IO</td><td>Servo LDSW
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<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[3:2]=2’b10</td><td>UA0_TXD</td><td>O</td></tr>
<tr><td>sft_cfg2[5:4]=2’b10</td><td>UA1_RXD</td><td>I</td></tr>
<tr><td>sft_cfg7[7:6]=2’b11</td><td>PCMCIA_IOR_B</td><td>O</td></tr>
<tr><td>Sft_cfg8[2]=1’b1</td><td>DSP_FL1</td><td>O</td></tr>
<tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_DATA_F[8]</td><td>I</td></tr>
<tr><td>sft_cfg7[15:14]=2’b11</td><td>CLK27_OUT</td><td>O</td></tr>
<tr><td>sft_cfg9[14:13]=2’b10</td><td>EXT_CLK48</td><td>I</td></tr>
<tr><td>sft_cfg6[4]=1’b1</td><td>DELAY_CHAIN2</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[7] (default)</td><td>I/O</td></tr>
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<table>
<tr><th>Symbol</th><th>Pin No.</th><th>I/O</th><th>Description</th></tr>
<tr><td>DFCT/GPIO</td><td>55</td><td>IO</td><td>Servo DFCT
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[11:10]=2’b01,2’b10</td><td>AT_INTRQ</td><td>I</td></tr>
<tr><td>sft_cfg4[6]=1’b1</td><td>DFCT (default)</td><td>O</td></tr>
<tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_DATA_F[7]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[8]</td><td>I/O</td></tr>
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<tr><td>VDD_K1</td><td>56</td><td>S</td><td>Kernel logic power supply #1</td></tr>
<tr><td>GPIO/TRAY_IS_IN</td><td>57</td><td>IO</td><td>GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[11:10]=2’b01,2’b10</td><td>AT_ADR[1]</td><td>O</td></tr>
<tr><td>Sft_cfg8[3]=1’b1</td><td>DSP_FL2</td><td>O</td></tr>
<tr><td>fm_gpio_len[3:0] > 0</td><td>FM_GPIOB[0]</td><td>I/O</td></tr>
<tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_DATA_F[6]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[9] (default)</td><td>I/O</td></tr>
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<tr><td>GPIO/TRAY_IS_OUT</td><td>58</td><td>IO</td><td>GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[11:10]=2’b01,2’b10</td><td>AT_ADR[2]</td><td>O</td></tr>
<tr><td>Sft_cfg8[4]=1’b1</td><td>DSP_FLAG_OUT</td><td>O</td></tr>
<tr><td>fm_gpio_len[3:0] > 0</td><td>FM_GPIOB[1]</td><td>I/O</td></tr>
<tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_DATA_F[5]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[10] (default)</td><td>I/O</td></tr>
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<tr><td>GPIO/ttio0_4</td><td>59</td><td>IO</td><td>GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[11:10]=2’b01,2’b10</td><td>AT_ADR[0]</td><td>O</td></tr>
<tr><td>sft_cfg4[9]=1’b1</td><td>ttio4/ttio0</td><td>I/O</td></tr>
<tr><td>Sft_cfg1[11:9]=3’b001</td><td>RISC_INT1_11</td><td>I</td></tr>
<tr><td>Sft_cfg3[11:10]=2’b01</td><td>ADC_BCK, digital audio input interface bit clock</td><td>I/O</td></tr>
<tr><td>fm_gpio_len[3:0] > 0</td><td>FM_GPIOB[2]</td><td>I/O</td></tr>
<tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_DATA_F[4]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[11] (default)</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>VSS_O1/ VSS_K1</td><td>60</td><td>S</td><td>Kernel logic / I/O power shared ground supply #1</td></tr>
<tr><td>GPIO/ttio1_5</td><td>61</td><td>IO</td><td>GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[11:10]=2’b01,2’b10</td><td>AT_CS1</td><td>O</td></tr>
<tr><td>sft_cfg4[9]=1’b1</td><td>Ttio5/ttio1</td><td>I/O</td></tr>
<tr><td>sft_cfg4[15:13]=3’b001</td><td>HSYNC_PC</td><td>O</td></tr>
<tr><td>Sft_cfg1[11:9]=3’b001</td><td>RISC_INT1_12</td><td>I</td></tr>
<tr><td>Sft_cfg3[11:10]=2’b01</td><td>ADC_LRCK, digital audio input interface L/R strobe</td><td>I/O</td></tr>
<tr><td>fm_gpio_len[3:0] > 0</td><td>FM_GPIOB[3]</td><td>I/O</td></tr>
<tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_DATA_F[3]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[12] (default)</td><td>I/O</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>I/O</th><th>Description</th></tr>
<tr><td>GPIO/ttio2_6</td><td>62</td><td>IO</td><td>GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[11:10]=2’b01,2’b10</td><td>AT_CS0</td><td>O</td></tr>
<tr><td>sft_cfg4[9]=1’b1</td><td>Ttio6/ttio2</td><td>I/O</td></tr>
<tr><td>sft_cfg4[15:13]=3’b001</td><td>VSYNC_PC</td><td>O</td></tr>
<tr><td>sft_cfg3[15:14]=2’b01</td><td>ISA_IOCHRDY</td><td>I</td></tr>
<tr><td>Sft_cfg1[11:9]=3’b001</td><td>RISC_INT1_13</td><td>I</td></tr>
<tr><td>Sft_cfg3[11:10]=2’b01</td><td>ADC_DATA, digital audio input interface data</td><td>I</td></tr>
<tr><td>fm_gpio_len[3:0] > 1</td><td>FM_GPIOB[4]</td><td>I/O</td></tr>
<tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_DATA_F[2]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[13] (default)</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>GPIO/ttio3_7</td><td>63</td><td>IO</td><td>GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg4[9]=1’b1</td><td>Ttio7/ttio3</td><td>I/O</td></tr>
<tr><td>sft_cfg2[9:8]=2’b11</td><td>PCMCIA_WAIT_B</td><td>I</td></tr>
<tr><td>sft_cfg7[11:8]=4’b0001</td><td>EXT_CLK27</td><td>I</td></tr>
<tr><td>Sft_cfg1[11:9]=3’b001</td><td>RISC_INT1_14</td><td>I</td></tr>
<tr><td>fm_gpio_len[3:0] > 2</td><td>FM_GPIOB[5]</td><td>I/O</td></tr>
<tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_DATA_F[1]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[14] (default)</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>VDD_O1</td><td>64</td><td>S</td><td>I/O power supply #1</td></tr>
<tr><td>GPIO</td><td>65</td><td>IO</td><td>GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[5:4]=2’b10</td><td>UA1_TXD</td><td>O</td></tr>
<tr><td>sft_cfg1[8:6]=3’b001</td><td>R_CSALL_B</td><td>O</td></tr>
<tr><td>sysclk_sel[4]</td><td>EXT_SYSCLK</td><td>I</td></tr>
<tr><td>sft_cfg7[11:8]=4’b0010</td><td>EXT_CLK27</td><td>I</td></tr>
<tr><td>fm_gpio_len[3:0] > 3</td><td>FM_GPIOB[6]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_F[0]</td><td>I</td></tr>
<tr><td>sft_cfg7[13:12]=2’b11</td><td>CLK54_OUT</td><td>O</td></tr>
<tr><td>sft_cfg9[14:13]=2’b11</td><td>EXT_CLK48</td><td>I</td></tr>
<tr><td>sft_cfg6[4]=1’b1</td><td>DELAY_CHAIN3</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[15] (default)</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>R_CS4_B/GPIO</td><td>66</td><td>IO</td><td>ROM / SRAM / flash chip select #4 or GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg1[3]=1’b1</td><td>R_CS4_B (default)</td><td>O</td></tr>
<tr><td>sft_cfg1[7]=1’b1 & fm_gpio_len[3:0] = 10,11,12</td><td>FM_GPIOB[20]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_E[9]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[16]</td><td>I/O</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>I/O</th><th>Description</th></tr>
<tr><td>R_CS3_B/GPIO</td><td>67</td><td>IO</td><td>ROM / SRAM / flash chip select #3 or GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg1[2]=1’b1</td><td>R_CS3_B (default)</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_E[8]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[17]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>R_CS2_B/GPIO</td><td>68</td><td>IO</td><td>ROM / SRAM / flash chip select #2 or GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg1[1]=1’b1</td><td>R_CS2_B (default)</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_E[7]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[18]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>R_CS1_B/GPIO</td><td>69</td><td>IO</td><td>ROM / SRAM / flash chip select #1 or GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg1[0]=1’b1</td><td>R_CS1_B (default)</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_E[6]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[19]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>RST_B</td><td>70</td><td>I</td><td>System reset (active low reset)</td></tr>
<tr><td>IR_IN/GPIO</td><td>71</td><td>IO</td><td>GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg8[0]=1’b1</td><td>IR_IN,GPIO[20]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[20] (default)</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>VFD_CLK/GPIO</td><td>72</td><td>IO</td><td>GPIO[21] for VFD_CLK</td></tr>
<tr><td>VFD_STB/GPIO</td><td>73</td><td>IO</td><td>GPIO[22] for VFD_STB
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_E[5]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[22] (default)</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>VFD_DATA/GPIO</td><td>74</td><td>IO</td><td>GPIO[23] for VFD_DATA
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_E[4]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[23] (default)</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>R_A20</td><td>75</td><td>IO</td><td>ROM / SRAM / flash address bus bit [20] (216pin package)</td></tr>
<tr><td>R_A19 (E_MX11)</td><td>76</td><td>IO</td><td>ROM / SRAM / flash address bus bit [19]</td></tr>
<tr><td>CLKIN</td><td>77</td><td>I</td><td>Clock input / crystal in (XTALI)</td></tr>
<tr><td>CLKOUT</td><td>78</td><td>O</td><td>Clock output / crystal out (XTALO)</td></tr>
<tr><td>RESERVED_N</td><td>79</td><td>A</td><td>Reserved</td></tr>
<tr><td>RESERVED_P</td><td>80</td><td>A</td><td>Reserved</td></tr>
<tr><td>RESERVED</td><td>81</td><td>A</td><td>Reserved</td></tr>
<tr><td>RESERVED</td><td>82</td><td>A</td><td>Reserved</td></tr>
<tr><td>VSS_PLLA</td><td>83</td><td>S</td><td>Ground pin for audio PLL</td></tr>
<tr><td>VDD_PLLA</td><td>84</td><td>S</td><td>3.3V power supply pin for audio PLL</td></tr>
<tr><td>VSS_PLLV</td><td>85</td><td>S</td><td>Ground pin for system PLL and audio PLL</td></tr>
<tr><td>VDD_PLLV</td><td>86</td><td>S</td><td>1.8V power supply pin for system PLL</td></tr>
<tr><td>M_DD[7]</td><td>87</td><td>IO</td><td>SDRAM data bus [7]</td></tr>
<tr><td>M_DD[6]</td><td>88</td><td>IO</td><td>SDRAM data bus [6]</td></tr>
<tr><td>M_DD[5]</td><td>89</td><td>IO</td><td>SDRAM data bus [5]</td></tr>
<tr><td>M_DD[4]</td><td>90</td><td>IO</td><td>SDRAM data bus [4]</td></tr>
</table>

Symbol	Pin No.	I/O	Description
M_DD[3]	91	IO	SDRAM data bus [3]
VDD_O2	92	S	I/O power supply #2
M_DD[2]	93	IO	SDRAM data bus [2]
M_DD[1]	94	IO	SDRAM data bus [1]
M_DD[0]	95	IO	SDRAM data bus [0]
M_WE_B	96	IO	SDRAM write enable / row precharge
M_CAS_B	97	IO	SDRAM column address strobe (CASB)
M_RAS_B	98	IO	SDRAM row address strobe (RASB)
VSS_O2/ VSS_K2	99	S	Kernel logic / I/O power shared ground supply #2
M_CS0_B/GPIO	100	IO	SDRAM chip select 0, or GPIO[24] Priority selection / Function / dir sft_cfg0[0]=1'b1 / SDRAM chip select (default) / O sft_cfg8[9]=1'b1 / DAC_DATA_D[2] / I (other) / GPIO[24] / I/O
M_BA0	101	IO	SDRAM bank select address [0]
M_DD[15]	102	IO	SDRAM data bus [15]
M_DD[14]	103	IO	SDRAM data bus [14]
M_DD[13]	104	IO	SDRAM data bus [13]
VDD_K2	105	S	Kernel logic power supply #2
M_DD[12]	106	IO	SDRAM data bus [12]
M_DD[11]	107	IO	SDRAM data bus [11]
M_DD[10]	108	IO	SDRAM data bus [10]
M_DD[9]	109	IO	SDRAM data bus [9]
M_DD[8]	110	IO	SDRAM data bus [8]
M_A[11]/ GPIO	111	IO	SDRAM address bus [11] or GPIO[25] Priority selection / Function / dir sft_cfg1[4]=1'b1 / SDRAM address bus M_A[11] (default) / O sft_cfg8[9]=1'b1 / DAC_DATA_C[2] / I (other) / GPIO[25] / I/O
VDD_O3	112	S	I/O power supply #3
M_CLKO	113	O	SDRAM clock output
VSS_O3/ VSS_K3	114	S	Kernel logic / I/O power shared ground supply #3
M_CKE/GPIO	115	IO	SDRAM clock enable, or GPIO[26] Priority selection / Function / dir sft_cfg0[1]=1'b1 / DRAM clock enable (default) / O sft_cfg8[9]=1'b1 / DAC_DATA_C[1] / I (other) / GPIO[26] / I/O
M_A[9]	116	IO	SDRAM address bus [9]
M_A[8]	117	IO	SDRAM address bus [8]
M_A[7]	118	IO	SDRAM address bus [7]
M_A[6]	119	I/O	SDRAM address bus [6]
M_A[5]	120	I/O	SDRAM address bus [5]

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>I/O</th><th>Description</th></tr>
<tr><td>VDD_K3</td><td>121</td><td>S</td><td>Kernel logic power supply #3</td></tr>
<tr><td>M_A[4]</td><td>122</td><td>I/O</td><td>SDRAM address bus [4]</td></tr>
<tr><td>M_DQM1/GPIO</td><td>123</td><td>I/O</td><td>SDRAM data input/output mask for M_DD[15:8], or GPIOA[27]</td></tr>
<tr><td>M_DQM0/GPIO</td><td>124</td><td>I/O</td><td>SDRAM data input/output mask for M_DD[7:0] or GPIOA[28]
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg0[2]=1’b1</td><td>SDRAM data input/output mask for M_DD[7:0] (default)</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_R[5]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_B[3]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[28]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>M_BA1/GPIO</td><td>125</td><td>I/O</td><td>SDRAM bank select address [1] or GPIOA[29]
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg0[6]=1’b1</td><td>SDRAM bank select address [1] (default)</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_R[6]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_B[2]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[29]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>M_A[10]</td><td>126</td><td>O</td><td>SDRAM address bus [10]</td></tr>
<tr><td>M_A[0]</td><td>127</td><td>O</td><td>SDRAM address bus [0]</td></tr>
<tr><td>VSS_O4/ VSS_K4</td><td>128</td><td>S</td><td>Kernel logic / I/O power shared ground supply #4</td></tr>
<tr><td>M_A[1]</td><td>129</td><td>O</td><td>SDRAM address bus [1]</td></tr>
<tr><td>M_A[2]</td><td>130</td><td>O</td><td>SDRAM address bus [2]</td></tr>
<tr><td>M_A[3]</td><td>131</td><td>O</td><td>SDRAM address bus [3]</td></tr>
<tr><td>R_WE_B</td><td>132</td><td>I/O</td><td>ROM / SRAM / flash write strobe</td></tr>
<tr><td>R_A17</td><td>133</td><td>I/O</td><td>ROM / SRAM / flash address bus bit [17]</td></tr>
<tr><td>R_A14</td><td>134</td><td>I/O</td><td>ROM / SRAM / flash address bus bit [14]</td></tr>
<tr><td>R_A13</td><td>135</td><td>I/O</td><td>ROM / SRAM / flash address bus bit [13]</td></tr>
<tr><td>VDD_O4</td><td>136</td><td>S</td><td>I/O power supply #4</td></tr>
<tr><td>R_A8</td><td>137</td><td>O</td><td>ROM / SRAM / flash address bus bit [8]</td></tr>
<tr><td>R_A9</td><td>138</td><td>O</td><td>ROM / SRAM / flash address bus bit [9]</td></tr>
<tr><td>R_A11</td><td>139</td><td>I/O</td><td>ROM / SRAM / flash address bus bit [11]</td></tr>
<tr><td>R_A10</td><td>140</td><td>O</td><td>ROM / SRAM / flash address bus bit [10]</td></tr>
</table>

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>I/O</th><th>Description</th></tr>
<tr><td>M_DQM3/GPIO</td><td>141</td><td>I/O</td><td>SDRAM data input/output mask for M_DD[31:24] , or GPIO[38]
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg0[5]=1’b1</td><td>SDRAM data input/output mask for M_DD[31:24] (default)</td><td>O</td></tr>
<tr><td>sft_cfg2[3:2]=2’b11</td><td>UA0_RXD</td><td>I</td></tr>
<tr><td>sft_cfg1[8:6]=3’b011</td><td>R_CSALL_B</td><td>O</td></tr>
<tr><td>sft_cfg3[13:12]=2’b10</td><td>TV_HSYNC</td><td>I/O</td></tr>
<tr><td>sft_cfg4[15:13]=3’b010</td><td>TV_HSYNC_PC</td><td>O</td></tr>
<tr><td>sft_cfg7[7:6]=2’b01</td><td>PCMCIA_IOW_B</td><td>O</td></tr>
<tr><td>sft_cfg0[13:12]=2’b01</td><td>TV_LCD_G[2]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]= 1’b0,
sft_cfg0[11]= 1’b 0,
fm_gpio_len[3:0]>9</td><td>FM_GPIOB[19]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_L[5]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_OPA[1]</td><td>I</td></tr>
<tr><td>sft_cfg8[10]=1’b1</td><td>OGT_BIST_FAIL</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[38]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>M_DQM2/GPIO</td><td>142</td><td>I/O</td><td>SDRAM data input/output mask for M_DD[23:16] , or GPIO[39]
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg0[4]=1’b1</td><td>SDRAM data input/output mask for M_DD[23:16] (default)</td><td>O</td></tr>
<tr><td>sft_cfg2[3:2]=2’b11</td><td>UA0_TXD</td><td>O</td></tr>
<tr><td>sft_cfg3[13:12]=2’b10</td><td>TV_VSYNC</td><td>I/O</td></tr>
<tr><td>sft_cfg4[15:13]=3’b010</td><td>TV_VSYNC_PC</td><td>O</td></tr>
<tr><td>sft_cfg7[7:6]=2’b01</td><td>PCMCIA_IOR_B</td><td>O</td></tr>
<tr><td>sft_cfg0[13:12]=2’b01</td><td>TV_LCD_G[3]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]= 1’b 0,
sft_cfg0[11]= 1’b 0,
fm_gpio_len[3:0]>9</td><td>FM_GPIOB[18]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_L[6]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_OPA[2]</td><td>I</td></tr>
<tr><td>sft_cfg8[10]=1’b1</td><td>BUF_CTRL_BIST_FAIL</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[39]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>VDD_K4</td><td>143</td><td>S</td><td>Kernel logic power supply #4</td></tr>
<tr><td>R_OE_B</td><td>144</td><td>I/O</td><td>ROM / SRAM / flash output enable</td></tr>
<tr><td>R_D7</td><td>145</td><td>I/O</td><td>ROM / SRAM / flash data bus bit [7]</td></tr>
<tr><td>R_D6</td><td>146</td><td>I/O</td><td>ROM / SRAM / flash data bus bit [6]</td></tr>
<tr><td>R_D5</td><td>147</td><td>I/O</td><td>ROM / SRAM / flash data bus bit [5]</td></tr>
<tr><td>R_D4</td><td>148</td><td>I/O</td><td>ROM / SRAM / flash data bus bit [4]</td></tr>
<tr><td>R_D3</td><td>149</td><td>I/O</td><td>ROM / SRAM / flash data bus bit [3]</td></tr>
<tr><td>VSS_O5/ VSS_K5</td><td>150</td><td>S</td><td>Kernel logic / I/O power shared ground supply #5</td></tr>
</table>

Symbol	Pin No.	I/O	Description
R_D2	151	I/O	ROM / SRAM / flash data bus bit [2]
R_D1	152	I/O	ROM / SRAM / flash data bus bit [1]
R_D0	153	I/O	ROM / SRAM / flash data bus bit [0]
R_A0	154	O	ROM / SRAM / flash address bus bit [0]
R_A1	155	O	ROM / SRAM / flash address bus bit [1]
R_A2	156	O	ROM / SRAM / flash address bus bit [2]
R_A3	157	O	ROM / SRAM / flash address bus bit [3]
R_A4	158	O	ROM / SRAM / flash address bus bit [4]
R_A5	159	O	ROM / SRAM / flash address bus bit [5]
R_A6	160	O	ROM / SRAM / flash address bus bit [6]
R_A7	161	O	ROM / SRAM / flash address bus bit [7]
R_A12	162	I/O	ROM / SRAM / flash address bus bit [12]
R_A15	163	I/O	ROM / SRAM / flash address bus bit [15]
DAC_VREF	164	A	Audio DAC reference voltage, connect a 0.1uF to ground
DAC_L	165	A	Audio DAC left-channel output
DAC_R	166	A	Audio DAC right-channel output
DAC_VDD	167	S	3.3v power supply for on-chip audio DAC
DAC_VSS	168	S	Ground pin for on-chip audio DAC
R_A16	169	I/O	ROM / SRAM / flash address bus bit [16]
R_A18	170	I/O	ROM / SRAM / flash address bus bit [18]
A_IEC_TX/GPIO	171	I/O	IEC-958 transmit data Priority selection / Function / Dir sft_cfg3[8]=1'b1 / A_IEC_TX (default) / O sft_cfg8[8]=1'b1 / ADC_MONO_C[0] / I sft_cfg8[9]=1'b1 / DAC_OPF[0] / I (other) / GPIO[52] / I/O
A_DATA[0] / GPIO	172	I/O	Serial audio data output for channel 1/0 or GPIO Priority selection / Function / Dir sft_cfg3[1]=1'b1 / A_DATA[0] (default) / O sft_cfg8[8]=1'b1 / ADC_MONO_C[1] / I sft_cfg8[9]=1'b1 / DAC_OPF[1] / I (other) / GPIO[53] / I/O
VDD_O5	173	S	I/O power supply #5
A_DATA[1] / GPIO	174	I/O	Serial audio data output for channel 3/2 or GPIO Priority selection / Function / Dir sft_cfg3[2]=1'b1 / A_DATA[1] (default) / O sft_cfg8[8]=1'b1 / ADC_MONO_C[2] / I sft_cfg8[9]=1'b1 / DAC_OPF[2] / I (other) / GPIO[54] / I/O

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>I/O</th><th>Description</th></tr>
<tr><td>A_DATA[2] / GPIO</td><td>175</td><td>I/O</td><td>Serial audio data output for channel 5/4 or GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>Dir</th></tr>
<tr><td>sft_cfg3[3]=1’b1</td><td>A_DATA[2] (default)</td><td>O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_PWAD</td><td>I</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_PDALL</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[55]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>A_DATA[3] / GPIO</td><td>176</td><td>I/O</td><td>Serial audio data output for channel 7/6 or GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>Dir</th></tr>
<tr><td>sft_cfg3[4]=1’b1</td><td>A_DATA[3] (default)</td><td>O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_SPGA</td><td>I</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_TEST</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[56]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>A_LRCK/GPIO</td><td>177</td><td>I/O</td><td>PCM data output L/R strobe
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg3[6]=1’b1</td><td>A_LRCK (default)</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_MODE1</td><td>I</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_UD</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[57]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>VSS_O6/ VSS_K6</td><td>178</td><td>S</td><td>Kernel logic / I/O power shared ground supply #6</td></tr>
<tr><td>A_BCK/GPIO</td><td>179</td><td>I/O</td><td>PCM bit clock
<table>
<tr><th>Priority selection</th><th>Function</th><th>Dir</th></tr>
<tr><td>sft_cfg3[0]=1’b1</td><td>A_BCK (default)</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_MODE1_1</td><td>I</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_BGPD</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[58]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>A_XCK/GPIO</td><td>180</td><td>I/O</td><td>Audio over-sampling clock
<table>
<tr><th>Priority selection</th><th>Function</th><th>Dir</th></tr>
<tr><td>sft_cfg3[9]=1’b1</td><td>A_XCK (default)</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_MODE2</td><td>I</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_CLK</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[59]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>UA0_RX/GPIO</td><td>181</td><td>I/O</td><td>UART #0 data receive or GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>Dir</th></tr>
<tr><td>sft_cfg2[3:2] =2’b01</td><td>UART0_RX (default)</td><td>I</td></tr>
<tr><td>sft_cfg3[13:12]=2’b01</td><td>TV_HSYNC</td><td>I/O</td></tr>
<tr><td>sft_cfg4[15:13]=3’b011</td><td>HSYNC_PC</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[60]</td><td>I/O</td></tr>
</table></td></tr>
</table>

Symbol	Pin No.	I/O	Description
UA0_TX/GPIO	182	I/O	UART #0 data transmit or GPIO Priority selection / Function / Dir sft_cfg2[3:2] =2'b01 / UART0_TX (default) / O sft_cfg3[13:12]=2'b01 / TV_VSYNC / I/O sft_cfg4[15:13]=3'b011 / VSYNC_PC / O (other) / GPIO[61] / I/O
V_COMP	183	A	(VDAC CBU) Compensation pin. Connect a 0.1pF ceramic capacitor to bypass this pin to VSSA. The lead length must be kept as short as possible to avoid noise.
V_BIAS	184		(VDAC CBL) Bias voltage. Connect a 0.1pF ceramic capacitor to bypass this pin to VSSA. The lead length must be kept as short as possible to avoid noise.
V_FSADJ	185	A	Full-Scale adjustment control pin. The full-scale current of D/A converters can be adjusted by connecting a resistor (R_{SET}) between this pin and ground.
V_REFOUT	186	A	(VDAC VREF/bandgap output) Voltage reference output. It generates typical 1.2V voltage reference and may be used to drive V_REFIN pin directly.
V_DAC[0]	187	A	Video DAC output #0. This is a high-impedance current source output. These outputs can drive a 37.5 Ω load directly.
VDD_TVA0	188	S	TV DAC power supply #0
VSS_TVA0	189	S	TV DAC ground pin #0
VDD_TVA1	190	S	TV DAC power supply #1
VSS_TVA1	191	S	TV DAC ground pin #1
V_DAC[3]	192	A	Video DAC output #3. This is a high-impedance current source output. These outputs can drive a 37.5 Ω load directly.
V_DAC[4]	193	A	Video DAC output #4. This is a high-impedance current source output. These outputs can drive a 37.5 Ω load directly.
VDD_TVA2	194	S	TV DAC power supply #2
V_DAC[5]	195	A	Video DAC output #5. This is a high-impedance current source output. These outputs can drive a 37.5 Ω load directly.
VSS_TVA2	196	S	TV DAC ground pin #2
PLL_AVDD	197	S	Servo PLL 3.3V power
LPFO	198	A	NC pin
LPFN	199	A	NC pin
VREFO	200	A	
PDFLT	201	A	
FDFLT	202	A	
LPFNIN	203	A	
LGIN	204	A	
PLL_DS_AVSS	205	S	Servo PLL/Data-slicer ground
RFI	206	A	
CNIN	207	A	
SLVL	208	A	
DS_AVDD	209	S	Servo Data slicer 3.3V power
RF_AVDD	210	S	Servo RF 3.3V power
GMRES	211	A	External reference resistor input.
AGCCAP	212	A	External AGC capacitor connected to ground.

Symbol	Pin No.	I/O	Description
RFRP	213	O	RFRP signal output.
RFO	214	O	RF signal output.
FLTIP	215	I	Differential RF equalizer input #P
FLTIN	216	I	Differential RF equalizer input #N

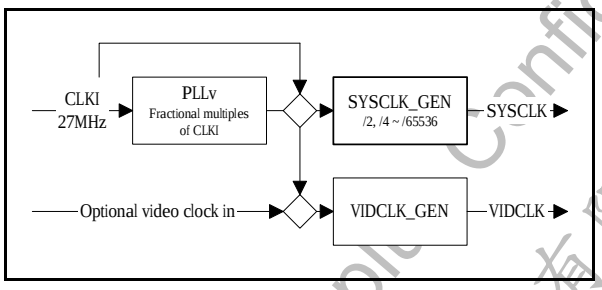
Note: Please reference SPHE802D servo datasheet for servo related information.

5.FUNCTIONAL DESCRIPTIONS

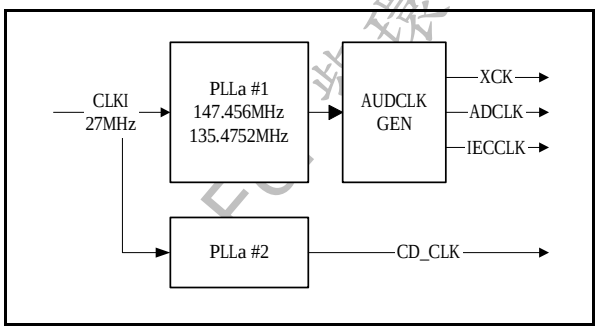
SPHE8281D is a highly integrated system-on-chip DVD player SoC design. It includes DVD/CD front-end RF, read-channel, data decoder, servo controller, host controller, MPEG1/2 video decoder, programmable audio decoder, programmable peripheral controller, audio DAC and multi-format TV-encoder on a single chip.

5.1. PLL and ClockGen

SPHE8281D contains multiple PLLs to generate system clock and audio reference clocks. All the PLLs reference a single external 27MHz clock or crystal to generate the required clocks. System clock is then derived from division of the system PLL output.



PLLa supports two center frequencies (for both 48kHz family and 44.1kHz family) and generates required audio clocks from the audio system clock.



5.2. Power Control

SPHE8281D provides various levels of power-control mechanism in order to achieve minimum power consumption.

- Automatic power-save:
  Most hardware modules are automatically power-saved when not operating.
- Module-level stop-operation:
  SPHE8281D provides a function to turn off specific module from operating. Without explicit wake-up, the hardware module will remain static and consume little power.
- System-level doze:
  For maximum power-saving, firmware could fine-tune system performance according to system task.

5.3. Embedded 32-bit RISC Controller

SPHE8281D includes a powerful 32-bit RISC processor as the host controller. This host controller is utilized to manage servo control, decoding tasks as well as UI tasks. It can access to all the memory and devices, cooperate between processor systems. Audio decoder and I/O processor handshake with RISC processor through the mailbox registers.

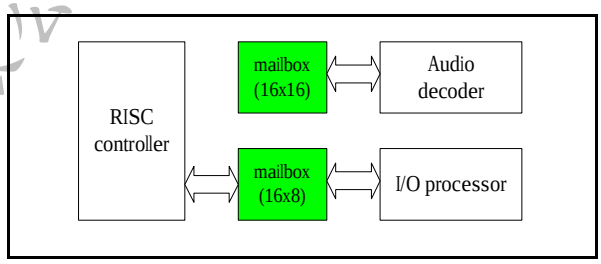


Figure 5-1 Communication between processors

The RISC processor is equipped with instruction and data caches. These caches can accelerate accesses to the SDRAM or ROM cacheable regions.

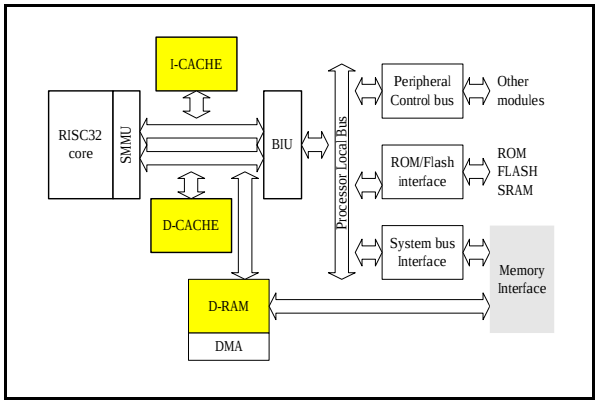


Figure 5-2 RISC subsystem

Table: RISC processor local memory configuration

Memory	Specification
I-Cache	8kbyte (2-way set associated)
D-Cache	4kbyte (direct-mapped)
D-RAM/DMA	1kbyte scratch buffer

SDRAM, ROM and other devices are mapped to RISC memory spaces as in the following table:

Table: RISC memory mapping

Memory Range	Description
8000_0000~87ff_ffff	SDRAM (cached)
a000_0000~a7ff_ffff	SDRAM (uncached)
8800_0000~8fff_ffff	ROM/FLASH/SRAM (cached)
a800_0000~afff_ffff	ROM/FLASH/SRAM (uncached)
bffe_8000~bffe_ffff	Peripheral control registers
bfff_0000~bfff_03ff	DMA buffer

SPHE8281D includes following dedicated RISC peripherals to assist the system tasks:

- Device interrupt controller:
  Device interrupt controller takes care of interrupt sources from on-chip devices and off chip sources. For each interrupt source the firmware is able to configure the interrupt behavior between edge-trigger and level-sensitive mode.
- Watchdog:
  Watchdog keeps monitoring RISC behavior and whenever firmware is in a deadlock or ill-behaved, the watchdog would trigger system-wise reset and keep the application functioning continuously.
- Timers
  There are 4-channel timers and 2 cascade counters for timed tasks. During A/V decoding, system time counters are utilized to synchronize audio and video playback timing.

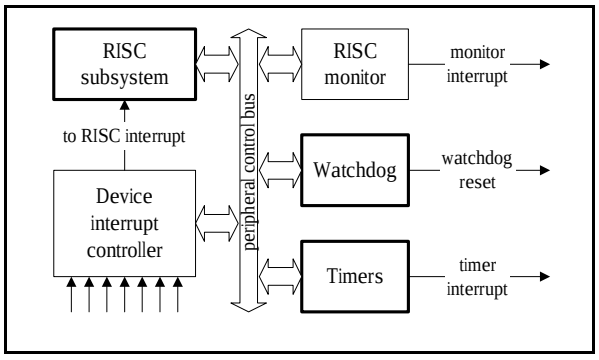


Figure 5-3 RISC dedicated hardware

Table: Device interrupt controller sources

Symbol	Description
INT_WDOG	Watchdog interrupt (if reset disabled)
INT_VSYNC	Interrupt when enter vertical resync
INT_FLD_ACT	Interrupt when enter active region
INT_FLD_SYNC	Interrupt when leave active region
INT_HOST	Host device interrupt
INT_TIMER0	Timer 0 interrupt
INT_TIMER1	Timer 1 interrupt
INT_TIMER2A	Timer 2 scale interrupt
INT_TIMER2B	Timer 2 count interrupt
INT_TIMER3A	Timer 3 scale interrupt
INT_TIMER3B	Timer 3 count interrupt
INT_TIMERW	Watchdog timer interrupt
INT_UART0	UART0 interrupt
INT_VDP0	Video decoder interrupt
INT_DSP	DSP interrupt
INT_EXT0	External interrupt #0
INT_EXT1	External interrupt #1
INT_EXT2	External interrupt #2
INT_EXT3	External interrupt #3
INT_IOP	IOP interrupt
INT_AUD	Audio hardware interrupt

5.4. ROM/Flash/SRAM Controller

The SPHE8281D provides flexible connections to external ROM, Flash or SRAM (RFS). It can support up to 4 external RFS devices by using different chip-selects (R_CS_B[3:0]). The firmware can configure RFS memory anchor registers and map these devices into locations of RISC memory space. For each memory space it can be in flash mode or in ISA mode. In FLASH mode the access timing is decided by wait-state setting, while in ISA mode the controller will reference external IO_CHRDY input.

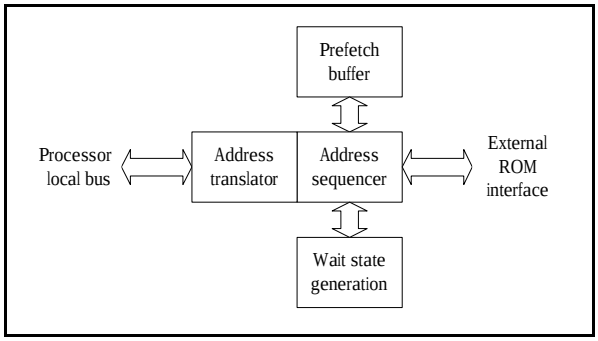


Figure 5-4 ROM/FLASH/SRAM controller

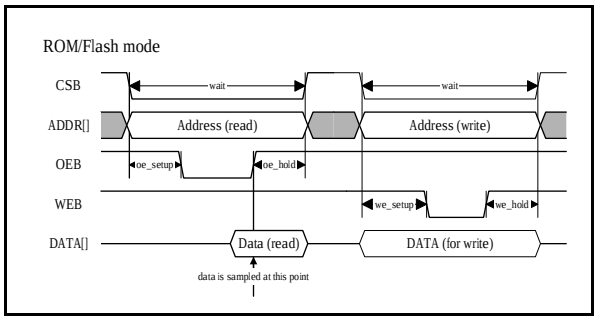


Figure 5-5 ROM/FLASH/SRAM mode timing

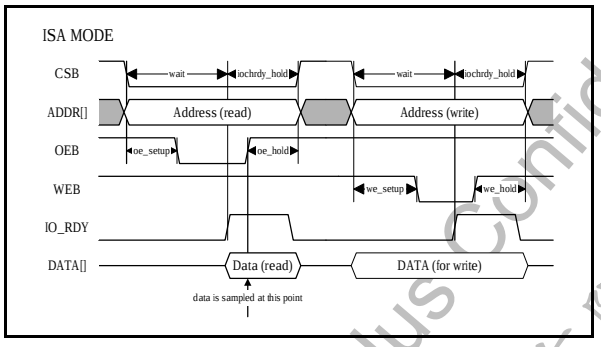


Figure 5-6 ISA mode timing

5.5. CSS Decryption Hardware

(Optional) SPHE8281D has built-in CSS decryption hardware DMA support.

5.6. MPEG Video Decoder

The system incorporates a powerful MPEG video decoding datapath and provides real-time video decoding of MPEGI/II bitstream.

The video decoder is a hardwired MPEG1/2 decoding datapath. The system architecture is as in the figure. RISC controller is in charge of pre-process and buffering source into SDRAM buffers. Upon correct timing video decoder will start to decode the bitstream and write back reconstructed video frame for playback.

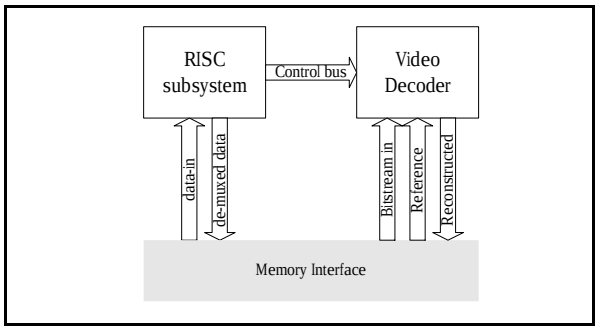


Figure 5-7 Interface between RISC and Video decoder

Advanced video decoding and display control mechanism is included to prevent tearing effect.

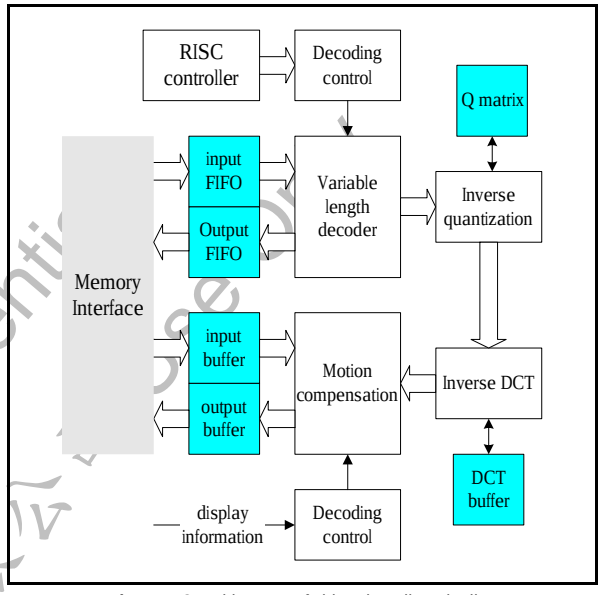


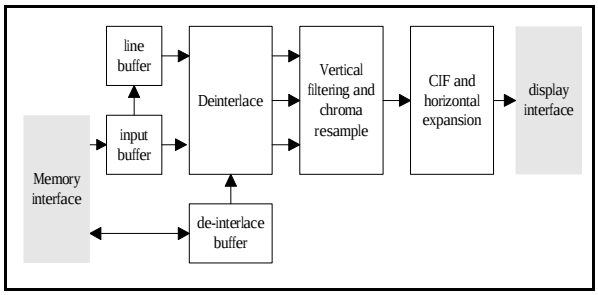
Figure 5-8 Architecture of video decoding pipeline

5.7. Video Post Processing

SPHE8281D includes powerful video-post-processing facilities to provide high video quality. It perform following functions:

- YUV411, YUV420, YUV422 and 8-bit indexed color
- SIF to CCIR601 interpolation
- MPEG1 CIF filter
- MPEG1/2 chroma vertical interpolation
- Up to 1/2x horizontal decimation
- Up to 1/512x vertical decimation
- Up to 1024x horizontal and vertical expansion
- Powerful de-interlacing hardware
- Pan and scan function
- De-flicker during interlaced display
- Video contrast/bright/color enhancement

During runtime video post-processing hardware will fetch video sources from framebuffer and process the data as in the following figure.



5.8. Programmable Audio Decoder

The SPHE8281D contains a high-performance 24-bit audio DSP optimized for embedded system applications. This audio DSP processor can fetch operands from two memories and perform multiplication-and-accumulation (MAC) in one cycle. During execution the DSP fetches instruction from main-memory or IROM, at the same time the ICACHE will store the LRU instructions. Data are loaded from and to main-memory by the cycle-stealing DMA channels.

The DSP works closely with RISC processors by using mailbox registers or shared-memory protocol. When downloaded with different firmware the DSP could support multi-standard audio and act as an accelerator for RISC in some case.

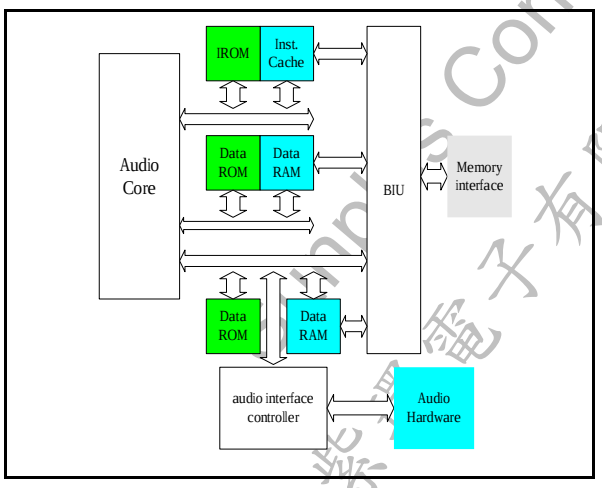


Figure 5-10 Audio DSP architecture

5.9. Audio Interface

The audio interface is in charge of servicing DSP and maintaining all audio-related tasks. It would buffer the audio PCM samples and format them to audio DAC and SPDIF formats. Up to 8 channel of digital audio are supported in I2S or normal mode.

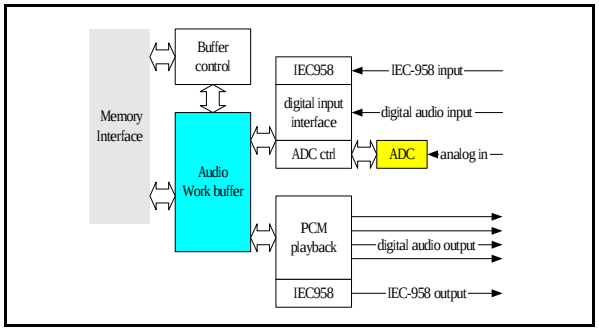


Figure 5-11 Audio Interface architecture

SPHE8281D support following audio DAC format combinations:

	32k	44.1k	48k	64k	88.2k	96k	192k
256fs	Ok	Ok	Ok	Ok	Ok	Ok	Ok
384fs	Ok	Ok	Ok	Ok	Ok	Ok	Ok

Data alignment	Left adjust, I2S, normal format
LRCK frame width	16b, 24b, 32b, 64b
Data bits	16b, 18b, 20b, 24b
Data sign extension	Zero-extended, sign-extended

5.10. Audio DAC

SPHE8281D includes a 2-channel 24-bit audio quality DAC for a minimum DVD system.

5.11. I/O Processor

The SPHE8281D includes an 8-bit micro-controller to help host controller handling I/O jobs. IR, VFD and other slow devices can be interfaced using this I/O processor.

5.12. SDRAM Controller

SDRAM controller in SPHE8281D is designed to meet both flexible and powerful requirements. It can be programmed to use 1Mx16 and 4Mx16 SDRAM chips. For different grade of memory chips it can support flexible timing select to meet different SDRAM timing requirements while achieving maximum performance. The actual speed of SDRAM interface depends on the system configuration.

SPHE8281D supports SDRAM power-down modes to save dynamic operating power.

5.13. Sub-picture Decoder

For DVD and SVCD sub-picture content SPHE8281D includes an advanced multi-format sub-picture decoder. It supports real-time vertical expansion for PAL/NTSC translation or special effect.

5.14. On Screen Display

The on screen display (OSD) function of the SPHE8281D provides an overlay bitmap graphics on the final TV display. Applications can use this function to display specific information over the video display plane without operating on the video source.

The SPHE8281D can display multiple OSD regions on a single display frame, where every OSD regions can be in different size, location and color format. The OSD hardware supports 4, 16, 256 indexed color or 16-bit direct color. OSD regions are stored in main memory before display. During display, OSD decoder would read these header and data and interpret to be a graphic data that overlay with video to be output to the display interface.

5.15. Display Interface

The display interface of SPHE8281D mixes the video content generated from video-post-processing, sub-picture-decoder and on-screen-display modules. It also performs content cropping, underflow and overflow correction and overall hue / brightness / contrast adjustment.

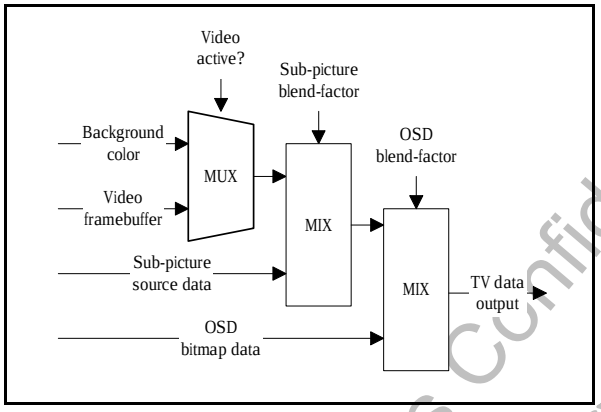


Figure 5-12 Display pipeline

The video enhancement process is show in following figure:

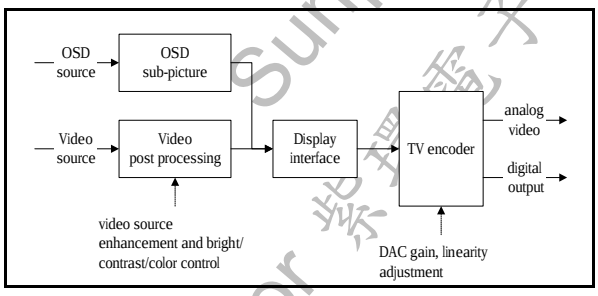


Figure 5-13 Display pipeline

5.16. Video DAC

SPHE8281D integrates 4-channel 10-bit high-speed current source DACs operating from 27MHz to 108MHz. These DAC outputs can drive a 37.5-Ohm load directly. Half current, quarter current modes are provided for low power operation using external current amplifiers.

5.17. GPIO

In SPHE8281D almost every pin that related to selectable features can serve as general-purpose input-output (GPIO) control function. When a pin is programmed to this mode, the RISC controller or the I/O processor can take full control over the direction and output level by simple firmware programming.

5.18. UART

SPHE8281D provide one UART channel for debugging, firmware upgrading and other user applications. This UART can support standard serial port baud-rate and formats. It also supports auto baud-rate detection and hardware flow control (CTS/RTS pair).

6.ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}	-0.3 to 5.5	V
Voltage on V_{DDIO} supply relative to V_{SS}	V_{DDIO}	-0.3 to 3.45	V
Voltage on V_{DDK} supply relative to V_{SS}	V_{DDK}	-0.3 to 1.90	V
Storage Temperature	T_{STG}	-55 to 150	°C
Soldering Temp. (Max. Time)	T_{SOLDER}	240 (for 5 Sec. Max.)	°C
Short circuit current	I_{OS}	50	mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.2. DC Operating Conditions

Recommended Operating Conditions (Voltage referenced to VSS=0V, TA=-0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Units
Voltage on V_{DDK} supply relative to V_{SS}	V_{DDK}	1.70	1.80	1.90	V
Voltage on V_{DDIO} supply relative to V_{SS}	V_{DDIO}	3.15	3.30	3.45	V
Input logic high voltage	V_{IH}	2.0	-	5.5	V
Input logic low voltage	V_{IL}	-0.3	-	0.8	V
Output logic high voltage	V_{OH}	2.4	-	-	V
Output logic low voltage	V_{OL}	-	-	0.4	V
Input leakage current	I_L	-10	-	10	uA

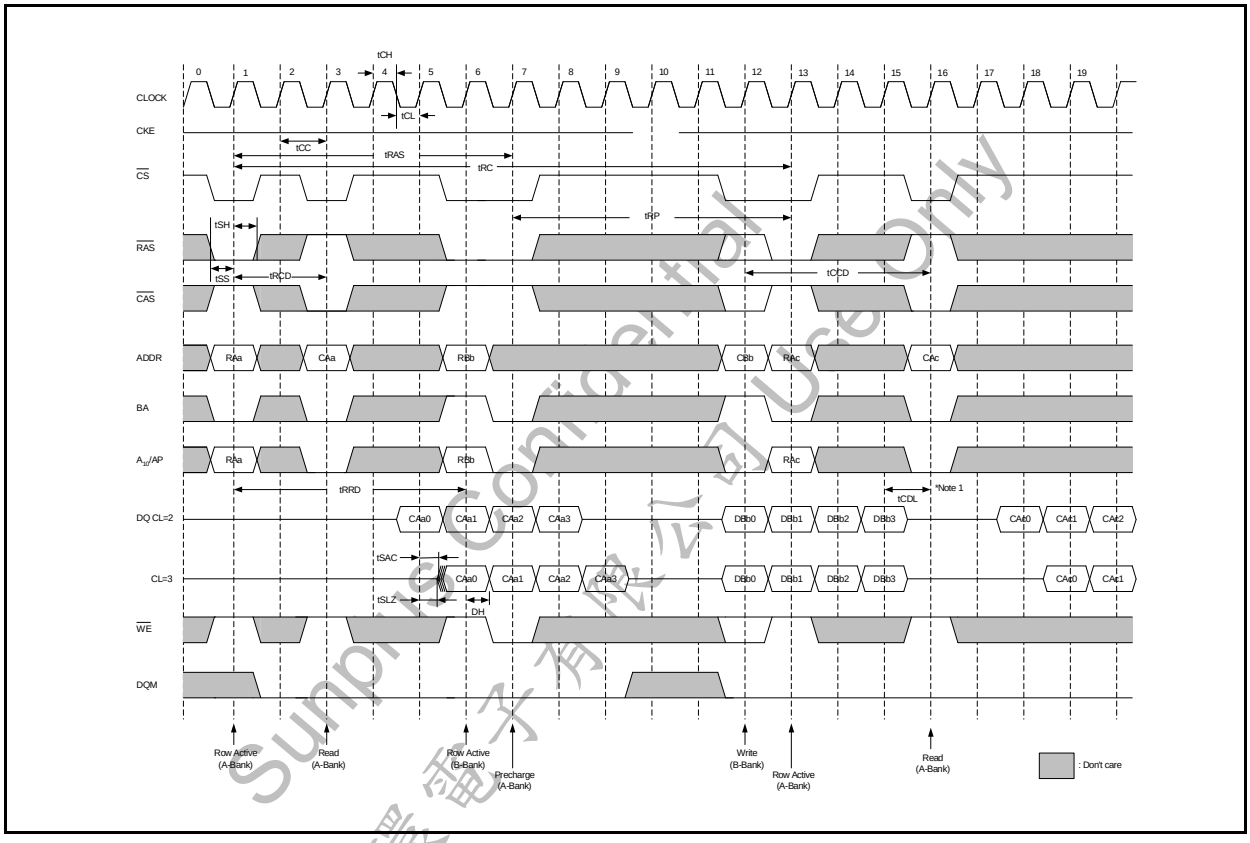
6.3. Capacitance

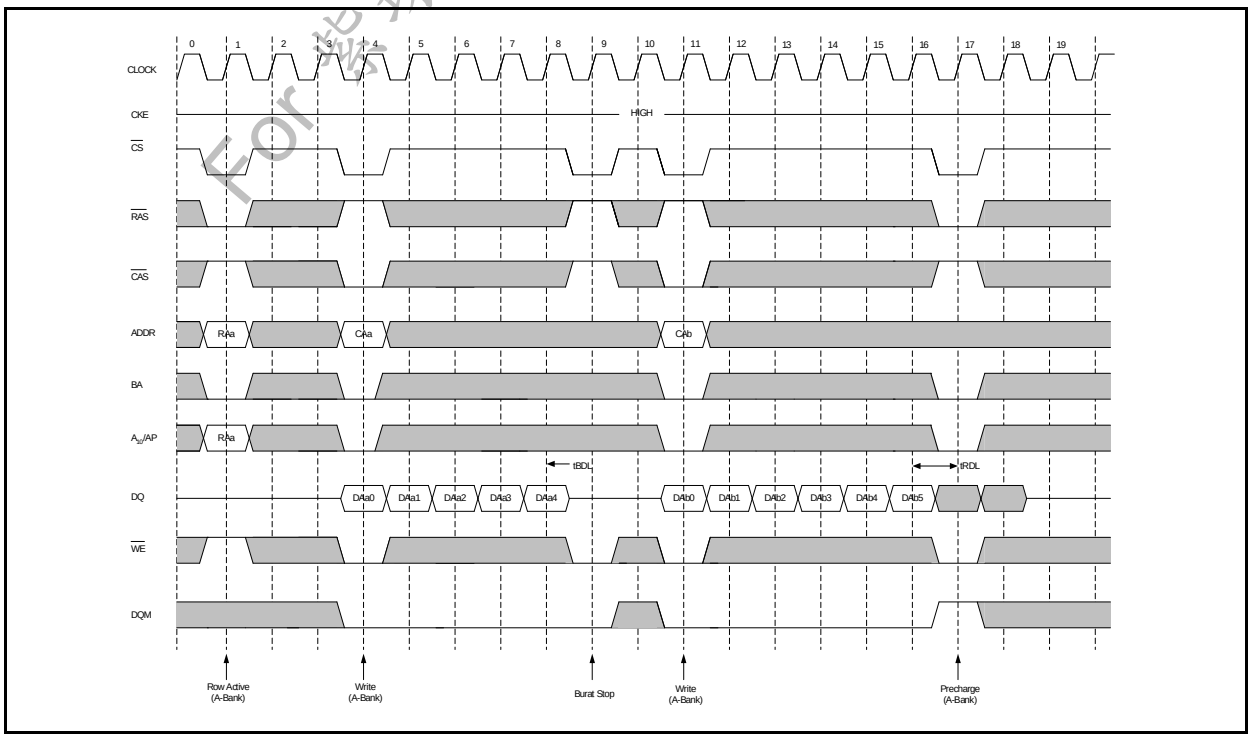
(V_{DDIO}=3.3V, TA=24°C, f=108MHz, V_{REF}=1.4V+-200mV)

Parameter	Symbol	Min.	Typ.	Max.	Units
Input pin capacitance	C_{IN}	-	3.5	-	pF
Input pin capacitance	C_{OUT}	-	3.5	-	pF
Bidirectional pin capacitance	C_{BIDIR}	-	3.5	-	pF

6.4. AC Characteristics

6.4.1. SDRAM interface timing diagrams





(Recommended condition for DVD playback is listed in typical condition with f=121.5MHz)

Parameter	Symbol	Min.	Typ.	Max.	Units
Row active to row active delay	t_{RRD}	1	2	4 *1	System clock cycle
RAS to CAS delay	t_{RCD}	1	2	4 *1	System clock cycle
Row precharge time	t_{RP}	1	2	4 *1	System clock cycle
Row active time	t_{RAS}	1	5	8 *1	System clock cycle
Row cycle time	t_{RC}	1	8	32 *1	System clock cycle
Last data in to new column address delay	t_{CDL}	1	1	4 *1	System clock cycle
Column address to column address delay	t_{CCD}	1	1	1	System clock cycle
CLK cycle time *2	t_{CC}	6	8.2	1000	ns
CLK to valid SDRAM output delay *2	t_{SAC}	-	6.0	6.5	ns
SDRAM output data hold time *2	t_{OH}	1	2	-	ns
CLK high pulse width *3	t_{CH}	-	3	-	ns
CLK low pulse width *3	t_{CL}	-	3	-	ns
CLK to SDRAM output Low-Z	t_{SLZ}	-	1.0	(t_{CC})	ns
CLK to SDRAM output High-Z	t_{SHZ}	-	6.0	(t_{SAC})	ns

Note: 1.Using maximum values may limit system performance.
2.Width of data window can be estimated from (t_{CC}-t_{SAC}+t_{OH}).
3.Width of clock pulse depends on system clock cycle.

6.4.2. ROM / flash interface timing diagrams

ROM Compatible Mode

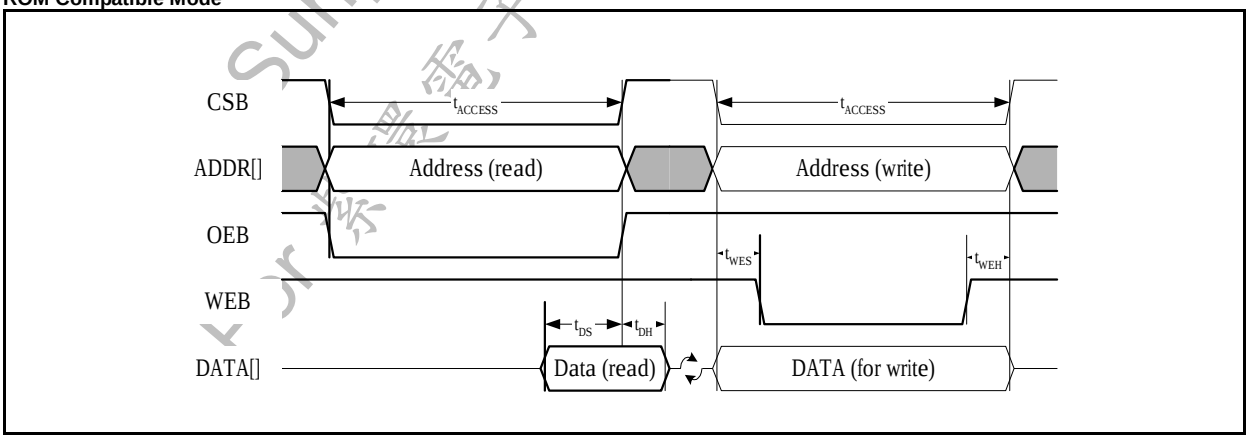


Figure 6-1 ROM / flash interface ROM mode access timing

Parameter	Symbol	Min.	Typ.	Max.	Units
ROM / SRAM / flash access time	t_{ACCESS}	2	8 *1	31	System clock cycle
Data setup time for read	t_{DS}	5	-	-	ns
Data hold time for read	t_{DH}	0	-	-	ns
Address/data setup time before write strobe	t_{WS}	0	1	31	System clock cycle
Address/data setup time after write strobe	t_{WH}	0	1	31	System clock cycle

Note: Recommended value when f=121.5MHz

ISA Compatible Mode

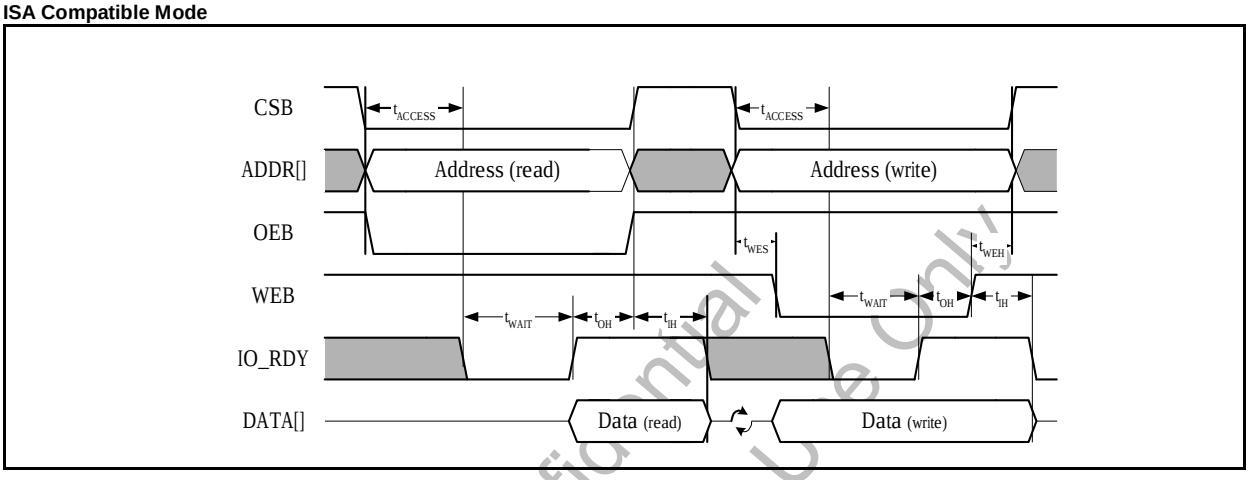


Figure 6-2 ROM / flash interface ISA mode access timing

Parameter	Symbol	Min.	Typ.	Max.	Units
ISA access time *1	t_{ACCESS}	2	-	31	System clock cycle
IO_RDY wait time	t_{WAIT}	0	-	1000	ns
Output hold time	t_{OH}	1	-	-	System clock cycle
Input hold time	t_{IH}	0	-	-	ns
Address/data setup time before write strobe	t_{WS}	0	1	31	System clock cycle
Address/data setup time after write strobe	t_{WH}	0	1	31	System clock cycle

Note: After this period of time IO_RDY_B must be stable and indicates correct status of target device.

6.4.3. Audio interface timing diagrams

Some audio interface configuration timing diagrams are shown below.

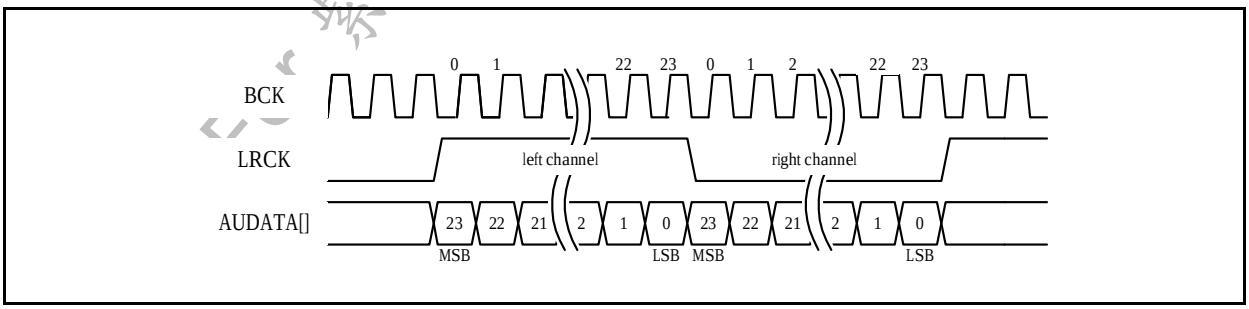


Figure 6-3 Normal mode / 24bit data / 24bit frame / MSB first

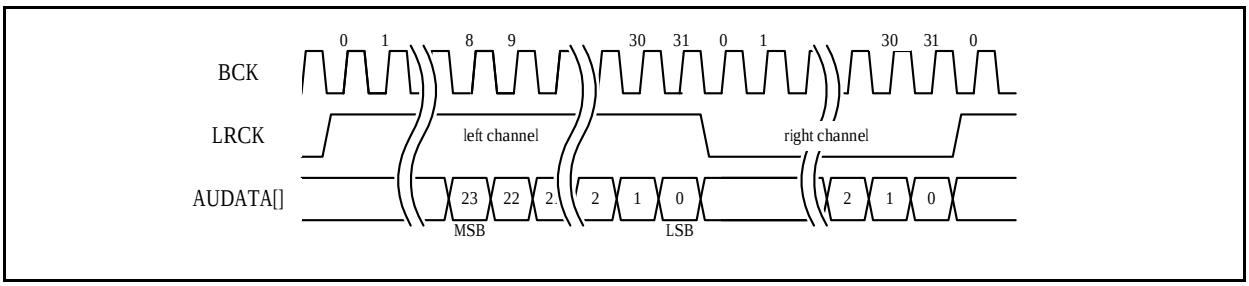


Figure 6-4 Right justified (normal) mode / 24bit data / 32bit frame / MSB first

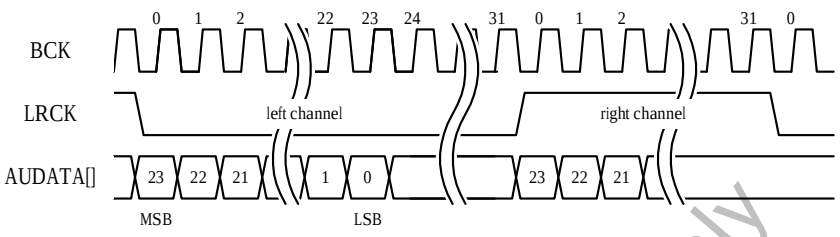


Figure 6-5 Left justified mode / 24bit data / 32bit frame / MSB first

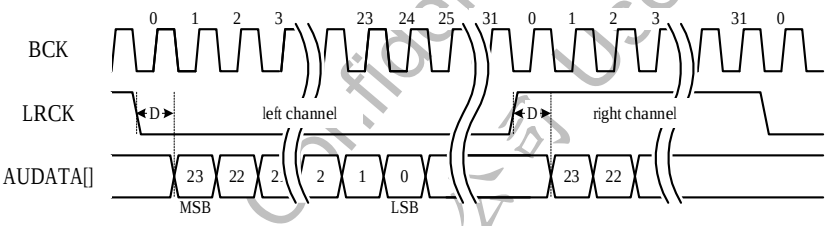


Figure 6-6 I²S mode / 24bit data / 32bit frame

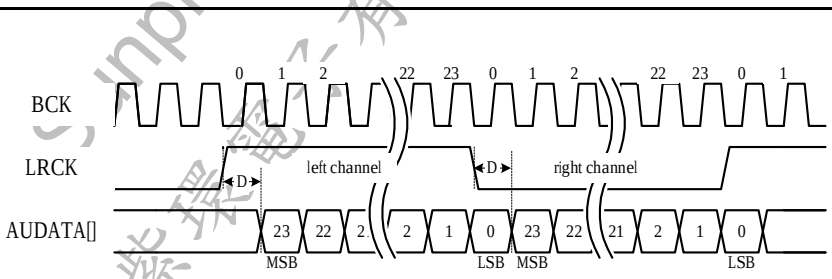


Figure 6-7 I²S mode / 24bit data / 24bit frame

Parameter	Symbol	Min.	Typ.	Max.	Units
BCK rising to LRCK / AUDATA transition	t_S	-	0.5	-	System clock cycle

6.4.4. Video timing diagrams

Interlaced Modes

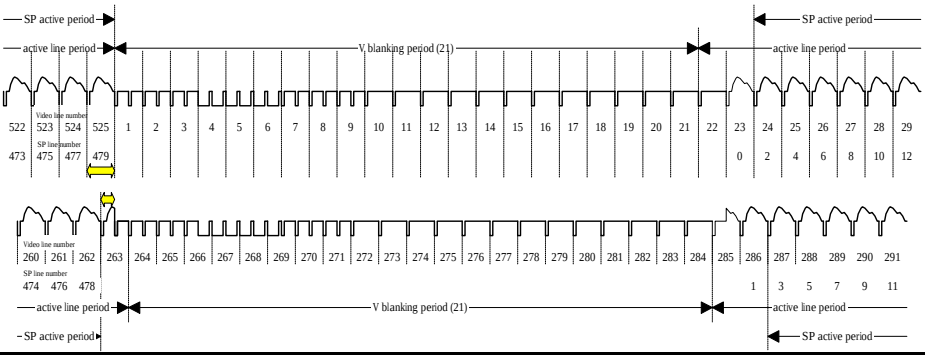


Figure 6-8 NTSC (480i) timing diagram

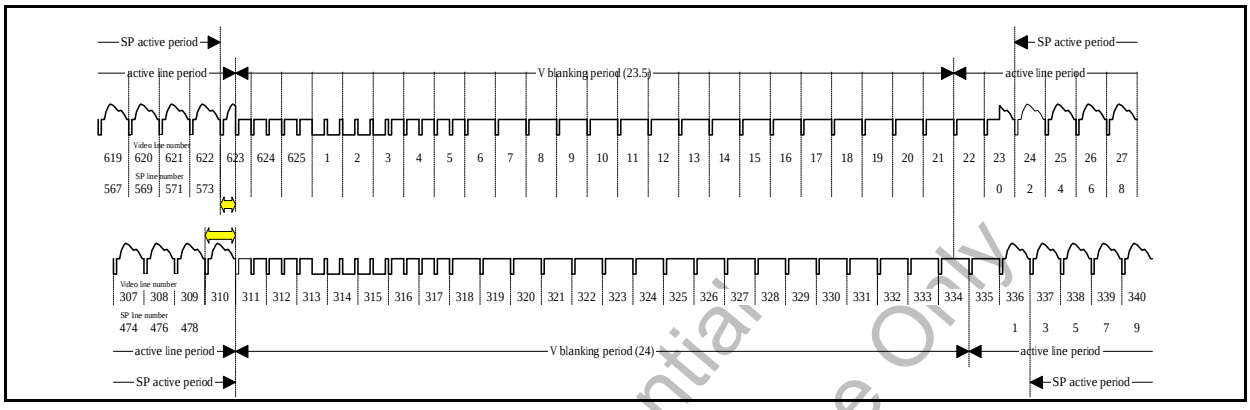


Figure 6-9 PAL (576i) timing diagram

Progressive Modes

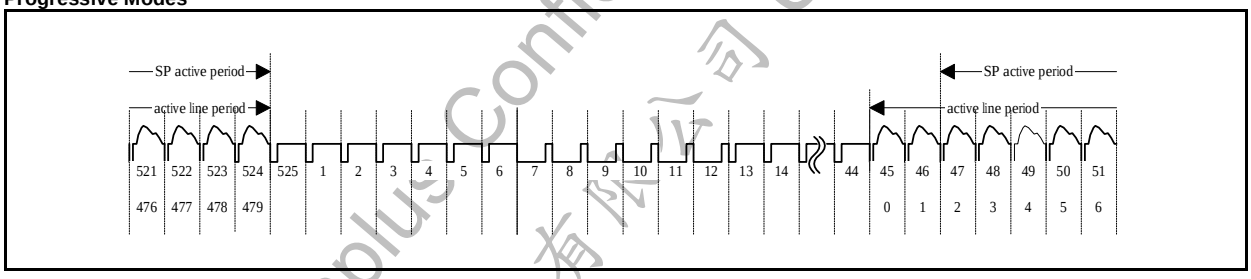


Figure 6-10 NTSC (480p) timing diagram

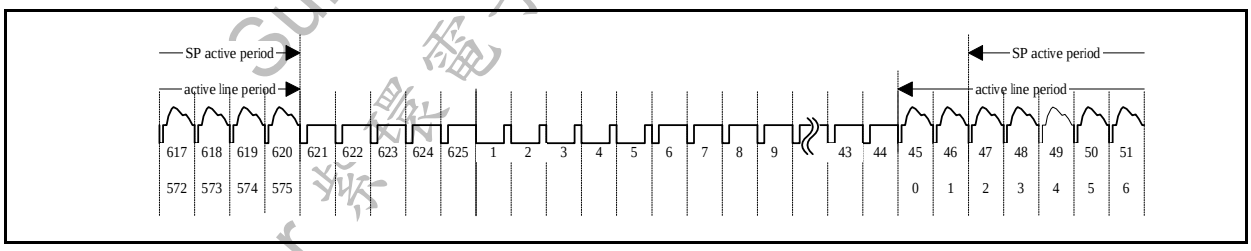
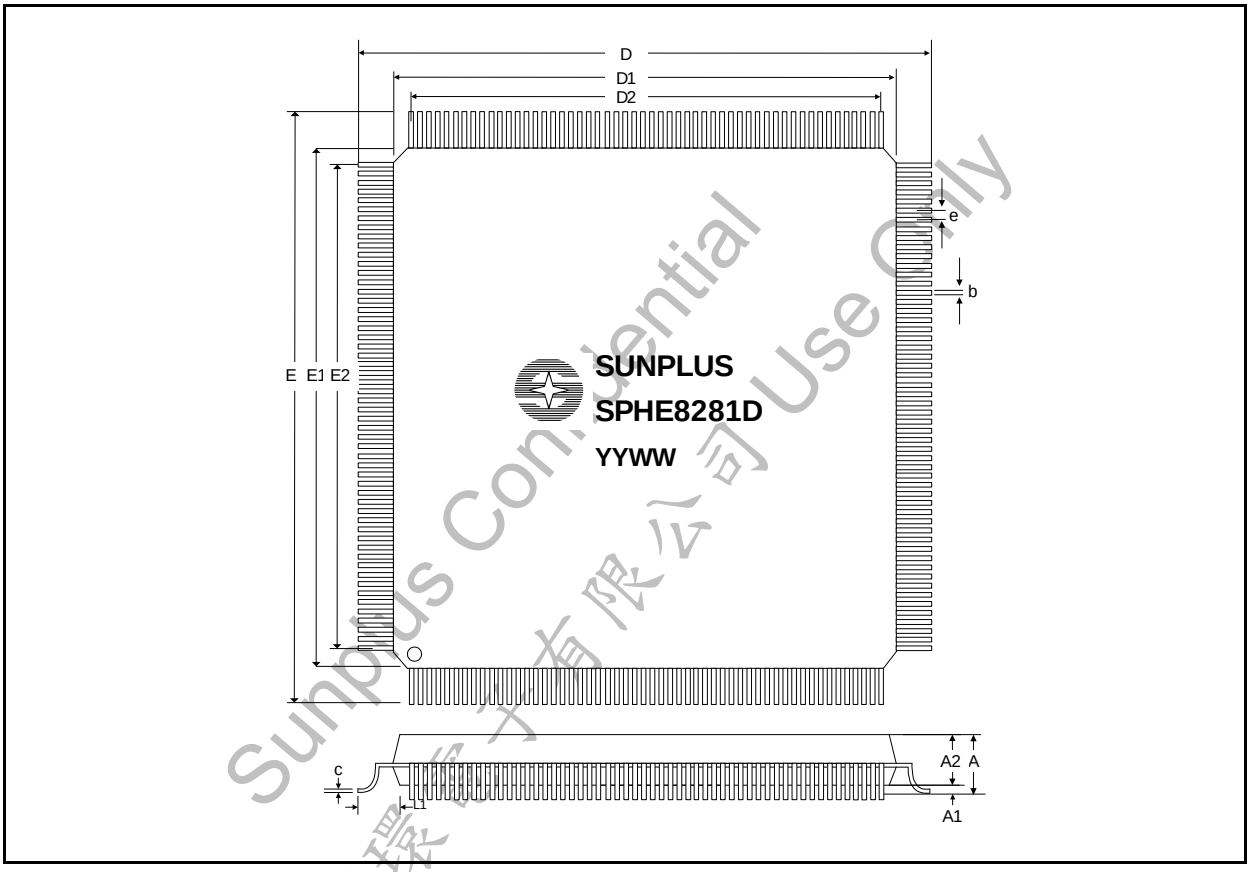


Figure 6-11 PAL (576p) timing diagram

7.PACKAGE/PAD LOCATION

7.1. Outline Dimensions



Symbol	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D	26.00 BSC.	26.00 BSC.	26.00 BSC.
D1	24.00 BSC.	24.00 BSC.	24.00 BSC.
E	26.00 BSC.	26.00 BSC.	26.00 BSC.
E1	24.00 BSC.	24.00 BSC.	24.00 BSC.
R2	0.08	-	0.20
R1	0.08	-	-
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°
c	0.09	-	0.20
L	0.45	0.60	0.75
L1	1.00 REF	1.00 REF	1.00 REF
S	0.20	-	-

Unit: Millimeter

8.DISCLAIMER

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9.REVISION HISTORY

Date	Revision #	Description	Page
MAY. 19, 2005	0.1	Original	35