ESS Technology, Inc.

ES6028
Vibratto DVD Processor
Product Brief

DESCRIPTION

The ES6028 Vibratto™ DVD processor is a single-chip MPEG video decoder that integrates a state-of-the-art 480-pixel progressive scan video feature to provide brilliant and sharp, flicker-free output to the video display. The ES6028 performs audio/video stream data processing, and TV encoding, and includes four video DACs, Macrovision™ copy protection, DVD system navigation, system control and housekeeping functions.

The Vibratto DVD processor is built on the ESS proprietary dual CPU Programmable Multimedia Processor (PMP) core consisting of 32-bit RISC and 64-bit DSP processors and offers the best DVD feature set. The processing units enable simultaneous parallel execution of system commands and data processing to perform specialized encoding and decoding tasks in the device architecture.

The RISC processor, and its associated hardware, perform bit stream parsing, control audio data output, transfer video and audio data to the vector engine and service system control and housekeeping functions. The vector engine (DSP), and associated hardware, perform audio and video micro-code processing required by A/V standards, such as Dolby® Digital, DTS™ surround, MPEG, and JPEG imaging. These processing tasks include audio processing, video motion compensation and estimation, loop filtering, discrete cosine transforms (DCT) and inverse DCT, quantization, and inverse quantization.

The Vibratto DVD processor supports both parallel and serial DVD loader interfaces, industry standard I²S audio data input and output, EPROM and SDRAM access, and audio/video data buffering. The Vibratto also supports both letterbox and pan-and-scan displays, sub-picture overlay, and On-Screen Display (OSD).

A new feature found with the Vibratto DVD solution is the ESS Music Slideshow™, which allows a user to do voiceovers while viewing JPEG images, Kodak® PictureCD, and Fujicolor® CD images. In addition, the Vibratto DVD solution offers support for SACD, Karaoke CD+G, MP3, HDCD, CD-DA, and Windows™ Media Audio (WMA) decoding and playback.

The ES6028 Vibratto DVD processor is available in 208-pin Plastic Quad Flat Pack (PQFP) device package.

FEATURES

- Single-chip DVD processor based on ESS proprietary dual CPU PMP core.
- Integrated NTSC/PAL encoder.
- Progressive scan video output for flicker-free video display.
- Four integrated 10-bit video DACs.
- DVD-Video, VCD 1.1, 2.0, and SVCD.
- 5.1 channel audio outputs.
- Interface for ATAPI devices and A/V DVD loaders.
- Interface for CF, MS, and SM memory cards.
- Direct interface of 8-/16-bit SDRAM up to 128-Mb capacity.
- Direct interface for up to 4 banks of 8-/16-bit EPROM or Flash EPROM for up to 16-MB capacity.
- Macrovision 7.1 for NTSC/PAL interlaced video.
- Macrovision AGC 1.03-compliant for 480p progressive scan video.
- Composite video, S-video, YUV and RGB outputs.
- 8-bit CCIR 601 YUV 4:2:2 output.
- On-Screen Display (OSD) controller with 3-bit blending provides display with 256 colors in 8 degrees of transparency.
- Subpicture Unit (SPU) decoder supports karaoke lyric, subtitles, and EIA-608 compliant Line 21 Captioning.
- Dolby Digital (AC-3), Dolby Pro Logic™, and Dolby Pro Logic II.
- DTS surround.
- S/PDIF digital audio output.
- High-Definition Compatible Digital™ (HDCD) decoding.
- SRS TruSurround®.
- Windows Media Audio.
- MP3.
- CD-DA.
- Karaoke.

ES6028 PINOUT DIAGRAM

The device pinout for the ES6028 is shown in Figure 1.

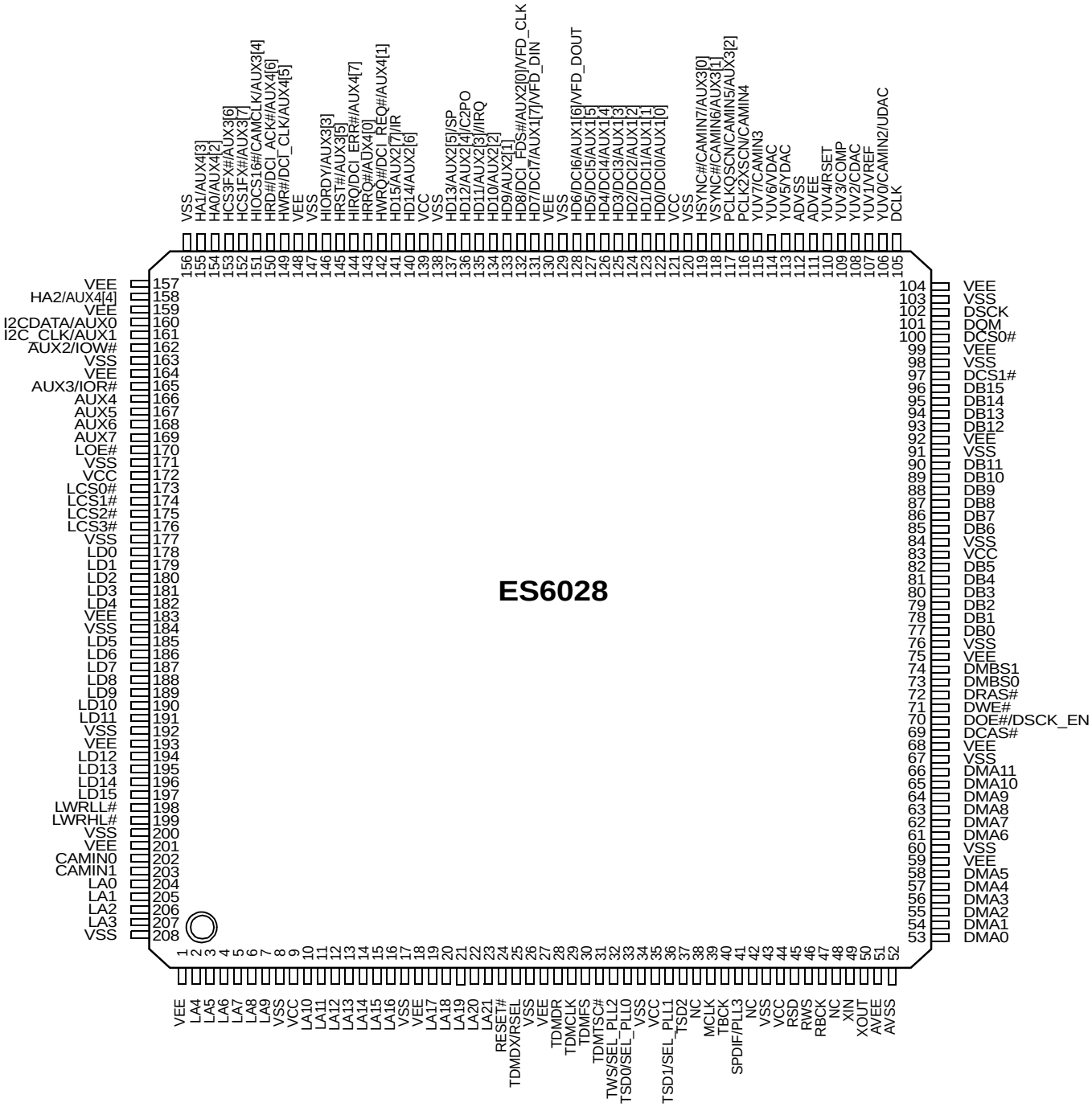

Figure 1 ES6028 Device Pinout

ES6028 PIN DESCRIPTION

Table 1 lists the pin descriptions for the ES6028.

Table 1 ES6028 Pin Description

<table>
<tr><th>Name</th><th>Pin Numbers</th><th>I/O</th><th>Definition</th></tr>
<tr><td>VEE</td><td>1,18, 27, 59, 68, 75, 92, 99, 104, 130, 148, 157, 159, 164, 183, 193, 201</td><td>P</td><td>I/O power supply.</td></tr>
<tr><td>LA[21:0]</td><td>2-7, 10-16, 19-23, 204-207</td><td>O</td><td>RISC port address bus.</td></tr>
<tr><td>VSS</td><td>8, 17, 26, 34, 43, 60, 67, 76, 84, 91, 98, 103, 120, 129, 138, 147, 156, 163, 171, 177, 184, 192, 200, 208</td><td>G</td><td>Ground.</td></tr>
<tr><td>VCC</td><td>9, 35, 44, 83, 121, 139, 172</td><td>P</td><td>Core power supply.</td></tr>
<tr><td>RESET#</td><td>24</td><td>I</td><td>Reset input, active-low.</td></tr>
<tr><td>TDMDX</td><td rowspan="2">25</td><td>O</td><td>TDM transmit data output.</td></tr>
<tr><td>RSEL</td><td>I</td><td>LCS3 ROM Boot Data Width Select. Strapped to VCC or ground via 4.7-kΩ resistor; read only during reset.
<table>
<tr><th>RSEL</th><th>Selection</th></tr>
<tr><td>0</td><td>16-bit ROM</td></tr>
<tr><td>1</td><td>8-bit ROM</td></tr>
</table></td></tr>
<tr><td>TDMDR</td><td>28</td><td>I</td><td>TDM receive data input.</td></tr>
<tr><td>TDMCLK</td><td>29</td><td>I</td><td>TDM clock input.</td></tr>
<tr><td>TDMFS</td><td>30</td><td>I</td><td>TDM frame sync input.</td></tr>
<tr><td>TDMTSC#</td><td>31</td><td>O</td><td>TDM output enable.</td></tr>
<tr><td>TWS</td><td rowspan="2">32</td><td>O</td><td>Audio transmit frame sync output.</td></tr>
<tr><td>SEL_PLL2</td><td>I</td><td>System and DSCK output clock frequency selection is made at the rising edge of RESET#. The matrix below lists the available clock frequencies and their respective PLL bit settings. Strapped to VCC or ground via 4.7-kΩ resistor; read only during reset.
<table>
<tr><th>SEL_PLL2</th><th>SEL_PLL1</th><th>SEL_PLL0</th><th>Clock Type</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>DCLK x 4.25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Bypass mode</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DCLK x 3.75</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>DCLK x 4.5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>DCLK x 3.5</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>DCLK x 4</td></tr>
</table></td></tr>
</table>

Table 1 ES6028 Pin Description (Continued)

Name	Pin Numbers	I/O	Definition
TSD0	33	O	Audio transmit serial data output 0.
SEL_PLL0		I	Refer to the description and matrix for SEL_PLL2 pin 32.
TSD1	36	O	Audio transmit serial data output 1.
SEL_PLL1		I	Refer to the description and matrix for SEL_PLL2 pin 32.
TSD2	37	O	Audio transmit serial data output 2.
NC	38, 42, 48	—	No connect pins. Leave open.
MCLK	39	I/O	Audio master clock for audio DAC.
TBCK	40	I/O	Audio transmit bit clock. TBCK is an input during reset and subsequently is programmed as an output via the AUDIOXMT register (addr 0x2000D00Ch, bit 4).
SPDIF	41	O	S/PDIF output.
SEL_PLL3		I	Clock source select. Strapped to VCC or ground via 4.7-kΩ resistor; read only during reset.

SEL_PLL3	Clock Source
0	Crystal oscillator
1	DCLK input

RSD	45	I	Audio receive serial data.
RWS	46	I	Audio receive frame sync.
RBCK	47	I	Audio receive bit clock.
XIN	49	I	27-MHz crystal input.
XOUT	50	O	27-MHz crystal output.
AVEE	51	P	Analog power for PLL.
AVSS	52	G	Analog ground for PLL.
DMA[11:0]	53-58, 61-66	O	DRAM address bus.
DCAS#	69	O	DRAM column address strobe.
DOE#	70	O	DRAM output enable.
DSCK_EN		O	DRAM clock enable.
DWE#	71	O	DRAM write enable.
DRAS#	72	O	DRAM row address strobe.
DMBS0	73	O	SDRAM bank select 0.
DMBS1	74	O	SDRAM bank select 1.
DB[15:0]	77-82, 85-90, 93-96	I/O	DRAM data bus.
DCS[1:0]#	97,100	O	SDRAM chip select.
DQM	101	O	Data input/output mask.
DSCK	102	O	Output clock to SDRAM.

Table 1 ES6028 Pin Description (Continued)

<table>
<tr><th>Name</th><th>Pin Numbers</th><th>I/O</th><th>Definition</th></tr>
<tr><td>DCLK</td><td>105</td><td>I</td><td>Clock input to PLL.</td></tr>
<tr><td>YUV0</td><td rowspan="3">106</td><td>O</td><td>YUV pixel 0 output data.</td></tr>
<tr><td>CAMIN2</td><td>I</td><td>Camera input 2.</td></tr>
<tr><td>UDAC</td><td>O</td><td>Video DAC output.
<table>
<tr><th>Pin</th><th>114</th><th>113</th><th>108</th><th>106</th></tr>
<tr><th>Value</th><th>DAC V</th><th>DAC Y</th><th>DAC C</th><th>DAC U</th></tr>
<tr><td>0</td><td>CVBS1</td><td>Y</td><td>C</td><td>N/A</td></tr>
<tr><td>1</td><td>CVBS1</td><td>Y</td><td>C</td><td>CVBS2</td></tr>
<tr><td>2</td><td>N/A</td><td>Y</td><td>C</td><td>N/A</td></tr>
<tr><td>3</td><td>CVBS1</td><td>N/A</td><td>N/A</td><td>CVBS2</td></tr>
<tr><td>4</td><td>CVBS1</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
<tr><td>5</td><td>CVBS1</td><td>Y</td><td>Pb</td><td>Pr</td></tr>
<tr><td>6</td><td>N/A</td><td>Y</td><td>Pb</td><td>Pr</td></tr>
<tr><td>7</td><td>SYNC</td><td>G</td><td>B</td><td>R</td></tr>
<tr><td>8</td><td>CHROMA</td><td>Y</td><td>Pb</td><td>Pr</td></tr>
<tr><td>9</td><td>CVBS1</td><td>G</td><td>B</td><td>R</td></tr>
<tr><td>10</td><td>CVBS1</td><td>G</td><td>R</td><td>B</td></tr>
<tr><td>11</td><td>SYNC</td><td>G</td><td>R</td><td>B</td></tr>
<tr><td>12</td><td>N/A</td><td>Y</td><td>Pr</td><td>Pb</td></tr>
<tr><td>13</td><td>CVBS1</td><td>Y</td><td>Pr</td><td>Pb</td></tr>
</table>
Y: Luma component for YUV and Y/C processing.
C: Chrominance signal for Y/C processing.
U: Chrominance component signal for YUV mode.
V: Chrominance component signal for YUV mode.</td></tr>
<tr><td>YUV1</td><td rowspan="2">107</td><td>O</td><td>YUV pixel 1output data.</td></tr>
<tr><td>VREF</td><td>I</td><td>Internal voltage reference to video DAC. Bypass to ground with 0.1-µF capacitor.</td></tr>
<tr><td>YUV2</td><td rowspan="2">108</td><td>O</td><td>YUV pixel 2 output data.</td></tr>
<tr><td>CDAC</td><td>O</td><td>Video DAC output. Refer to description and matrix for UDAC pin 106.</td></tr>
<tr><td>YUV3</td><td rowspan="2">109</td><td>O</td><td>YUV pixel 3 output data.</td></tr>
<tr><td>COMP</td><td>I</td><td>Compensation input. Bypass to ADVEE with 0.1-µF capacitor.</td></tr>
<tr><td>YUV4</td><td rowspan="2">110</td><td>O</td><td>YUV pixel 4 output data.</td></tr>
<tr><td>RSET</td><td>I</td><td>DAC current adjustment resistor input.</td></tr>
<tr><td>ADVEE</td><td>111</td><td>P</td><td>Analog power for video DAC.</td></tr>
<tr><td>ADVSS</td><td>112</td><td>G</td><td>Analog ground for video DAC.</td></tr>
</table>

Table 1 ES6028 Pin Description (Continued)

Name	Pin Numbers	I/O	Definition
YUV5	113	O	YUV pixel 5 output data.
YDAC		O	Video DAC output. Refer to description and matrix for UDAC pin 106.
YUV6	114	O	YUV pixel 6 output data.
VDAC		O	Video DAC output. Refer to description and matrix for UDAC pin 106.
YUV7	115	O	YUV pixel 7 output data.
CAMIN3		I	Camera YUV 3.
PCLK2XSCN	116	I/O	27-MHz video output pixel clock.
CAMIN4		I	Camera YUV 4.
PCLKQSCN	117	O	13.5-MHz video output pixel clock.
CAMIN5		I	Camera YUV 5.
AUX3[2]		I/O	Aux3 data I/O.
VSYNC#	118	I/O	Vertical sync, active-low.
CAMIN6		I	Camera YUV 6.
AUX3[1]		I/O	Aux3 data I/O.
HSYNC#	119	I/O	Horizontal sync, active-low.
CAMIN7		I	Camera YUV 7.
AUX3[0]		I/O	Aux3 data I/O.
HD[5:0]	122-127	I/O	Host data bus lines 5:0.
DCI[5:0]		I/O	DVD channel data I/O.
AUX1[5:0]		I/O	Aux1 data I/O.
HD6	128	I/O	Host data bus line 6.
DCI6		I/O	DVD channel data I/O.
AUX1[6]		I/O	Aux1 data I/O.
VFD_DOUT		I	VFD data output.
HD7	131	I/O	Host data bus line 7.
DCI7		I/O	DVD channel data I/O.
AUX1[7]		I/O	Aux1 data I/O.
VFD_DIN		I	VFD data input.
HD8	132	I/O	Host data bus line 8.
DCI_FDS#		I/O	DVD input sector start.
AUX2[0]		I/O	Aux2 data I/O.
VFD_CLK		I	VFD clock input.
HD9	133	I/O	Host data bus line 9.
AUX2[1]		I/O	Aux2 data I/O.

Table 1 ES6028 Pin Description (Continued)

Name	Pin Numbers	I/O	Definition
HD10	134	I/O	Host data bus line 10.
AUX2[2]		I/O	Aux2 data I/O.
HD11	135	I/O	Host data bus line 11.
AUX2[3]		I/O	Aux2 data I/O.
IRQ		O	IRQ.
HD12	136	I/O	Host data bus line 12.
AUX2[4]		I/O	Aux2 data I/O.
C2PO		I	C2PO error correction flag from CD-ROM.
HD13	137	I/O	Host data bus line 13.
AUX2[5]		I/O	Aux2 data I/O.
SP		I	16550 UART serial port input.
HD14	140	I/O	Host data bus line 14.
AUX2[6]		I/O	Aux2 data I/O.
HD15	141	I/O	Host data bus line 15.
AUX2[7]		I/O	Aux2 data I/O.
IR		I	IR remote control input.
HWRQ#	142	O	Host write request.
DCI_REQ#		O	DVD control interface request.
AUX4[1]		I/O	Aux4 data I/O.
HRRQ#	143	O	Host read request.
AUX4[0]		I/O	Aux4 data I/O.
HIRQ	144	I/O	Host interrupt.
DCI_ERR#		I/O	DVD channel data error.
AUX4[7]		I/O	Aux4 data I/O.
HRST#	145	O	Host reset.
AUX3[5]		I/O	Aux3 data I/O.
HIORDY	146	I	Host I/O ready.
AUX3[3]		I/O	Aux3 data I/O.
HWR#	149	I/O	Host write.
DCI_CLK		I/O	DVD channel data clock.
AUX4[5]		I/O	Aux4 data I/O.
HRD#	150	O	Host read.
DCI_ACK#		O	DVD channel data valid.
AUX4[6]		I/O	Aux4 data I/O.

Table 1 ES6028 Pin Description (Continued)

Name	Pin Numbers	I/O	Definition
HIOCS16#	151	I	Device 16-bit data transfer.
CAMCLK		I	Camera port pixel clock input.
AUX3[4]		I/O	Aux3 data I/O.
HCS1FX#	152	O	Host select 1.
AUX3[7]		I/O	Aux3 data I/O.
HCS3FX#	153	O	Host select 3.
AUX3[6]		I/O	Aux3 data I/O.
HA[2:0]	154, 155, 158	I/O	Host address bus.
AUX4[4:2]		I/O	Aux4 data I/Os.
AUX0	160	I/O	Auxiliary port 0 (open collector).
I2CDATA		I/O	I^2C data I/O.
AUX1	161	I/O	Auxiliary port 1 (open collector).
I2C_CLK		I/O	I^2C clock I/O.
AUX2	162	I/O	Auxiliary port.
IOW#		O	I/O Write strobe (LCS1).
AUX3	165	I/O	Auxiliary port.
IOR#		O	I/O Read strobe (LCS1).
AUX7-4	166-169	I/O	Auxiliary ports.
LOE#	170	O	RISC port output enable.
LCS[3:0]#	173-176	O	RISC port chip select.
LD[15:0]	178-182, 185-191, 194-197	I/O	RISC port data bus.
LWRLL#	198	O	RISC port low-byte write enable.
LWRHL#	199	O	RISC port high-byte write enable.
CAMIN0	202	I	Camera YUV 0.
CAMIN1	203	I	Camera YUV 1.

SYSTEM BLOCK DIAGRAM

A sample system block diagram for the ES6028 Vibratto DVD player board design is shown in Figure 2.

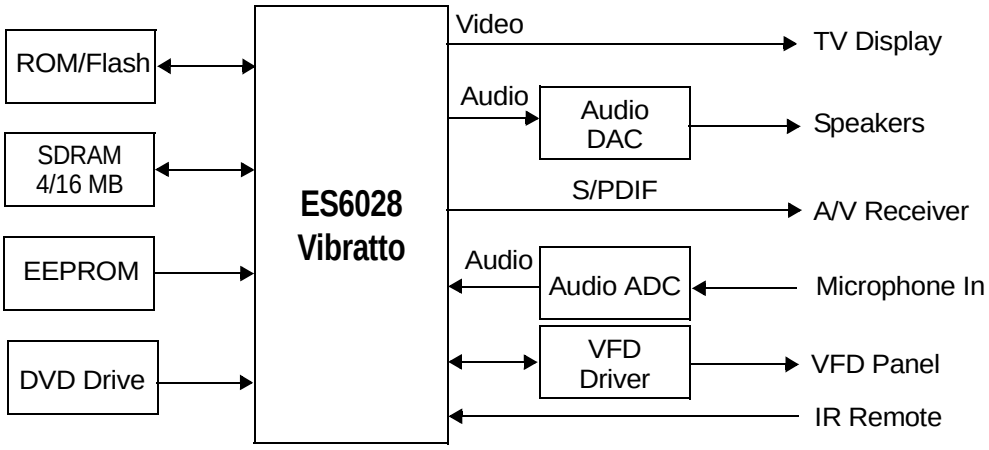

Figure 2 ES6028 Vibratto System Block Diagram

ORDERING INFORMATION

Part Number	Description	Package
ES6028F	Vibratto 5.1-channel DVD, DTS, Progressive Scan and TV Encoder	208-pin PQFP

The letter F at the end of the part number identifies the package type PQFP.

Other Vibratto DVD Processors

Part Number	Description	Package
ES6008F	Vibratto 2-channel DVD and TV Encoder	208-pin PQFP
ES6018F	Vibratto 5.1-channel DVD, DTS and TV Encoder	208-pin PQFP
ES6038F	Vibratto 5.1-channel DVD, DTS, Progressive Scan, DVD-Audio and TV Encoder	208-pin PQFP

The letter F at the end of the part number identifies the package type PQFP.

ESS Technology, Inc.
48401 Fremont Blvd.
Fremont, CA 94538
Tel: (510) 492-1088
Fax: (510) 492-1898