
PAN101B CMOS OPTICAL NAVIGATION SENSOR

General Description

The PAN101B is a low cost CMOS process optical navigation sensor with DSP integration chip that serves as a non-mechanical motion estimation engine for implementing a computer mouse.

Features

- Single 3.0 volt power supply
- Optical motion estimation technology
- Complete 2-D motion sensor
- No mechanical parts
- Accurate motion estimation over a wide range of surfaces
- High speed motion detection up to 16+ inches/sec
- High resolution up to 800 cpi
- Shutdown pin for low power dissipation.
- Power saving mode during times of no movement
- Serial Interface for programming and data transfer
- I/O pin 5.0 volt tolerance

Key Specification

| | |
|--------------------------|--|
| Power Supply | Wide operating supply range 2.7V~3.6V |
| Optical Lens | 1:1 |
| System Clock | 18.432 MHz |
| Speed | 16+ inches/sec |
| Resolution | 400/800 cpi |
| Frame Rate | 3000 frames/sec |
| Operating Current | <15mA @Mouse moving (Normal) < 5mA @Mouse not moving (sleep1) < 2mA @Mouse not moving (sleep2) < 100uA @Shutdown mode |
| Package | Shrunk DIP20 |

Ordering Information

| Order number | I/O | Resolution |
|---------------------|-------------------|-------------------|
| PAN101BOI-204 | Open-drain output | 400 cpi |
| PAN101BOI-208 | Open-drain output | 800 cpi |
| PAN101BSI-204 | CMOS output | 400 cpi |
| PAN101BSI-208 | CMOS output | 800 cpi |

1. Pin Description

| Pin No. | Name | Type | Definition |
|---------|---------|----------------------------|------------------------------------|
| 1 | VSS_LED | GND | LED ground |
| 2 | LED | I/O | LED control |
| 3 | OSCOUT | OUT | Resonator output |
| 4 | OSCIN | IN | Resonator input |
| 5 | VSSD | GND | Chip digital ground |
| 6 | VSSA | GND | Chip analog ground |
| 7 | VDDD | PWR | Chip digital power VDD, 3.0V |
| 8 | VDDA | PWR | Chip analog power VDD, 3.0V |
| 9 | VRB | BYPASS | Analog voltage reference |
| 10 | VRT | BYPASS | Analog voltage reference |
| 11 | VAY | BYPASS | Analog voltage reference |
| 12 | XA | Open-drain OUT (PAN101BOI) | XA quadrature output |
| | | CMOS OUT (PAN101BSI) | |
| 13 | NC | - | No connection |
| 14 | XB | Open-drain OUT (PAN101BOI) | XB quadrature output |
| | | CMOS OUT (PAN101BSI) | |
| 15 | YA | Open-drain OUT (PAN101BOI) | YA quadrature output |
| | | CMOS OUT (PAN101BSI) | |
| 16 | NC | - | No connection |
| 17 | YB | Open-drain OUT (PAN101BOI) | YB quadrature output |
| | | CMOS OUT (PAN101BSI) | |
| 18 | SCLK | IN | Serial interface clock |
| 19 | SDIO | Open-drain I/O (PAN101BOI) | Serial interface bi-direction data |
| | | CMOS I/O (PAN101BSI) | |
| 20 | PD | IN | Power down pin, active high |

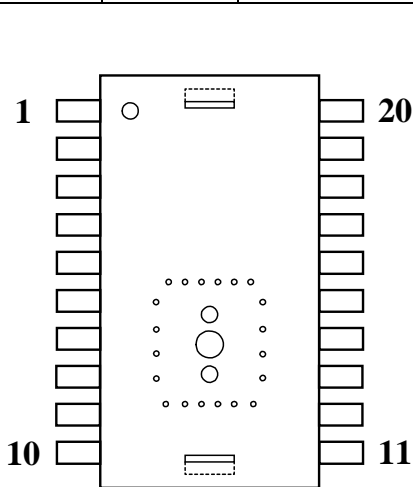


Figure 1. Top View Pinout

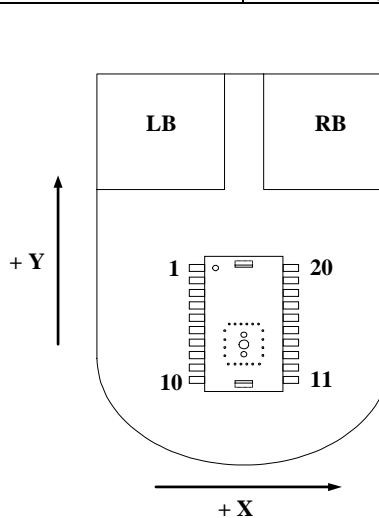


Figure 2. Top View of Mouse

2. Block Diagram and Operation

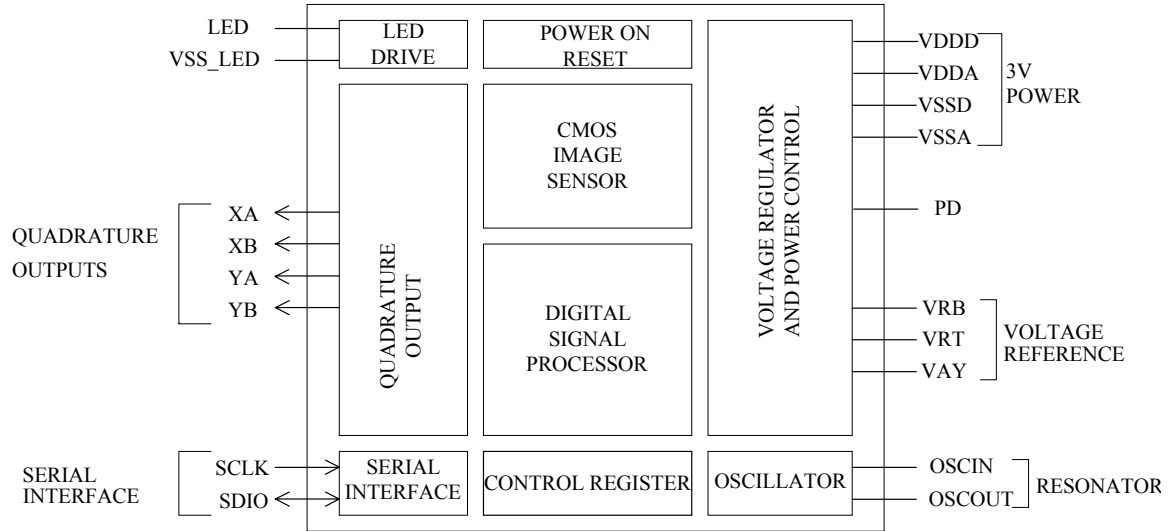


Figure 3. Block Diagram

The PAN101B is a low cost CMOS-process optical navigation sensor with DSP integration chip that serves as a non-mechanical motion estimation engine for implementing a computer mouse. It is based on optical navigation technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement. The sensor is in a 20 pin optical package. The output format is two-channel quadrature (X and Y direction), which emulates encoder phototransistors. The current X and Y information are also available in registers accessed via a serial port.

3. Registers and Operation

The PAN101B can be programmed through registers, via the serial port, and DSP configuration and motion data can be read from these registers. All registers not listed are reserved, and should never be written by firmware.

3.1 Registers

| Address | Name | R/W | Default | Data Type |
|---------|----------------|-----|---------|--|
| 0x00 | Product_ID | R | 0x02 | Eight bits number with the product identifier. |
| 0x01 | Reserved | - | - | Reserved for future. |
| 0x02 | Motion_Status | R | - | Bit field |
| 0x03 | Delta_X | R | - | Eight bits 2's complement number. |
| 0x04 | Delta_Y | R | - | Eight bits 2's complement number. |
| 0x05 | Operation_Mode | R/W | - | Bit field |

3.2 Register descriptions

| | | | | | | | | |
|-------------|--|------|------|------|------|------|------|------|
| 0x00 | Product_ID | | | | | | | |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | PID7 | PID6 | PID5 | PID4 | PID3 | PID2 | PID1 | PID0 |
| Usage | The value in this register can not change, it can be used to verify that the serial communications link is OK. | | | | | | | |
| 0x01 | Reserved | | | | | | | |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Reserved | | | | | | | |
| Usage | Reserved for future | | | | | | | |

| 0x02 | Motion_Status | | | | | | | |
|-------|--|--|----------|-------|-------|----------|----------|-----|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Motion | Reserved | Reserved | DYOVF | DXOVF | Reserved | Reserved | RES |
| Usage | <p>Register 0x02 allows the user to determine if motion has occurred since the last time it was read. If so, then the user should read registers 0x03 and 0x04 to get the accumulated motion. It also tells if the motion buffers have overflowed since the last reading. The current resolution is also shown.</p> <p>Reading this register freezes the Delta_X and Delta_Y register values. Read this register before reading the Delta_X and Delta_Y registers. If Delta_X and Delta_Y are not read before the motion register is read a second time, the data in Delta_X and Delta_Y will be lost.</p> | | | | | | | |
| Notes | Field Name | Description | | | | | | |
| | Motion | Motion since last report or PD 0 = No motion (Default) 1 = Motion occurred, data ready for reading in Delta_X and Delta_Y registers | | | | | | |
| | Reserved | Reserved for future | | | | | | |
| | Reserved | Reserved for future | | | | | | |
| | DYOVF | Motion Delta Y overflow, ΔY buffer has overflowed since last report 0 = no overflow (Default) 1 = Overflow has occurred | | | | | | |
| | DXOVF | Motion Delta X overflow, ΔX buffer has overflowed since last report 0 = no overflow (Default) 1 = Overflow has occurred | | | | | | |
| | Reserved | Reserved for future | | | | | | |
| | Reserved | Reserved for future | | | | | | |
| | RES | Resolution in counts per inch 0 = 800 (Default @ PAN101BXX-208) 1 = 400 (Default @ PAN101BXX-204) | | | | | | |
| 0x03 | Delta_X | | | | | | | |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | X7 | X6 | X5 | X4 | X3 | X2 | X1 | X0 |
| Usage | X movement is counts since last report. Absolute value is determined by resolution. Reading clears the register. Report range -128~+127. | | | | | | | |
| 0x04 | Delta_Y | | | | | | | |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Y7 | Y6 | Y5 | Y4 | Y3 | Y2 | Y1 | Y0 |
| Usage | Y movement is counts since last report. Absolute value is determined by resolution. Reading clears the register. Report range -128~+127. | | | | | | | |

| 0x05 | Operation_Mode | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|--|----------------------------------|-----|---------|--------|--------|--------|--------|------------|------------------------------|----------------------------------|--|--------|--|--------|---|---------|---|--------|--|--------|---|--------|---|--------|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | | | | | | | | | | | | | | | |
| Field | Reserved | XY_enh | RES | Slp_enh | Slp2au | Slp2mu | Slp1mu | Wakeup | | | | | | | | | | | | | | | | | | |
| Usage | <p>Register 0x05 allows the user to change the operation of the sensor. Shown below are the bits, their default values, and optional values.</p> <p>Operation_Mode[4:0] “0xxxx”=Disable sleep mode “10xxx”=Enable sleep mode¹ “11xxx”=Enable sleep mode² “1x100”=Force enter sleep2³ “1x010”=Force enter sleep1³ “1x001”=Force wakeup from sleep mode³</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. Enable sleep mode, but disable automatic entering sleep2 mode, that is, only 2 modes will be used, normal mode and sleep1 mode. After 1 sec not moving during normal mode, the chip will enter sleep1 mode, and keep on sleep1 mode until moving is detected or wakeup is asserted. 2. Enable sleep mode full function, that is 3 modes will be used, normal mode, sleep1 mode and sleep2 mode. After 1 sec not moving during normal mode, chip will enter sleep1 mode, and keep on sleep1 mode until moving is detected or wakeup is asserted. <p>And after 90 sec not moving during sleep1 mode, the chip will enter sleep2 mode, and keep on sleep2 mode until detect moving or force wakeup to normal mode.</p> <table border="1"> <thead> <tr> <th>Mode</th> <th>Sampling rate @3000frame/sec</th> <th>Active duty cycle @3000frame/sec</th> </tr> </thead> <tbody> <tr> <td>Sleep1</td> <td>30/sec</td> <td>20%</td> </tr> <tr> <td>Sleep2</td> <td>3/sec</td> <td>2%</td> </tr> </tbody> </table> <ol style="list-style-type: none"> 3. Only one of these three bits slp2mu_enh, slp1mu_enh, and wakeup can be set to 1 at the same time, others have to be set to 0. After a period of time, the bits, which was set to 1, will be reset to 0 by internal signal. | | | | | | | | Mode | Sampling rate @3000frame/sec | Active duty cycle @3000frame/sec | Sleep1 | 30/sec | 20% | Sleep2 | 3/sec | 2% | | | | | | | | | |
| Mode | Sampling rate @3000frame/sec | Active duty cycle @3000frame/sec | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep1 | 30/sec | 20% | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep2 | 3/sec | 2% | | | | | | | | | | | | | | | | | | | | | | | | |
| Notes | <table border="1"> <thead> <tr> <th>Field Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>Reserved</td> <td>Reserved for future, Please set Reserved= “0” (Default)</td> </tr> <tr> <td>XY_enh</td> <td>XY quadrature output enable/disable 0=disable 1= enable (Default)</td> </tr> <tr> <td>RES</td> <td>Resolution in counts per inch 0 = 800 (Default @ PAN101BXX-208) 1 = 400 (Default @ PAN101BXX-204)</td> </tr> <tr> <td>Slp_enh</td> <td>Sleep mode enable/disable 0 = Disable 1 = Enable (Default)</td> </tr> <tr> <td>Slp2au</td> <td>Automatic enter sleep2 mode enable/disable 0 = Disable 1 = Enable (Default)</td> </tr> <tr> <td>Slp2mu</td> <td>Manual enter sleep2 mode, set “1” will enter sleep2 and this bit will be reset to “0”</td> </tr> <tr> <td>Slp1mu</td> <td>Manual enter sleep1 mode, set “1” will enter sleep2 and this bit will be reset to “0”</td> </tr> <tr> <td>Wakeup</td> <td>Manual wake up from sleep mode, set “1” will enter wakeup and this bit will be reset to “0”</td> </tr> </tbody> </table> | | | | | | | | Field Name | Description | Reserved | Reserved for future, Please set Reserved= “0” (Default) | XY_enh | XY quadrature output enable/disable 0=disable 1= enable (Default) | RES | Resolution in counts per inch 0 = 800 (Default @ PAN101BXX-208) 1 = 400 (Default @ PAN101BXX-204) | Slp_enh | Sleep mode enable/disable 0 = Disable 1 = Enable (Default) | Slp2au | Automatic enter sleep2 mode enable/disable 0 = Disable 1 = Enable (Default) | Slp2mu | Manual enter sleep2 mode, set “1” will enter sleep2 and this bit will be reset to “0” | Slp1mu | Manual enter sleep1 mode, set “1” will enter sleep2 and this bit will be reset to “0” | Wakeup | Manual wake up from sleep mode, set “1” will enter wakeup and this bit will be reset to “0” |
| Field Name | Description | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reserved | Reserved for future, Please set Reserved= “0” (Default) | | | | | | | | | | | | | | | | | | | | | | | | | |
| XY_enh | XY quadrature output enable/disable 0=disable 1= enable (Default) | | | | | | | | | | | | | | | | | | | | | | | | | |
| RES | Resolution in counts per inch 0 = 800 (Default @ PAN101BXX-208) 1 = 400 (Default @ PAN101BXX-204) | | | | | | | | | | | | | | | | | | | | | | | | | |
| Slp_enh | Sleep mode enable/disable 0 = Disable 1 = Enable (Default) | | | | | | | | | | | | | | | | | | | | | | | | | |
| Slp2au | Automatic enter sleep2 mode enable/disable 0 = Disable 1 = Enable (Default) | | | | | | | | | | | | | | | | | | | | | | | | | |
| Slp2mu | Manual enter sleep2 mode, set “1” will enter sleep2 and this bit will be reset to “0” | | | | | | | | | | | | | | | | | | | | | | | | | |
| Slp1mu | Manual enter sleep1 mode, set “1” will enter sleep2 and this bit will be reset to “0” | | | | | | | | | | | | | | | | | | | | | | | | | |
| Wakeup | Manual wake up from sleep mode, set “1” will enter wakeup and this bit will be reset to “0” | | | | | | | | | | | | | | | | | | | | | | | | | |

4. Specifications

Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Unit | Notes |
|------------------|-----------------------|------|-----|------|--|
| T _{STG} | Storage temperature | -40 | 85 | °C | |
| T _A | Operating Temperature | -15 | 55 | °C | |
| | Lead Solder Temp | | 260 | °C | For 10 seconds, 1.6mm below seating plane. |
| V _{DD} | DC supply voltage | -0.5 | 4.0 | V | |
| ESD | | | 2 | kV | All pins, human body model MIL 883 Method 3015 |
| V _{IN} | DC input voltage | -0.5 | 5.5 | V | PD, SDIO, SCLK, XA, XB, YA, YB |

Recommend Operating Condition

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|------------------|---|------|--------|---------------------|----------|--|
| T _A | Operating Temperature | 0 | | 40 | °C | |
| V _{DD} | Power supply voltage | 2.7 | 3.0 | 3.6 | V | |
| V _N | Supply noise | | | 100 | mV | Peak to peak within 0-100 MHz |
| F _{CLK} | Clock Frequency | | 18.432 | 24.576 | MHz | Set by ceramic resonator |
| FR | Frame Rate | | 3000 | 4000 | Frames/s | 4000Frames/s @ F _{CLK} =24.567MHz |
| SCLK | Serial Port Clock Frequency | | | F _{CLK} /4 | MHz | |
| Z | Distance from lens reference plane to surface | 2.1 | 2.2 | 2.3 | mm | Refer to Figure 4. |
| S | Speed | 0 | 16 | | in/sec | |
| A | Acceleration | | | 3.9 | g | |
| R | Resolution | | 400 | 800 | cpi | |

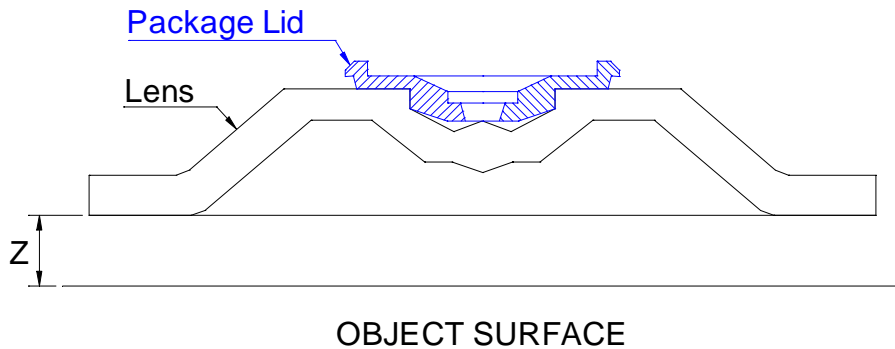


Figure 4. Distance from Lens Reference Plane to Surface

AC Operating Condition

Electrical Characteristics over recommended operating conditions. Typical values at 25 °C, $V_{DD}=3.0$ V

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---------------|--|------|--------|------|------|--|
| t_{PD} | Power Down | | 0.5 | | us | From PD \uparrow . (Refer to Figure 5.) |
| t_{PDW} | PD Pulse Width | 1 | | | us | Pulse width to reset the serial interface. (Refer to Figure 5.) |
| t_{PUPD} | Power Up from PD \downarrow | | | 42.8 | ms | From PD \downarrow to valid quad signals 200usec + 128frames. (Refer to Figure 5.) |
| t_{PU} | Power Up from $V_{DD}\uparrow$ | | | 41.7 | ms | From $V_{DD}\uparrow$ to valid quad signals. 400usec + 124frames. |
| t_{HOLD} | SDIO read hold time | | 3 | | us | Minimum hold time for valid data. (Refer to Figure 14.) |
| $t_{COMPUTE}$ | Data delay after PD \downarrow | 4 | | | ms | After $t_{COMPUTE}$, all registers contain valid data from first image after PD \downarrow . Note that an additional 128 frames for Auto-Exposure (AE) stabilization may be required if mouse movement occurred while PD was high. (Refer to Figure 8.) |
| t_r, t_f | Rise and Fall Times: SDIO | | 500, 5 | | ns | Pull-up 10Kohm (PAN101BOI) |
| | | | 25, 20 | | ns | $C_L = 30$ pf (PAN101BSI) |
| t_r, t_f | Rise and Fall Times: XA, XB, YA, YB | | 500, 5 | | ns | Pull-up 10Kohm (PAN101BOI) |
| | | | 25, 20 | | ns | $C_L = 30$ pf (PAN101BSI) |
| t_r, t_f | Rise and Fall Times: ILED | | 10, 10 | | ns | LED bin:N ; R1=100ohm |

DC Electrical Characteristics

Electrical Characteristics over recommended operating conditions. Typical values at 25 °C, V_{DD} = 3.0 V

| Symbol | Parameter | Min. | Typ. | Max. | Unit | |
|-----------------------------|---|---------------------|------|--------------------|------|--------------------------------------|
| Type: PWR | | | | | | |
| I _{DD} | Supply Current Mouse moving (Normal) | | 15 | | mA | XA, XB, YA, YB, SCLK, SDIO = no load |
| I _{DD} | Supply Current Mouse not moving (sleep1) | | 5 | | mA | |
| I _{DD} | Supply Current Mouse not moving (sleep2) | | 2 | | mA | |
| I _{DDPD} | Supply Current (Power Down) | | 100 | | uA | PD, SCLK, SDIO = high |
| Type: SCLK, SDIO, PD | | | | | | |
| V _{IH} | Input voltage HIGH | 2 | | | | |
| V _{IL} | Input voltage LOW | | | 0.8 | V | |
| V _{OH} | Output voltage HIGH | 0.8 V _{DD} | | | V | @I _{OH} = 3mA (SDIO only) |
| V _{OL} | Output voltage LOW | | | 0.2V _{DD} | V | @I _{OL} = 3mA (SDIO only) |
| Type: OSCIN | | | | | | |
| V _{IH} | Input voltage HIGH | 2 | | | V | When driving from an external source |
| V _{IL} | Input voltage LOW | | | 0.8 | V | When driving from an external source |
| Type: LED | | | | | | |
| V _{OL} | Output voltage LOW | | | 150 | mV | @I _{OL} = 25mA |
| Type: XA, XB, YA, YB | | | | | | |
| V _{OH} | Output voltage HIGH | 0.8 V _{DD} | | | V | @I _{OH} = 3mA |
| V _{OL} | Output voltage LOW | | | 0.2V _{DD} | V | @I _{OL} = 3mA |

5. PD Pin Timing

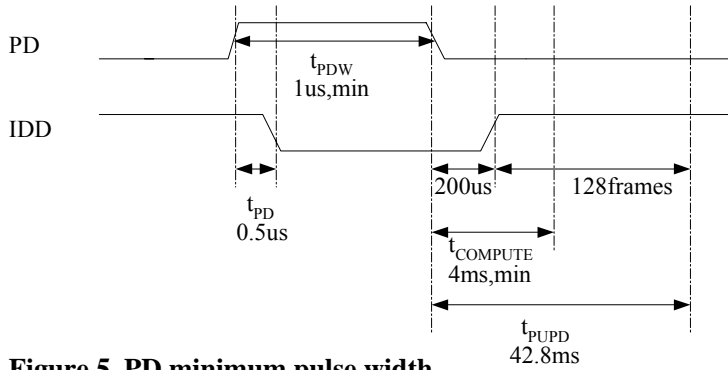


Figure 5. PD minimum pulse width

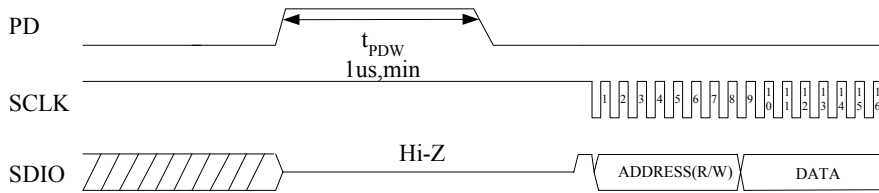


Figure 6. Forcing PAN101B SDIO line to the Hi-Z state

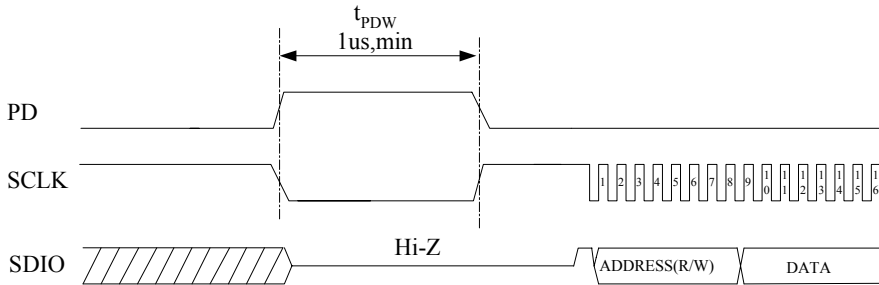


Figure 7. Forcing PAN101B full chip reset and SDIO line to the Hi-Z state

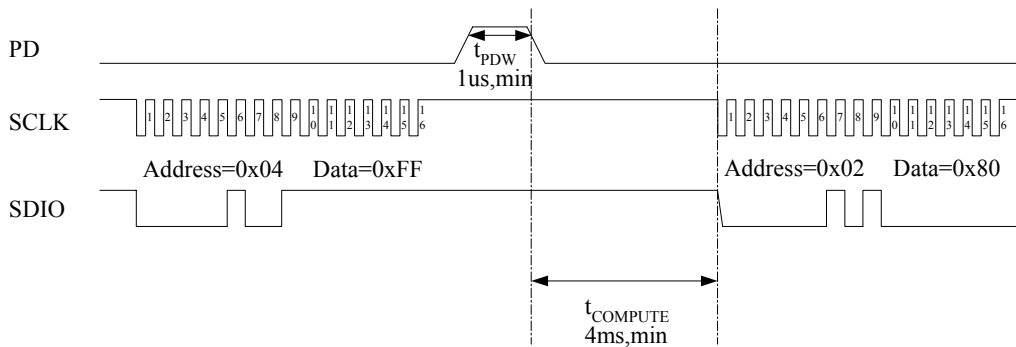


Figure 8. Read the motion data from PAN101B

6. Quadrature Mode

The quadrature state of the PAN101B tells mouse controller which direction the mouse is moving in. The output format is two channels quadrature (X and Y direction), which emulates encoder phototransistors. The DSP generates the Δx and Δy relative displacement values that are converted into two channel quadrature signals. PAN101B support 400cpi, 800cpi, two types of resolution. The following diagrams show the timing for positive X motion, to the right or positive Y motion, up.

6.1 Quadrature Output Timing

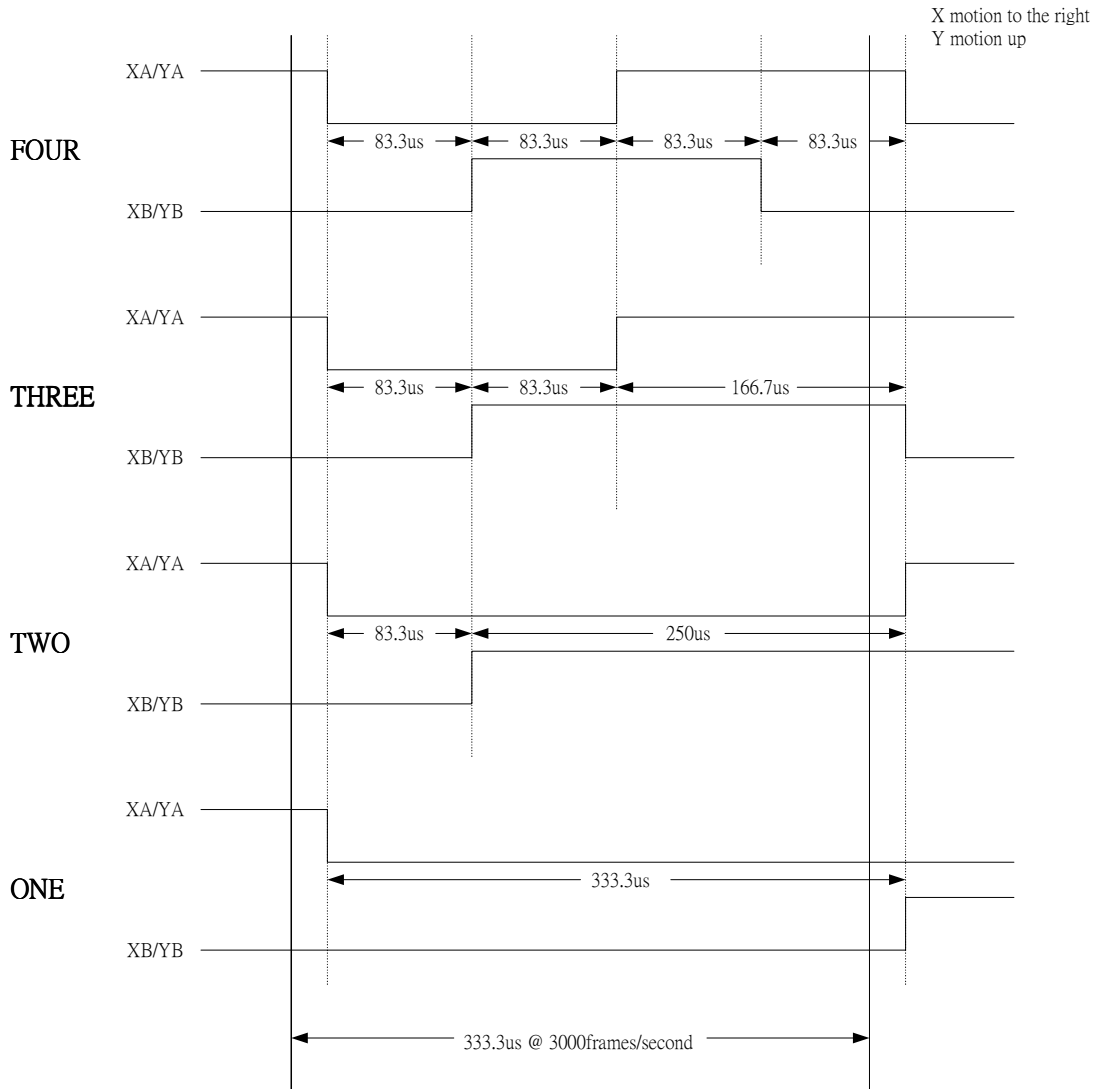


Figure 9. Quadrature Output Timing

6.2 Quadrature Output State Machine

The following state machine shows the states of the quadrature output pins. The three things to note are that state 0 is entered after a power on reset. While the PD pin is asserted, the state machine is halted. Once PD is de-asserted, the state machine picks up from where it left off. During times of mouse no movement will entry power saving mode, until mouse was moved.

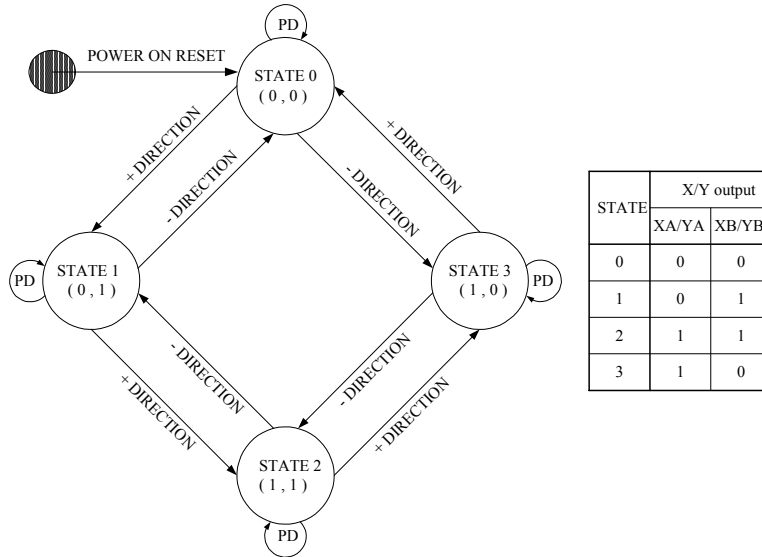


Figure 10. State Machine

6.3 Quadrature Output Waveform

The following diagrams show the waveform of the two channel quadrature outputs. If the X, Y is motionless, the (XA, XB), (YA, YB) will keep in final state. Each state change (ex. STATE2 → STATE3) is one count.

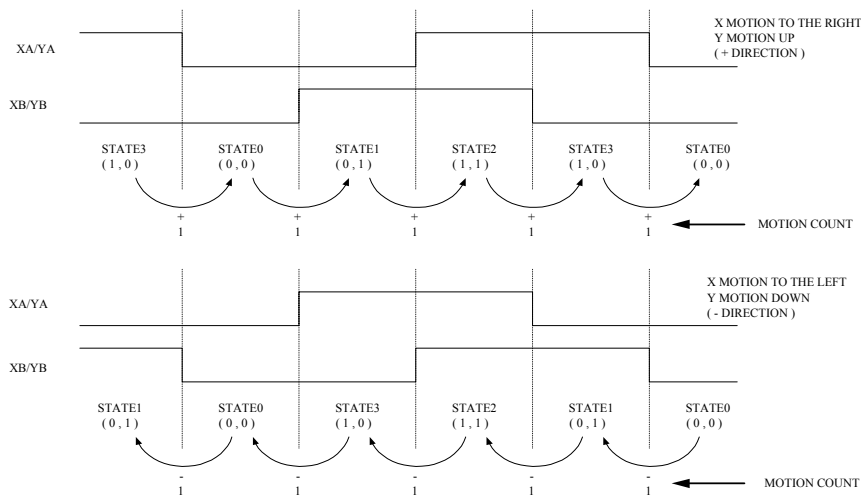


Figure 11. Quadrature Output Waveform

7. Serial Interface

The synchronous serial port is used to set and read parameters in the PAN101B, and can be used to read out the motion information instead of the quadrature data pins.

SCLK: The serial clock line. It is always generated by the host micro-controller.

SDIO: The serial data line used for write and read data.

PD: A third line is sometimes involved. PD (Power Down pin) is usually used to place the PAN101B in a low power mode to meet USB suspend specification. PD can also be used to force re-synchronization between the micro-controller and the PAN101B in case of an error.

7.1 Transmission Protocol

The transmission protocol is a two-wire link, half duplex protocol between the micro-controller and PAN101B. All data changes on SDIO are initiated by the falling edge on SCLK. The host micro-controller always initiates communication; the PAN101B never initiates data transfers.

The transmission protocol consists of the two operation modes:

- Write Operation.
- Read Operation.

Both of the two operation modes consist of two bytes. The first byte contains the address (seven bits) and has a bit7 as its MSB to indicate data direction. The second byte contains the data.

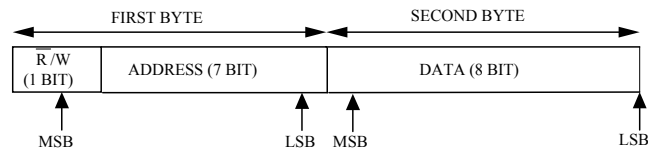


Figure 12. Transmission Protocol

7.1.1 Write Operation

A write operation, which means that data is going from the micro-controller to the PAN101B, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address (seven bits) and has a “1” as its MSB to indicate data direction. The second byte contains the data. The transfer is synchronized by SCLK. The micro-controller changes SDIO on falling edges of SCLK. The PAN101B reads SDIO on rising edges of SCLK.

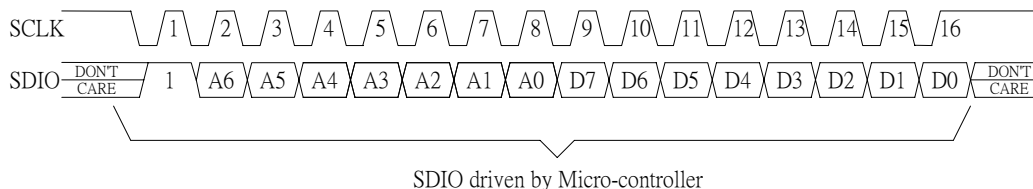


Figure 13. Write Operation

7.1.2 Read Operation

A read operation, which means that data is going from the PAN101B to the micro-controller, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address, is written by the micro-controller, and has a “0” as its MSB to indicate data direction. The second byte contains the data and is driven by the PAN101B. The transfer is synchronized by SCLK. SDIO is changed on falling edges of SCLK and read on every rising edge of SCLK. The micro-controller must go to a high Z state after the last address data bit. The PAN101B will go to the high Z state after the last data bit.

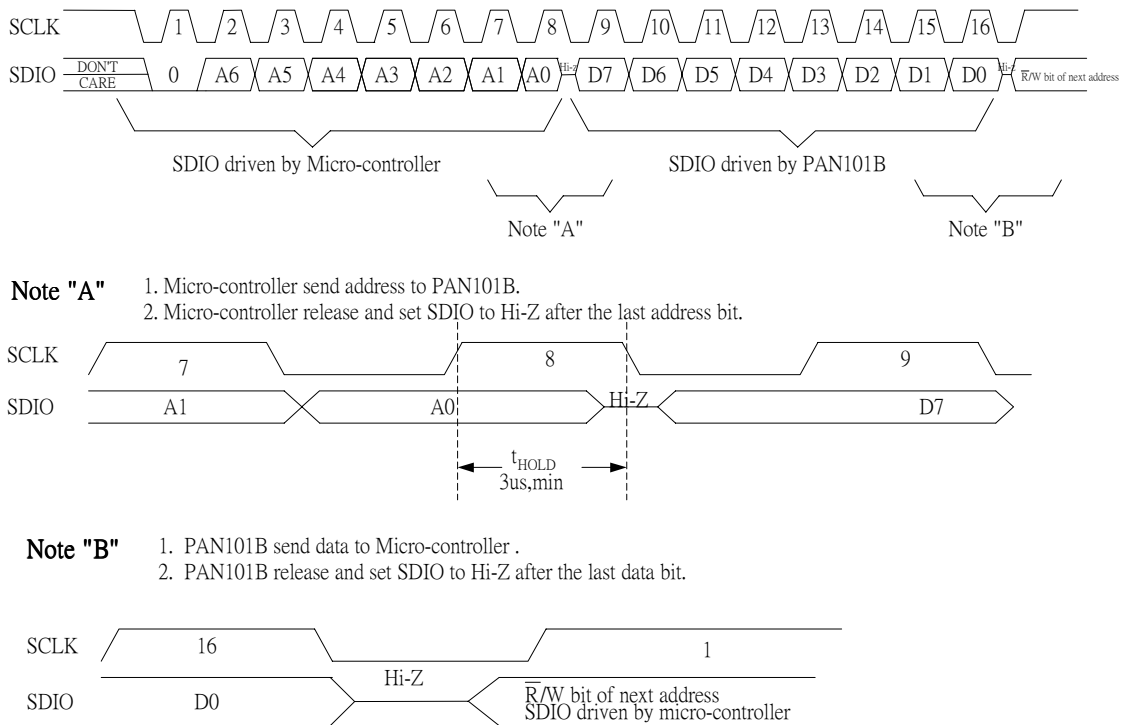


Figure 14. Read Operation

7.2 Re-Synchronous Serial Interface

There are times when the SDIO line from the PAN101B should be in the Hi-Z state. If the microprocessor has completed a write to the PAN101B, the SDIO line is Hi-Z, since the SDIO pin is still configured as an input. However, if the last operation from the microprocessor was a read, the PAN101B will hold the D0 state on SDIO until a rising edge of SCLK. To place the SDIO pin into the Hi-Z state, first raise the PD pin, and then toggle the SCLK line from high to low to high. The SDIO line will now be in the Hi-Z state. The PAN101B and the micro-controller might get out of synchronization due to following condition.

7.2.1 USB suspend

Termination of a transmission by the micro-controller may sometimes be required (for example, due to a USB suspend interrupt during a read operation). To accomplish this the micro-controller should raise PD. The PAN101B will not write to any register and will reset the serial port (but nothing else) and be prepared for the beginning of future transmissions after PD goes low.

7.2.2 Firmware flaws error, or others error

The PAN101B and the micro-controller might get out of synchronization due to micro-controller firmware flaws. The PD pin can stay high, with the PAN101B in the shutdown state, or the PD pin can be lowered, returning the PAN101B to normal operation.

If the microprocessor and the PAN101B get out of sync, then the data either written or read from the registers will be incorrect. In such a case, an easy way to solve this is to raise PD to re-sync the parts after an incorrect read. The PAN101B will reset the serial port but will not reset the registers and be prepared for the beginning of a new transmission

7.2.3 Power on problem

The problem occurs if the PAN101B powers up before the microprocessor sets the SCLK and SDIO lines to be output.

7.2.4 ESD events

The PAN101B and the micro-controller might get out of synchronization due to ESD events.

If the PAN101B and the micro-controller might get out of synchronization due to power on problem or ESD events. An easy way to solve this is to reset PAN101B.

Power on reset to resync PAN101B
 => Reset full chip and SDIO line set to Hi-Z state)

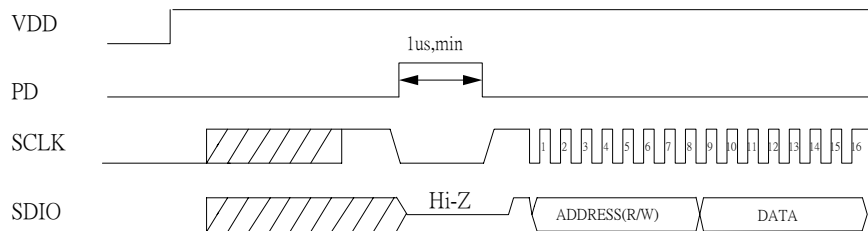


Figure 15. Power on reset to resync. PAN101B

7.3 Collision detection on SDIO

The only time that the PAN101B drives the SDIO line is during a READ operation. To avoid data collisions, the micro-controller should release SDIO before the falling edge of SCLK after the last address bit. The PAN101B begins to drive SDIO after the next falling edge of SCLK. The PAN101B release SDIO of the rising SCLK edge after the last data bit. The micro-controller can begin driving SDIO any time after that. In order to maintain low power consumption in normal operation or when the PD pin is pulled high, the micro-controller should not leave SDIO floating until the next transmission (although that will not cause any communication difficulties).

7.4 Error detection and recovery

1. The micro-controller can verify success of write operations by issuing a read command to the same address and comparing written data to read data.
2. The micro-controller can verify the synchronization of the serial port by periodically reading the product ID register.

8. Referencing application circuit

8.1 Recommended typical application using serial interface

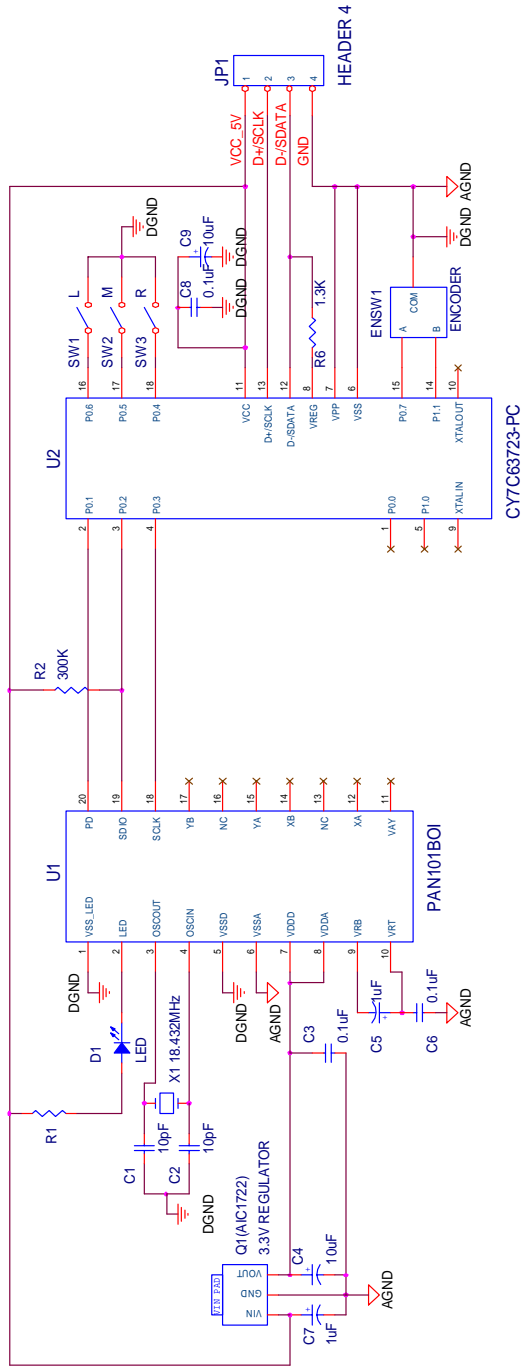


Figure 16. Application circuit using serial interface with PAN101BOI

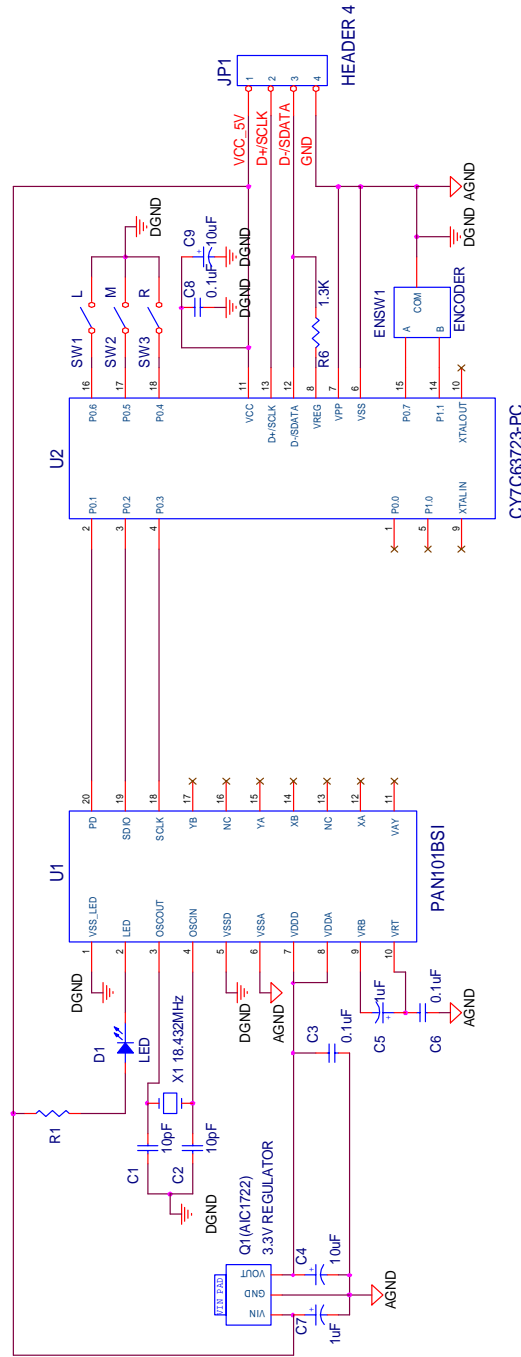


Figure 17. Application circuit using serial interface with PAN101BSI

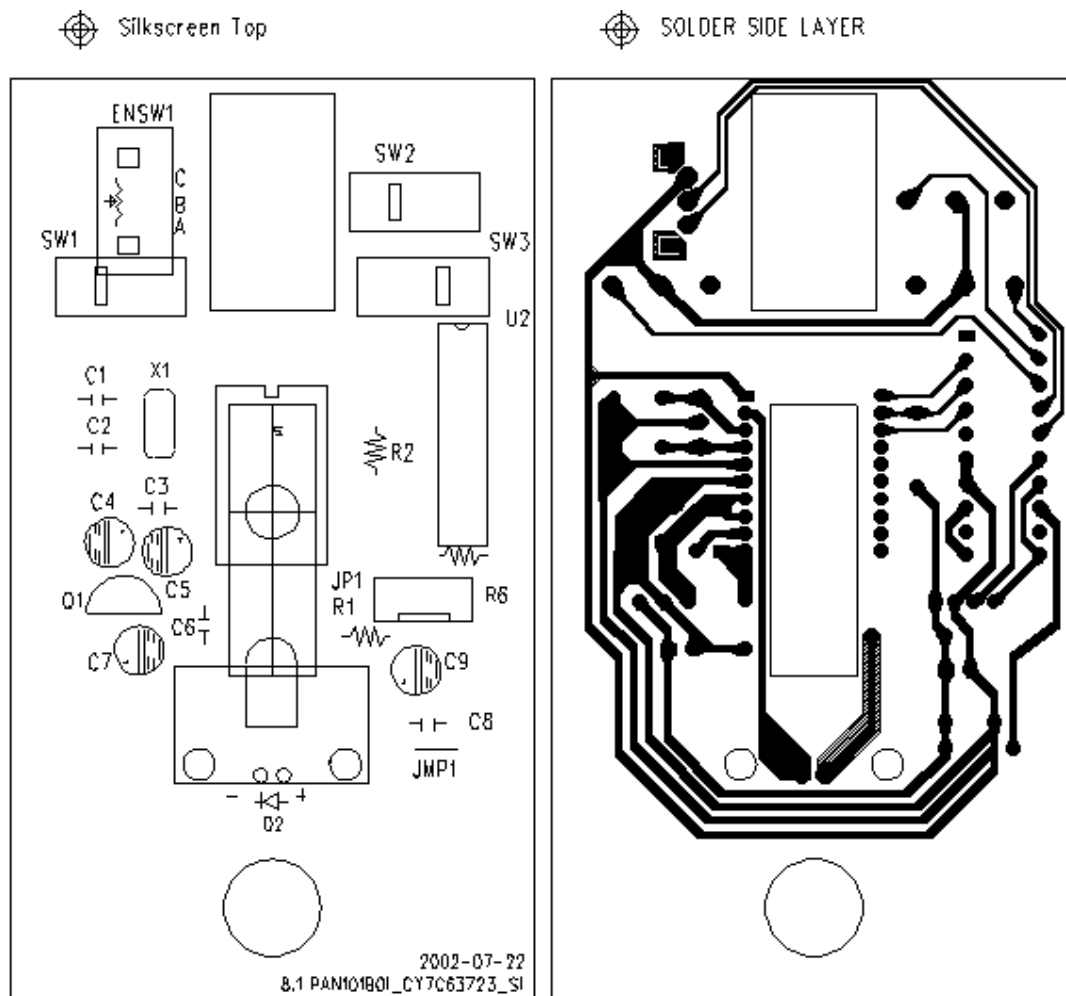


Figure 18. Example printed circuit board layout. (PAN101BOI V.S CY7C63723-PC)

8.2 Application circuit using quadrature output pins

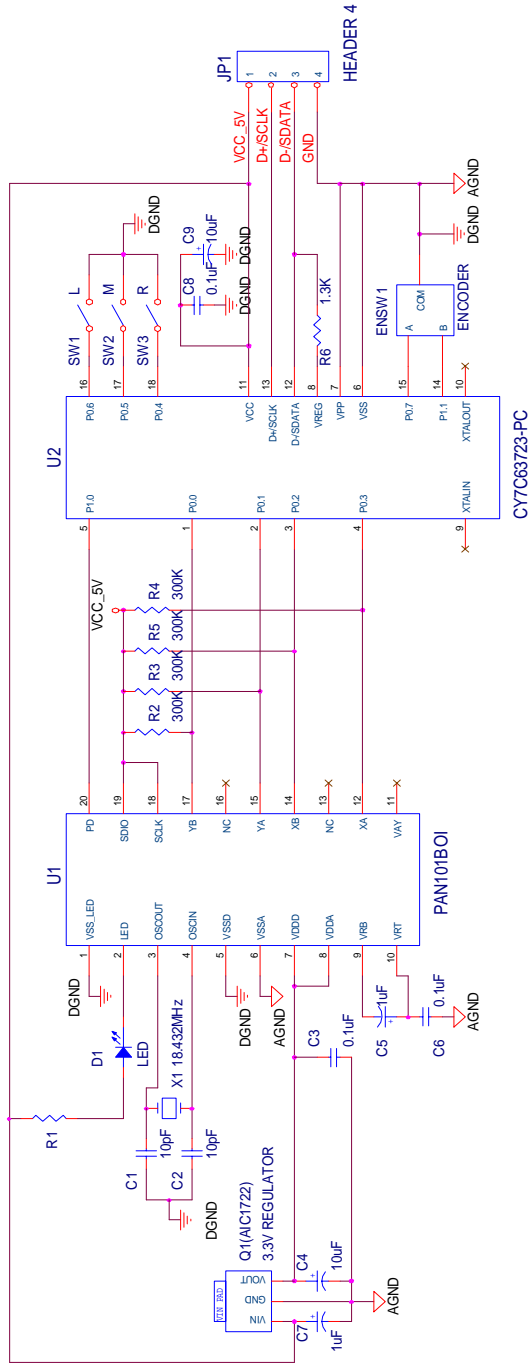


Figure 19. Application circuit using quadrature output pins with PAN101BOI

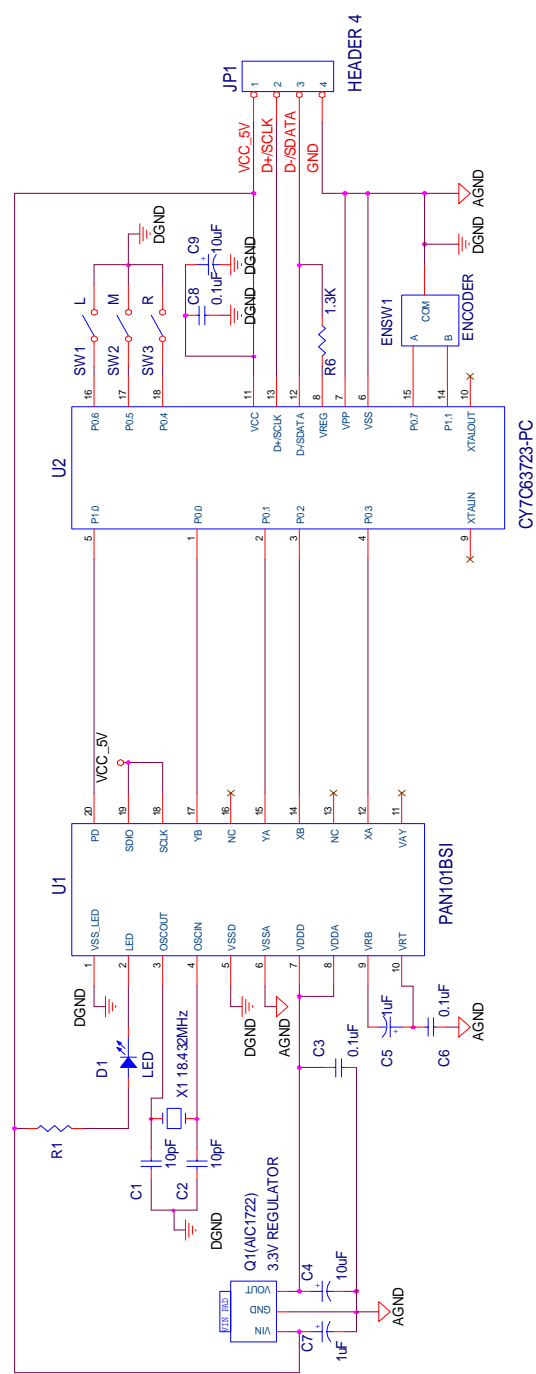


Figure 20. Application circuit using quadrature output pins with PAN101BSI

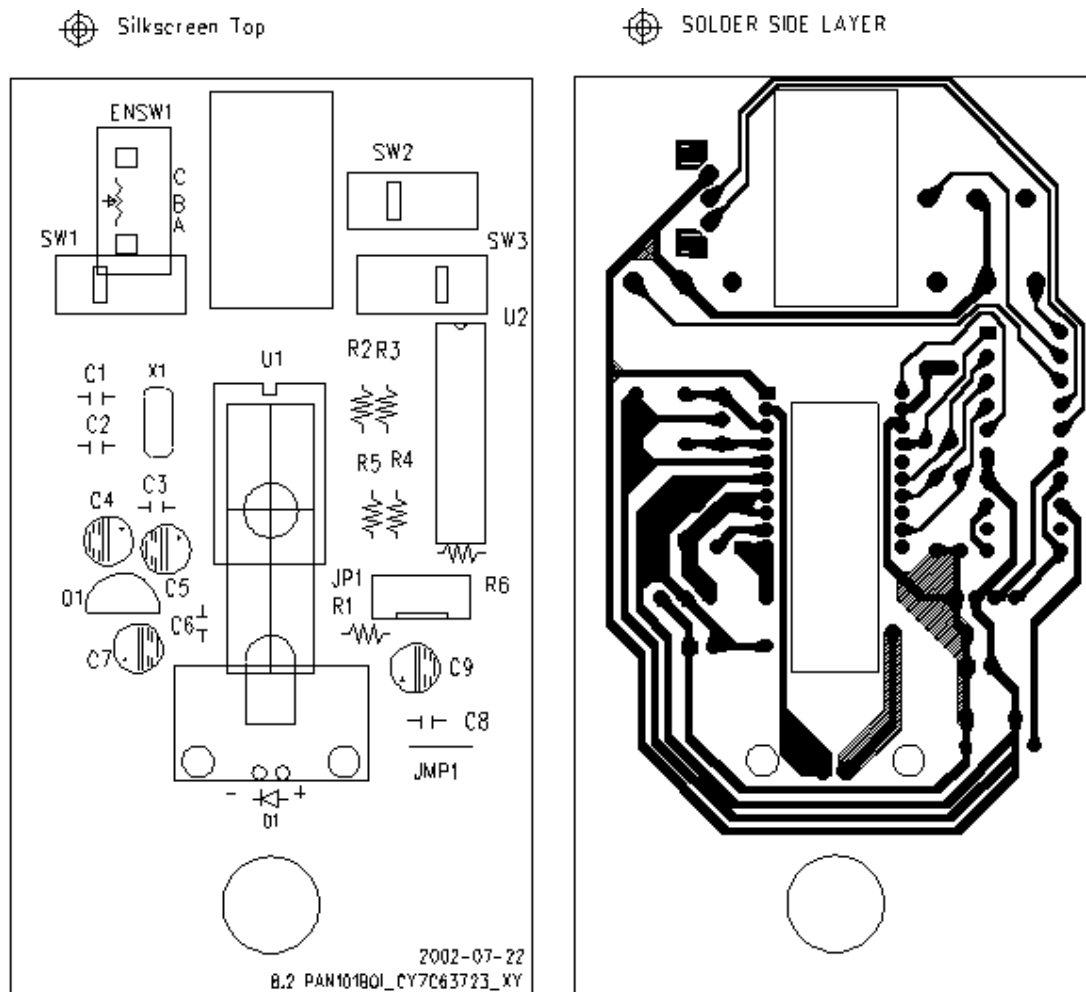


Figure 21. Example printed circuit board layout. (PAN101BOI V.S CY7C63723-PC)

8.3 Typical application for PS/2 interface

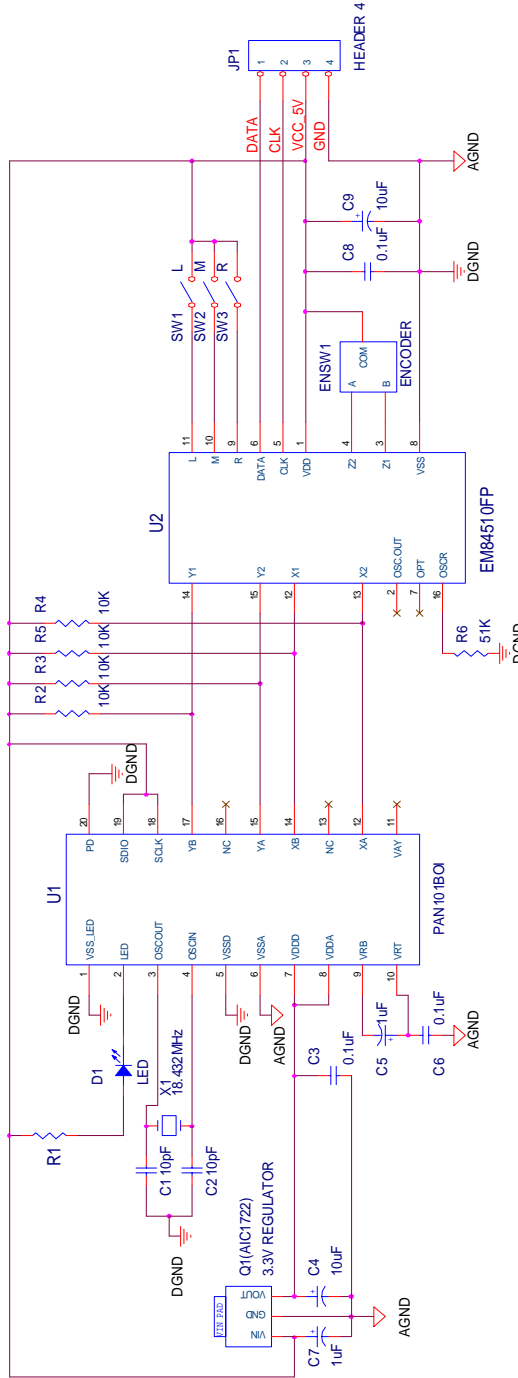


Figure 22. Application circuit using PS/2 interface with PAN101BOI

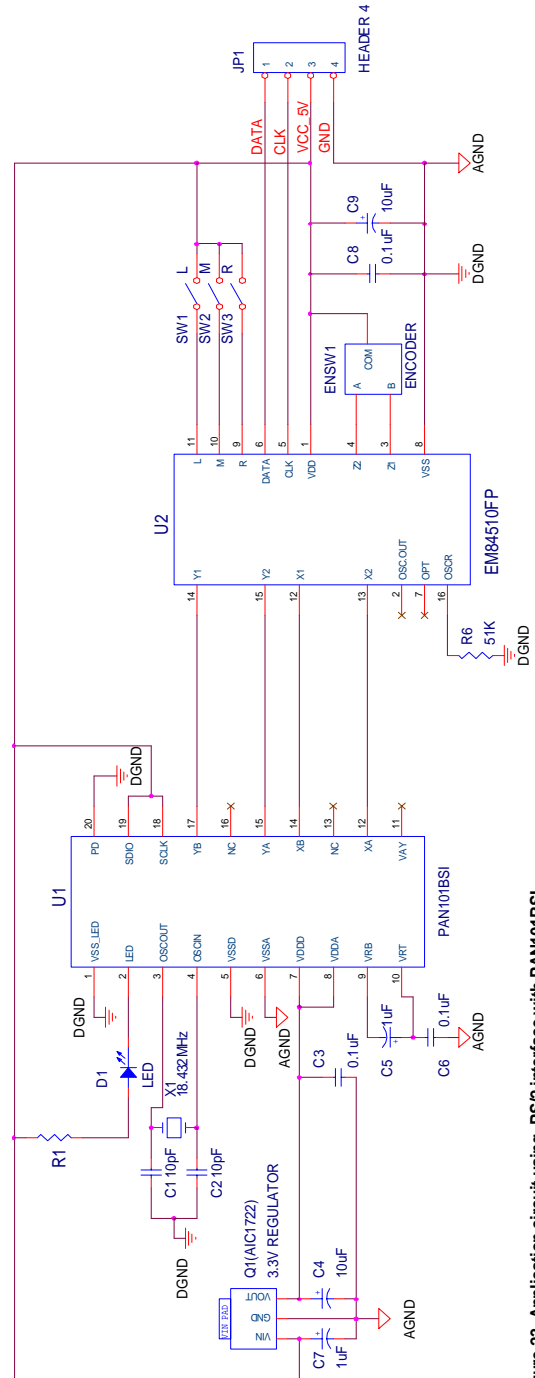


Figure 23. Application circuit using PS/2 interface with PAN101BSI

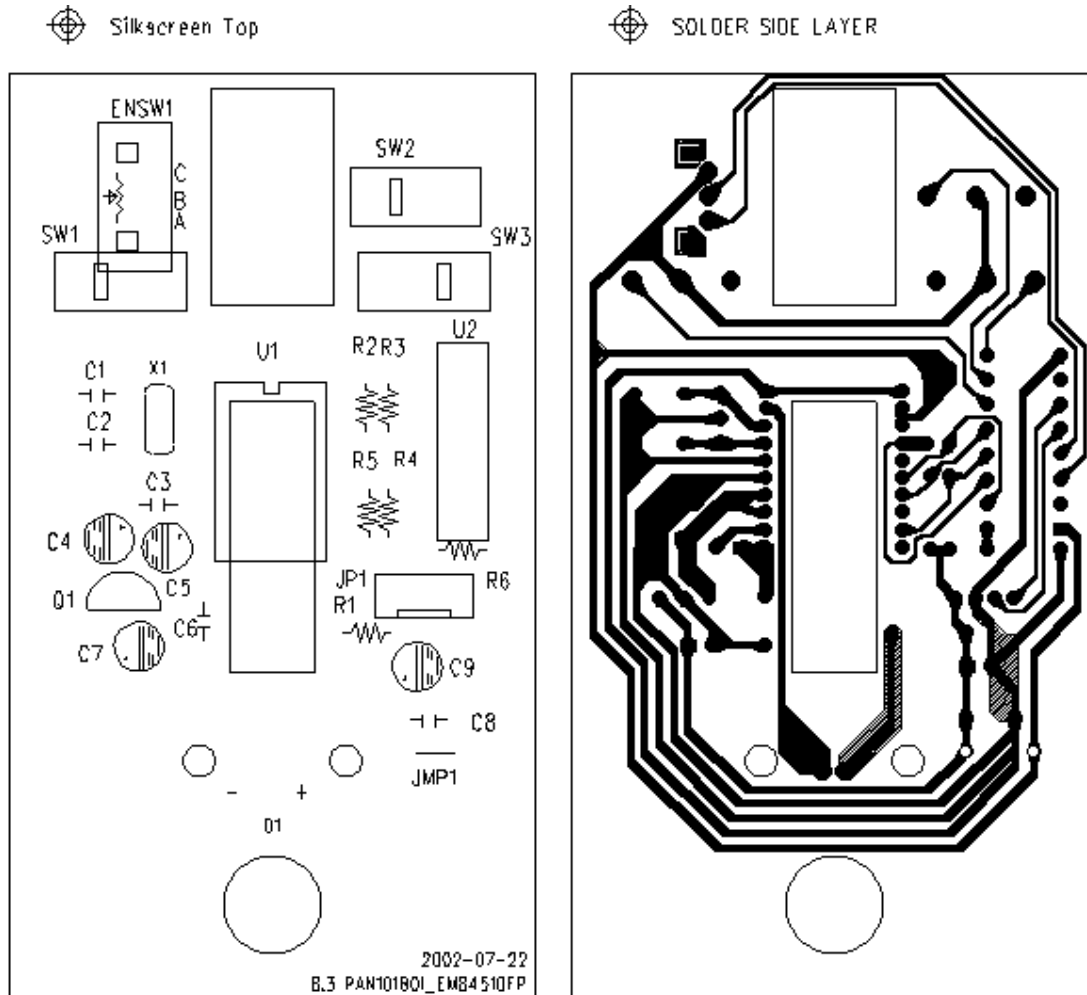


Figure 24. Example printed circuit board layout. (PAN101BOI V.S EM8451QFP)

8.4 PCB layout consideration

1. Caps for pins 9, 10 **MUST** have trace lengths **LESS** than **5mm**.
2. The ground wires of pin1(VSS_LED), pin5(VSSD), pin6(VSSA) must be separated from PS2/USB connector ground node in PCB layout.
3. VSS_LED and VSSD must have trace lengths less than 100mm, VSSA must have trace lengths less than 80mm, and typical trace width is 30mil.
4. The trace lengths of OSCOUT, OSCIN must less than 6mm.

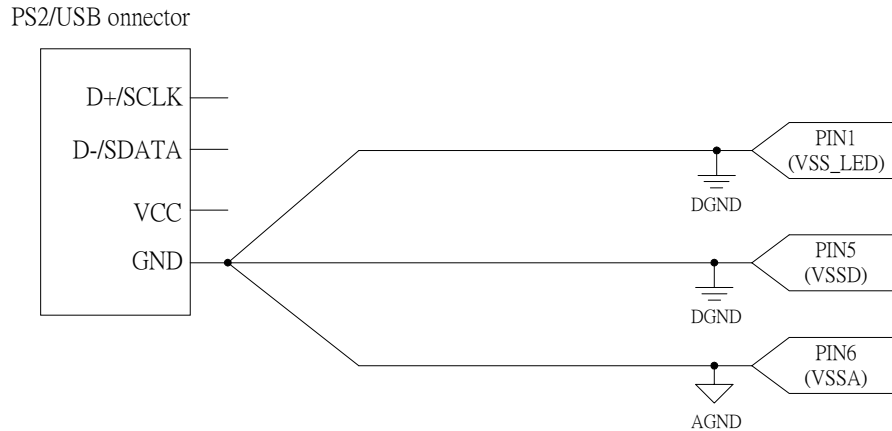


Figure 25. PCB layout consideration

8.5 Recommended value for R1

Radiometric intensity of LED
Bin limits (mW/Sr at 20mA)

| Bin | Min | Max |
|-----|------|------|
| N | 14.7 | 17.7 |
| P | 17.7 | 21.2 |
| Q | 21.2 | 25.4 |
| R | 25.4 | 30.5 |
| S | 30.5 | 36.6 |
| T | 36.6 | 43.9 |

Note: Tolerance for each bin will be $\pm 15\%$

@5V:

| LED bin | N | P | Q | R | S | T |
|----------------|-----|-----|-----|-----|-----|-----|
| R1 value (ohm) | 100 | 100 | 100 | 120 | 120 | 120 |

Figure 26. Recommended value for R1

9. Package Information

9.1 Package Outline Drawing

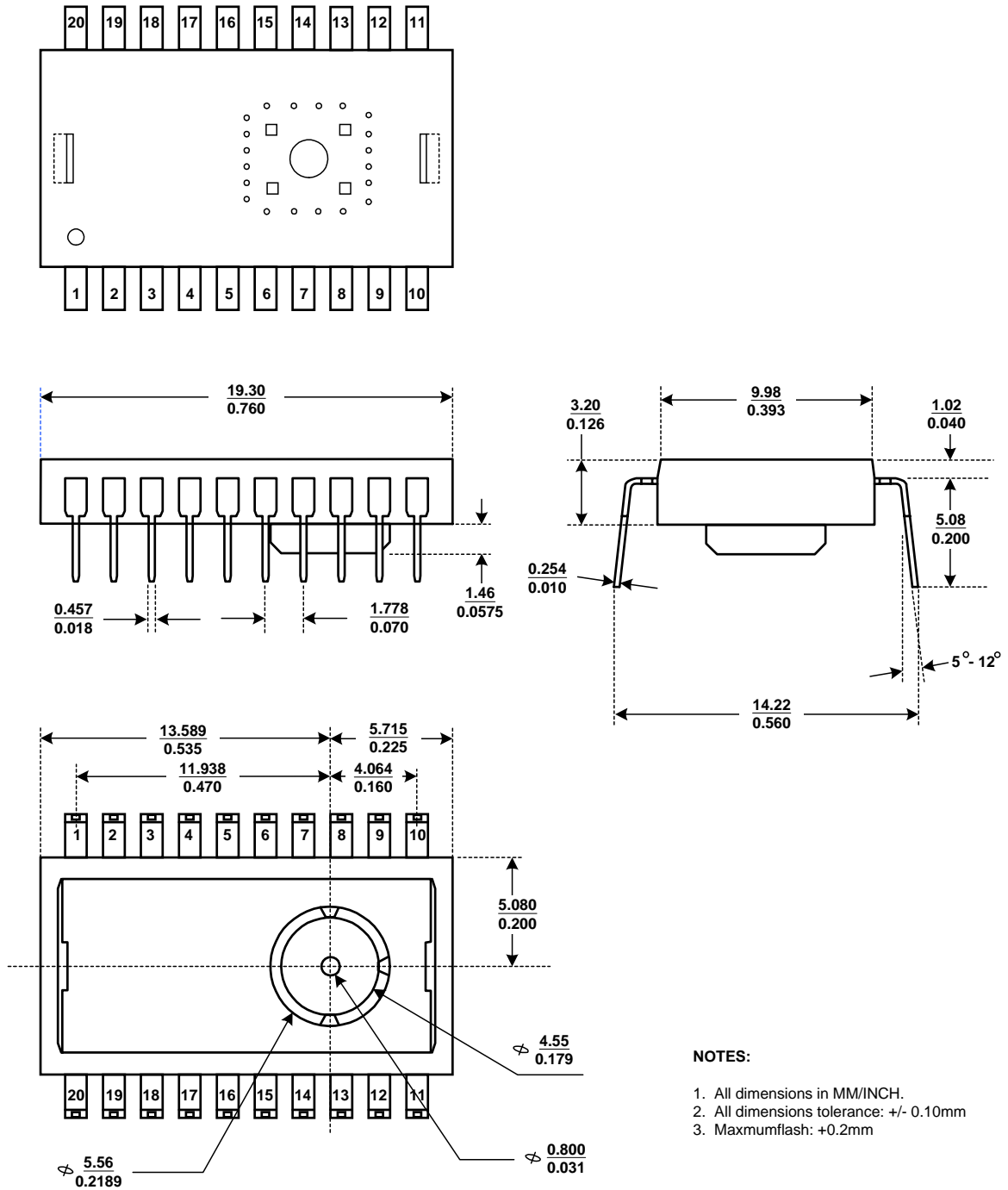


Figure 27. Package Outline Drawing

9.2 Recommended PCB Mechanical Cutouts and Spacing

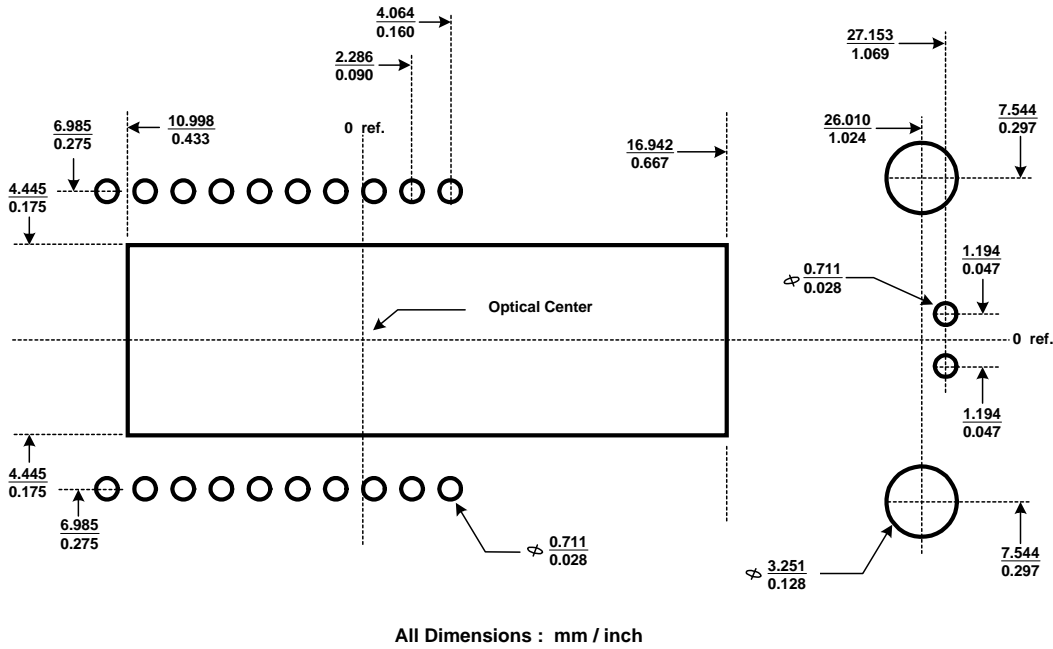


Figure 28. Recommended PCB Mechanical Cutouts and Spacing

10. Update history

| Version | Update | Date |
|---------|---|------------|
| V1.0 | Creation, 1 st version | 07/02/2002 |
| V1.1 | 8.4 PCB layout consideration Figure 27. Package Outline Drawing | 08/29/2002 |
| V1.2 | 4. Specifications - DC Electrical Characteristics Figure 27. Package Outline Drawing | 10/02/2002 |
| V1.3 | 3.2 Register descriptions 8.4 PCB layout consideration | 10/14/2002 |
| V1.4 | Figure 25. PCB layout consideration Figure 27. Package Outline Drawing | 02/10/2003 |
| | | |