ATA Flash Disk Controller

SST55LD017A / SST55LD017B / SST55LD017C

EOL Product Data Sheet

FEATURES:

- **Industry Standard ATA/IDE Bus Interface**
  - Host Interface: 8 or 16 bit access
  - Support up to PIO Mode-4
- **Interface for standard NAND Flash Media**
  - Flash Media Interface: 8 bit access
  - Up to 1 Gbit flash media components
  - SST55LD017A:
    - supports up to 5 flash media devices directly for 128 MB maximum capacity
  - SST55LD017B/SST55LD017C:
    - supports up to 5 flash media devices directly for 640 MB maximum capacity
    - supports up to 16 flash media devices with external decoder for 2 GB maximum capacity
- **Low power, 3.3V core operation**
- **5.0V or 3.3V host interface through V_{DDQ} pins**
- **Low current operation:**
  - Active mode: 25 mA/35 mA (3.3V/5.0V) (typical)
  - Sleep mode: 40 µA/50 µA (3.3V/5.0V) (typical)
- **Power Management Unit**
  - Immediate disabling of unused circuitry
- **20 Byte Unique ID for Enhanced Security**
  - Factory Set 10 Byte Unique ID
  - User Programmable 10 Byte ID
- **Pre-programmed Embedded Firmware**
  - Performs self-initialization on first system power-up
  - Executes industry standard ATA/IDE commands
  - Implements wear-leveling algorithms to substantially increase the longevity of flash media
  - Embedded Flash File System
  - Built-in ECC corrects up to 3 random 12-bit symbols of error per 512 Byte sector
- **Internal or External System Clock Option**
- **Write-Protect (WP_PD#) pin for preventing data overwrites**
- **Fast Sustained Read Performance**
  - Up to 5.0 MB/sec
- **Fast Sustained Write Performance (Host to Flash)**
  - SST55LD017A supports up to 1.2MB/sec
  - SST55LD017B supports up to 2.4MB/sec
  - SST55LD017C supports up to 4.0MB/sec
- **Multi-tasking Technology enables Fast Sustained Write Performance**
- **Support for Both Commercial and Industrial Temperature Ranges**
  - 0°C to 70°C for operating commercial
  - -40°C to +85°C for operating industrial
- **100-lead TQFP package**

PRODUCT DESCRIPTION

SST's ATA flash disk controller is the heart of a high-performance, flash media-based data storage system. The ATA flash disk controller recognizes the control, address, and data signals on the ATA/IDE bus and translates them into memory accesses to the standard NAND-type flash media. This technology suits solid state mass storage applications offering new, expanded functionality while enabling smaller, low power consuming, and lighter designs.

The ATA/IDE interface is widely used in such products as portable and desktop computers, digital cameras, music players, handheld data collection scanners, PDAs, handy terminals, personal communicators, audio recorders, monitoring devices, and set-top boxes.

Utilizing SST's proprietary SuperFlash embedded memory technology, The ATA flash disk controller is preprogrammed with an embedded flash file system which, upon power-up, recognizes the flash media devices and performs all the necessary handshaking routines for flash media support. This enables the product manufacturer a completely seamless integration of flash drive into an embedded design. The ATA flash disk controller integrates an on-chip clock circuitry and Serial Communication Interface (SCI) for system reset and user customization.

The SST55LD017A is a standard performance ATA disk controller supporting capacities up to 128 MB. SST55LD017B is a high-performance ATA disk controller with sustained write performance up to 2.4 MB/sec. SST55LD017C is a super high-performance ATA disk controller with sustained write performance up to 4.0 MB/sec. Both the SST55LD017B and SST55LD017C can support up to 5 flash media devices directly for a maximum capacity of 640 MB. By using an external decoder, the SST55LD017B and SST55LD017C can support up to 16 flash media devices for the equivalent capacity of 2 GB.

Users can select either an internal or external system clock option for optimal performance vs. the supply current.

The ATA flash disk controller comes packaged in an industry standard 100-lead TQFP package for easy integration into an SMT manufacturing process. The ATA flash disk controller also comes preprogrammed with a 10-byte unique serial ID. For even greater system security and data protection, the user has the option of programming an additional 10 Bytes of ID space to create a unique, 20 Byte ID. The controller also offers a WP_PD# pin to protect data stored on flash media from unauthorized overwrites.

EOL Product Data Sheet

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1.0 GENERAL DESCRIPTION

The SST's ATA flash disk controller contains a microcontroller and embedded flash file system integrated in a 100-lead TQFP package. Refer to Figure 2-1 for SST's ATA flash disk controller block diagram. The controller interfaces with the host system allowing data to be written to and read from the flash media.

1.1 Performance-optimized ATA Flash Disk Controller

The heart of the Flash Drive is the ATA flash disk controller which translates standard ATA signals into flash media data and control signals. The following components contribute to the ATA flash disk controller's operation.

1.1.1 Microcontroller Unit (MCU)

The MCU translates ATA/IDE commands into data and control signals required for flash media operation.

1.1.2 Internal Direct Memory Access (DMA)

The ATA flash disk controller uses Internal DMA allowing instant data transfer from buffer to flash media. This implementation eliminates microcontroller overhead associated with traditional, firmware-based approach, thereby increasing the data transfer rate.

1.1.3 Power Management Unit (PMU)

Power Management Unit controls the power consumption of the ATA flash disk controller. The PMU dramatically reduces the power consumption of ATA flash disk controller by putting the part of the circuitry that is not in operation into sleep mode.

1.1.4 SRAM Buffer

A key contributor to the ATA flash disk controller performance is an SRAM buffer. The buffer optimizes host's data transfer to and from flash media.

1.1.5 Embedded Flash File System

Embedded Flash File System is an integral part of the SST's ATA flash disk controller. It contains MCU Firmware that performs the following tasks:

1. Translates host side signals into flash media Writes and Reads.
2. Provides flash media wear leveling to spread the Flash writes across all unused memory address space to increase the longevity of flash media.
3. Keeps track of data file structures.

1.1.6 Error Correction Code (ECC)

The SST's ATA flash disk controller utilizes 72-bit Reed-Solomon Error Detection Code (EDC) and Error Correction Code (ECC), which provides following error immunity for each 512-Byte block of data:

1. Corrects up to three random 12-bit symbol errors
2. Corrects single bursts up to 25 bits
3. Detects single bursts up to 61 bits and double bursts up to 15 bits
4. Detects up to six random 12-bit symbol errors.

1.1.7 Serial Communication Interface (SCI)

The Serial Communication Interface is designed to enable the user to restart the self-initialization process and to customize the Drive Identification Information.

1.1.8 Multi-tasking Technology

Multi-tasking technology enables fast, sustained write performance by allowing concurrent Read, Program, and Erase operations to multiple flash media devices.

2.0 FUNCTIONAL BLOCKS

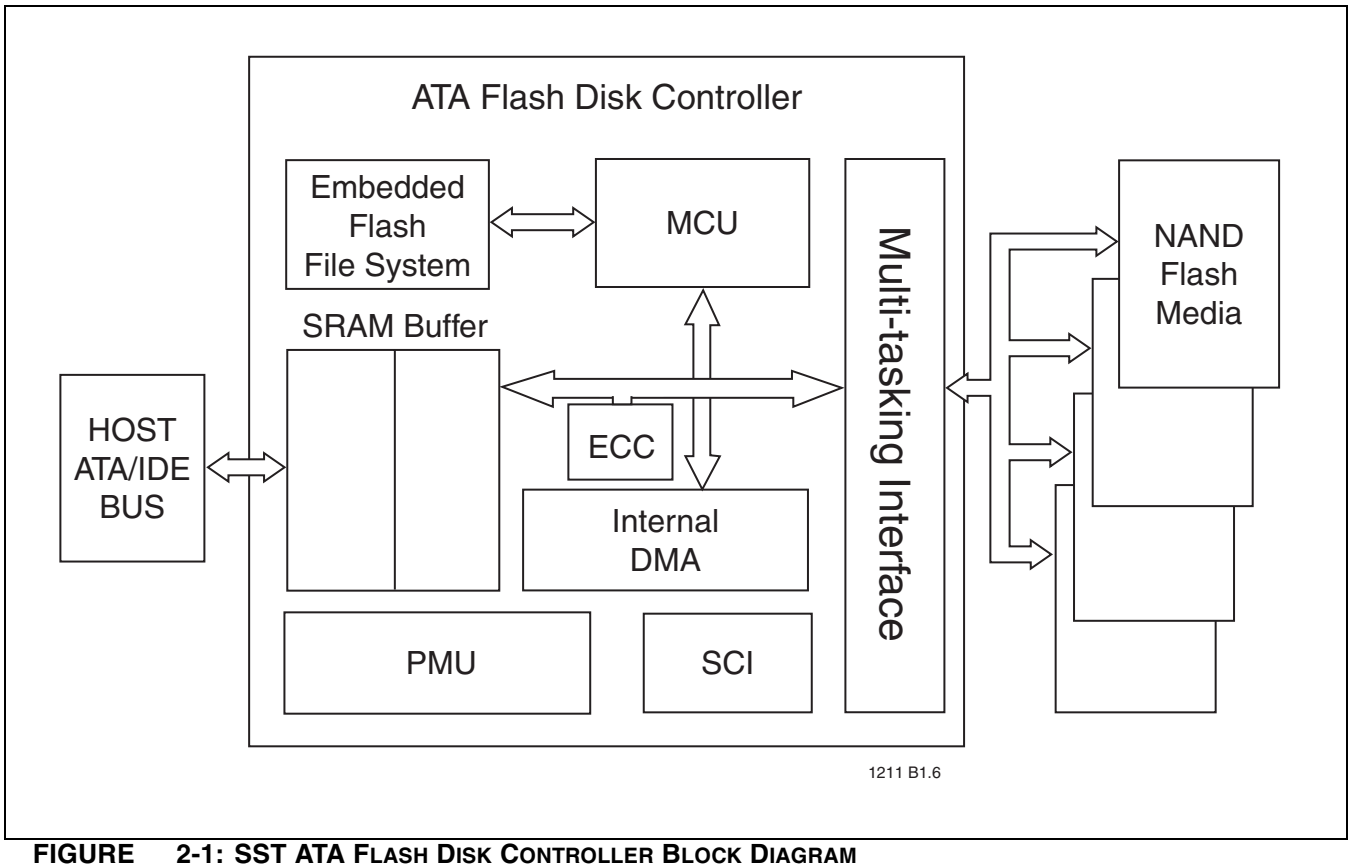


FIGURE 2-1: SST ATA FLASH DISK CONTROLLER BLOCK DIAGRAM

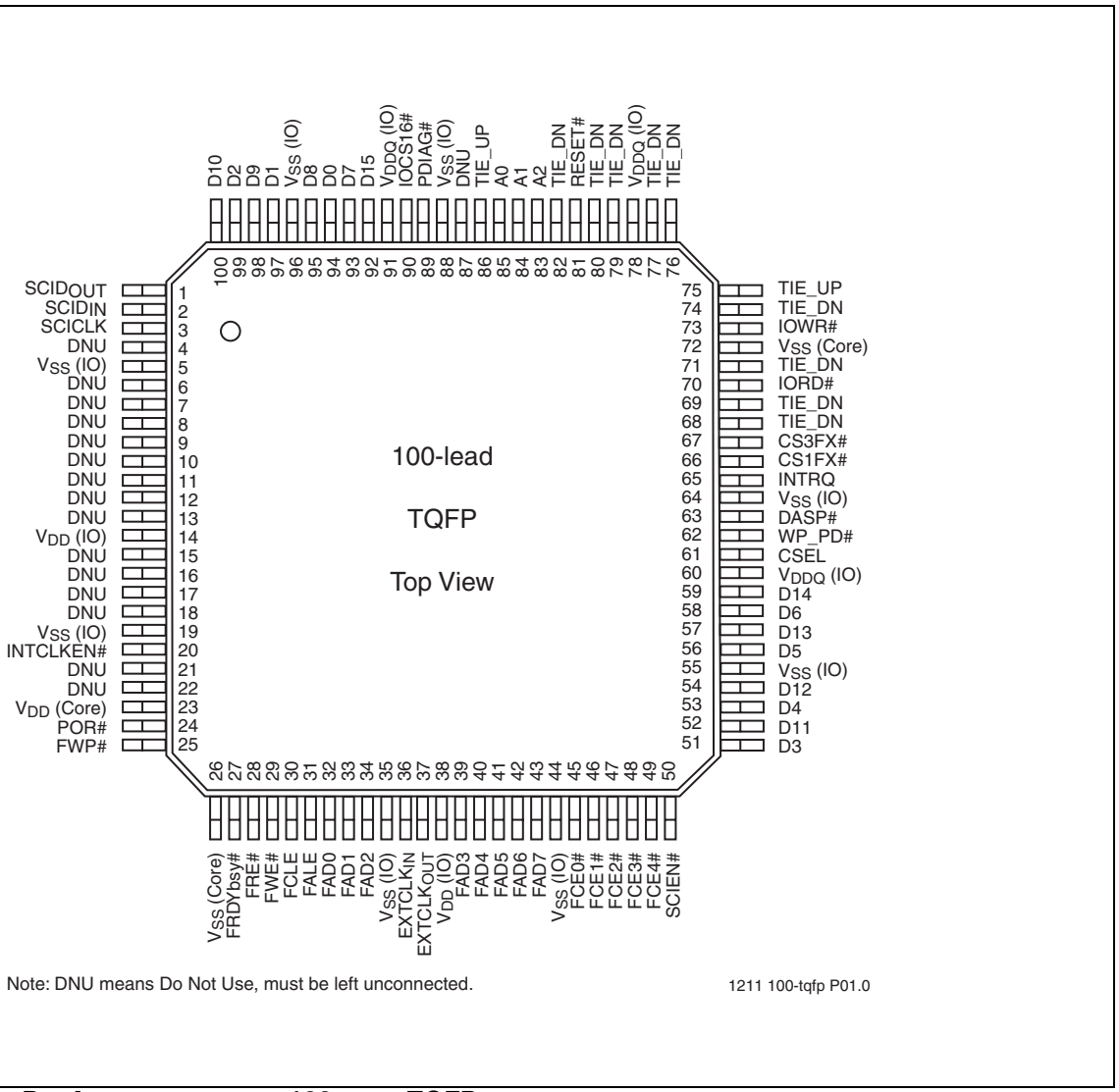
EOL Product Data Sheet

3.0 PIN ASSIGNMENTS

The signal/pin assignments are listed in Table 3-1. Low active signals have a "#" suffix. Pin types are Input, Output or Input/Output. Section 11.0 defines the DC characteristics for all input and output type structures.

The ATA flash disk controller functions in ATA Mode, which is compatible with IDE hard disk drives.

Table 3-2 to Table 3-6 describe the I/O signals. Signals whose source is the host are designated as inputs while signals that the ATA flash disk controller sources are outputs. Refer to Section 11.0 for definitions of Input and Output types.



Note: DNU means Do Not Use, must be left unconnected.

1211 100-tqfp P01.0

FIGURE 3-1: PIN ASSIGNMENTS FOR 100-LEAD TQFP

TABLE 3-1: PIN ASSIGNMENTS

Pin No.	Signal Name	Pin Type	I/O Type[1]
1	$SCID_{OUT}$	O	O1
2	$SCID_{IN}$	I	I5Z
3	SCICLK	I	I5Z
4	DNU[2]		
5	V_{SS} (IO)		
6	DNU		
7	DNU		
8	DNU		
9	DNU		
10	DNU		
11	DNU		
12	DNU		
13	DNU		
14	V_{DD} (IO)		
15	DNU		
16	DNU		
17	DNU		
18	DNU		
19	V_{SS} (IO)		
20	INTCLKEN#	I	I5U
21	DNU		
22	DNU		
23	V_{DD} (Core)		
24	POR#	I	I5Z
25	FWP#	O	O3
26	V_{SS} (Core)		
27	FRDYbsy#	I	I6Z
28	FRE#	O	O3
29	FWE#	O	O3
30	FCLE	O	O3
31	FALE	O	O3
32	FAD0	I/O	I5U/O3
33	FAD1	I/O	I5U/O3
34	FAD2	I/O	I5U/O3
35	V_{SS} (IO)		
36	$EXTCLK_{IN}$	I	I6Z
37	$EXTCLK_{OUT}$	O	O1
38	V_{DD} (IO)		
39	FAD3	I/O	I5U/O3
40	FAD4	I/O	I5U/O3
41	FAD5	I/O	I5U/O3
42	FAD6	I/O	I5U/O3
43	FAD7	I/O	I5U/O3
44	V_{SS} (IO)		
45	FCE0#	O	O1
46	FCE1#	O	O1
47	FCE2#	O	O1
48	FCE3#	O	O1
49	FCE4#	O	O1
50	SCIEN#	I	I5U
51	D3	I/O	I2D/O4

TABLE 3-1: PIN ASSIGNMENTS (CONTINUED)

Pin No.	Signal Name	Pin Type	I/O Type[1]
52	D11	I/O	I2D/O4
53	D4	I/O	I2D/O4
54	D12	I/O	I2D/O4
55	V_{SS} (IO)		
56	D5	I/O	I2D/O4
57	D13	I/O	I2D/O4
58	D6	I/O	I2D/O4
59	D14	I/O	I2D/O4
60	V_{DDQ} (IO)		
61	CSEL	I	I1U
62	WP_PD#	I	I2U
63	DASP#	I/O	I2U/O2
64	V_{SS} (IO)		
65	INTRQ	O	O2
66	CS1FX#	I	I3U
67	CS3FX#	I	I3U
68	T_{IE}_DN		
69	T_{IE}_DN		
70	IORD#	I	I3U
71	T_{IE}_DN		
72	V_{SS} (Core)		
73	IOWR#	I	I3U
74	T_{IE}_DN		
75	T_{IE}_UP		
76	T_{IE}_DN		
77	T_{IE}_DN		
78	V_{DDQ} (IO)		
79	T_{IE}_DN		
80	T_{IE}_DN		
81	RESET#	I	I4U
82	T_{IE}_DN		
83	A2	I	I2D
84	A1	I	I2D
85	A0	I	I2D
86	T_{IE}_UP		
87	DNU		
88	V_{SS} (IO)		
89	PDIAG#	I/O	I2U/O2
90	IOCS16#	O	O4
91	V_{DDQ} (IO)		
92	D15	I/O	I2D/O4
93	D7	I/O	I2D/O4
94	D0	I/O	I2D/O4
95	D8	I/O	I2D/O4
96	V_{SS} (IO)		
97	D1	I/O	I2D/O4
98	D9	I/O	I2D/O4
99	D2	I/O	I2D/O4
100	D10	I/O	I2D/O4

T3-1.18 1211

1. Please refer to Section 11.1 for details.
2. All DNU pins should not be connected.

3.1 Pin Description

TABLE 3-2: HOST SIDE INTERFACE

Symbol	Type[1]	Pin	Name and Functions
A2 - A0	I	83,84,85	A[2:0] are used to select one of eight registers in the Task File.
D15 - D0	I/O	92,59,57, 54,52,100, 98,95,93, 58,56,53, 51,99,97, 94	Data bus
CS1FX#, CS3FX#	I	66,67	CS1FX# is the chip select for the task file registers while CS3FX# is used to select the Alternate Status register and the Device Control register.
CSEL	I	61	This internally pulled-up signal is used to configure this device as a Master or a Slave. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave. The pin setting should remain the same from power-up to power-down.
IORD#	I	70	This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the chip.
IOWR#	I	73	The I/O Write strobe pulse is used to clock I/O data into the chip.
IOCS16#	O	90	This output signal is asserted low when the device is indicating a word data transfer cycle.
INTRQ	O	65	This signal is the active high Interrupt Request to the host.
PDIAG#	I/O	89	The Pass Diagnostic signal in the Master/Slave handshake protocol.
DASP#	I/O	63	The Drive Active/Slave Present signal in the Master/Slave handshake protocol.
RESET#	I	81	This input pin is the active low hardware reset from the host.
WP_PD#	I	62	The WP_PD# pin can be used for either the Write-Protect mode or Power-Down mode, but only one mode is active at any time. The Write-Protect or Power-Down modes can be selected through the host command. The Write-Protect mode is the factory default setting. For details, please refer to Section 7.0 and Section 10.2.1.18

T3-2.11 1211

1. Please refer to Section 11.1 for detail

TABLE 3-3: FLASH MEDIA INTERFACE

Symbol	Type	Pin	Name and Functions
FWP#	O	25	This signal is an Active Low Flash Media Chip Write-Protect. Connect this pin to NAND Flash Media Write-Protect Pin.
FRDYbsy#	I	27	This signal is Flash Media Chip Ready/Busy#. Signal High is Flash Media Ready signal. Low is Busy.
FRE#	O	28	This signal is an Active Low Flash Media Chip Read.
FWE#	O	29	This signal is an Active Low Flash Media Chip Write.
FCLE	O	30	This signal is an Active High Flash Media Chip Command Latch Enable.
FALE	O	31	This signal is an Active High Flash Media Chip Address Latch Enable.
FAD7-FAD0	I/O	43,42,41, 40,39,34, 33,32	These are Flash Media Chip Address/Data Bus pins.
FCE4#-FCE0#	O	49,48,47, 46,45	These are Active Low Flash Media Chip Enable pins.

T3-3.7 1211

TABLE 3-4: SERIAL COMMUNICATION INTERFACE (SCI)

Symbol	Type	Pin	Name and Functions
$SCID_{OUT}$	O	1	This signal is SCI interface data output.
$SCID_{IN}$	I	2	This signal is SCI interface data input.
SCICLK	I	3	This signal is SCI interface clock.
SCIEN#	I	50	This signal is Active Low SCI interface enable.

T3-4.8 1211

TABLE 3-5: EXTERNAL CLOCK OPTION

Symbol	Type	Pin	Name and Functions
INTCLKEN#	I	20	Internal Clock enable pin. Signal low enables an internal clock, high enables external clock source.
$EXTCLK_{IN}$	I	36	External Clock source input pin.
$EXTCLK_{OUT}$	O	37	External Clock source output pin.

T3-5.1 1211

TABLE 3-6: MISCELLANEOUS

Symbol	Type	Pin	Name and Functions
V_{SS} (IO)	PWR	5,19,35,44,55,64,88,96	Ground for I/O
V_{SS} (Core)	PWR	26,72	Ground for Core
V_{DD} (IO)	PWR	14,38	V_{DD} (3.3V)
V_{DD} (Core)	PWR	23	V_{DD} (3.3V)
V_{DDQ} (IO)	PWR	60,78,91	V_{DDQ} (5V/3.3V) for Host interface
POR#	I	24	Power On Reset. Active Low, Refer to Section 8.0.
T_{IE}_UP	I	75, 86	Pins need to be connected to V_{DDQ}.
T_{IE}_DN	I	68,69,71,74,76,77,79,80,82	Pins need to be connected to V_{SS}.
DNU		4,6,7,8,9,10,11,12,13,15,16, 17,18,21,22,87	Do Not Use, must be left unconnected.

T3-6.11 1211

4.0 CAPACITY SPECIFICATION

Table 4-1 shows the default capacity and specific settings for heads, sectors and cylinders. Users can change the default settings in the Drive ID table (see Table 10-4) for customization. It should be noted that the total Flash Drive capacity should not exceed the total number of bytes listed in Table 4-1.

TABLE 4-1: DEFAULT ATA FLASH DRIVE SETTINGS

Capacity	Total Bytes[1]	Cylinders	Heads	Sectors
8 MB	8,028,160	245	2	32
16 MB	16,023,552	489	2	32
24 MB	24,051,712	367	4	32
32 MB	32,047,104	489	4	32
48 MB	48,037,888	733	4	32
64 MB	64,028,672	977	4	32
96 MB	96,075,776	733	8	32
128 MB	128,057,344	977	8	32
192 MB[2]	192,413,696	734	16	32
256 MB[2]	256,901,120	980	16	32
384 MB[2]	384,491,520	745	16	63
512 MB[2]	512,483,328	993	16	63
640 MB[2]	640,475,136	1241	16	63

T4-1.4 1211

1. C, H, and S can be user-configurable, but the total number of bytes should not exceed the default setting
2. Only SST55LD017B and SST55LD017C support these capacities.

4.1 Functional Specifications

Table 4-2 shows the performance and the maximum capacity supported by each controller.

TABLE 4-2: FUNCTIONAL SPECIFICATION OF SST55LD017A/SST55LD017B/SST55LD017C

Functions	SST55LD017A	SST55LD017B	SST55LD017C
ATA Controller Supported Capacity	8MB to 128MB	8MB to 640MB, up to 2GB with External Decoding[1]	8MB to 640MB, up to 2GB with External Decoding[1]
ATA Controller Performance-Sustained Write speed	Up to 1.2MB/sec	Up to 2.4MB/sec with 2-chip multi-tasking[2] Up to 1.2MB/sec with 1-chip operation	Up to 4.0 MB/sec with 4-chip multi-tasking[2] Up to 3.2 MB/sec with 3-chip multi-tasking[2]
Multi-tasking Enabled	No	Yes	Yes
Support 2GB Through External Decoding	No	Yes	Yes

T4-2.2 1211

1. Please refer to the application note, *Design Consideration for High Capacity Flash Drive*
2. The ATA flash disk controller handles multiple flash operations.

5.0 SERIAL COMMUNICATION INTERFACE

The Serial Communication Interface is designed to enable the user to restart the self-initialization process and to customize the Drive Identification Information.

The Serial Communication Interface consists of 4 signals: $SCID_{OUT}$, $SCID_{IN}$, SCICLK and SCIEN#. Please refer to the *Design Consideration for ATA Flash Disk Controller's Serial Communication Interface* application note for further details.

6.0 EXTERNAL CLOCK INTERFACE

The External Clock interface allows an external clock source to drive the ATA flash disk controller. While the controller has an internal clock source, the External Clock interface allows slowing of the clock operation to limit the peak current. Please see the *External Clock Operation for ATA Flash Disk Controller* application note for further details.

The External Clock interface consists of three signals: INTCLKEN#, $EXTCLK_{IN,}$ and $EXTCLK_{OUT.}$ The INTCLKEN# pin selects between external and internal clock sources for the ATA flash disk controller. If this pin is pulled low before device power-up, then the internal clock source is selected; otherwise, the external clock source is selected. The $EXTCLK_{IN}$ and $EXTCLK_{OUT}$ signals are the input and output clock signals, respectively. Please see Section 12.2 for the detailed circuit schematic.

7.0 CONFIGURABLE WRITE-PROTECT/POWER-DOWN MODES

The WP_PD# pin can be used for either Write-Protect mode or Power-Down mode, but only one mode is active at any time. Either mode can be selected through the host command, Set-WP_PD#-Mode, explained in Section 10.2.1.18.

Once the mode is set with this command, the device will stay in the configured mode until the next time this command is issued. Power-off or reset will not change the configured mode.

7.1 Write-Protect Mode

When the device is configured in the Write-Protect mode, the WP_PD# pin offers extended data protection. This feature can be either selected through a jumper or host logic to protect the stored data from inadvertent system writes or erases, and viruses. The Write-Protect feature protects the full address space of the data stored on the flash media.

In the Write-Protect mode, the WP_PD# pin should be asserted prior to issuing the destructive commands: Format-Track, Write-Buffer, Write-Long-Sector, Write-Multiple, Write-Sector(s), or Write-Verify. This will force the ATA flash disk controller to reject any destructive commands from the ATA interface. All destructive commands will return 51H in the Status register and 04H in the Error register signifying an invalid command. All non-destructive commands will be executed normally.

7.2 Power-Down Mode

When the device is configured in the Power-Down mode, if the WP_PD# pin is asserted during a command, the ATA disk controller completes the current command and returns to the standby mode immediately to save power. Afterwards, the device will not accept any other commands. Only a power-on reset or hardware reset will bring the device to normal operation with the WP_PD# pin de-asserted.

8.0 POWER-ON AND BROWN-OUT RESET CHARACTERISTICS

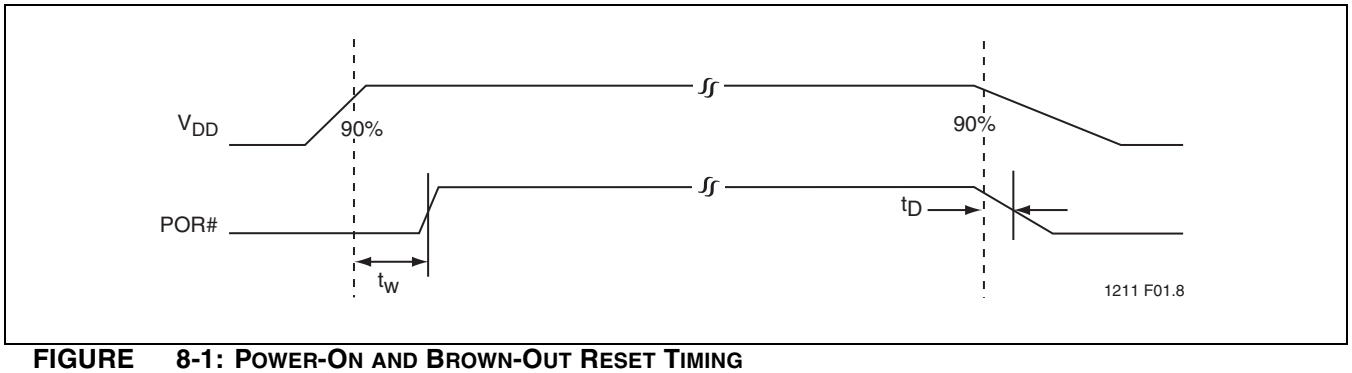


FIGURE 8-1: POWER-ON AND BROWN-OUT RESET TIMING

TABLE 8-1: POWER-ON AND BROWN-OUT RESET TIMING

Item	Symbol	Min	Max	Units
POR Wait Time	t_w	0.1		ms
Brown-out Delay Time	t_D		30	µs

T8-1.1 1211

9.0 I/O TRANSFER FUNCTION

The default operation for ATA flash disk controller is 16-bit. ATA flash disk controller, however, permits 8-bit data access if the host issues a Set Feature Command to enable 8-bit mode.

The following table defines the function of various operations.

TABLE 9-1: I/O FUNCTION

Function Code	CS3FX#	CS1FX#	A0-A2	IORD#	IOWR#	D15-D8	D7-D0
Invalid Mode	V_{IL}	V_{IL}	X	X	X	Undefined	Undefined
Standby Mode	V_{IH}	V_{IH}	X	X	X	High Z	High Z
Task File Write	V_{IH}	V_{IL}	1-7H	V_{IH}	V_{IL}	X	Data In
Task File Read	V_{IH}	V_{IL}	1-7H	V_{IL}	V_{IH}	High Z	Data Out
Data Register Write	V_{IH}	V_{IL}	0	V_{IH}	V_{IL}	In[1]	In
Data Register Read	V_{IH}	V_{IL}	0	V_{IL}	V_{IH}	Out[1]	Out
Control Register Write	V_{IL}	V_{IH}	6H	V_{IH}	V_{IL}	X	Control In
Alt Status Read	V_{IL}	V_{IH}	6H	V_{IL}	V_{IH}	High Z	Status Out
Drive Address	V_{IL}	V_{IH}	7H	V_{IL}	V_{IH}	High Z	Data Out

T9-1.2 1211

1. If 8-bit data transfer mode is enabled.
In 8-bit data transfer mode, High Byte is undefined for Data Out. For Data In, X can be V_{IH} or V_{IL}, but no other value.

10.0 SOFTWARE INTERFACE

10.1 ATA Flash Disk Controller Drive Register Set Definitions and Protocol

10.1.1 ATA Flash Disk Controller Addressing

The I/O decoding for an ATA flash disk controller is as follows:

TABLE 10-1: TASK FILE REGISTERS

CS3FX#	CS1FX#	A2	A1	A0	Registers	
					IORD# = 0 (IOWR#=1)	IOWR# = 0 (IORD#=1)
1	0	0	0	0	Data (Read)	Data (Write)
1	0	0	0	1	Error	Feature
1	0	0	1	0	Sector Count	Sector Count
1	0	0	1	1	Sector Number (LBA 7-0)	Sector Number (LBA 7-0)
1	0	1	0	0	Cylinder Low (LBA 15-8)	Cylinder Low (LBA 15-8)
1	0	1	0	1	Cylinder High (LBA 23-16)	Cylinder High (LBA 23-16)
1	0	1	1	0	Drive/Head	Drive/Head
1	0	1	1	1	Status	Command
0	1	1	1	0	Alternate Status	Device Control
0	1	1	1	1	Drive Address	Reserved

T10-1.6 1211

10.1.2 ATA Flash Disk Controller Registers

The following section describes the hardware registers used by the host software to issue commands to the ATA flash disk controller. These registers are often collectively referred to as the “Task File” registers. The registers are only selectable through CS3FX#, CS1FX#, and A_2-A_0 signals. Please see Table 10-1 for register addressing.

10.1.2.1 Data Register (Read/Write) (See Table 10-1 for register addressing)

This 16-bit register is used to transfer data blocks between the device data buffer and the host. It is also the register through which sector information is transferred on a Format-Track command. Data transfer can be performed in PIO mode.

10.1.2.2 Error Register (Read Only) (See Table 10-1 for register addressing)

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0	**Reset Value**
BBK	UNC	0	IDNF	0	ABRT	0	AMNF	**0000 0000b**

Symbol	**Function**
BBK	This bit is set when a Bad Block is detected.
UNC	This bit is set when an Uncorrectable Error is encountered.
IDNF	The requested sector ID is in error or cannot be found.
ABRT	This bit is set if the command has been aborted because of an ATA flash disk controller status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued.
AMNF	This bit is set in case of a general error.

10.1.2.3 Feature Register (Write Only) (See Table 10-1 for register addressing)

This register provides information regarding features of the ATA flash disk controller that the host can utilize.

10.1.2.4 Sector Count Register (See Table 10-1 for register addressing)

This register contains the numbers of sectors of data requested to be transferred on a Read or Write operation between the host and the ATA flash disk controller. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

10.1.2.5 Sector Number (LBA 7-0) Register (See Table 10-1 for register addressing)

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any ATA flash disk controller data access for the subsequent command.

10.1.2.6 Cylinder Low (LBA 15-8) Register (See Table 10-1 for register addressing)

This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of then Logical Block Address.

10.1.2.7 Cylinder High (LBA 23-16) Register (See Table 10-1 for register addressing)

This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

10.1.2.8 Drive/Head (LBA 27-24) Register (See Table 10-1 for register addressing)

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0	**Reset Value**
1	LBA	1	DRV	HS3	HS2	HS1	HS0	**1010 0000b**

Symbol	**Function**
LBA	LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows: LBA7-LBA0: Sector Number register D7-D0. LBA15-LBA8: Cylinder Low register D7-D0. LBA23-LBA16: Cylinder High register D7-D0. LBA27-LBA24: Drive/Head register bits HS3-HS0.
DRV	DRV is the drive number. When DRV=0 (Master), Master is selected. When DRV=1(Slave), Slave is selected.
HS3	When operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number. It is Bit 27 in the Logical Block Address mode.
HS2	When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is Bit 26 in the Logical Block Address mode.
HS1	When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.
HS0	When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

10.1.2.9 Status & Alternate Status Registers (Read Only) (See Table 10-1 for register addressing)

These registers return the ATA flash disk controller status when read by the host. Reading the Status register does clear a pending interrupt while reading the Alternate Status register does not. The meaning of the status bits are described as follows:

D7	D6	D5	D4	D3	D2	D1	D0	**Reset Value**
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR	**1000 0000b**

Symbol	**Function**
BUSY	The busy bit is set when the ATA flash disk controller has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit is set to a 1.
RDY	RDY indicates whether the device is capable of performing ATA flash disk controller operations. This bit is cleared at power up and remains cleared until the ATA flash disk controller is ready to accept a command.
DWF	This bit, if set, indicates a write fault has occurred.
DSC	This bit is set when the ATA flash disk controller is ready.
DRQ	The Data Request is set when the ATA flash disk controller requires that information be transferred either to or from the host through the Data register.
CORR	This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector Read operation.
ERR	This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error. It is recommended that media access commands (such as Read-Sectors and Write-Sectors) that end with an error condition should have the address of the first sector in error in the command block registers.

10.1.2.10 Device Control Register (Write Only) (See Table 10-1 for register addressing)

This register is used to control the ATA flash disk controller interrupt request and to issue a software Reset. This register can be written to even if the device is BUSY. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0	**Reset Value**
X	X	X	X	1	SW Rst	-IEn	0	**0000 1010b**

Symbol	**Function**
SW Rst	This bit is set to 1 in order to force the ATA flash disk controller to perform a software Reset operation. The chip remains in Reset until this bit is reset to ‘0.’
-IEn	0: The Interrupt Enable bit enables interrupts 1: Interrupts from the ATA flash disk controller are disabled This bit is set to 1 at Power-On and Reset.

10.1.2.11 Drive Address Register (Read Only) (See Table 10-1 for register addressing)

This register contains the inverted drive select and head select addresses of the currently selected drive. The bits in this register are as follows:

D7	D6	D5	D4	D3	D2	D1	D0	**Reset Value**
X	-WTG	-HS3	-HS2	-HS1	-HS0	-DS1	-DS0	**x111 1110b**

Symbol	**Function**
-WTG	This bit is 0 when a Write operation is in progress, otherwise, it is 1.
-HS3	This bit is the negation of bit 3 in the Drive/Head register.
-HS2	This bit is the negation of bit 2 in the Drive/Head register.
-HS1	This bit is the negation of bit 1 in the Drive/Head register.
-HS0	This bit is the negation of bit 0 in the Drive/Head register.
-DS1	This bit is 0 when drive 1 is active and selected.
-DS0	This bit is 0 when drive 0 is active and selected.

10.1.2.12 Command Register (Write Only) (See Table 10-1 for register addressing)

This register contains the command code being sent to the drive. Command execution begins immediately after this register is written. The executable commands, the command codes, and the necessary parameters for each command are listed in Table 10-2.

10.2 ATA Flash Disk Controller Command Description

This section defines the software requirements and the format of the commands the host sends to the ATA flash disk controller. Commands are issued to the ATA flash disk controller by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register. The manner in which a command is accepted varies. There are three classes (see Table 10-2) of command acceptance, all dependent on the host not issuing commands unless the ATA flash disk controller is not busy (BSY=0).

10.2.1 ATA Flash Disk Controller Command Set

Table 10-2 summarizes the ATA flash disk controller command set with the paragraphs that follow describing the individual commands and the task file for each.

TABLE 10-2: ATA FLASH DISK CONTROLLER COMMAND SET

Class	Command	Code	FR[1]	SC[2]	SN[3]	CY[4]	DH[5]	LBA[6]
1	Check-Power-Mode	E5H or 98H	-	-	-	-	D[8]	-
1	Execute-Drive-Diagnostic	90H	-	-	-	-	D	-
2	Format-Track	50H	-	Y[7]	-	Y	Y[8]	Y
1	Identify-Drive	ECH	-	-	-	-	D	-
1	Idle	E3H or 97H	-	Y	-	-	D	-
1	Idle-Immediate	E1H or 95H	-	-	-	-	D	-
1	Initialize-Drive-Parameters	91H	-	Y	-	-	Y	-
1	Read-Buffer	E4H	-	-	-	-	D	-
1	Read-Long-Sector	22H or 23H	-	-	Y	Y	Y	Y
1	Read-Multiple	C4H	-	Y	Y	Y	Y	Y
1	Read-Sector(s)	20H or 21H	-	Y	Y	Y	Y	Y
1	Read-Verify-Sector(s)	40H or 41H	-	Y	Y	Y	Y	Y
1	Recalibrate	1XH	-	-	-	-	D	-
1	Seek	7XH	-	-	Y	Y	Y	Y
1	Set-Features	EFH	Y	-	-	-	D	-
1	Set-Multiple-Mode	C6H	-	Y	-	-	D	-
1	Set-Sleep-Mode	E6H or 99H	-	-	-	-	D	-
1	Set-WP_PD#-Mode	8BH	Y	-	-	-	D	-
1	Stand-By	E2H or 96H	-	-	-	-	D	-
1	Stand-By-Immediate	E0H or 94H	-	-	-	-	D	-
2	Write-Buffer	E8H	-	-	-	-	D	-
2	Write-Long-Sector	32H or 33H	-	-	Y	Y	Y	Y
3	Write-Multiple	C5H	-	Y	Y	Y	Y	Y
2	Write-Sector(s)	30H or 31H	-	Y	Y	Y	Y	Y
3	Write-Verify	3CH	-	Y	Y	Y	Y	Y

T10-2.3 1211

1. FR - Features register
2. SC - Sector Count register
3. SN - Sector Number register
4. CY - Cylinder registers
5. DH - Drive/Head register
6. LBA - Logical Block Address Mode Supported (see command descriptions for use)
7. Y - The register contains a valid parameter for this command.
8. For the Drive/Head register: Y means both the ATA flash disk controller and Head parameters are used;
   D means only the ATA flash disk controller parameter is valid and not the Head parameter.

10.2.1.1 Check-Power-Mode - 98H or E5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	98H or E5H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command checks the power mode.

Because SST ATA flash disk controller can recover from sleep in 200 ns, Idle Mode is never enabled.

ATA flash disk controller sets BSY, sets the Sector Count register to 00H, clears BSY and generates an interrupt.

10.2.1.2 Execute-Drive-Diagnostic - 90H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	90H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command performs the internal diagnostic tests implemented by the ATA flash disk controller.

If the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with status for both devices.

The Diagnostic codes shown in Table 10-3 are returned in the Error register at the end of the command.

TABLE 10-3: DIAGNOSTIC CODES

Code	Error Type
01H	No Error Detected
02H	Formatter Device Error
03H	Sector Buffer Error
04H	ECC Circuitry Error
05H	Controlling Microprocessor Error
8XH	Slave Error

T10-3.1 1211

10.2.1.3 Format-Track - 50H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	50H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is accepted for host backward compatibility. The ATA flash disk controller expects a sector buffer of data from the host to follow the command with the same protocol as the Write-Sector(s) command although the information in the buffer is not used by the ATA flash disk controller. The use of this command is not recommended.

10.2.1.4 Identify-Drive - ECH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	ECH							
C/D/H (6)	X	X	X	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Identify-Drive command enables the host to receive parameter information from the ATA flash disk controller. This command has the same protocol as the Read-Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 10-4. All reserved bits or words are zero. Table 10-4 gives the definition for each field in the Identify-Drive Information.

TABLE 10-4: IDENTIFY-DRIVE INFORMATION

Word Address	Default Value	Total Bytes	Data Field Type Information
0	044AH	2	General configuration bit-significant information
1	bbbb[1]	2	Default number of cylinders
2	0000H	2	Reserved
3	bbbb[1]	2	Default number of heads
4	0000H	2	Reserved
5	0000H	2	Reserved
6	bbbb[1]	2	Default number of sectors per track
7-8	nnnnH[2]	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	nnnnH	2	Vendor Unique
10-14	dddd[3]	10	SST preset, unique ID in ASCII
15-19	eeee[4]	10	User-programmable serial number in ASCII
20	0002H	2	Buffer type
21	nnnnH	2	Buffer size in 512 Byte increments
22	0004H	2	# of ECC bytes passed on Read/Write-Long-Sector Commands
23-26	aaaa[5]	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	cccc[6]	40	User Definable Model number
47	000nH	2	Maximum number of sectors on Read/Write-Multiple command
48	0000H	2	Reserved
49	0200H	2	Capabilities
50	0000H	2	Reserved
51	0n00H	2	PIO data transfer cycle timing mode
52	0000H	2	Reserved (DMA data transfer is not supported in ATA flash disk controller)
53	000nH	2	Translation parameters are valid
54	nnnnH	2	Current numbers of cylinders
55	nnnnH	2	Current numbers of heads
56	nnnnH	2	Current sectors per track
57-58	nnnnH	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW)
59	010nH	2	Multiple sector setting
60-61	nnnnH	4	Total number of sectors addressable in LBA Mode
62-63	0000H	4	Reserved (DMA data transfer is not supported in ATA flash disk controller)
64	00nnH	2	Advanced PIO Transfer Mode Supported
65-66	0000H	4	Reserved
67	nnnnH	2	Minimum PIO transfer cycle time without flow control
68	nnnnH	2	Minimum PIO transfer cycle time with IORDY flow control
69-127	0000H	138	Reserved
128-159	0000H	64	Vendor unique bytes
160-255	0000H	192	Reserved

T10-4.10 1211

1. bbbb - default value set by controller. The selections could be user programmable.
2. n - calculated data based on product configuration
3. dddd - unique number of each device
4. eeee - the default value is 2020H
5. aaaa - any unique SST firmware revision
6. cccc - default value is “xxxMB ATA Flash Disk” where xxx is the flash drive capacity.
   The user has an option to change the model number during manufacturing.

10.2.1.4.1 General Configuration

This field informs the host that this is a non-magnetic, hard sectored, removable storage device with a transfer rate greater than 10 MByte/sec and is not MFM encoded.

10.2.1.4.2 Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

10.2.1.4.3 Default Number of Heads

This field contains the number of translated heads in the default translation mode.

10.2.1.4.4 Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

10.2.1.4.5 Number of Sectors

This field contains the number of sectors per ATA flash disk controller. This double word value is also the first invalid address in LBA translation mode.

10.2.1.4.6 Serial Number

The contents of this field are right justified and padded with spaces (20H). The first ten bytes are a SST preset, unique ID. The second ten bytes are a user-programmable value with a default value of spaces.

10.2.1.4.7 Buffer Type

This field defines the buffer capability:

0002H: a dual ported multi-sector buffer capable of simultaneous data transfers to or from the host and the ATA flash disk controller.

10.2.1.4.8 Buffer Size

This field defines the buffer capacity in 512 Byte increments. SST's ATA flash disk controller has up to 2 sector data buffer for host interface.

10.2.1.4.9 ECC Count

This field defines the number of ECC bytes used on each sector in the Read- and Write-Long-Sector commands.

10.2.1.4.10 Firmware Revision

This field contains the revision of the firmware for this product.

10.2.1.4.11 Model Number

This field is reserved for the model number for this product.

10.2.1.4.12 Read-/Write-Multiple Sector Count

This field contains the maximum number of sectors that can be read or written per interrupt using the Read-Multiple or Write-Multiple commands.

10.2.1.4.13 Capabilities

Bit 13: Standby Timer	Set to 0, forces sleep mode when host is inactive.
Bit 11: IORDY Support	Set to 0, indicates that this device may support IORDY operation.
Bit 9: LBA support	Set to 1, SST's ATA flash disk controllers support LBA mode addressing.
Bit 8: DMA Support	This bit is set to 0. DMA mode is not supported.

10.2.1.4.14 PIO Data Transfer Cycle Timing Mode

This field defines the mode for PIO data transfer. ATA flash disk controller supports up to PIO Mode-4.

10.2.1.4.15 Translation Parameters Valid

If bit 0 is 1, it indicates that words 54 to 58 are valid and reflect the current number of cylinders, heads and sectors. If bit 1 is 1, it indicates that words 64 to 70 are valid to support PIO Mode-3 and 4.

10.2.1.4.16 Current Number of Cylinders, Heads, Sectors/Track

These fields contains the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

10.2.1.4.17 Current Capacity

This field contains the product of the current cylinders times heads times sectors.

10.2.1.4.18 Multiple Sector Setting

This field contains a validity flag in the Odd Byte and the current number of sectors that can be transferred per interrupt for R/W Multiple in the Even Byte. The Odd Byte is always 01H which indicates that the Even Byte is always valid.

The Even Byte value depends on the value set by the Set Multiple command. The Even Byte of this word by default contains a 00H which indicates that R/W Multiple commands are not valid.

10.2.1.4.19 Total Sectors Addressable in LBA Mode

This field contains the number of sectors addressable for the ATA flash disk controller in LBA mode only.

10.2.1.4.20 Advanced PIO Data Transfer Mode

ATA flash disk controller supports up to PIO Mode-4.

10.2.1.4.21 Minimum PIO Transfer Cycle Time Without Flow Control

The ATA flash disk controller's minimum cycle time is 120 ns.

10.2.1.4.22 Minimum PIO Transfer Cycle Time With IORDY

The ATA flash disk controller's minimum cycle time is 120 ns, e.g., PIO Mode-4.

10.2.1.5 Idle - 97H or E3H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	97H or E3H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Timer Count (5 msec increments)							
Feature (1)	X							

This command causes the ATA flash disk controller to set BSY, enter the Idle Mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic Power-Down mode is enabled. If the sector count is zero, the automatic Power-Down mode is also enabled, the timer count is set to 3, with each count being 5 ms. Note that this time base (5 msec) is different from the ATA specification.

10.2.1.6 Idle-Immediate - 95H or E1H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	95H or E1H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the ATA flash disk controller to set BSY, enter the Idle Mode, clear BSY and generate an interrupt.

10.2.1.7 Initialize-Drive-Parameters - 91H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	91H							
C/D/H (6)	X	0	X	Drive	Max Head (no. of heads-1)			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Number of Sectors							
Feature (1)	X							

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Drive/Head registers are used by this command.

10.2.1.8 Read-Buffer - E4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E4H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Read-Buffer command enables the host to read the current contents of the ATA flash disk controller's sector buffer. This command has the same protocol as the Read-Sector(s) command

10.2.1.9 Read-Multiple - C4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C4H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Note: The current revision of the SST ATA flash disk controller can support up to a block count of 1 as indicated in the Identify-Drive Command information.

The Read-Multiple command is similar to the Read-Sector(s) command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

Command execution is identical to the Read-Sectors operation except that the number of sectors defined by a Set Multiple command are transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set-Multiple-Mode command, which must be executed prior to the Read-Multiple command. When the Read-Multiple command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where

n = remainder (sector count/block count).

If the Read-Multiple command is attempted before the Set-Multiple-Mode command has been executed or when Read-Multiple commands are disabled, the Read-Multiple operation is rejected with an Aborted Command error. Disk errors encountered during Read-Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer will take place as it normally would, including transfer of corrupted data, if any.

Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read-Sector(s) command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

At command completion, the Command Block registers contain the cylinder, head and sector number of the last sector read.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error.

10.2.1.10 Read-Long-Sector - 22H or 23H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	22H or 23H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

The Read-Long-Sector command performs similarly to the Read-Sector(s) command except that it returns 516 Bytes of data instead of 512 Bytes. During a Read-Long-Sector command, the ATA flash disk controller does not check the ECC bytes to determine if there has been a data error. Only single-sector Read-Long-Sector operations are supported. The transfer consists of 512 Bytes of data transferred in Word-Mode followed by 4 Bytes of ECC data transferred in Byte-Mode. This command has the same protocol as the Read-Sector(s) command. Use of this command is not recommended.

10.2.1.11 Read-Sector(s) - 20H or 21H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	20H or 21H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register. When this command is issued and after each sector of data (except the last one) has been read by the host, the ATA flash disk controller sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 Bytes of data from the buffer.

At command completion, the Command Block registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

10.2.1.12 Read-Verify-Sector(s) - 40H or 41H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	40H or 41H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is identical to the Read-Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the ATA flash disk controller sets BSY.

When the requested sectors have been verified, the ATA flash disk controller clears BSY and generates an interrupt. Upon command completion, the Command Block registers contain the cylinder, head, and sector number of the last sector verified.

If an error occurs, the verify terminates at the sector where the error occurs. The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count register contains the number of sectors not yet verified.

10.2.1.13 Recalibrate - 1XH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	1XH							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command is effectively a NOP command to the ATA flash disk controller and is provided for compatibility purposes.

10.2.1.14 Seek - 7XH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	7XH							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command is effectively a NOP command to the ATA flash disk controller although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

10.2.1.15 Set-Features - EFH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	EFH							
C/D/H (6)		X		Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	Feature							

This command is used by the host to establish or select certain features. Table 10-5 defines all features that are supported.

TABLE 10-5: FEATURES SUPPORTED

Feature	Operation
01H	Enable 8-bit data transfers.
03H	Set transfer mode based on value in Sector Count register. Table 10-6 defines the values.
55H	Disable Read Look Ahead.
66H	Disable Power on Reset (POR) establishment of defaults at software Reset.
69H	NOP - Accepted for backward compatibility.
81H	Disable 8-bit data transfer.
96H	NOP - Accepted for backward compatibility.
97H	Accepted for backward compatibility. Use of this Feature is not recommended.
9AH	NOP - accepted for compatibility.
BBH	4 Bytes of data apply on Read/Write-Long-Sector commands.
CCH	Enable Power on Reset (POR) establishment of defaults at software Reset.

T10-5.1 1211

Features 01H and 81H are used to enable and clear 8-bit data transfer mode. If the 01H feature command is issued all data transfers will occur on the low order D7-D0 data bus and the IOCS16# signal will not be asserted for data register accesses.

Features 55H and BBH are the default features for the ATA flash disk controller; thus, the host does not have to issue this command with these features unless it is necessary for compatibility reasons.

Features 66H and CCH can be used to enable and disable whether the Power On Reset (POR) Defaults will be set when a software Reset occurs.

TABLE 10-6: TRANSFER MODE VALUES

Mode	Bits [7:3]	Bits [2:0]
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	mode[1]
Reserved	Other	N/A

T10-6.1 1211

1. Mode = transfer mode number, all other values are not valid

10.2.1.16 Set-Multiple-Mode - C6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C6H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command enables the ATA flash disk controller to perform Read and Write-Multiple operations and establishes the block count for these commands. The Sector Count register is loaded with the number of sectors per block. Upon receipt of the command, the ATA flash disk controller sets BSY to 1 and checks the Sector Count register.

If the Sector Count register contains a valid value (see Section 10.2.1.4.12 for details) and the block count is supported, the value is loaded for all subsequent Read-Multiple and Write-Multiple commands and execution of those commands is enabled. If a block count is not supported, an Aborted Command error is posted, and Read-Multiple and Write-Multiple commands are disabled. If the Sector Count register contains 0 when the command is issued, Read and Write-Multiple commands are disabled. At power on, or after a hardware or (unless disabled by a Set Feature command) software reset, the default mode is Read and Write-Multiple disabled.

10.2.1.17 Set-Sleep-Mode - 99H or E6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	99H or E6H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the ATA flash disk controller to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 15 milliseconds.

10.2.1.18 Set-WP_PD#-Mode - 8BH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	8BH							
C/D/H (6)	X	X	X	Drive	X			
Cyl High (5)	6EH							
Cyl Low (4)	44H							
Sec Num (3)	72H							
Sec Cnt (2)	50H							
Feature (1)	55H or AAH							

This command configures the WP_PD# pin for either the Write-Protect mode or the Power-Down mode. When the host sends this command to the device with the value AAH in the feature register, the WP_PD# pin is configured for the Write-Protect mode described in Section 7.1. The Write-Protect mode is the factory default setting. When the host sends this command to the device with the value 55H in the feature register, WP_PD# is configured for the Power-Down mode.

All values in the C/D/H register, the Cylinder Low register, the Cylinder High register, the Sector Number register, the Sector Count register, and the Feature register need to match the values shown above, otherwise, the command will be treated as an invalid command.

Once the mode is set with this command, the device will stay in the configured mode until the next time this command is issued. Power-off or reset will not change the configured mode.

10.2.1.19 Standby - 96H or E2H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	96H or E2H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the ATA flash disk controller to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

10.2.1.20 Standby-Immediate - 94H or E0H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	94H or E0H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the ATA flash disk controller to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

10.2.1.21 Write-Buffer - E8H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E8H							
C/D/H (6)		X		Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Write-Buffer command enables the host to overwrite contents of the ATA flash disk controller’s sector buffer with any data pattern desired. This command has the same protocol as the Write-Sector(s) command and transfers 512 Bytes.

10.2.1.22 Write-Long-Sector - 32H or 33H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	32H or 33H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command is similar to the Write-Sector(s) command except that it writes 516 Bytes instead of 512 Bytes. Only single sector Write-Long-Sector operations are supported. The transfer consists of 512 Bytes of data transferred in Word-Mode followed by 4 Bytes of ECC transferred in Byte-Mode. Because of the unique nature of the solid-state ATA flash disk controller, the 4 Bytes of ECC transferred by the host may be used by the ATA flash disk controller. The ATA flash disk controller may discard these 4 Bytes and write the sector with valid ECC data. This command has the same protocol as the Write-Sector(s) command. Use of this command is not recommended.

10.2.1.23 Write-Multiple - C5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C5H							
C/D/H (6)	X	LBA	X	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Note: The current revision of the SST ATA flash disk controller can support up to a block count of 1 as indicated in the Identify-Drive Command information.

This command is similar to the Write-Sectors command. The ATA flash disk controller sets BSY within 400 ns of accepting the command. Interrupts are not presented on each sector but on the transfer of a block which contains the number of sectors defined by Set Multiple. Command execution is identical to the Write-Sectors operation except that the number of sectors defined by the Set Multiple command is transferred without intervening interrupts.

DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set-Multiple-Mode command, which must be executed prior to the Write-Multiple command.

When the Write-Multiple command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the sector/block, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

n = remainder (sector count/block).

If the Write-Multiple command is attempted before the Set-Multiple-Mode command has been executed or when Write-Multiple commands are disabled, the Write-Multiple operation will be rejected with an aborted command error.

Errors encountered during Write-Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred and the Sector Count register contains the residual number of sectors that need to be transferred for successful completion of the command e.g. each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count register contains 6 and the address is that of the third sector.

10.2.1.24 Write-Sector(s) - 30H or 31H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	30H or 31H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register. When this command is accepted, the ATA flash disk controller sets BSY, then sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY will be set and DRQ will be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It will remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated.

If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

10.2.1.25 Write-Verify - 3CH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	3CH							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is similar to the Write-Sector(s) command, except each sector is verified immediately after being written. This command has the same protocol as the Write-Sector(s) command.

10.2.2 Error Posting

The following table summarizes the valid status and error value for all the ATA flash disk controller Command set.

TABLE 10-7: ERROR AND STATUS REGISTER

Command	Error Register					Status Register				
	BBK	UNC	IDNF	ABRT	AMNF	RDY	DWF	DSC	CORR	ERR
Check-Power-Mode				V		V	V	V		V
Execute-Drive-Diagnostic[1]						V		V		V
Format-Track			V	V	V	V	V	V		V
Identify-Drive				V		V	V	V		V
Idle				V		V	V	V		V
Idle-Immediate				V		V	V	V		V
Initialize-Drive-Parameters						V		V		V
Read-Buffer				V		V	V	V		V
Read-Multiple	V	V	V	V	V	V	V	V	V	V
Read-Long-Sector	V		V	V	V	V	V	V		V
Read-Sector(s)	V	V	V	V	V	V	V	V	V	V
Read-Verify-Sector(s)	V	V	V	V	V	V	V	V	V	V
Recalibrate				V		V	V	V		V
Seek			V	V		V	V	V		V
Set-Features				V		V	V	V		V
Set-Multiple-Mode				V		V	V	V		V
Set-Sleep-Mode				V		V	V	V		V
Set-WP_PD#-Mode				V		V		V		V
Standby				V		V	V	V		V
Standby-Immediate				V		V	V	V		V
Write-Buffer				V		V	V	V		V
Write-Long-Sector	V		V	V	V	V	V	V		V
Write-Multiple	V		V	V	V	V	V	V		V
Write-Sector(s)	V		V	V	V	V	V	V		V
Write-Verify	V		V	V	V	V	V	V		V
Invalid-Command-Code				V		V	V	V		V

T10-7.4 1211

1. See Table 10-3
   V = valid on this command

11.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
D.C. Voltage on any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -2.0V to V_{DD}+2.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Through Hole Lead Soldering Temperature (10 Seconds) . . . . . 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) . . . . . 240°C
Output Short Circuit Current[1] . . . . . 50 mA

1. Outputs shorted for no more than one second. No more than one output shorted at a time.

TABLE 11-1: ABSOLUTE MAXIMUM POWER PIN STRESS RATINGS

Parameter	Symbol	Conditions
Input Power	V_{DDQ} V_{DD}	-0.3V min to 6.5V max -0.3V min to 4.0V max
Voltage on any flash media interface pin with respect to V_{SS}		-0.5V min to V_{DD} + 0.5V max
Voltage on all other pins with respect to V_{SS}		-0.5V min to V_{DDQ} + 0.5V max

T11-1.3 1211

OPERATING RANGE

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.135-3.465V	4.5-5.5V; 3.135-3.465V
Industrial	-40°C to +85°C	3.135-3.465V	4.75-5.25V; 3.135-3.465V

AC CONDITIONS OF TEST

Input Rise/Fall Time . . . . . 10 ns
Output Load . . . . . C_L = 100 pF
See Figure 11-1

Note: All AC specifications are guaranteed by design.

TABLE 11-2: RECOMMENDED SYSTEM POWER-UP TIMING

Symbol	Parameter	Typical	Maximum	Units
$T_{PU-INITIAL}$	First-time Power-up/Reset to Ready	0.5	1.5	sec/MB
$T_{PU-READY}$[1]	Host Power-up/Reset to Ready Operation	200	500	ms
$T_{PU-WRITE}$[1]	Host Power-up/Reset to Write Operation	200	500	ms

T11-2.5 1211

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 11-3: CAPACITANCE (Ta = 25°C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum	Units
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	15	pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	9	pF

T11-3.1 1211

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 11-4: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

T11-4.1 1211

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

11.1 DC Characteristics

In the table below, x refers to the characteristics described in Section 11.1.1. For example, I1U indicates a pull up resistor with a type 1 input characteristic.

TABLE 11-5: INPUT CHARACTERISTICS, V_{DD} = V_{DDQ} = 3.135-3.465V

Type	Parameter	Symbol	Conditions	Min	Max	Units
IxZ	Input Leakage Current	IL	V_{IH} = V_{DDQ} Max; V_{IL} = V_{SS} V_{DD} = V_{DDQ} = V_{DD} Max	-10	10	µA
I5U	Pull Up Resistor	RPU2	V_{DDQ} = V_{DDQ} Min; V_{DD} = V_{DD} Min	50	500	KOhm
I1U-I4U	Pull Up Resistor	RPU1	V_{DDQ} = V_{DDQ} Min; V_{DD} = V_{DD} Min	50	1500	KOhm
I2D	Pull Down Resistor	RPD1	V_{DDQ} = V_{DDQ} Min; V_{DD} = V_{DD} Min	50	1500	KOhm

T11-5.7 1211

TABLE 11-6: INPUT CHARACTERISTICS, V_{DDQ} = 4.5-5.5V, V_{DD} = 3.135-3.465V

Type	Parameter	Symbol	Conditions	Min	Max	Units
I1U-I4U	Pull Up Resistor	RPU1	V_{DDQ} = V_{DDQ} Min; V_{DD} = V_{DD} Min	50	700	KOhm
I2D	Pull Down Resistor	RPD1	V_{DDQ} = V_{DDQ} Min; V_{DD} = V_{DD} Min	50	700	KOhm

T11-6.9 1211

11.1.1 Input Characteristics

TABLE 11-7: INPUT VOLTAGE CHARACTERISTICS (Ta = 0°C to +70°C), V_{DD} = V_{DDQ} = 3.135-3.465V

Type[1]	Parameter	Symbol	Min	Max	Units	Conditions
I1	Input Voltage CMOS	V_{IH}	V_{DDQ}-1.3		Volts	V_{DDQ}=V_{DDQ} Max
		V_{IL}		V_{DDQ}-2.5		V_{DDQ}=V_{DDQ} Min
I2	Input Voltage CMOS	V_{IH}	V_{DDQ}-1.3		Volts	V_{DDQ}=V_{DDQ} Max
		V_{IL}		V_{DDQ}-2.5		V_{DDQ}=V_{DDQ} Min
I3	Input Voltage CMOS Schmitt Trigger	V_{T+}	V_{DDQ}-1.3		Volts	V_{DDQ}=V_{DDQ} Max
		V_{T-}		V_{DDQ}-2.7		V_{DDQ}=V_{DDQ} Min
I4	Input Voltage CMOS Schmitt Trigger	V_{T+}	V_{DDQ}-1.3		Volts	V_{DDQ}=V_{DDQ} Max
		V_{T-}		V_{DDQ}-2.5		V_{DDQ}=V_{DDQ} Min
I5	Input Voltage CMOS	V_{IH}	V_{DD}-1.2		Volts	V_{DD}=V_{DD} Max
		V_{IL}		V_{DD}-2.5		V_{DD}=V_{DD} Min
I6	Input Voltage CMOS Schmitt Trigger	V_{T+}	V_{DD}-0.6		Volts	V_{DD}=V_{DD} Max
		V_{T-}		V_{DD}-2.55		V_{DD}=V_{DD} Min

T11-7.2 1211

1. I1-I4 are for host side interface only. I5-I6 are for flash media interface only.

TABLE 11-8: INPUT VOLTAGE CHARACTERISTICS (Ta = 0°C to +70°C), V_{DDQ} = 4.5-5.5V, V_{DD} = 3.135-3.465V

Type[1]	Parameter	Symbol	Min	Max	Units	Conditions
I1	Input Voltage CMOS	V_{IH}	V_{DDQ}-2.7		Volts	V_{DDQ}=V_{DDQ} Max
		V_{IL}		V_{DDQ}-4.2		V_{DDQ}=V_{DDQ} Min
I2	Input Voltage CMOS	V_{IH}	V_{DDQ}-2.3		Volts	V_{DDQ}=V_{DDQ} Max
		V_{IL}		V_{DDQ}-4.2		V_{DDQ}=V_{DDQ} Min
I3	Input Voltage CMOS Schmitt Trigger	V_{T+}	V_{DDQ}-2.7		Volts	V_{DDQ}=V_{DDQ} Max
		V_{T-}		V_{DDQ}-4.2		V_{DDQ}=V_{DDQ} Min
I4	Input Voltage CMOS Schmitt Trigger	V_{T+}	V_{DDQ}-2.7		Volts	V_{DDQ}=V_{DDQ} Max
		V_{T-}		V_{DDQ}-4.2		V_{DDQ}=V_{DDQ} Min
I5	Input Voltage CMOS	V_{IH}	V_{DD}-1.2		Volts	V_{DD}=V_{DD} Max
		V_{IL}		V_{DD}-2.5		V_{DD}=V_{DD} Min
I6	Input Voltage CMOS Schmitt Trigger	V_{T+}	V_{DD}-0.6		Volts	V_{DD}=V_{DD} Max
		V_{T-}		V_{DD}-2.55		V_{DD}=V_{DD} Min

T11-8.2 1211

1. I1-I4 are for host side interface only. I5-I6 are for flash media interface only.

TABLE 11-9: INPUT VOLTAGE CHARACTERISTICS (Ta = -40°C to +85°C), V_{DD} = V_{DDQ} = 3.135-3.465V

Type[1]	Parameter	Symbol	Min	Max	Units	Conditions
I1	Input Voltage CMOS	V_{IH}	V_{DDQ}-1.3		Volts	V_{DDQ}=V_{DDQ} Max
		V_{IL}		V_{DDQ}-2.5		V_{DDQ}=V_{DDQ} Min
I2	Input Voltage CMOS	V_{IH}	V_{DDQ}-1.3		Volts	V_{DDQ}=V_{DDQ} Max
		V_{IL}		V_{DDQ}-2.5		V_{DDQ}=V_{DDQ} Min
I3	Input Voltage CMOS Schmitt Trigger	V_{T+}	V_{DDQ}-1.3		Volts	V_{DDQ}=V_{DDQ} Max
		V_{T-}		V_{DDQ}-2.7		V_{DDQ}=V_{DDQ} Min
I4	Input Voltage CMOS Schmitt Trigger	V_{T+}	V_{DDQ}-1.3		Volts	V_{DDQ}=V_{DDQ} Max
		V_{T-}		V_{DDQ}-2.5		V_{DDQ}=V_{DDQ} Min
I5	Input Voltage CMOS	V_{IH}	V_{DD}-1.2		Volts	V_{DD}=V_{DD} Max
		V_{IL}		V_{DD}-2.5		V_{DD}=V_{DD} Min
I6	Input Voltage CMOS Schmitt Trigger	V_{T+}	V_{DD}-0.6		Volts	V_{DD}=V_{DD} Max
		V_{T-}		V_{DD}-2.55		V_{DD}=V_{DD} Min

T11-9.4 1211

1. I1-I4 are for host side interface only. I5-I6 are for flash media interface only.

TABLE 11-10: INPUT VOLTAGE CHARACTERISTICS (Ta = -40°C to +85°C), V_{DDQ} = 4.5-5.5V, V_{DD} = 3.135-3.465V

Type[1]	Parameter	Symbol	Min	Max	Units	Conditions
I1	Input Voltage CMOS	V_{IH}	V_{DDQ}-2.7		Volts	V_{DDQ}=V_{DDQ} Max
		V_{IL}		V_{DDQ}-4.2		V_{DDQ}=V_{DDQ} Min
I2	Input Voltage CMOS	V_{IH}	V_{DDQ}-2.3		Volts	V_{DDQ}=V_{DDQ} Max
		V_{IL}		V_{DDQ}-4.2		V_{DDQ}=V_{DDQ} Min
I3	Input Voltage CMOS Schmitt Trigger	V_{T+}	V_{DDQ}-2.7		Volts	V_{DDQ}=V_{DDQ} Max
		V_{T-}		V_{DDQ}-4.2		V_{DDQ}=V_{DDQ} Min
I4	Input Voltage CMOS Schmitt Trigger	V_{T+}	V_{DDQ}-2.7		Volts	V_{DDQ}=V_{DDQ} Max
		V_{T-}		V_{DDQ}-4.2		V_{DDQ}=V_{DDQ} Min
I5	Input Voltage CMOS	V_{IH}	V_{DD}-1.2		Volts	V_{DD}=V_{DD} Max
		V_{IL}		V_{DD}-2.5		V_{DD}=V_{DD} Min
I6	Input Voltage CMOS Schmitt Trigger	V_{T+}	V_{DD}-0.6		Volts	V_{DD}=V_{DD} Max
		V_{T-}		V_{DD}-2.55		V_{DD}=V_{DD} Min

T11-10.4 1211

1. I1-I4 are for host side interface only. I5-I6 are for flash media interface only.

11.1.2 Output Characteristics

TABLE 11-11: OUTPUT VOLTAGE CHARACTERISTICS (Ta = 0°C to +70°C), V_{DD} = V_{DDQ} = 3.135-3.465V

Type[1]	Parameter	Symbol	Min	Max	Units	Conditions
O1	Output Voltage	V_{OH}	V_{DD}-0.9		Volts	I_{OH}=-1.3 mA, V_{DD}=V_{DDQ}=V_{DDQ} Min
		V_{OL}		V_{DD}-3.0		I_{OL}=1.3 mA, V_{DD}=V_{DDQ}=V_{DDQ} Min
O2	Output Voltage	V_{OH}	V_{DDQ}-1.0		Volts	I_{OH}=-2.5 mA, V_{DD}=V_{DDQ}=V_{DDQ} Min
		V_{OL}		V_{DDQ}-2.9		I_{OL}=2.5 mA, V_{DD}=V_{DDQ}=V_{DDQ} Min
O3	Output Voltage	V_{OH}	V_{DD}-0.9		Volts	I_{OH}=-4 mA, V_{DD}=V_{DDQ}=V_{DDQ} Min
		V_{OL}		V_{DD}-3.0		I_{OL}=4 mA, V_{DD}=V_{DDQ}=V_{DDQ} Min
O4	Output Voltage	V_{OH}	V_{DDQ}-1.0		Volts	I_{OH}=-5 mA, V_{DD}=V_{DDQ}=V_{DDQ} Min
		V_{OL}		V_{DDQ}-2.9		I_{OL}=5 mA, V_{DD}=V_{DDQ}=V_{DDQ} Min

T11-11.4 1211

1. O2 and O4 are for host side interface only. O1 and O3 are for flash media interface only.

TABLE 11-12: OUTPUT VOLTAGE CHARACTERISTICS (Ta = 0°C to +70°C), V_{DDQ} = 4.5-5.5V, V_{DD} = 3.135-3.465V

Type[1]	Parameter	Symbol	Min	Max	Units	Conditions
O1	Output Voltage	V_{OH}	V_{DD}-0.9		Volts	I_{OH}=-1.3 mA, V_{DD}=V_{DD} Min, V_{DDQ}=V_{DDQ} Min
		V_{OL}		V_{DD}-3.0		I_{OL}=1.3 mA, V_{DD}=V_{DD} Min, V_{DDQ}=V_{DDQ} Min
O2	Output Voltage	V_{OH}	V_{DDQ}-1.3		Volts	I_{OH}=-4 mA, V_{DD}=V_{DD} Min; V_{DDQ}=V_{DDQ} Min
		V_{OL}		V_{DDQ}-4.6		I_{OL}=4 mA, V_{DD}=V_{DD} Min, V_{DDQ}=V_{DDQ} Min
O3	Output Voltage	V_{OH}	V_{DD}-0.9		Volts	I_{OH}=-4 mA, V_{DD}=V_{DD} Min, V_{DDQ}=V_{DDQ} Min
		V_{OL}		V_{DD}-3.0		I_{OL}=4 mA, V_{DD}=V_{DD} Min, V_{DDQ}=V_{DDQ} Min
O4	Output Voltage	V_{OH}	V_{DDQ}-1.3		Volts	I_{OH}=-8 mA, V_{DD}=V_{DD} Min; V_{DDQ}=V_{DDQ} Min
		V_{OL}		V_{DDQ}-4.6		I_{OL}=8 mA, V_{DD}=V_{DD} Min, V_{DDQ}=V_{DDQ} Min

T11-12.2 1211

1. O2 and O4 are for host side interface only. O1 and O3 are for flash media interface only.

TABLE 11-13: OUTPUT VOLTAGE CHARACTERISTICS (Ta = -40°C to +85°C), V_{DD} = V_{DDQ} = 3.135-3.465V

Type[1]	Parameter	Symbol	Min	Max	Units	Conditions
O1	Output Voltage	V_{OH}	V_{DD}-0.9		Volts	I_{OH}=-1.3 mA, V_{DD}=V_{DDQ}=V_{DDQ} Min
		V_{OL}		V_{DD}-3.0		I_{OL}=1.3 mA, V_{DD}=V_{DDQ}=V_{DDQ} Min
O2	Output Voltage	V_{OH}	V_{DDQ}-1.0		Volts	I_{OH}=-2 mA, V_{DD}=V_{DDQ}=V_{DDQ} Min
		V_{OL}		V_{DDQ}-2.9		I_{OL}=2 mA, V_{DD}=V_{DDQ}=V_{DDQ} Min
O3	Output Voltage	V_{OH}	V_{DD}-0.9		Volts	I_{OH}=-4 mA, V_{DD}=V_{DDQ}=V_{DDQ} Min
		V_{OL}		V_{DD}-3.0		I_{OL}=4 mA, V_{DD}=V_{DDQ}=V_{DDQ} Min
O4	Output Voltage	V_{OH}	V_{DDQ}-1.0		Volts	I_{OH}=-4 mA, V_{DD}=V_{DDQ}=V_{DDQ} Min
		V_{OL}		V_{DDQ}-2.9		I_{OL}=4 mA, V_{DD}=V_{DDQ}=V_{DDQ} Min

T11-13.9 1211

1. O2 and O4 are for host side interface only. O1 and O3 are for flash media interface only.

TABLE 11-14: OUTPUT VOLTAGE CHARACTERISTICS (Ta = -40°C to +85°C), V_{DDQ} = 4.5-5.5V, V_{DD} = 3.135-3.465V

Type[1]	Parameter	Symbol	Min	Max	Units	Conditions
O1	Output Voltage	V_{OH}	V_{DD}-0.9		Volts	I_{OH}=-1.3 mA, V_{DD}=V_{DD} Min, V_{DDQ}=V_{DDQ} Min
		V_{OL}		V_{DD}-3.0		I_{OL}=1.3 mA, V_{DD}=V_{DD} Min, V_{DDQ}=V_{DDQ} Min
O2	Output Voltage	V_{OH}	V_{DDQ}-1.3		Volts	I_{OH}=-3 mA, V_{DD}=V_{DD} Min; V_{DDQ}=V_{DDQ} Min
		V_{OL}		V_{DDQ}-4.6		I_{OL}=3 mA, V_{DD}=V_{DD} Min, V_{DDQ}=V_{DDQ} Min
O3	Output Voltage	V_{OH}	V_{DD}-0.9		Volts	I_{OH}=-4 mA, V_{DD}=V_{DD} Min, V_{DDQ}=V_{DDQ} Min
		V_{OL}		V_{DD}-3.0		I_{OL}=4 mA, V_{DD}=V_{DD} Min, V_{DDQ}=V_{DDQ} Min
O4	Output Voltage	V_{OH}	V_{DDQ}-1.3		Volts	I_{OH}=-6 mA, V_{DD}=V_{DD} Min; V_{DDQ}=V_{DDQ} Min
		V_{OL}		V_{DDQ}-4.6		I_{OL}=6 mA, V_{DD}=V_{DD} Min, V_{DDQ}=V_{DDQ} Min

T11-14.7 1211

1. O2 and O4 are for host side interface only. O1 and O3 are for flash media interface only.

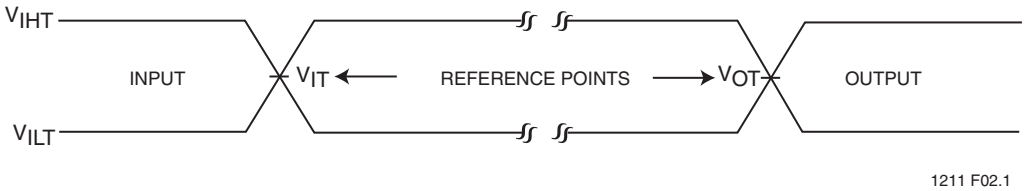
TABLE 11-15: DC CHARACTERISTICS, V_{DDQ} = 4.5-5.5V, V_{DD} = 3.135-3.465V

Symbol	Parameter	Typ	Max	Units	Conditions
I_{DD}active[1,2]	Power supply current (Ta = -40°C to +85°C)	35	50	mA	V_{DD}=V_{DD} Max; V_{DDQ}=V_{DDQ} Max
I_{SP}	Sleep/Standby/Idle current (Ta = 0°C to +70°C)	50	75	µA	V_{DD}=V_{DD} Max; V_{DDQ}=V_{DDQ} Max
I_{SP}	Sleep/Standby/Idle current (Ta = -40°C to +85°C)	75	200	µA	V_{DD}=V_{DD} Max; V_{DDQ}=V_{DDQ} Max

T11-15.7 1211

1. Sequential data transfer for 1 sector read data from Host interface and write data to media.
2. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

11.2 AC Characteristics



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <10 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 11-1: AC INPUT/OUTPUT REFERENCE WAVEFORMS

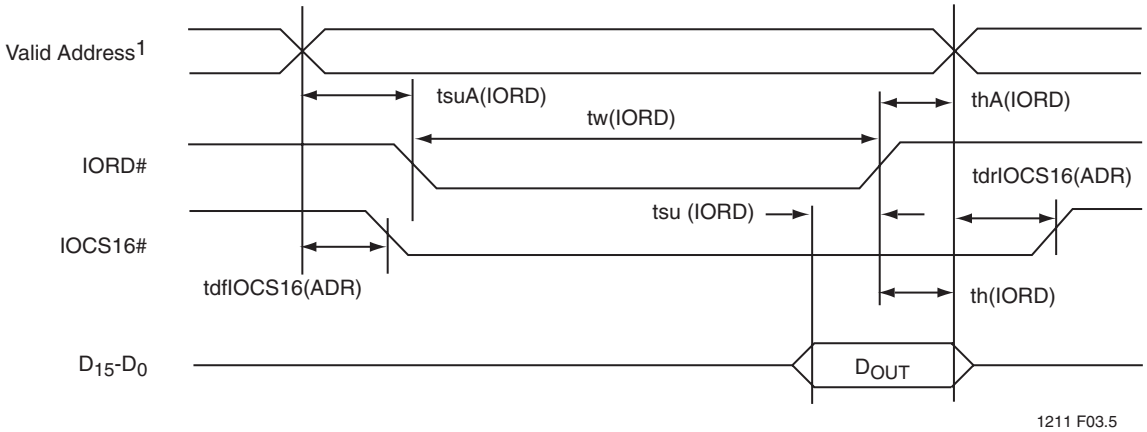
11.2.1 Host Side Interface I/O Input (Read) Timing Specification

TABLE 11-16: HOST SIDE INTERFACE I/O READ TIMING

Item	Symbol	Min	Max	Units
Data Setup before IORD#	tsu(IORD)	20	-	ns
Data Hold following IORD#	th(IORD)	5	-	ns
IORD# Width Time	tw(IORD)	70	-	ns
Address Setup before IORD#	tsuA(IORD)	25	-	ns
Address Hold following IORD#	thA(IORD)	10	-	ns
IOCS16# Delay Falling from Address	tdfIOCS16(ADR)	-	20	ns
IOCS16# Delay Rising from Address	tdrIOCS16(ADR)	-	20	ns

T11-16.6 1211

Note: The maximum load on IOCS16# is 1 LSTTL with 50pF total load.
All AC specifications are guaranteed by design.



1. Valid Address consists of signals CS1FX#, CS3FX# and A_2-A_0.

FIGURE 11-2: HOST SIDE INTERFACE I/O READ TIMING DIAGRAM

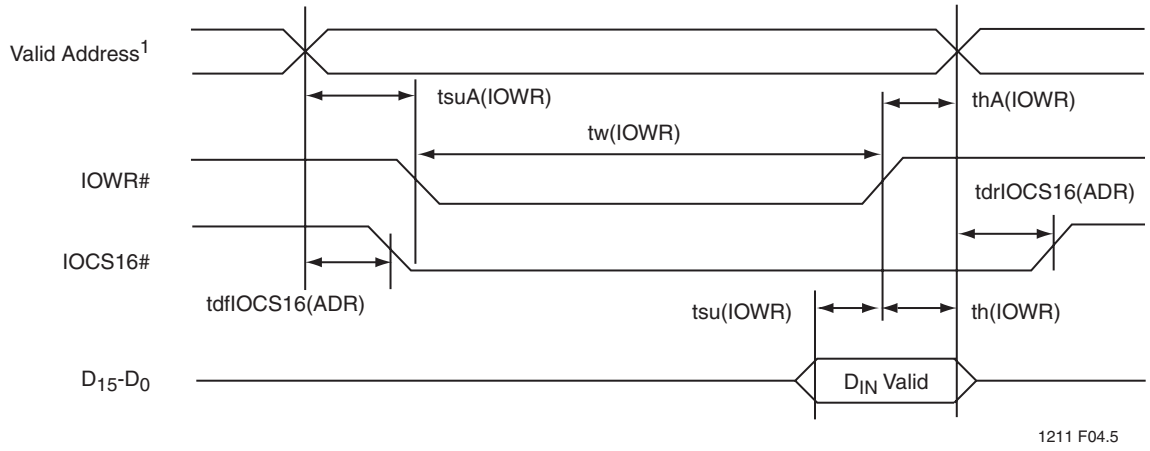
11.2.2 Host Side Interface I/O Output (Write) Timing Specification

TABLE 11-17: HOST SIDE INTERFACE I/O WRITE TIMING SPECIFICATION

Item	Symbol	Min	Max	Units
Data Setup before IOWR#	tsu(IOWR)	20	-	ns
Data Hold following IOWR#	th(IOWR)	10	-	ns
IOWR# Width Time	tw(IOWR)	70	-	ns
Address Setup before IOWR#	tsuA(IOWR)	25	-	ns
Address Hold following IOWR#	thA(IOWR)	10	-	ns
IOCS16# Delay Falling from Address	tdfIOCS16(ADR)	-	20	ns
IOCS16# Delay Rising from Address	tdrIOCS16(ADR)	-	20	ns

T11-17.5 1211

Note: The maximum load on IOCS16# is 1 LSTTL with 50pF total load.
All AC specifications are guaranteed by design.



1. Valid Address consists of signals CS1FX#, CS3FX# and A_2-A_0.

FIGURE 11-3: HOST SIDE INTERFACE I/O WRITE TIMING DIAGRAM

11.2.3 Media Side Interface I/O Timing Specifications

TABLE 11-18: SST55LD017A/B/C TIMING PARAMETERS

Item	Symbol	Min	Max	Units
FCLE Setup Time	T_{CLS}	30	-	ns
FCLE Hold Time	T_{CLH}	30	-	ns
FCE# Setup Time	T_{CS}	30	-	ns
FCE# Hold Time for Command/Data Write Cycle	T_{CH}	30	-	ns
FCE# Hold Time for Sequential Read Last Cycle	T_{CHR}	-	30	ns
FWE# Pulse Width	T_{WP}	30	-	ns
FWE# High Hold Time	T_{WH}	30	-	ns
Write Cycle Time	T_{WC}	60	-	ns
FALE Setup Time	T_{ALS}	30	-	ns
FALE Hold Time	T_{ALH}	30	-	ns
FAD[7:0] Setup Time	T_{DS}	25	-	ns
FAD[7:0] Hold Time	T_{DH}	25	-	ns
FRE# Pulse Width	T_{RP}	30	-	ns
Ready to FRE# Low	T_{RR}	30	-	ns
FRE# Data Setup Access Time	T_{REA}	20	-	ns
Read Cycle Time	T_{RC}	60	-	ns
FRE# High Hold Time	T_{REH}	30	-	ns
FRE# High to Data Hi-Z	T_{RHZ}	5	-	ns

T11-18.9 1211

Note: All AC specifications are guaranteed by design.

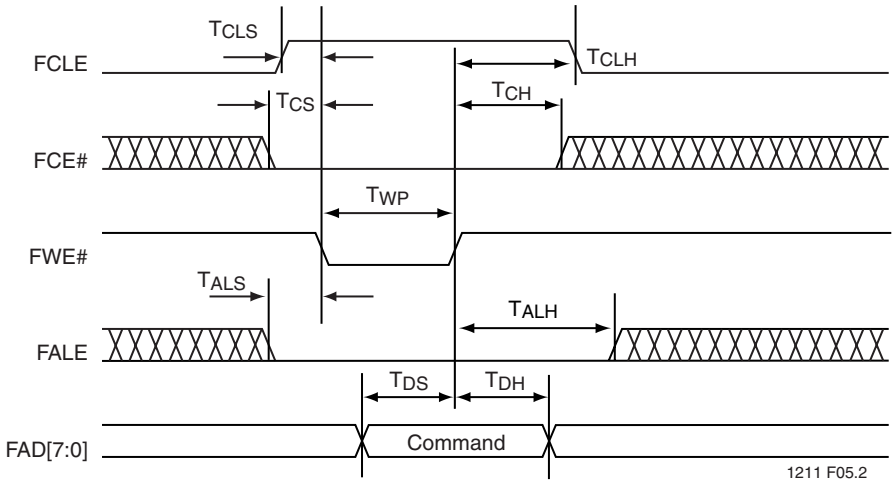


FIGURE 11-4: MEDIA COMMAND LATCH CYCLE

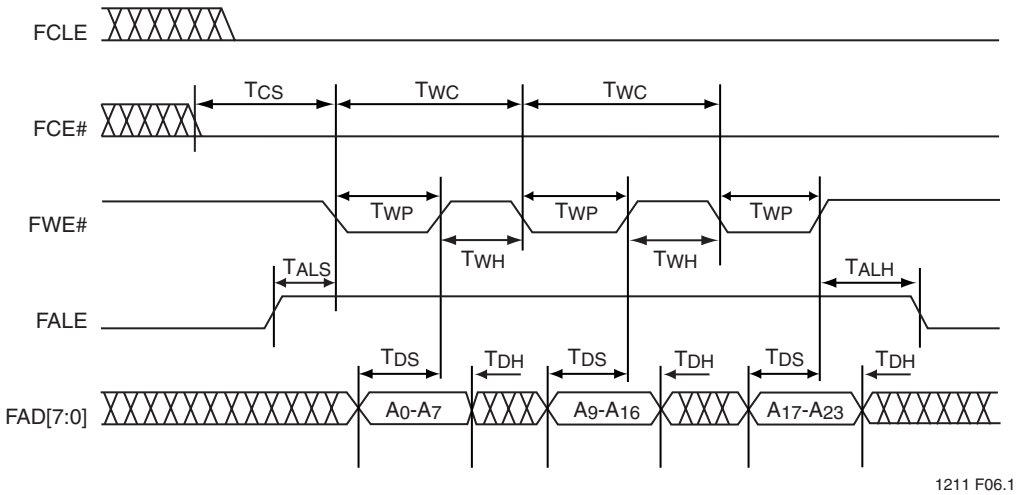


FIGURE 11-5: MEDIA ADDRESS LATCH CYCLE

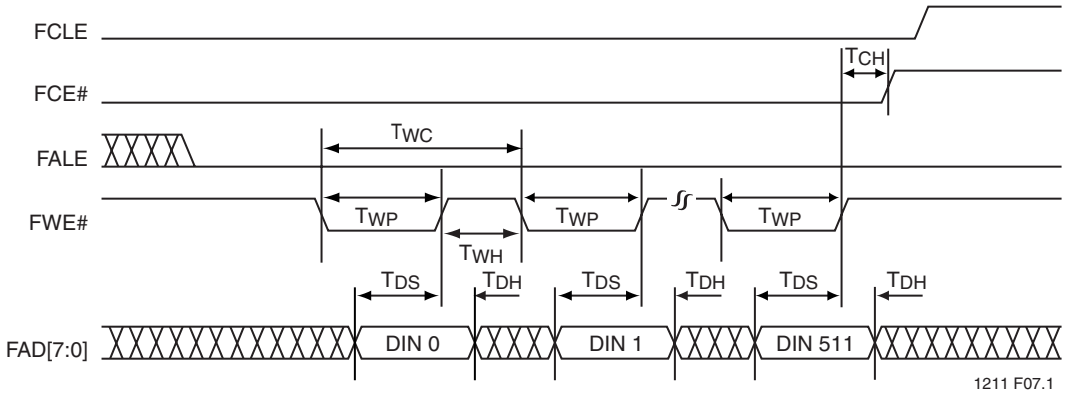


FIGURE 11-6: MEDIA DATA LOADING LATCH CYCLE

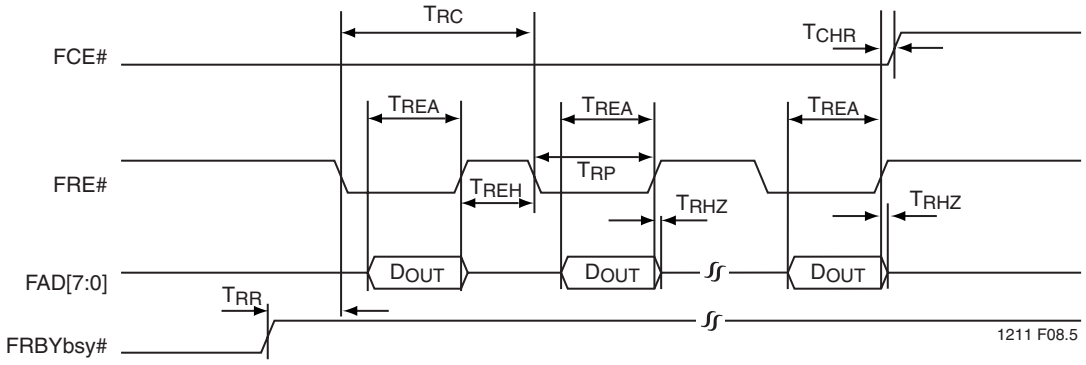


FIGURE 11-7: MEDIA DATA READ CYCLE

12.0 APPENDIX

12.1 Differences between SST ATA Flash Disk Controller and ATA/ATAPI-5 Specifications

12.1.1 Idle Timer

The Idle timer uses an incremental value of 5 ms, rather than the 5 sec minimum increment value specified in ATA specifications.

12.1.2 Recovery from Sleep Mode

For ATA flash disk controller devices, recovery from sleep mode is accomplished by simply issuing another command to the device. A hardware or software reset is not required.

12.2 Reference Design Schematics

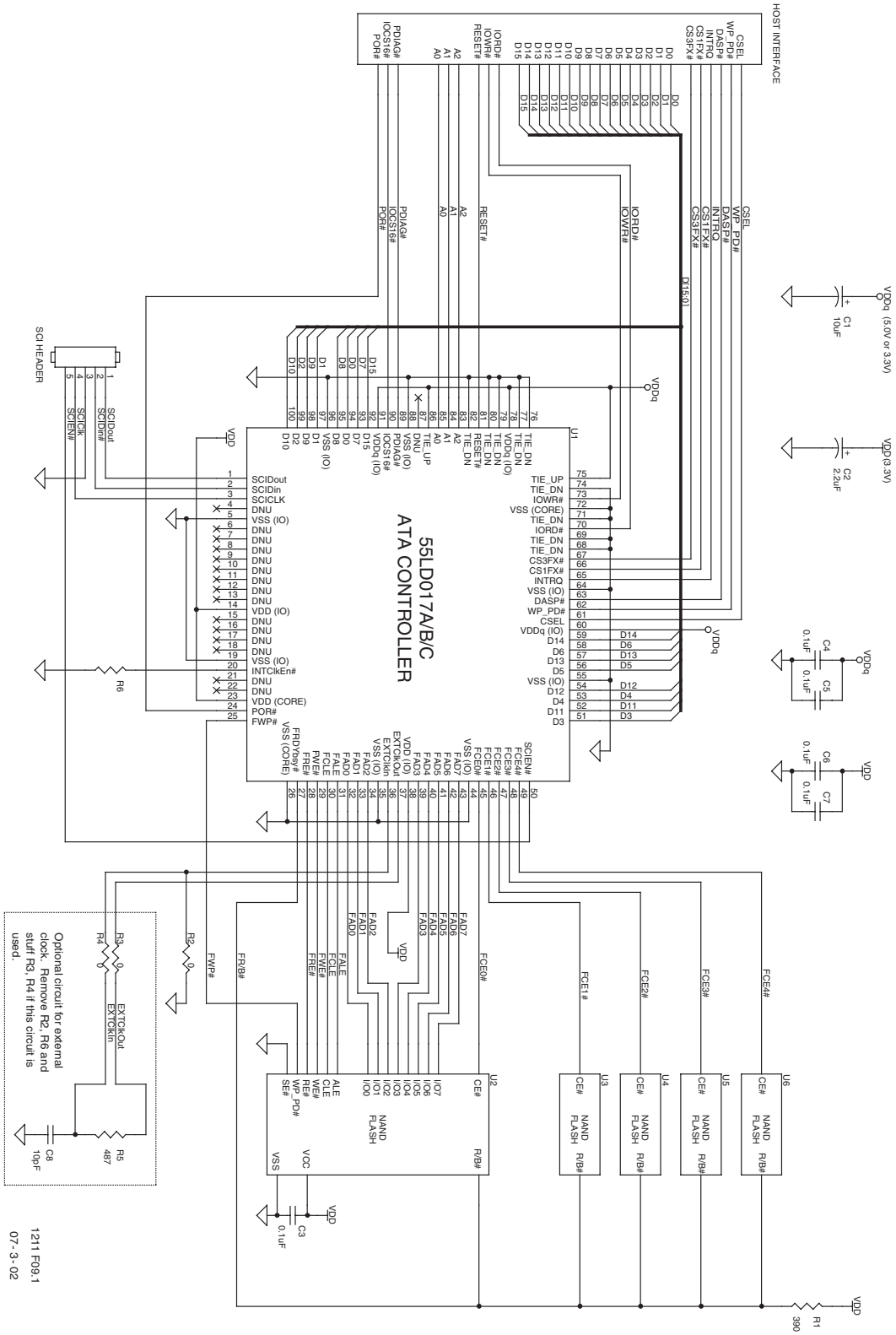


FIGURE 12-1: SCHEMATIC FOR ATA FLASH MODULE, UP TO 640 MBYTE

12.3 Bill of Materials

TABLE 12-1: SAMPLE BILL OF MATERIALS

Item	Specification
U1	SST55LD017A/B/C ATA flash disk controller
U2 to U6	NAND Flash Media Chip
C1	10 µF
C2	2.2 µF
C3 to C7	0.1 µF
R1	390Ω

T12-1.3 1211

TABLE 12-2: OPTIONAL COMPONENTS

Item	Specification
R2 to R4	0Ω
R5	487Ω
R6	0Ω
C8	10 pF

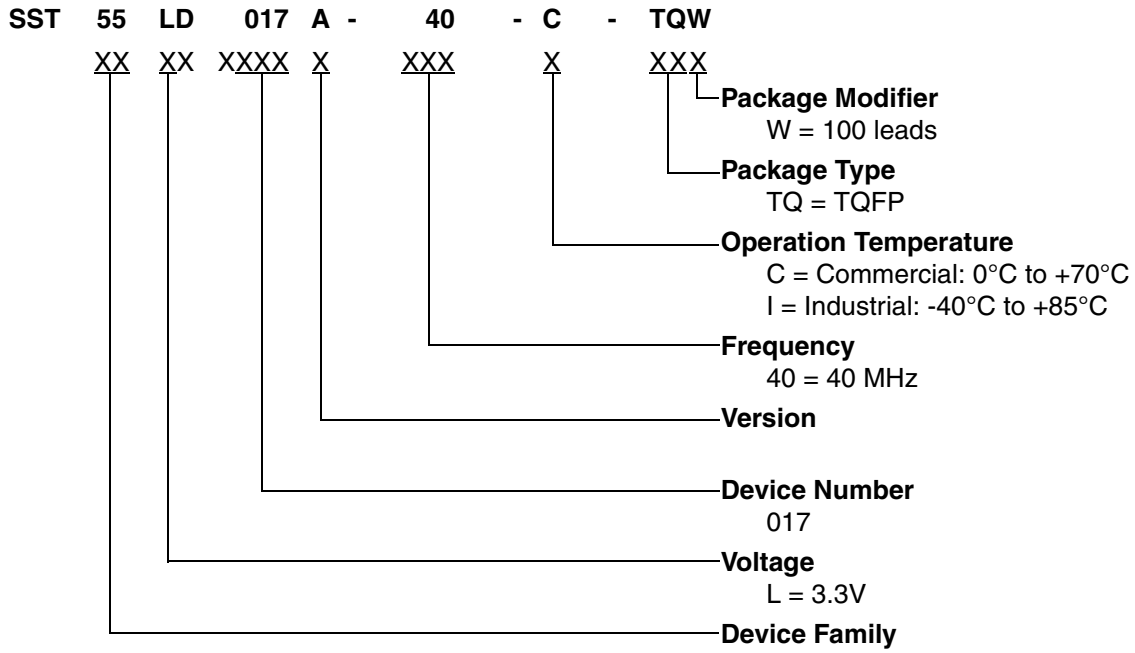
T12-2.0 1211

TABLE 12-3: SUPPORTED NAND FLASH MEDIA

NAND Flash Media Density	Manufacturer	Part Number
32MB	Samsung	KM29W32000T
	Samsung	K9F3208W0A
64MB	Samsung	KM29U64000T
	Samsung	K9F6408U0B
	Toshiba	TC58V64FT
128MB	Samsung	KM29U128T
	Samsung	K9F2808U0B
	Toshiba	TC58128FT
256MB	Samsung	KM29U256T
	Samsung	K9F5608U0A
	Toshiba	TC58256FT
512MB	Samsung	K9F1208U0M
	Toshiba	TC58512FT
1GB	Samsung	K9K1G08U0M
	Toshiba	TH58100FT

T12-3.4 1211

13.0 PRODUCT ORDERING INFORMATION



13.1 Valid Combinations

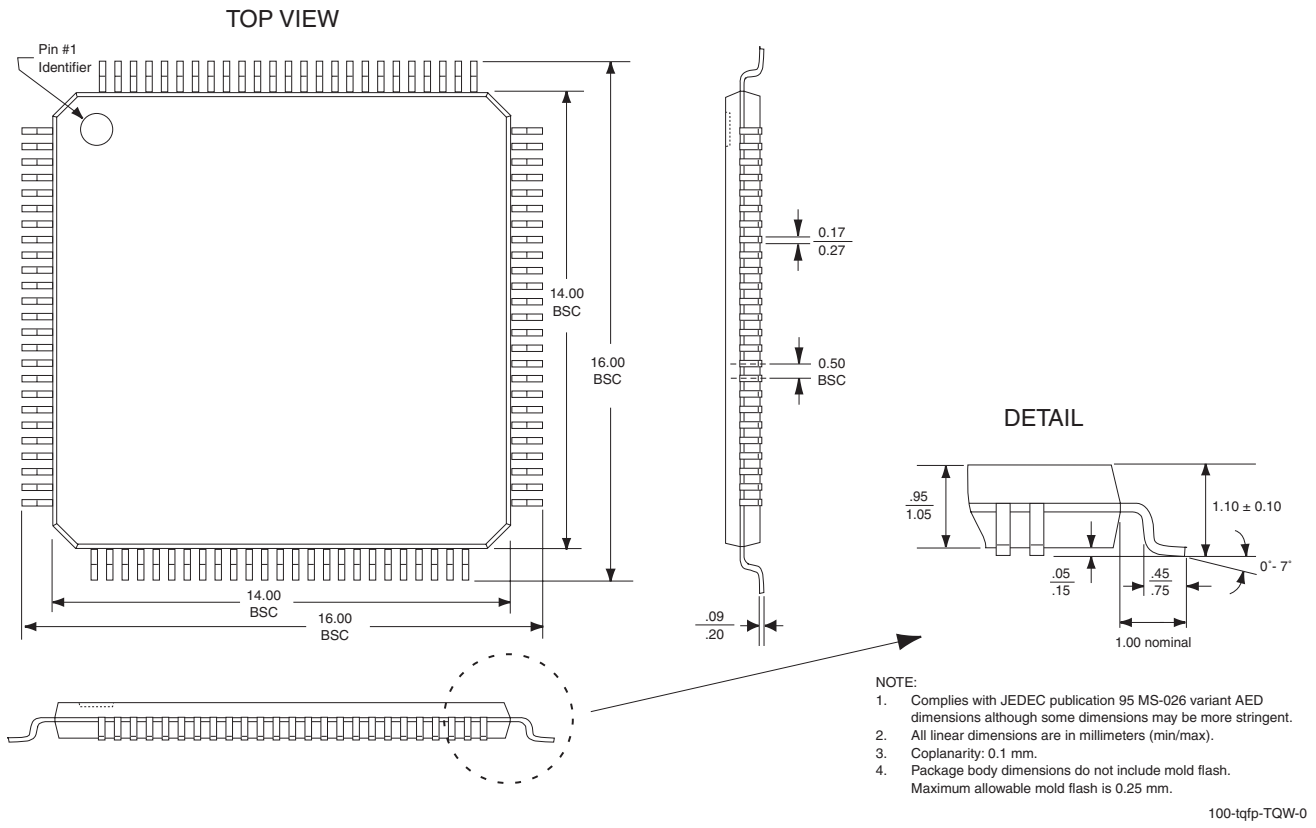
SST55LD017A-40-C-TQW
SST55LD017A-40-I-TQW

SST55LD017B-40-C-TQW
SST55LD017B-40-I-TQW

SST55LD017C-40-C-TQW
SST55LD017C-40-I-TQW

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

14.0 PHYSICAL DIMENSIONS



100-LEAD THIN QUAD FLAT PACK (TQFP)
SST PACKAGE CODE: TQW

TABLE 14-1: REVISION HISTORY

Number	Description	Date
00	• Initial release	Mar 2002
01	• Added B and C versions	Jul 2002
02	• End-of-Life product data sheet for all parts in S71211 • Recommended replacement part for SST55LD017A is SST55LD019A (S71241) • Recommended replacement part for SST55LD017B is SST55LD019B (S71241) • Recommended replacement part for SST55LD017C is SST55LD019C (S71241) • Swapped Product Ordering and Packaging Diagram sections • Added a Revision History table	Aug 2005
03	• End-Of-Life product data sheet for all devices in S71211 • Recommended replacement device is SST55LD017x which can be found S71312	Apr 2006