UMC

T-52-33-15

UM82C55A

CMOS Programmable Peripheral Interface

Features

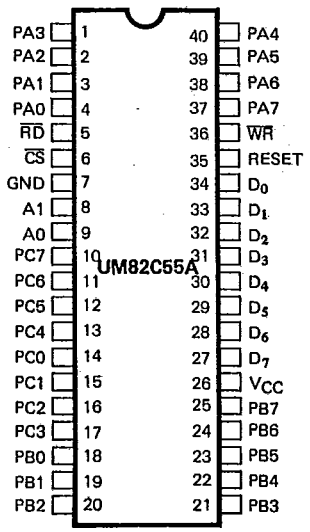
- Pin compatible with NMOS 8255A
- 24 programmable I/O pins
- Fully TTL compatible
- Bus-hold circuitry on all I/O ports eliminates pull-up resistors
- High speed, no "wait state" operation with 8MHz 80C86
- Direct bit set/reset capability
- Enhanced control word read capability
- Single 5V power supply
- 2.5mA drive capability on all I/O port outputs
- Low standby current – I_{CCSB} = 10μA

General Description

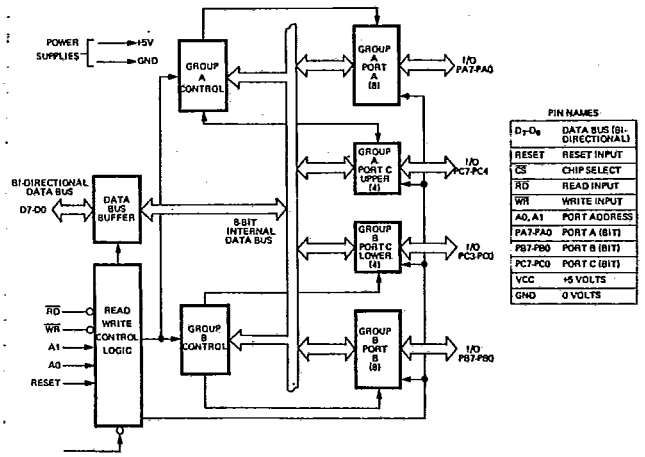
The UM82C55A is a high performance CMOS version of the industry standard 8255A and is manufactured using a self aligned silicon gate CMOS process. It is a general purpose programmable I/O device which may be used with many different microprocessors. There are 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The high performance of the UM82C55A makes it compatible with microprocessors such as the 8086, 8048, 8051.

Static CMOS circuit design ensures low operating power. TTL compatibility of V_{IH}=2.0 volts over the industrial temperature range and bus hold circuitry eliminates the need for pull-up resistors.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Supply Voltage . . . . . +8.0 VOLTS
Operating Voltage Range . . . . . +4V to +7V
Input Voltage Applied . . . . . GND–2.0V to 6.5V
I/O Pin Voltage Applied . . . . . GND–0.5V to VCC+0.5V
Storage Temperature Range . . . . . –65°C to +150°C
Operating Temperature Range . . . . . 0°C to +70°C
Maximum Power Dissipation . . . . . 1 Watt

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Electrical Characteristics

($VCC = 5.0V+/-5\%$; $T_A = 0°C$ to $+70°C$)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IH}	Logical One Input Voltage	2.0		V	
V_{IL}	Logical Zero Input Voltage		0.8	V	
V_{OH}	Logical One Output Voltage	3.0 VCC–0.4		V V	$I_{OH} = -2.5mA$ $I_{OH} = -100\ \mu A$
V_{OL}	Logical Zero Output Voltage		0.4	V	$I_{OL} = +2.5$ mA
I_{IL}	Input Leakage Current	–1.0	1.0	μA	$0V \leqslant V_{IN} \leqslant V_{CC}$
I_O	I/O Pin Leakage Current	–10.0	10.0	μA	$0V \leqslant V_O \leqslant V_{CC}$
I_{BHH}	Bus Hold High Leakage Current	–50	–300	μA	$V_O = 3.0V$ Ports A, B, C
I_{BHL}	Bus Hold Low Leakage Current	+50	+300	μA	$V_O = 1.0V$ Port A only
I_{DAR}	Darlington Drive Current	–2.0		mA	Ports A, B, C Test Condition 3
I_{CC}	Power Supply Current		10	μA	$V_{CC} = 5.5V$ $V_{IN} = V_{CC}$ or G_{ND} Outputs Open

Capacitance

($T_A = 25°C$; $V_{CC} = GND = 0V$; $V_{IN} = +5V$ or GND)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_{IN}*	Input Capacitance		5	pF	FREQ = 1 MHZ Unmeasured Pins Returned to GND
$C_{I/O}$*	I/O Pin Capacitance		20	pF	

*Guaranteed and sampled, but not 100% tested

PC Mainboard

A.C. Characteristics

(V_{CC} = +5V ±5%, GND = 0V; T_A = 0°C to +70°C)

READ

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AR}	Address Stable Before READ	0		ns	
t_{RA}	Address Stable After READ	0		ns	
t_{RR}	READ Pulse Width	150		ns	
t_{RD}	Data Valid From READ		100	ns	1
t_{DF}	Data Float After READ	10	75	ns	2
t_{RV}	Time Between READs and/or WRITEs	300		ns	

WRITE

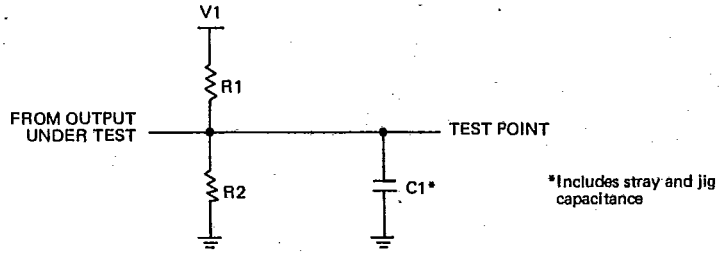
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AW}	Address Stable Before WRITE	0		ns	
t_{WA}	Address Stable After WRITE	20		ns	Ports A & B
		60		ns	Port C
t_{WW}	WRITE Pulse Width	100		ns	
t_{DW}	Data Valid to WRITE High	100		ns	
t_{WD}	Data Valid After WRITE High	30		ns	Ports A & B
		60		ns	Port C

OTHER TIMING

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{WB}	WR = 1 to Output		350	ns	1
t_{IR}	Peripheral Data Before RD	0		ns	
t_{HR}	Peripheral Data After RD	0		ns	
t_{AK}	ACK Pulse Width	100		ns	
t_{ST}	STB Pulse Width	100		ns	
t_{PS}	Per. Data Before STB High	20		ns	
t_{PH}	Per. Data After STB High	50		ns	
t_{AD}	ACK = 0 to Output		175	ns	1
t_{KD}	ACK = 1 to Output Float	20	250	ns	2
t_{WOB}	WR = 1 to OBF = 0		150	ns	1
t_{AOB}	ACK = 0 to OBF = 1		150	ns	1
t_{SIB}	STB = 0 to IBF = 1		150	ns	1
t_{RIB}	RD = 1 to IBF = 0		150	ns	1
t_{RIT}	RD = 0 to INTR = 0		200	ns	1
t_{SIT}	STB = 1 to INTR = 1		150	ns	1
t_{AIT}	ACK = 1 to INTR = 1		150	ns	1
t_{WIT}	WR = 0 to INTR = 0		200	ns	1
t_{RES}	Reset Pulse Width	500		ns	see note 1

Note: Period of initial Reset pulse after power-on must be at least 50usec. Subsequent Reset pulses may be 500 ns minimum.

A.C. Test Circuits

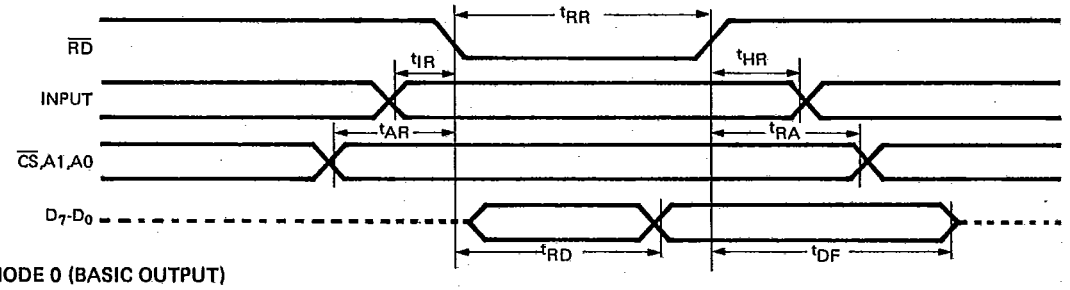


Test Condition	V1	R1	R2	C1
1	1.7V	523Ω	Open	150 pf
2	5.0V	2kΩ	1.7kΩ	50 pf
3	1.5V	750Ω	Open	Open

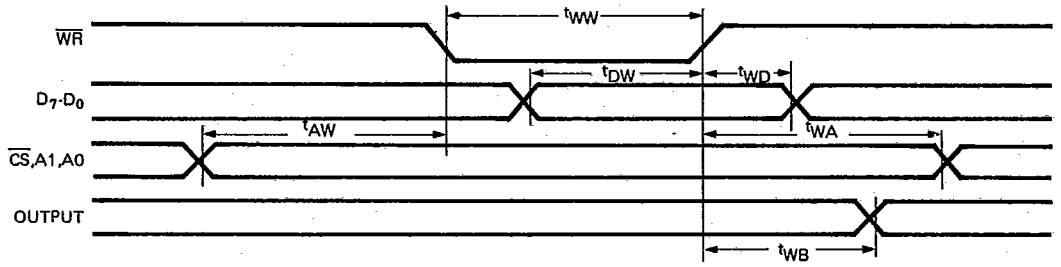
TEST CONDITION DEFINITION TABLE

Timing Waveforms

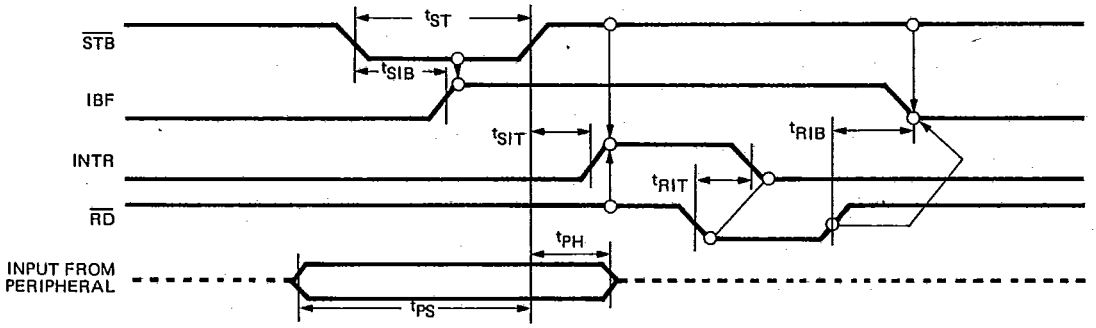
MODE 0 (BASIC INPUT)



MODE 0 (BASIC OUTPUT)

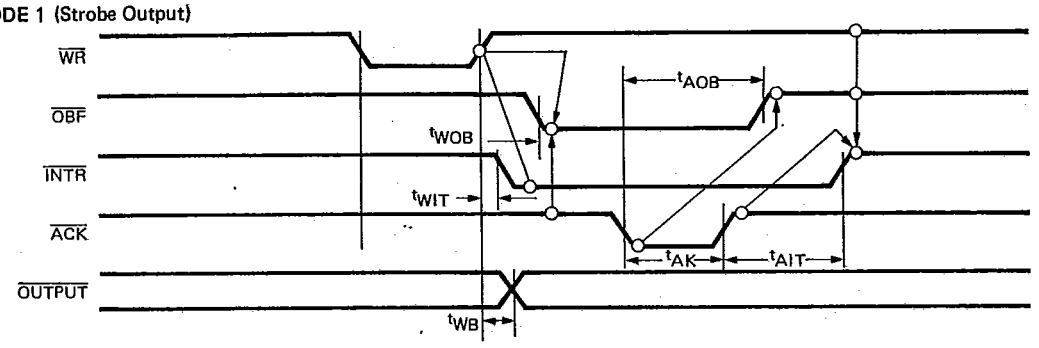


MODE 1 (STROBED INPUT)

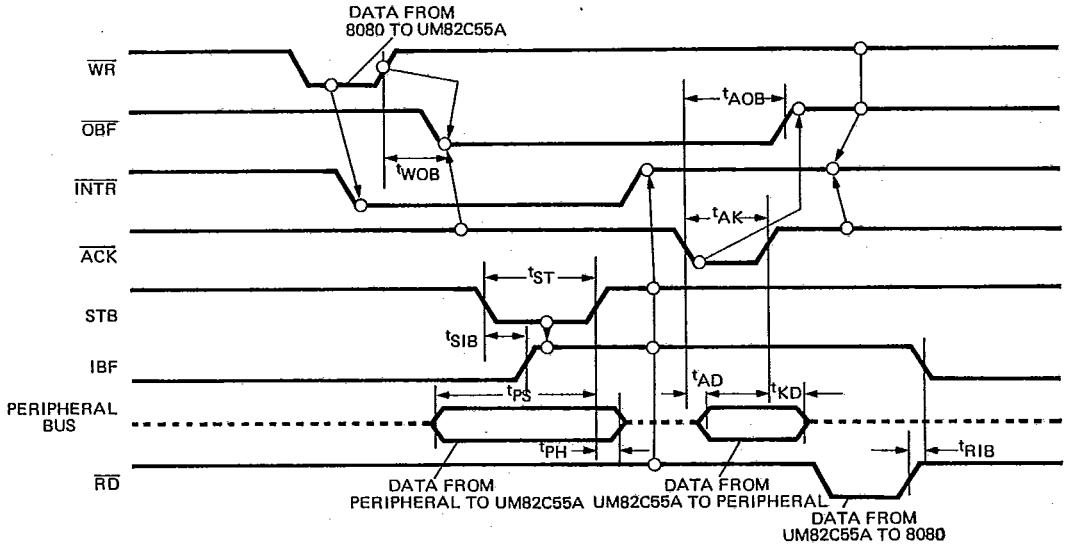


Timing Waveforms (Continued)

MODE 1 (Strobe Output)

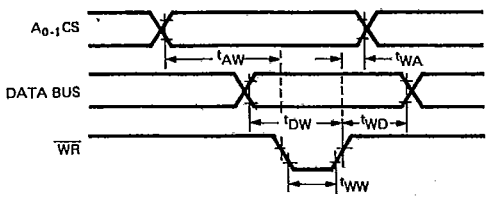


MODE 2 (BIDIRECTIONAL)

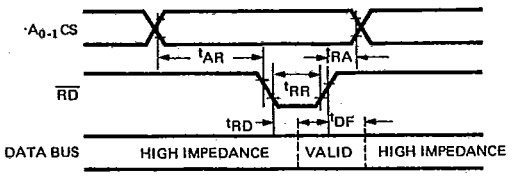


Note: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible. ($INTR = IBF \cdot \overline{MASK} \cdot \overline{STB} \cdot \overline{RD} + \overline{OBF} \cdot \overline{MASK} \cdot \overline{ACK} \cdot \overline{WR}$)

WRITE TIMING



READ TIMING



Pin Description

Data Bus Buffer
This 3-state bidirectional 8-bit buffer is used to interface the UM82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic
The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control buses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)
Chip Select. A "low" on this input pin enables the communication between the UM82C55A and the CPU.

($\overline{RD}$)
Read. A "low" on this input pin enables the UM82C55A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the UM82C55A.

($\overline{WR}$)
Write. A "low" on this input pin enables the CPU to write data or control words into the UM82C55A.

(A_0 and A_1)
Port Select 0 and Port Select 1. These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A_0 and A_1).

UM82C55A BASIC OPERATION

A_0	A_1	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Input Operation (Read)
0	0	0	1	0	Port A → Data Bus
0	1	0	1	0	Port B → Data Bus
1	0	0	1	0	Port C → Data Bus
1	1	0	1	0	Control Word → Data Bus
					Output Operation (Write)
0	0	1	0	0	Data Bus → Port A
0	1	1	0	0	Data Bus → Port B
1	0	1	0	0	Data Bus → Port C
1	1	1	0	0	Data Bus → Control
					Disable Function
x	x	x	x	1	Data Bus → 3-State
x	x	1	1	0	Data Bus → 3-State

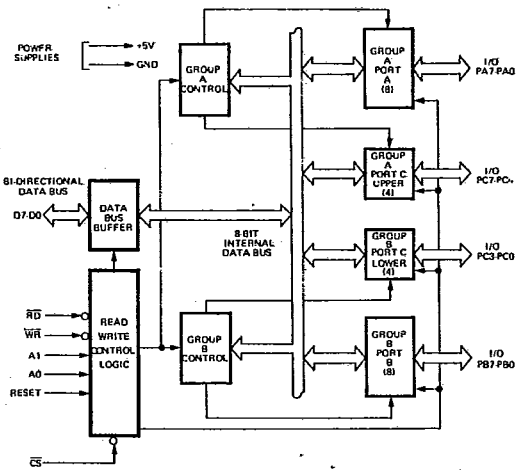


Figure 1. UM82C55A Block Diagram Data Bus Buffer and Read/Write Control Logic Functions

(Reset)
Reset. A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode. "Bus hold" devices internal to the UM82C55A will hold the I/O port inputs to a logic "1" state with a maximum hold current of 300 μA.

Group A and Group B Controls
The functional configuration of each port is programmed by the system software. In essence, the CPU "outputs" a control word to the UM82C55A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the UM82C55A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A– Port A and Port C upper (C7-C4)
Control Group B–Port B and Port C lower (C3-C0)

The control word register can be both written and read as shown in the "Basic Operation" table. Figure 4 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic "1", as this implies control word mode information.

Ports A, B and C
The UM82C55A contains three 8-bit ports (A, B, and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the UM82C55A.

Port A One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull-up" and "pull-down" bus-hold devices are present on Port A.

Port B One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input) This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

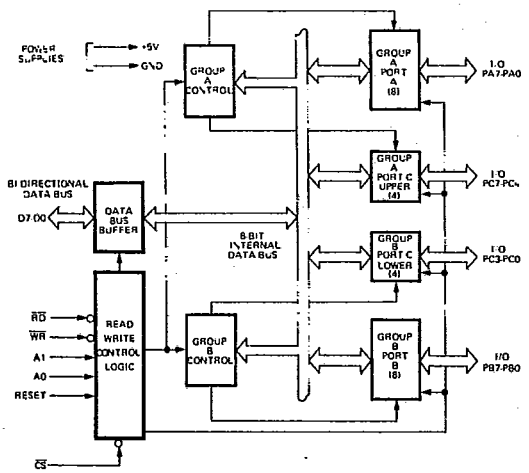


Figure 2. UM82C55A Block Diagram Showing Group A and Group B Control Functions

Operational Description

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 – Basic Input/Output
Mode 1 – Strobed Input/Output
Mode 2 – Bi-Directional Bus

When the reset input goes "high", all ports will be set to the input mode with all 24 port lines held at a logic "one" level by internal bus hold devices. After the reset is removed, the UM82C55A can remain in the input mode with no additional initialization required. This eliminates the need for pullup or pulldown resistors in all-CMOS designs. During the execution of the system program, any of the other modes may be selected using a single output instruction. This allows a single UM82C55A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance: Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

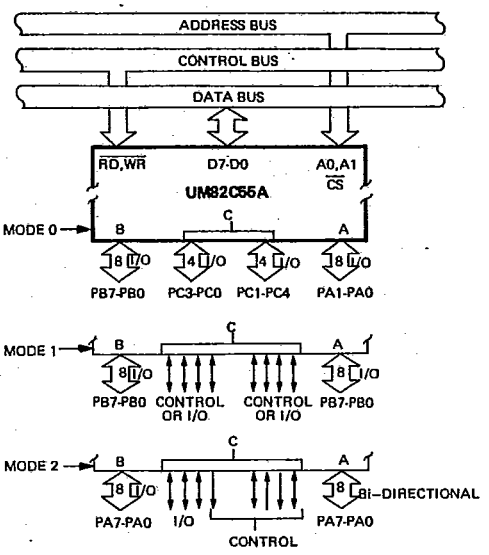


Figure 3. Basic Mode Definitions and Bus Interface

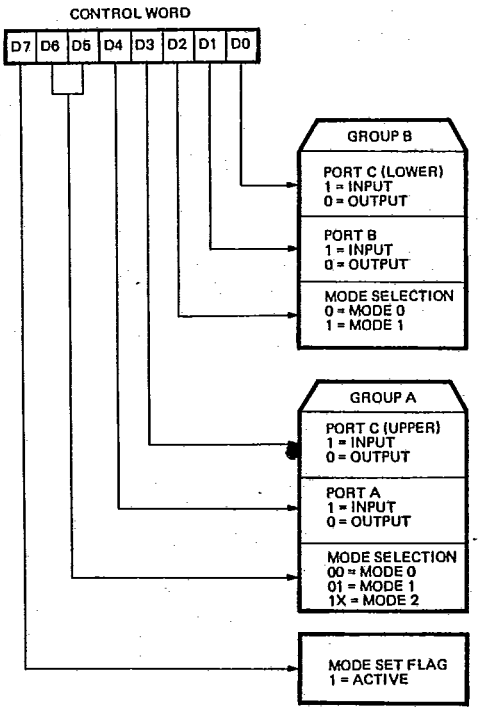


Figure 4. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the UM82C55A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

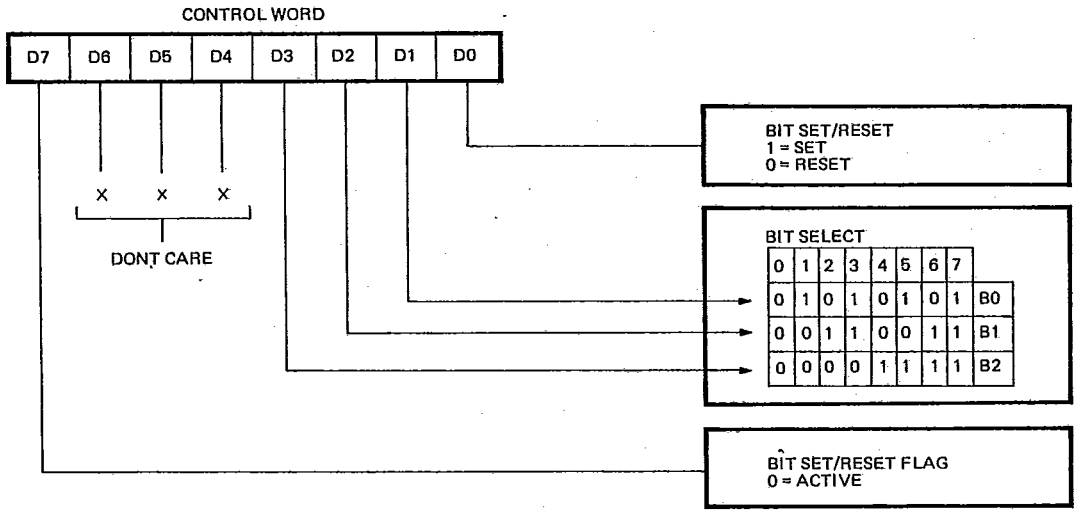


Figure 5. Bit Set/Reset Format

Single Bit Set/Reset Feature
Any of the eight bits of Port C can be Set or Reset using a single OUT put instruction. This feature reduces software requirements in control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions
When the UM82C55A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the programmer to enable or disable a CPU interrupt by a specific I/O device without affecting any other device in the interrupt structure.

INTE Flip-flop Definition
(BIT-SET) – INTE is SET – Interrupt enable.
(BIT–RESET) – INTE is RESET – Interrupt disable.

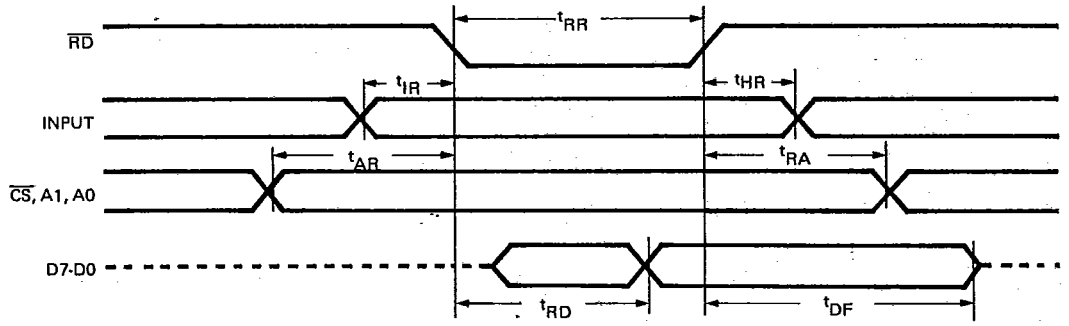
Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes
Mode 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No handshaking is required, data is simply written to or read from a specific port.

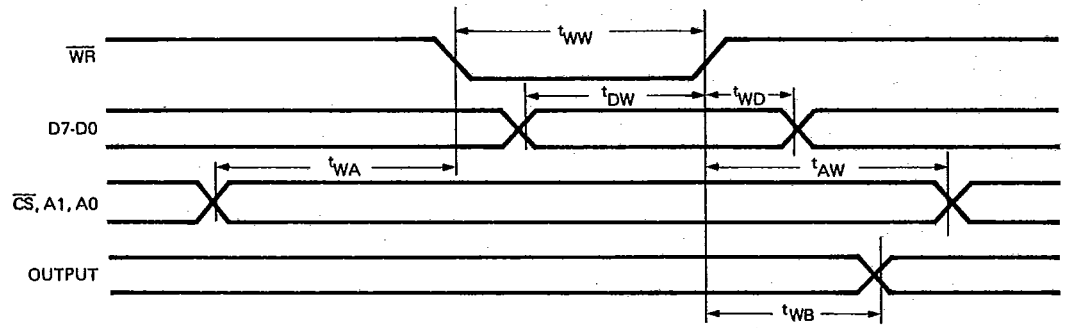
Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports
- Any port can be input or output
- Outputs are latched
- Inputs are not latched
- 16 different Input/Output configurations possible.

MODE 0 (BASIC INPUT)



MODE 0 (BASIC OUTPUT)

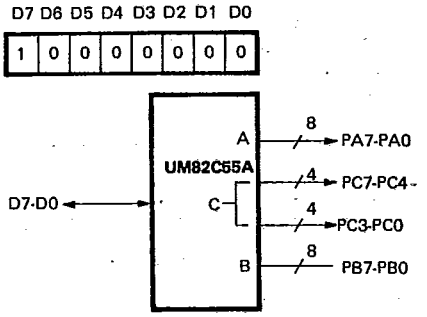


Mode 0 Port Definition

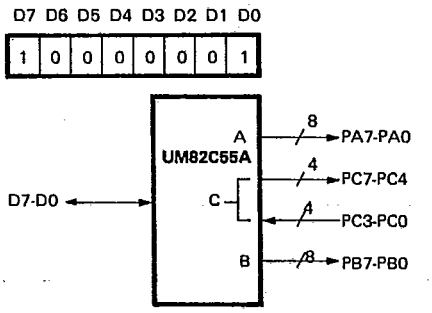
A		B		Group A			Group B	
D_4	D_3	D_1	D_0	Port A	Port C (Upper)	#	Port B	Port C (Lower)
0	0	0	0	Output	Output	0	Output	Output
0	0	0	1	Output	Output	1	Output	Input
0	0	1	0	Output	Output	2	Input	Output
0	0	1	1	Output	Output	3	Input	Input
0	1	0	0	Output	Input	4	Output	Output
0	1	0	1	Output	Input	5	Output	Input
0	1	1	0	Output	Input	6	Input	Output
0	1	1	1	Output	Input	7	Input	Input
1	0	0	0	Input	Output	8	Output	Output
1	0	0	1	Input	Output	9	Output	Input
1	0	1	0	Input	Output	10	Input	Output
1	0	1	1	Input	Output	11	Input	Input
1	1	0	0	Input	Input	12	Output	Output
1	1	0	1	Input	Input	13	Output	Input
1	1	1	0	Input	Input	14	Input	Output
1	1	1	1	Input	Input	15	Input	Input

Mode 0 Configurations

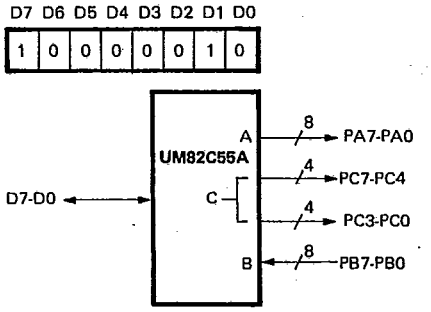
CONTROL WORD #0



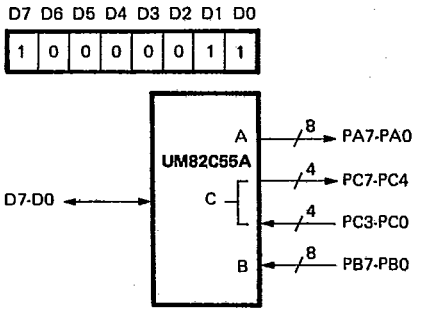
CONTROL WORD #1



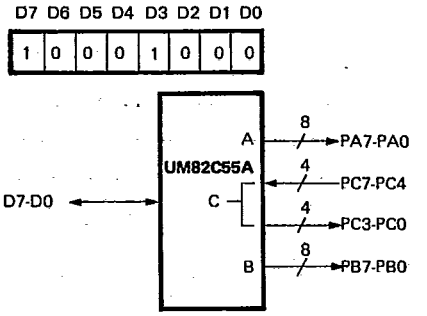
CONTROL WORD #2



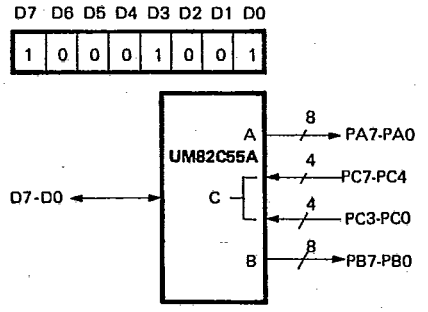
CONTROL WORD #3



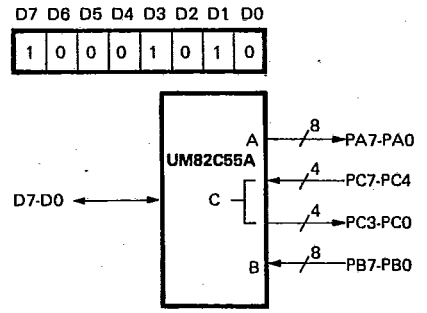
CONTROL WORD #4



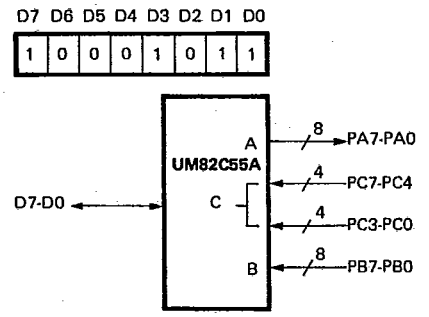
CONTROL WORD #5



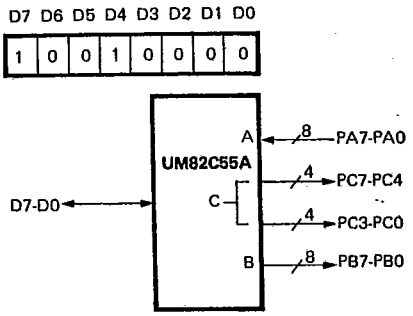
CONTROL WORD #6



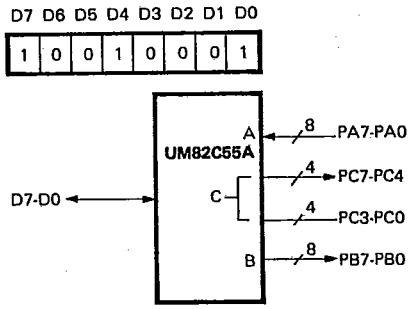
CONTROL WORD #7



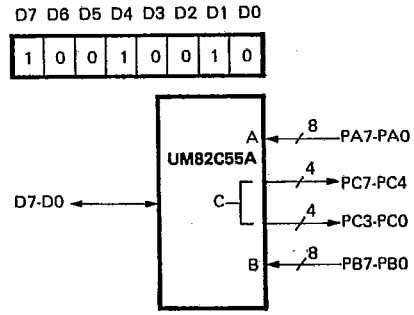
CONTROL WORD #8



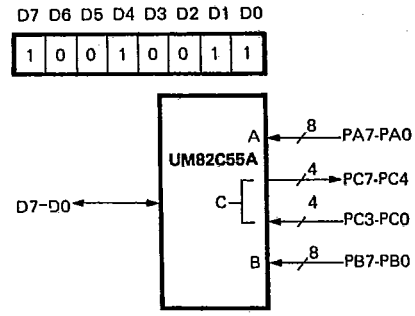
CONTROL WORD #9



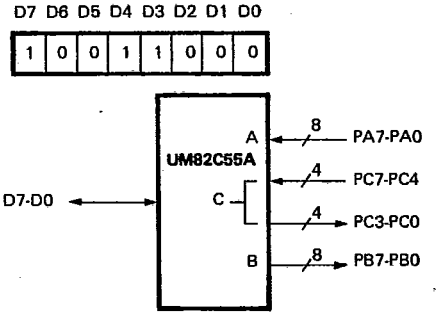
CONTROL WORD #10



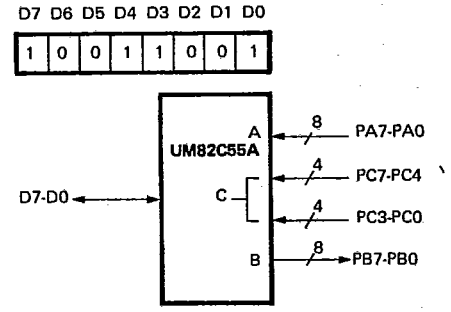
CONTROL WORD #11



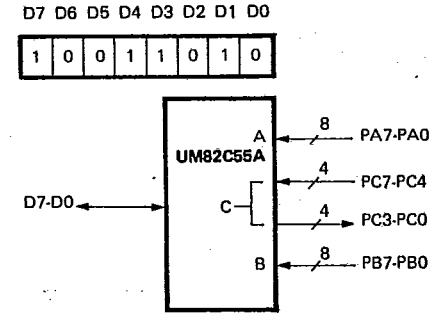
CONTROL WORD #12



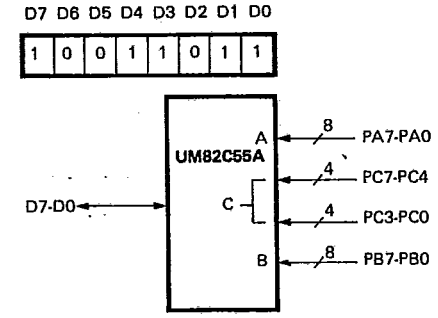
CONTROL WORD #13



CONTROL WORD #14



CONTROL WORD #15



PC Mainboard

Operating Modes

Mode 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, port A and port B use the lines on port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions

- Two Groups (Group A and Group B)
- Each group contains one 8-bit port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit port.

Input Control Signal Definition

$\overline{STB}$ (Strobe Input)
A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by $\overline{STB}$ input being low and is reset by the rising edge of the $\overline{RD}$ input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the condition; STB is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC_4.

INTE B

Controlled by bit set/reset of PC_2.

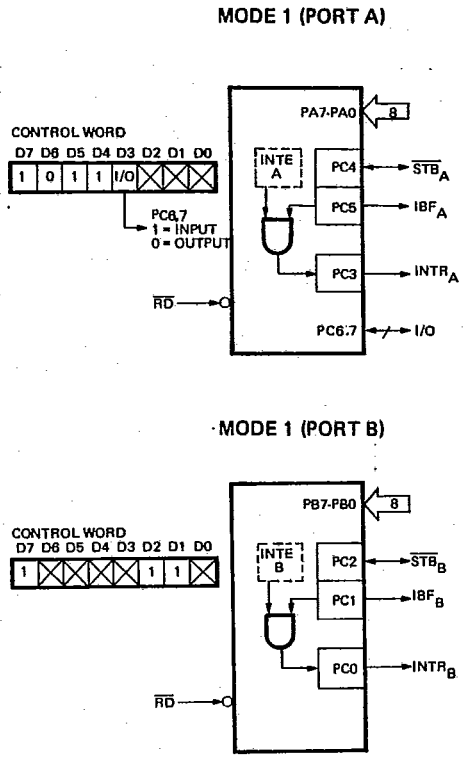


Figure 6. MODE 1 Input

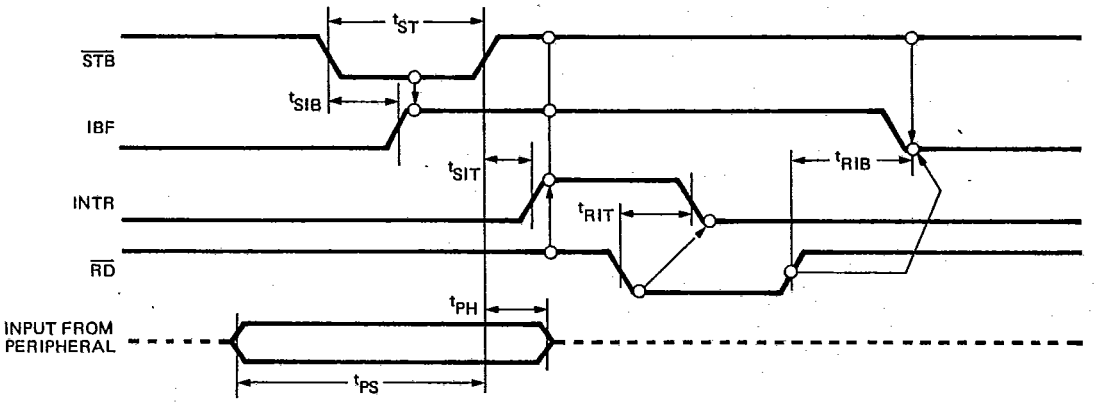


Figure 7. MODE 1 (Strobed Input)

Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F). The OBF output will go "low" to indicate that the CPU has written data out to the specified port. The $\overline{OBF}$ F/F will be set by the rising edge of the $\overline{WR}$ input and reset by $\overline{ACK}$ Input being low.

$\overline{ACK}$ (Acknowledge Input). A "low" on this input informs the UM82C55A that the data from port A or port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the $\overline{CPU}$.

INTR (Interrupt Request). A "high" on this output can be used to interrupt the $\overline{CPU}$ when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a "one", OBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{WR}$.

INTE A

Controlled by Bit Set/Reset of PC_6.

INTE B

Controlled by Bit Set/Reset of PC_2.

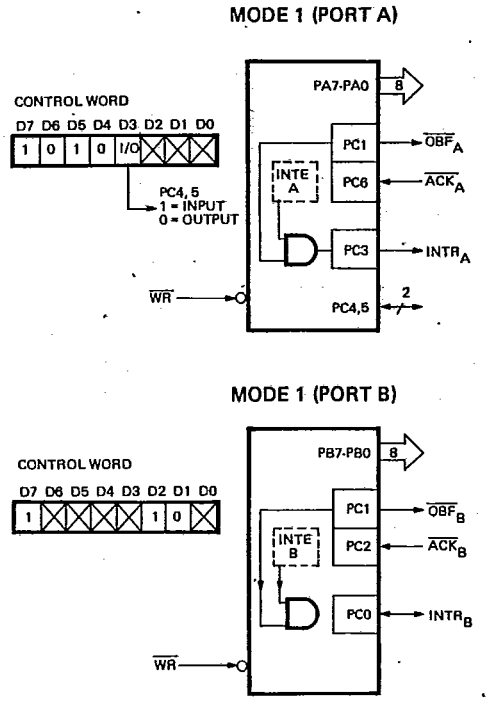


Figure 8. MODE 1 Output

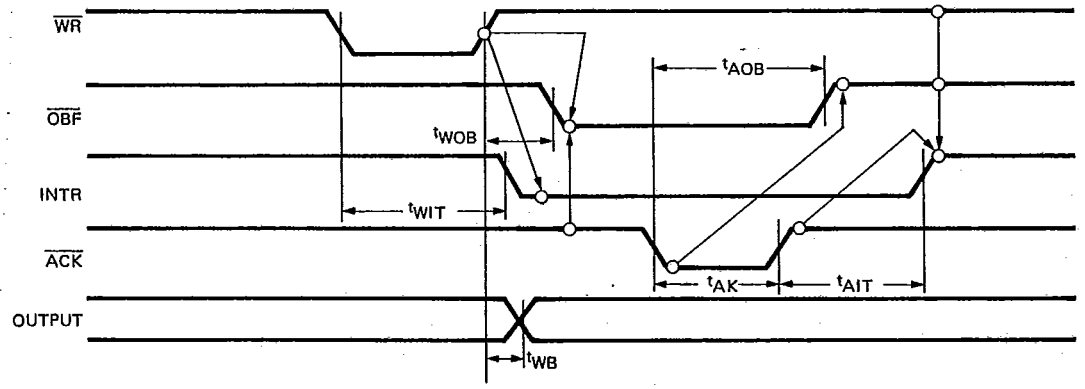


Figure 9. MODE 1 (Strobed Output)

Combinations of MODE 1: Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications:

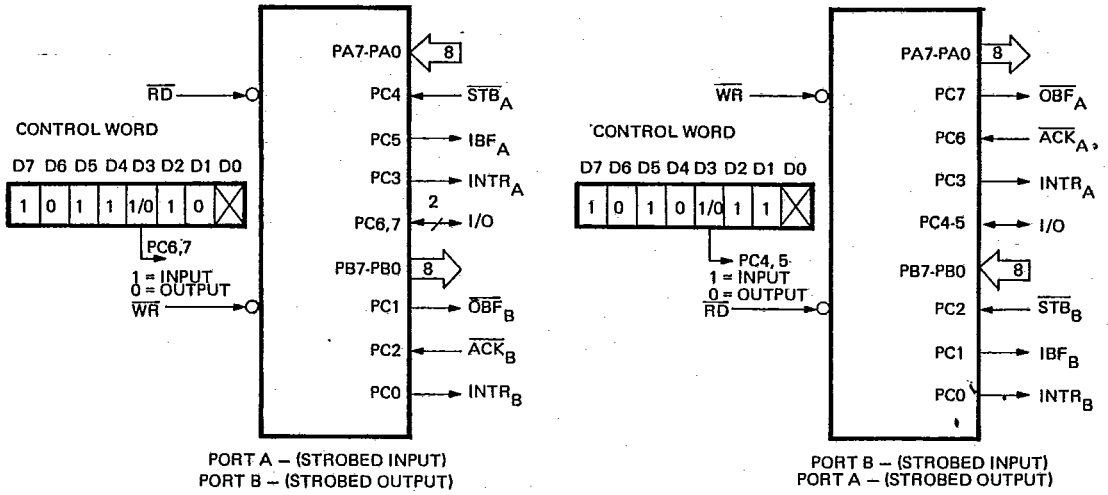


Figure 10. Combinations of MODE 1

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O)
The functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline similar to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Function Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition
INTR (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations
$\overline{OBF}$ (Output Buffer Full). The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to port A.

$\overline{ACK}$ (Acknowledge). A "Low" on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with $\overline{OBF}$). Controlled by bit set/reset of PC_6.

Input Operations
$\overline{STB}$ (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF). Controlled by bit set/reset of PC_4.

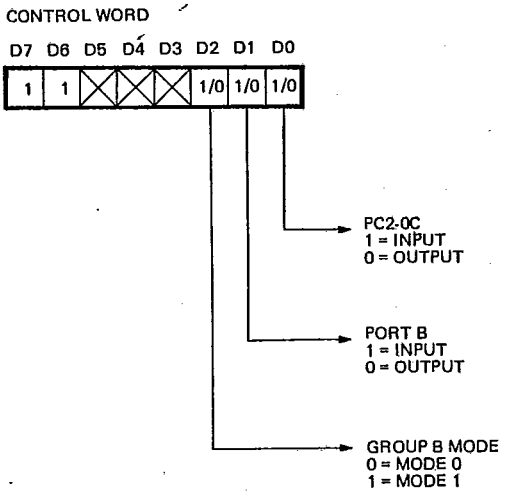


Figure 11. MODE Control Word

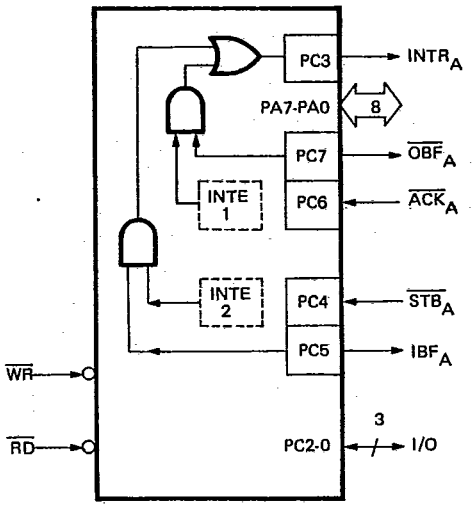


Figure 12. MODE 2

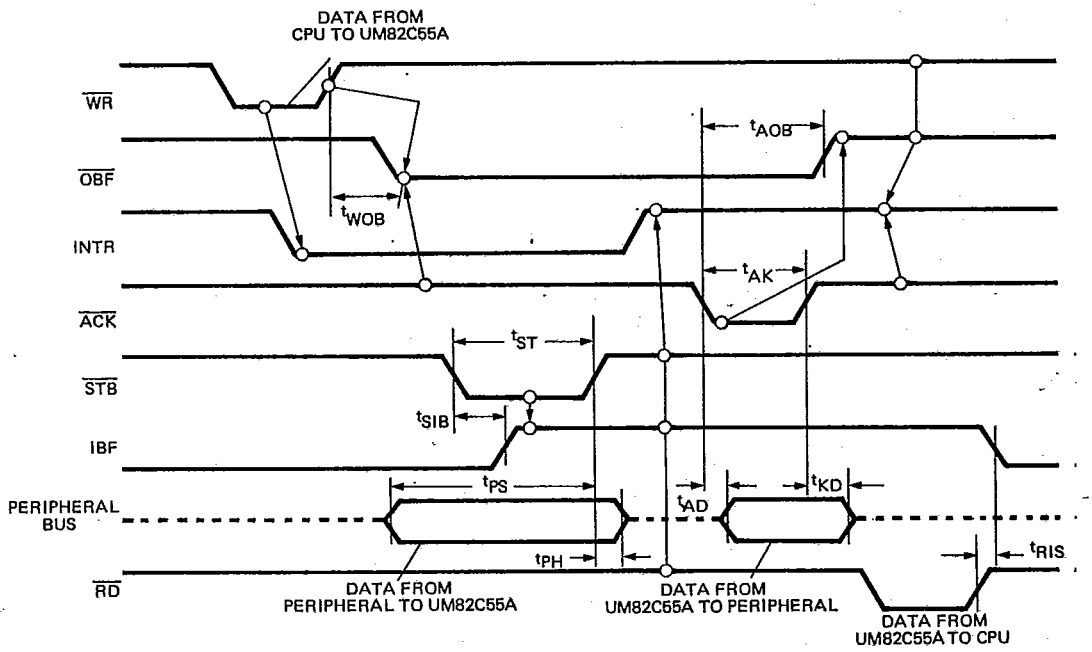
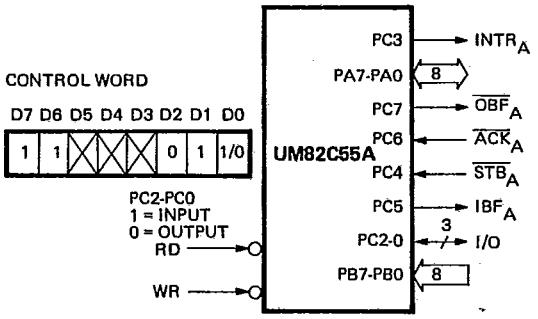


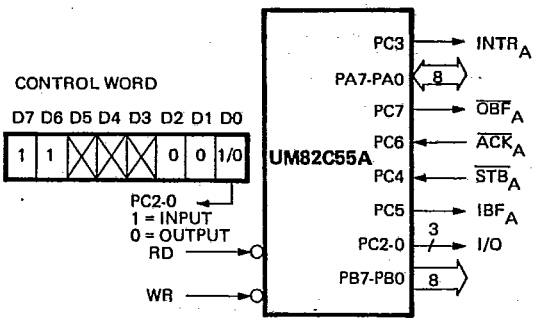
Figure 13. MODE 2 (Bidirectional)

Note: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before RD is permissible. (INTR = IBF · MASK · $\overline{STB}$ · $\overline{RD}$ + $\overline{OBF}$ · MASK · $\overline{ACK}$ · $\overline{WR}$)

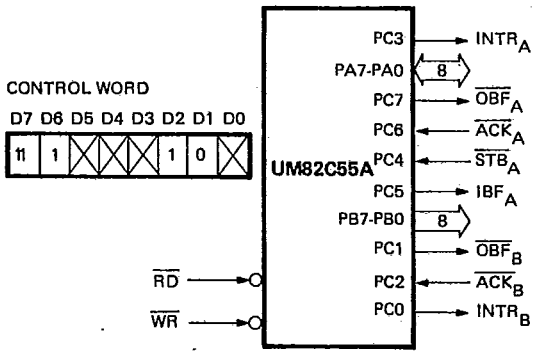
MODE 2 AND MODE 0 (INPUT)



MODE 2 AND MODE 0 (OUTPUT)



MODE 2 AND MODE 1 (OUTPUT)



MODE 2 AND MODE 1 (INPUT)

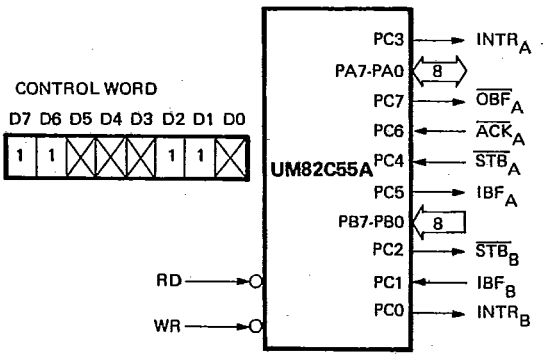


Figure 14. MODE 2 Combinations

Mode Definition Summary

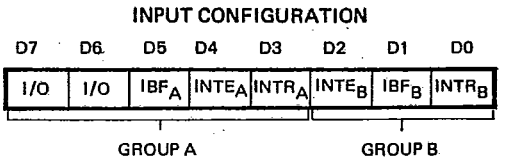
	MODE 0		MODE 1		MODE 2
	IN	OUT	IN	OUT	Group A Only
PA_0	IN	OUT	IN	OUT	←
PA_1	IN	OUT	IN	OUT	←
PA_2	IN	OUT	IN	OUT	←
PA_3	IN	OUT	IN	OUT	←
PA_4	IN	OUT	IN	OUT	→
PA_5	IN	OUT	IN	OUT	→
PA_6	IN	OUT	IN	OUT	→
PA_7	IN	OUT	IN	OUT	→
PB_0	IN	OUT	IN	OUT	MODE 0 OR MODE 1 ONLY
PB_1	IN	OUT	IN	OUT	
PB_2	IN	OUT	IN	OUT	
PB_3	IN	OUT	IN	OUT	
PB_4	IN	OUT	IN	OUT	
PB_5	IN	OUT	IN	OUT	
PB_6	IN	OUT	IN	OUT	
PB_7	IN	OUT	IN	OUT	
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O
PC_3	IN	OUT	$INTR_A$	$INTR_A$	INTRA
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$
PC_5	IN	OUT	IBF_A	I/O	IBF_A
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$

Special Mode Combination Considerations:
There are several combinations of modes possible. For any combination, some or all of Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a "Set Mode" command.

During a read of Port C, the state of all the Port C lines except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus. In place of the $\overline{ACK}$ and $\overline{STB}$ line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated by Figure 17.

Through a "Write Port C" command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a "Write Port C" command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in a Mode 1 group or to change an interrupt enable flag, the "Set/Reset Port C Bit" command must be used.

With a "Set/Reset Port C Bit" command, any Port C line programmed as an output (including INTR, IBF and OBF) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, associated with Port C are not affected by a "Set/Reset Port C Bit" command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the "Set/Reset Port C Bit" command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 17.



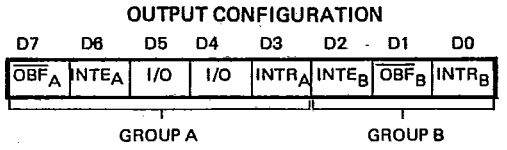
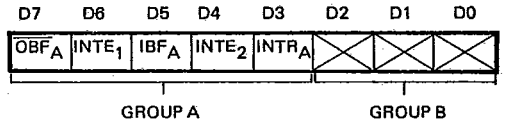


Figure 15. MODE 1 Status Word Format



(DEFINED BY MODE 0 OR MODE 1 SELECTION)

Figure 16. MODE 2 Status Word Format

Interrupt Enable Flag	Position	Alternate Port C Pin Signal (Mode)
INTE B	PC2	$\overline{ACK}_B$ (Output Mode 1) or $\overline{STB}_B$ (Input Mode 1)
INTE A2	PC4	$\overline{STB}_A$ (Input Mode 1 or Mode 2)
INTE A1	PC6	$\overline{ACK}_A$ (Output Mode 1 or Mode 2)

Figure 17. Interrupt Enable Flags in Modes 1 and 2

Current Drive Capability:
Any output on Port A, B or C can sink or source 2.5mA. This feature allows the UM82C55A to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status
In Mode 0, Port C transfers data to or from the peripheral device. When the UM82C55A is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows that programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

Applications of the UM82C55A

The UM82C55A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the UM82C55A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the UM82C55A to exactly "fit" the application. Figures 18 through 24 present a few examples of typical applications of the UM82C55A.

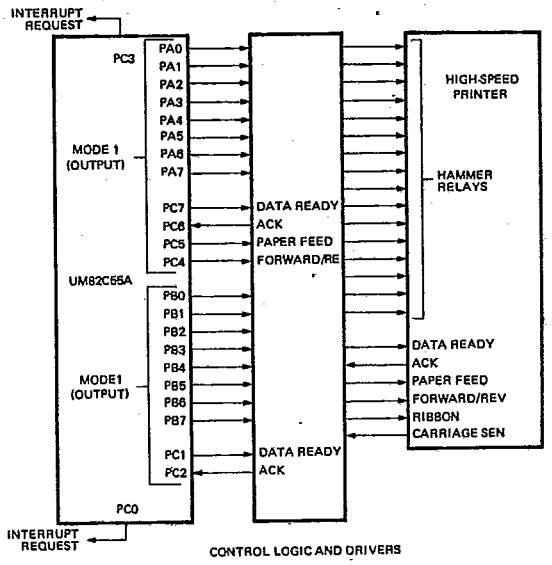


Figure 18. Printer Interface

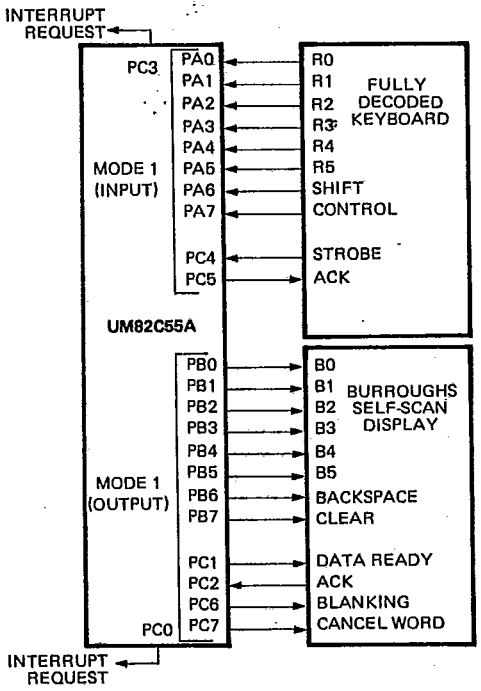


Figure 19. Keyboard and Display Interface

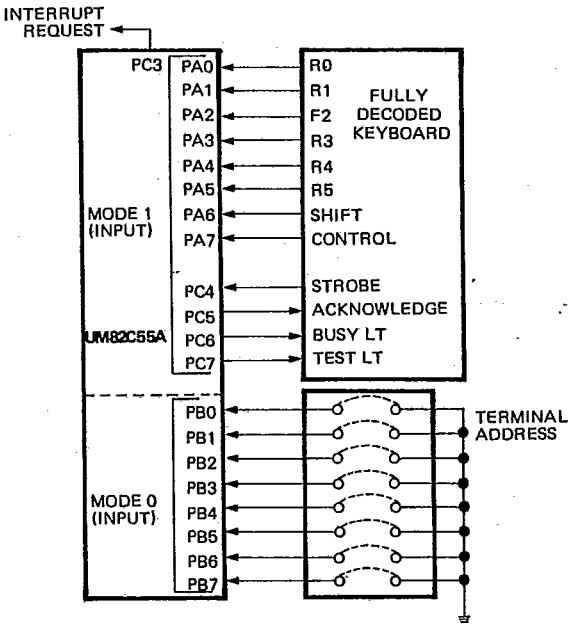


Figure 20. Keyboard and Terminal Address Interface

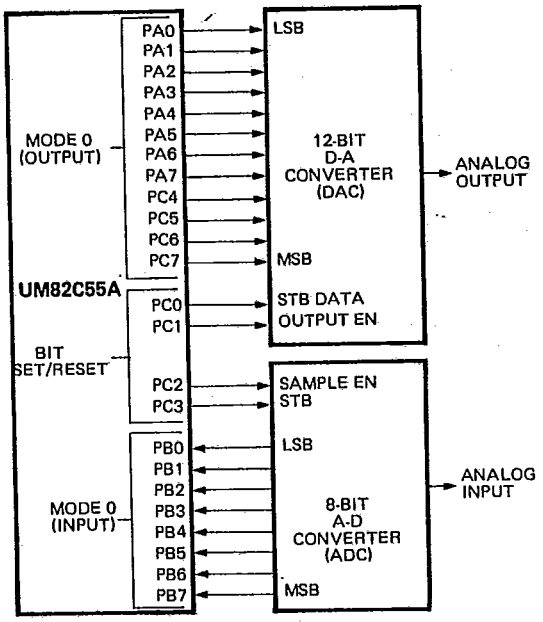


Figure 21. Digital to Analog, Analog to Digital

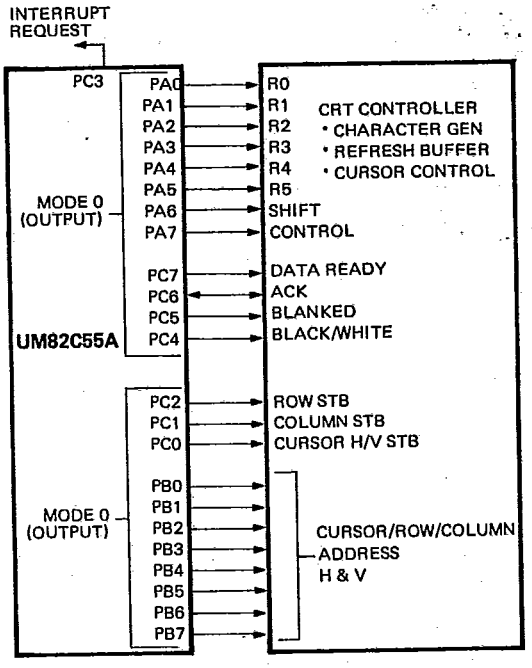


Figure 22. Basic CRT Controller Interface

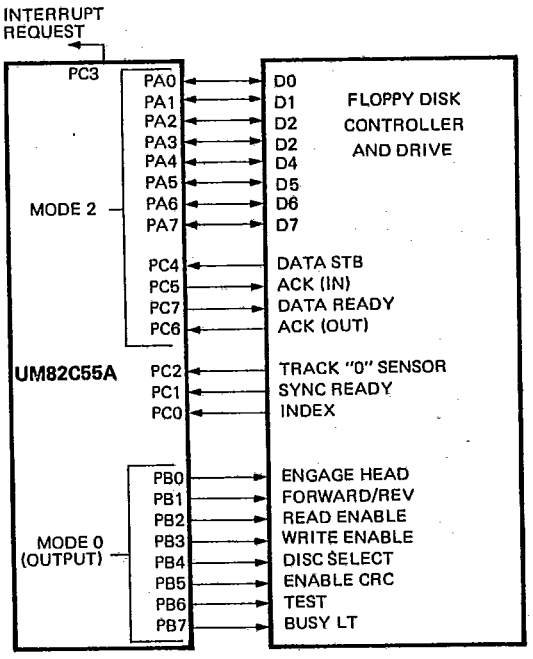


Figure 23. Basic Floppy Disk Interface

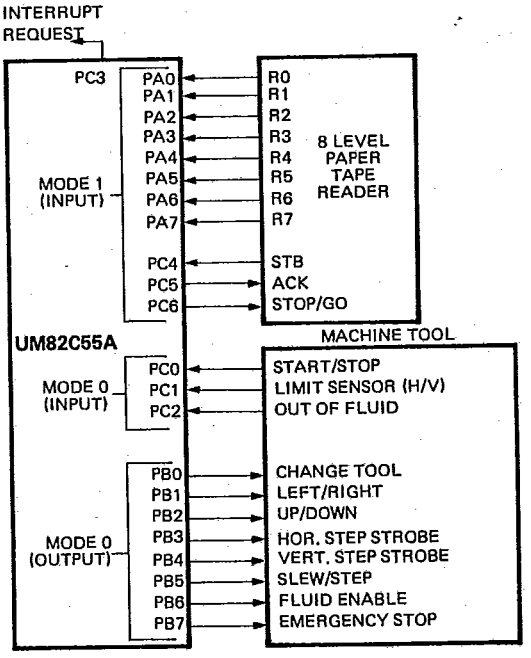


Figure 24. Machine Tool Controller Interface