

TD3842A/3843A/3844A/3845A

HIGH PERFORMANCE CURRENT MODE PWM CONTROLLERS

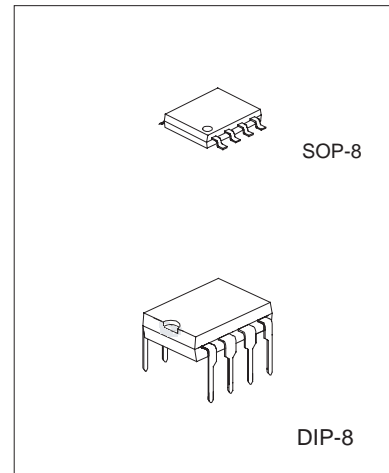
DESCRIPTION

The TD3842A/3843A/3844A/3845A are fixed frequency current-mode PWM controller. They are specially designed for Off - Line and DC-to-DC converter applications with minimum external components.

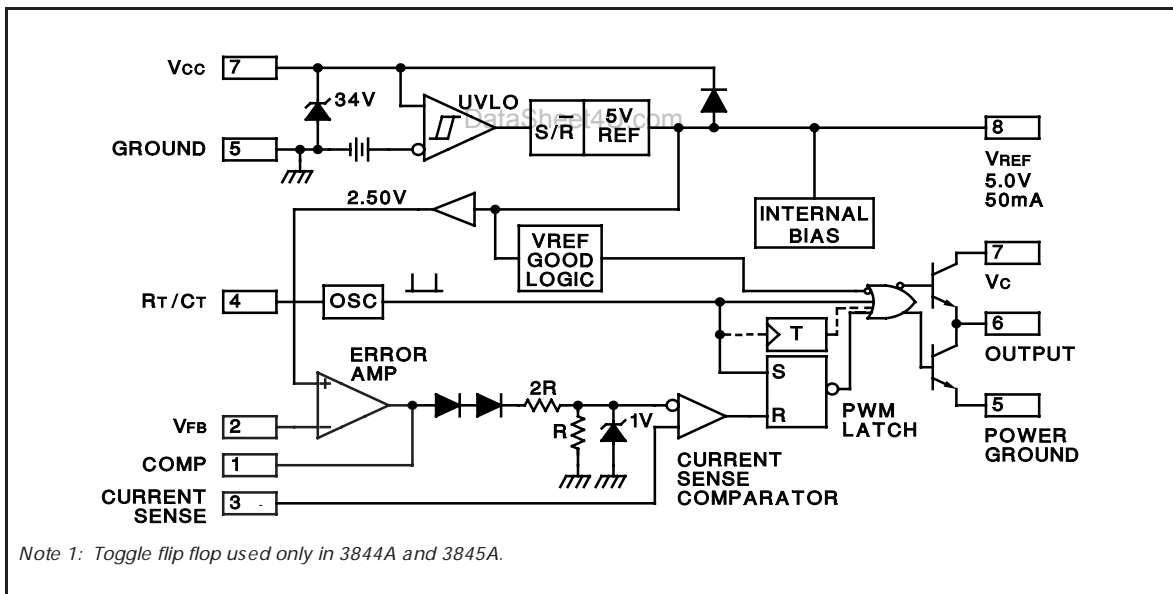
These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totempole output. Ideally suited for driving a power MOSFET. Protection circuitry includes built in under-voltage lockout and current limiting. The TD3842A and TD3844A have UVLO thresholds of 16V (on) and 10V (off). The TD3843A and TD3845A are 8.4V (on) and 7.6V (off). The TD3842A and TD3843A can operate within 100% duty cycle. The TD3844A and TD3845A can operate with 50% duty cycle.

FEATURES

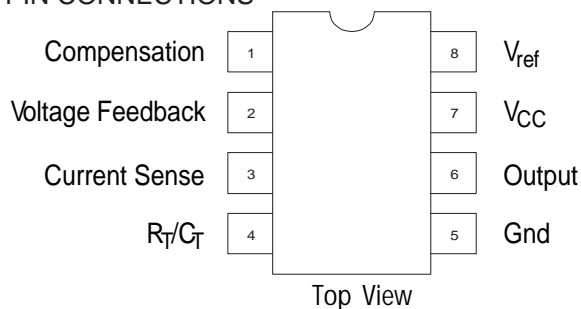
- Low Start Up Current
- Maximum Duty Clamp
- UVLO With Hysteresis
- Operating Frequency Up To 500KHz



BLOCK DIAGRAM



PIN CONNECTIONS



TD3842A / 3843A / 3844A / 3845A

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Bias and Driver Voltages (Zero Series Impedance, see also Total Device spec)	V_{CC}, V_C	30	V
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense and Voltage Feedback Inputs	V_{in}	- 0.3 to + 5.5	V
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics			
D Suffix, Plastic Package			
Maximum Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	862	mW
Thermal Resistance, Junction-to-Air	R_{JA}	145	$^\circ\text{C/W}$
N Suffix, Plastic Package			
Maximum Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.25	W
Thermal Resistance, Junction-to-Air	R_{JA}	100	$^\circ\text{C/W}$
Operating Junction Temperature	T_J	+ 150	$^\circ\text{C}$
Operating Ambient Temperature	T_A	0 to + 70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	- 65 to + 150	$^\circ\text{C}$

- Maximum Package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS ($V_{CC} = 15\text{ V}$, [Note 2], $R_T = 10\text{ k}$, $C_T = 3.3\text{ nF}$, $T_A = T_{low}$ to T_{high} [Note 3], unless otherwise noted.)

Characteristics	Symbol	TD3842A/43A/44A/45A			Unit
		Min	Typ	Max	

REFERENCE SECTION

Reference Output Voltage ($I_O = 1.0\text{ mA}$, $T_J = 25^\circ\text{C}$)	V_{ref}	4.9	5.0	5.1	V
Line Regulation ($V_{CC} = 12\text{ V}$ to 25 V)	Reg_{line}	-	2.0	20	mV
Load Regulation ($I_O = 1.0\text{ mA}$ to 20 mA)	Reg_{load}	-	3.0	25	mV
Temperature Stability	T_S	-	0.2	-	mV/ $^\circ\text{C}$
Total Output Variation over Line, Load, Temperature	V_{ref}	4.82	-	5.18	V
Output Noise Voltage ($f = 10\text{ Hz}$ to 10 kHz , $T_J = 25^\circ\text{C}$)	V_n	-	50	-	μV
Long Term Stability ($T_A = 125^\circ\text{C}$ for 1000 Hours)	S	-	5.0	-	mV
Output Short Circuit Current	I_{SC}	- 30	- 85	- 180	mA

OSCILLATOR SECTION

Frequency $T_J = 25^\circ\text{C}$ $T_A = T_{low}$ to T_{high}	f_{osc}	47 46	52 -	57 60	kHz
Frequency Change with Voltage ($V_{CC} = 12\text{ V}$ to 25 V)	f_{osc}/V	-	0.2	1.0	%
Frequency Change with Temperature $T_A = T_{low}$ to T_{high}	f_{osc}/T	-	5.0	-	%
Oscillator Voltage Swing (Peak \pm to \pm Peak)	V_{osc}	-	1.6	-	V
Discharge Current ($V_{osc} = 2.0\text{ V}$) $T_J = 25^\circ\text{C}$ $T_A = T_{low}$ to T_{high}	I_{dischg}	7.5 7.2	8.4 -	9.3 9.5	mA

TD3842A / 3843A / 3844A / 3845A

ERROR AMPLIFIER SECTION

Characteristics	Symbol	TD3842A/43A/44A/45A			Unit
		Min	Typ	Max	
Voltage Feedback Input ($V_O = 2.5\text{ V}$)	V_{FB}	2.42	2.5	2.58	V
Input Bias Current ($V_{FB} = 2.7\text{ V}$)	I_{IB}	-	-0.1	-2.0	μA
Open Loop Voltage Gain ($V_O = 2.0\text{ V to }4.0\text{ V}$)	A_{VOL}	65	90	-	dB
Unity Gain Bandwidth ($T_J = 25^\circ\text{C}$)	BW	0.7	1.0	-	MHz
Power Supply Rejection Ratio ($V_{CC} = 12\text{ V to }25\text{ V}$)	PSRR	60	70	-	dB
Output Current Sink ($V_O = 1.1\text{ V}, V_{FB} = 2.7\text{ V}$) Source ($V_O = 5.0\text{ V}, V_{FB} = 2.3\text{ V}$)	I_{Sink} I_{Source}	2.0 -0.5	12 -1.0	- -	mA
Output Voltage Swing High State ($R_L = 15\text{ k to ground}, V_{FB} = 2.3\text{ V}$) Low State ($R_L = 15\text{ k to }V_{ref}, V_{FB} = 2.7\text{ V}$)	V_{OH} V_{OL}	5.0 -	6.2 0.8	- 1.1	V

- Adjust V_{CC} above the S startup threshold before setting to 15 V.
- Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
 $T_{low} = 0^\circ\text{C}$ for TD3842A/43A/44A/45A $T_{high} = +70^\circ\text{C}$ for TD3842A/43A/44A/45A

ELECTRICAL CHARACTERISTICS ($V_{CC} = 15\text{ V}$, [Note 4], $R_T = 10\text{ k}$, $C_T = 3.3\text{ nF}$, $T_A = T_{low}$ to T_{high} [Note 5], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
-----------------	--------	-----	-----	-----	------

CURRENT SENSE SECTION

Current Sense Input Voltage Gain (Notes 6 & 7)	A_y	2.85	3.0	3.15	V/V
Maximum Current Sense Input Threshold (Note 6)	V_{th}	0.9	1.0	1.1	V
Power Supply Rejection Ratio $V_{CC} = 12\text{ to }25\text{ V}$ (Note 6)	PSRR	-	70	-	dB
Input Bias Current	I_{IB}	-	-2.0	-10	μA
Propagation Delay (Current Sense Input to Output)	$t_{pLH(in/out)}$	-	150	300	ns

OUTPUT SECTION

Output Voltage Low State ($I_{Sink} = 20\text{ mA}$) ($I_{Sink} = 200\text{ mA}$) High State ($I_{Sink} = 20\text{ mA}$) ($I_{Sink} = 200\text{ mA}$)	V_{OL} V_{OH}	- - 13 12	0.1 1.6 13.5 13.4	0.4 2.2 - -	V
Output Voltage with UVLO Activated $V_{CC} = 6.0\text{ V}, I_{Sink} = 1.0\text{ mA}$	$V_{OL(UVLO)}$	-	0.1	1.1	V
Output Voltage Rise Time ($C_L = 1.0\text{ nF}, T_J = 25^\circ\text{C}$)	t_r	-	50	150	ns
Output Voltage Fall Time ($C_L = 1.0\text{ nF}, T_J = 25^\circ\text{C}$)	t_f	-	50	150	ns

UNDERVOLTAGE LOCKOUT SECTION

Startup Threshold TD3842A/TD3844A TD3843A/TD3845A	V_{th}	14.5 7.8	16 8.4	17.5 9.0	V
Minimum Operating Voltage After Turn On TD3842A/TD3844A TD3843A/TD3845A	$V_{CC(min)}$	8.5 7.0	10 7.6	11.5 8.2	V

TD3842A / 3843A / 3844A / 3845A

PWM SECTION

Characteristics		Symbol	Min	Typ	Max	Unit
Duty Cycle	Maximum	TD3842A/TDd3843A	94	96	100	%
		TD3844A/TDd3845A	47	48	50	
	Minimum	DC _{min}	-	-	0	

TOTAL DEVICE

Power Supply Current (Note 4) Startup: (V _{CC} = 6.5 V for TD3843A, 14 V for TD3842A) Operating	I _{CC}	-	0.5	1.0	mA
		-	12	17	
Power Supply Zener Voltage (I _{CC} = 25 mA)	V _Z	30	36	-	V

- Adjust V_{CC} above the Startup threshold before setting to 15 V.
- Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for TD3842A/43A/44A/45A T_{high} = +70°C for TD3842A/43A/44A/45A
- This parameter is measured at the latch trip point with V_{FB} = 0 V.
- Comparator gain is defined as: $A_V = \frac{V \text{ Output Compensation}}{V \text{ Current Sense Input}}$

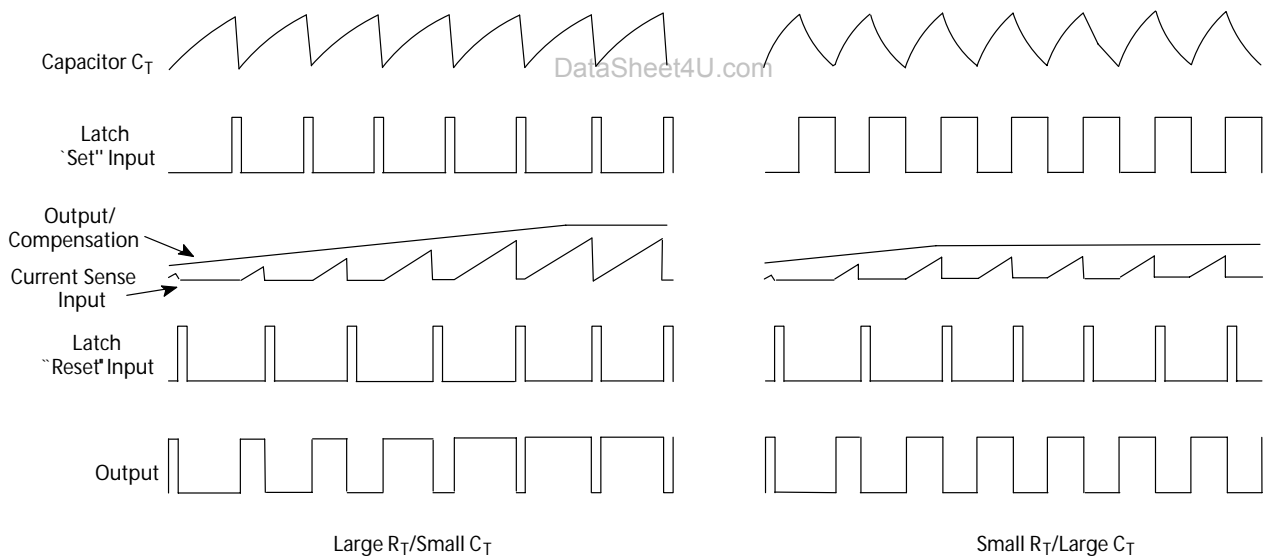
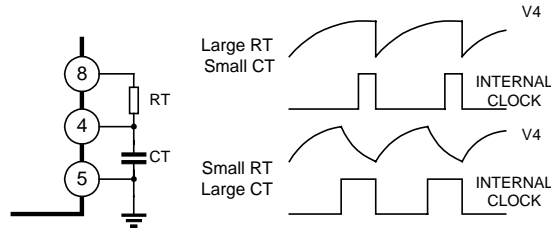


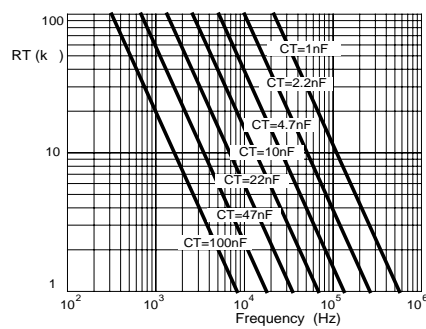
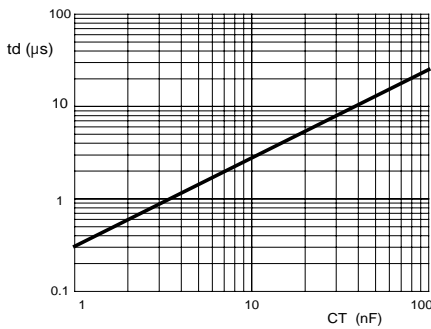
Figure 1. Timing Diagram

TD3842A / 3843A / 3844A / 3845A

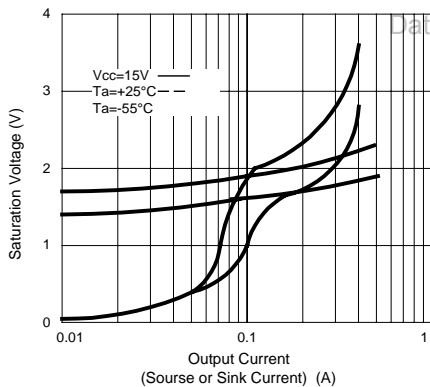
OSCILLATOR SECTION



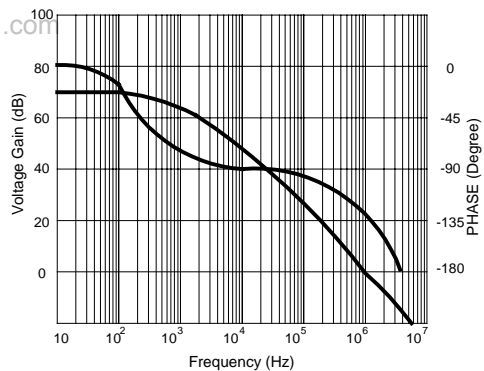
Dead time VS C_T ($R_T > 5k$) Timing Resistance Vs Frequency



TYPICAL PERFORMANCE CHARACTERISTICS



Output Saturation Characteristics

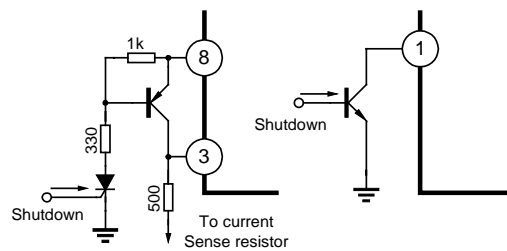


Error Amplifier Open-Loop Frequency Response

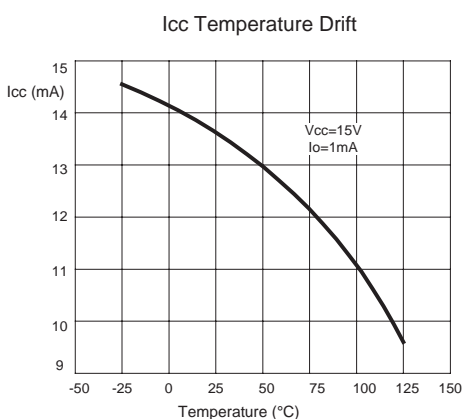
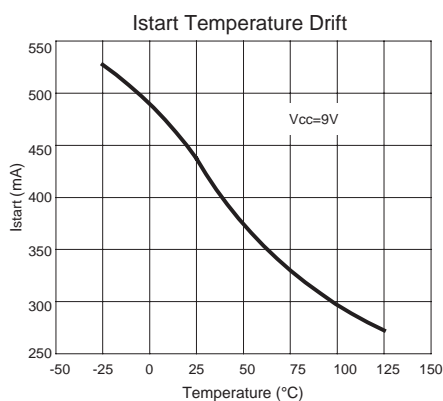
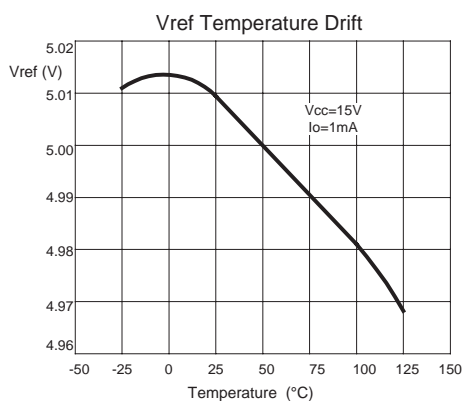
Shutdown TD3842A can be accomplished by two methods; either raise pin 3 above 1V or pull Pin 1 below a voltage two diode drops above ground. Either method caused the output of PWM comparator to be high (refer to block diagram).

The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pins 1 and/or 3 is removed. In one example, an externally latched shut-down may be accomplished by adding an SCR which be reset by cycling V_{cc} below the lower UVLO threshold. At this point the reference turns off allowing the SCR to reset.

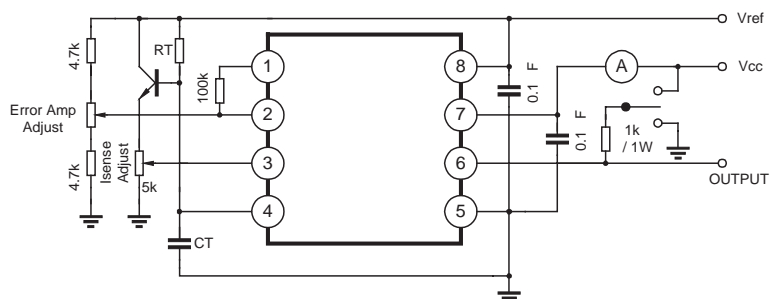
SHUTDOWN TECHNIQUES



TD3842A / 3843A / 3844A / 3845A

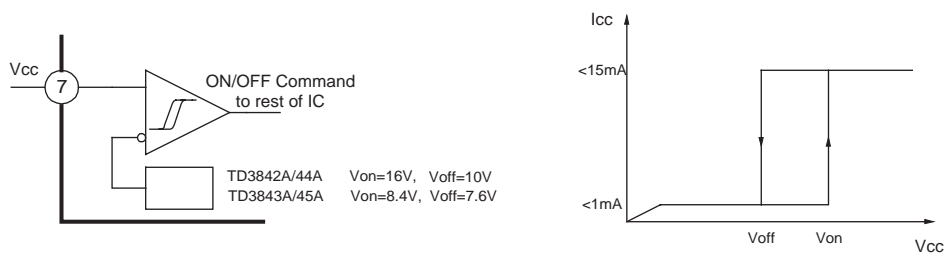


OPEN-LOOP LABORATORY TEST FIXTURE



High peak current associated with capacity loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in single point GND. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable Ramp to Pin 3.

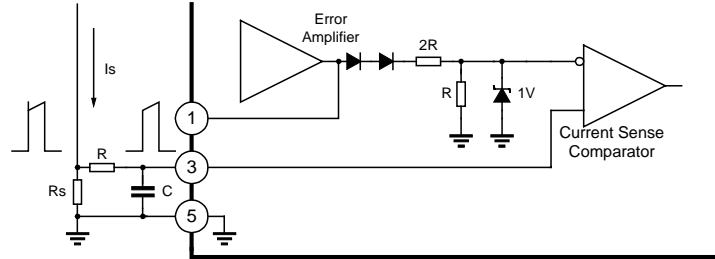
UNDER-VOLTAGE LOCKOUT



During Under-Voltage Lockout, the output driver is biased to a high impedance state. Pin 6 should be shunt to GND with a bleeder resistor to prevent activating the power switch with output leakage currents.

TD3842A / 3843A / 3844A / 3845A

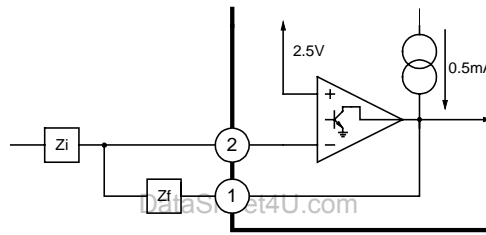
CURRENT SENSE CIRCUIT



Peak current (I_s) determined by the formula:
 $I_s(\text{MAX}) = 1.0\text{V}/R_s$.

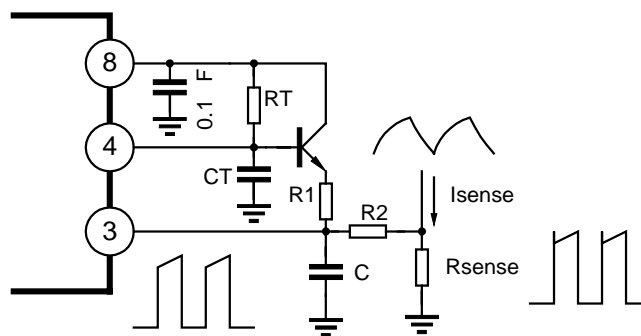
A small RC filter be required to suppress switch transients.

ERROR AMPLIFIER CONFIGURATION



Error amplifier can source or sink up to 0.5mA

SLOPE COMPENSATION



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converts requiring duty cycles over 50%. Note that capacitor C, forms a filter with R2 to suppress the leading edge switch spikes.