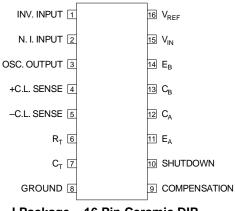


### **TOP VIEW**



J Package – 16 Pin Ceramic DIP N Package – 16 Pin Plastic DIP

D Package – 16 Pin Plastic (150) SOIC

# REGULATING PULSE WIDTH MODULATORS

## FEATURES

- Guaranteed ±2% reference voltage tolerance
- Guaranteed ±6% oscillator tolerance
- Fully specified temperature performance
- Guaranteed 10mV/1000 hours long term stability
- Interchangeable with SG1524 series

## **Order Information**

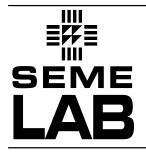
Part Number	J–Pack 16 Pin	N–Pack 16 Pin	D–16 16 Pin	Temp. Range	<b>Note:</b> To order, add the package identifier to the part number.
IP1524	<ul> <li>✓</li> </ul>			-55 to +125°C	eg. IP1524J
IP2524	V	~	~	-25 to +85°C	IP3524D–16
IP3524	<ul> <li>✓</li> </ul>	~	~	0 to +70°C	

## **ABSOLUTE MAXIMUM RATINGS** (T<sub>case</sub> = 25°C unless otherwise stated)

		( CL3C	,		
+V <sub>IN</sub>	Input Voltage		+40V		
	Collector Voltage		+40V		
	Output Current	(each transistor)	100mA		
	Reference Load Current		Internally Limited		
	Oscillator Charging Curre	ent	5mA		
	Shut Down Pin Voltage	Shut Down Pin Voltage			
	Current Limit Sense Corr	Current Limit Sense Common Mode Range			
P <sub>D</sub>	Power Dissipation	$T_A = 25^{\circ}C$	1W		
		Derate @ T <sub>A</sub> > 50°C	10mW/°C		
PD	Power Dissipation	$T_{\rm C} = 25^{\circ}{\rm C}$	2W		
		Derate @ T <sub>C</sub> > 25°C	16mW/°C		
TJ	Operating Junction Temp	perature	See Ordering Information		
T <sub>STG</sub>	Storage Temperature Ra	nge	–65 to +150°C		
ΤL	Lead Temperature	(soldering, 10 seconds)	+300°C		

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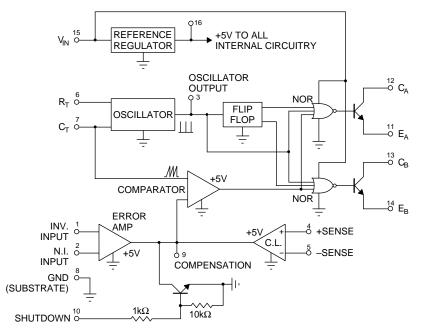


### DESCRIPTION

The IP1524 series of PWM switching regulator control circuits contains all the functions required to implement singleended or push-pull switching regulators. Included are voltage reference, error amplifer, oscillator, PWM comparator, output drivers, current limiting and shutdown circuitry.

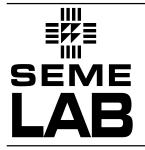
Although functionally indentical to the SG1524 series, SEMELAB has incorporated several improvements to the IP1524 allowing tighter and more complete specification of electrical performance.

## **BLOCK DIAGRAM**



## **RECOMMENDED OPERATING CONDITIONS**

V <sub>IN</sub>	Input Voltage		+8 to +40V
	Collector Voltage		0 to +40V
	Error Amp Common Mode Range		+1.8 to +3.4V
	Output Current	(each transistor)	0 to 100mA
	Reference Load Current		0 to 20mA
	Oscillator Charging Current		30μA to 2mA
	Oscillator Frequency Range		50Hz to 500kHz
R <sub>T</sub>	Oscillator Timing Resistor		1.8kΩ to 100kΩ
CT	Oscillator Timing Capacitor		1nF to 0.1μF
T <sub>AMB</sub>	Operating Ambient Temperature Range	IP1524	–55 to +125°C
		IP2524	-25 to +85°C
		IP3524	0 to +70°C



## **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise stated)

	Test Conditions <sup>1</sup>		IP1524 IP2524			IP3524			
Parameter			Тур.	Max.	Min.	Тур.	Max.	Units	
	REFERENCE SECTION								
Output Voltage	T <sub>J</sub> = Over Temp. Range	4.90	5.00	5.10	4.60	5.00	5.40	V	
Line Regulation	$+V_{IN} = 8$ to 40V $T_J = Over Temp. Range$		1	10		10	30	mV	
Load Regulation	$I_L = 0$ to 20mA $T_J = Over Temp. Range$		5	20		20	50	IIIV	
Ripple Rejection	f = 120Hz		80			66		dB	
Short Circuit Current	$V_{REF} = 0$ $T_J = Over Temp. Range$	25	50	120		100		mA	
Temperature Stability	T <sub>J</sub> = Over Temp. Range		0.3	1		0.3	1	%	
Long Term Stability	T <sub>J</sub> = 125°C		1	10		20		mV khr	
	OSCILLATOR SECTION								
Initial Accuracy	$R_T = 2.7k\Omega$ $C_T = 0.01\mu F$			6		5			
Voltage Stability	+V <sub>IN</sub> = 8 to 40V		0.1	1		0.5	1	%	
Temperature Stability	T <sub>J</sub> = Over Temp. Range		1	2			2		
	$R_T = 100 k\Omega$ $C_T = 0.1 \mu F$		400	0.40		400		Hz	
Minimum Frequency	T <sub>J</sub> = Over Temp. Range	1	120	240		120			
	$R_T = 2k\Omega$ $C_T = 0.001\mu F$	200	200			300		kHz	
Maximum Frequency	T <sub>J</sub> = Over Temp. Range	200	300			300		KITZ	
Sawtooth Peak Voltage	$C_{T} = 0.01 \mu F$		3.6			3.6		V	
Sawtooth Valley Voltage	$C_{T} = 0.01 \mu F$	0.6	1			1			
	Output, Pin 3 $C_{T} = 0.01 \mu F$	2.0	4.0			2 5		V	
Clock Amplitude	T <sub>J</sub> = Over Temp. Range	3.0	4.0			3.5		v	
Clock Pulse Width	Output, Pin 3 $C_{T} = 0.01 \mu F$	0.3	0.5	1.0		0.5		μs	
	ERROR AMP SECTION <sup>2</sup>								
Input Offset Voltage	T <sub>J</sub> = Over Temp. Range		0.1	5		2	10	mV	
Input Bias Current	T <sub>J</sub> = Over Temp. Range		1	2		1	10		
Input Offset Current	T <sub>J</sub> = Over Temp. Range			0.5			1	μA	
DC Open Loop Gain	T <sub>J</sub> = Over Temp. Range	72	80		60	80		dB	
Output Low Level	$V_{PIN1} - V_{PIN2} \ge 150 \text{mV}$			0.5			0.5	V	
Output High Level	$V_{PIN2} - V_{PIN2} \ge 150 mV$	3.8			3.8			- V	
Common Mode Rejection		70	90		70				
Supply Voltage Rejection	+V <sub>IN</sub> = 8 to 40V	70	100		70			dB	
Gain Bandwidth Product			3			3		MHz	

#### NOTES

- 1. Test Conditions unless otherwise stated:  $V_{\text{IN}}$  = 20V ,  $I_{\text{REF}}$  = 0.
- 2.  $V_{CM} = +1.8 \text{ to } +3.4 \text{V}$ 3.  $V_{CM} = -1 \text{ to } +1 \text{V}$

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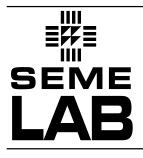


## **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise stated)

			IP1524 IP2524			IP3524			
Parameter	Test Condition	IS <sup>1</sup>	Min.	Тур.	Max.	Min.	Тур.	Max.	Units
	PWM COMPA	RATOR							
Minimum Duty Cycle	$V_{PIN1} - V_{PIN2} \ge 150 \text{mV}$ T <sub>J</sub> = Over Temp. Range				0			0	%
Willing and Daty Oyole									
Maximum Duty Cycle	$V_{PIN2} - V_{PIN1} \ge$	150mV	45	49		45	49		%
Maximum Duty Cycle	T <sub>J</sub> = Over Temp	o. Range	45			43	49		
	CURRENT LIN	/IT AMPLIFIER <sup>3</sup>							
	$V_{CM} = 0$		190	200	210	180	200	220	mV
Sense Voltage	$V_{CM} = 0$	T <sub>J</sub> = Over Temp. Range	170	200	230		200		
	SHUTDOWN I	NPUT							
High Input Voltage	$V_{PIN9} \le 0.6V$	T <sub>J</sub> = Over Temp. Range	1.2			1.2			V
Lifet land Ormerst	V <sub>SHUTDOWN</sub> = +	-5V	4 8		4			mA	
High Input Current	T <sub>J</sub> = Over Temp	o. Range		4 8		4			
Low Input Voltage	V <sub>PIN9</sub> ≥ 3.5V	T <sub>J</sub> = Over Temp. Range			0.3			0.3	V
	OUTPUT SEC	TION (each transistor)							
Collector – Emitter Voltage	I <sub>C</sub> = 50μA	T <sub>J</sub> = Over Temp. Range	40			40			V
Collector Leakage Current	V <sub>CE</sub> = 40V	T <sub>J</sub> = Over Temp. Range		0.1	50		0.1	50	μA
Collector Saturation	L 50mA			4	0		4	2	V
Voltage	I <sub>C</sub> = 50mA	T <sub>J</sub> = Over Temp. Range	I	1	1 2		1	2	V
Emitter Output Voltage	V <sub>IN</sub> = 20V	T <sub>J</sub> = Over Temp. Range	17	18		17	18		V
Emitter Voltage Rise Time	$R_E = 2k\Omega$			0.2	0.4		0.2		
Collector Voltage Fall Time	ollector Voltage Fall Time $R_{C} = 2k\Omega$			0.1	0.2		0.1		μs
	POWER CON	SUMPTION							
Standby Current	$V_{IN} = 40V$	T <sub>J</sub> = Over Temp. Range		5	10		5	10	mA

### NOTES

- 1. Test Conditions unless otherwise stated:  $V_{\text{IN}}$  = 20V ,  $I_{\text{REF}}$  = 0.
- 2.  $V_{CM} = +1.8 \text{ to } +3.4 \text{V}$ 3.  $V_{CM} = -1 \text{ to } +1 \text{V}$



## **APPLICATIONS INFORMATION**

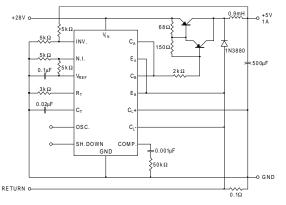
The IP1524 is a fixed-frequency pulse-width modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor ( $R_T$ ) and one timing capacitor ( $C_T$ ).  $R_T$  establishes a constant charging current for  $C_T$ , which is fed to the comparator providing linear control of the output pulse width by the error amplifier.

The IP1524 contains an on-board 5V regulator that serves as a reference as well as powering the IP1524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generate a feedback signal to the error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at C<sub>T</sub>. The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistor (Q<sub>1</sub> or Q<sub>2</sub>) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both outputs are never on simultaneously during the transition times.

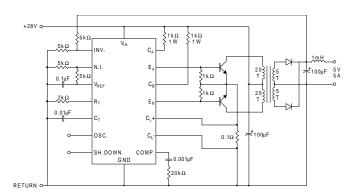
The width of the blanking pulse is controlled by the value of  $C_{T}$ .

The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current limiting and shutdown circuitry and can be overridden by signals from either of these inputs.

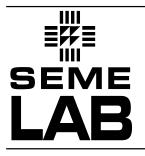
This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier, or to provide additional control to the regulator.



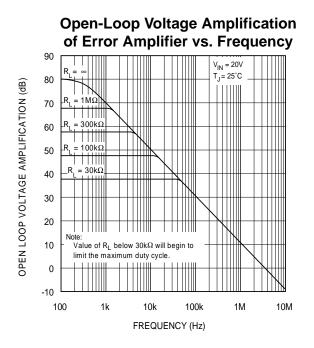
In this conventional single-ended regulator circuit, the two outputs of the IP1524 are connected in parallel for effective 0-90% duty cycle modulation. The use of an output inductor requires an R-C phase compensation network for loop stability.



Push-pull outputs are used in this transformer-coupled DC-DC regulating converter. Note that the oscillator must be set at twice the desired output frequency as the IP1524's internal flip-flop divides the frequency by 2 as it switches the PWM signal from one output to the other. Current limiting is done in the primary so that the pulse width will be reduced should transformer saturation occur.



## **TYPICAL PERFORMANCE CHARACTERISTICS**



Oscillator Frequency vs. Timing Components

