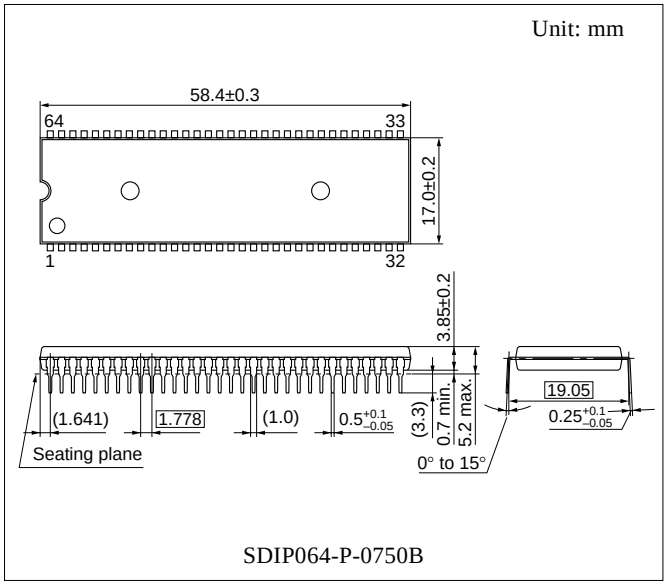
AN5095K

Single chip IC with I²C bus interface for PAL/NTSC color TV system

■ Overview

The AN5095K is an IC in which PAL/NTSC color television signal processing circuits are integrated into a single chip. Also, since the I²C bus interface is built in the IC, the rationalization of set production line can be realized.



SDIP064-P-0750B

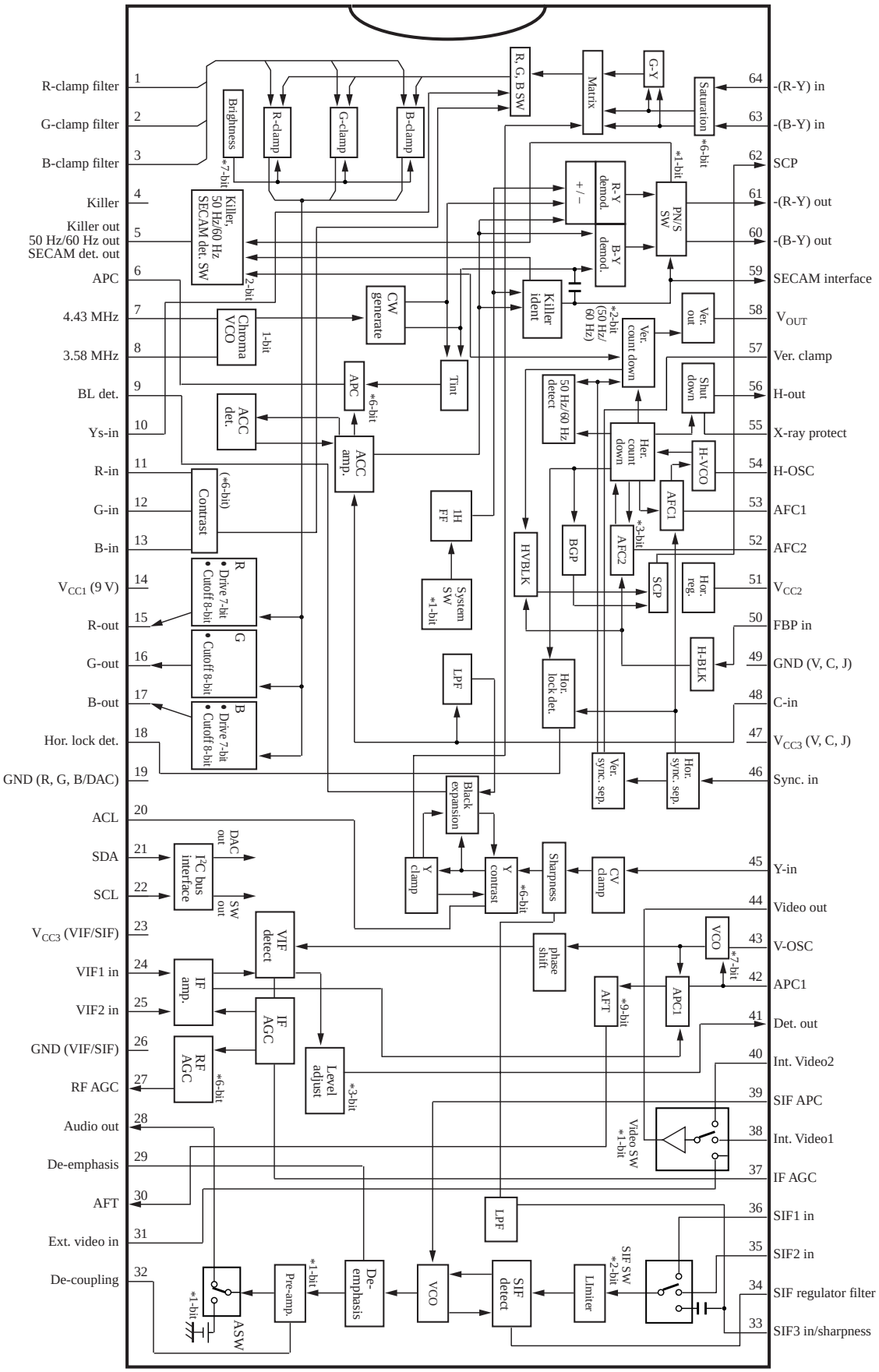
■ Features

- Built- in video IF circuit, sound IF circuit, video signal processing circuit, color signal processing circuit, sync. signal processing circuit
- Suitable for PAL/NTSC/AV-NTSC/M-NTSC systems
- 6 dB improved sound S/N (compared with the AN5195K-B/-C)
- Package: 64-SDIP, supply voltage: 5 V, 9 V

■ Applications

- Television and televideo

■ Block Diagram



■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	(R) clamp	33	SIF3 input/sharpness
2	(G) clamp	34	SIF regurator filter
3	(B) clamp	35	SIF2 input
4	Killer filter	36	SIF1 input
5	Killer out, 50 Hz/60 Hz out, SECAM det. out	37	IF AGC filter
6	Chroma APC filter	38	Internal videol input
7	Chroma VCO (4.43 MHz)	39	SIF APC filter
8	Chroma VCO (3.58 MHz)	40	Internal video2 input
9	Black level det./Blank off SW	41	VIF detect output
10	Y_S input (fast blanking)	42	VIF APC 1 filter
11	External R-input	43	VIF VCO (f_P/2)
12	External G-input	44	Video output
13	External B-input	45	Y-input
14	V_{CC1}	46	H, V sync. input
15	R-output	47	V_{CC3}-2 (chroma/jungle/DAC)
16	G-output	48	Chroma input/black expansion start
17	B-output	49	GND (video/chroma/jungle)
18	Hor.lock detect	50	FBP input
19	GND (R, G, B/I^2C/DAC)	51	V_{CC2} (hor. stability supply)
20	ACL	52	AFC2 filter
21	SDA	53	AFC1 filter
22	SCL	54	Hor. VCO (32 f_H)
23	V_{CC3}-1 (VIF/SIF)	55	X-ray protection input
24	VIF1 input	56	Hor. pulse output
25	VIF2 input	57	Ver. sync. clamp
26	GND (VIF/SIF)	58	Ver. pulse output
27	RF AGC output	59	SECAM interface
28	Audio output	60	-(B-Y) output
29	De-emphasis	61	-(R-Y) output
30	AFT output	62	Sandcastle pulse output
31	External video input	63	-(B-Y) input
32	DC De-coupling filter	64	-(R-Y) input

■ Absolute Maximum Ratings

Parameter	Symbol		Rating	Unit
Supply voltage	V_{CC}	$V_{CC1\ (14)}$	10.5	V
		$V_{CC3\ (23,\ 47)}$	6.0	
Supply current	I_{CC}	I_{14}	67	mA
		I_{23+47}	126	
		I_{51}	27	
Power dissipation *2	P_D		1 480	mW
Operating ambient temperature *1	T_{opr}		−20 to +70	°C
Storage temperature *1	T_{stg}		−55 to +150	°C

Note) ∗1: Except for the operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.
∗2: The power dissipation shown is for the IC package in free air at T_a = 70°C.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC1}	8.1 to 9.9	V
	V_{CC3}	4.5 to 5.5	
Terminal voltage	V_5	0 to 6	V
	V_{10}	0 to 6	
	V_{11}	0 to 6	
	V_{12}	0 to 6	
	V_{13}	0 to 6	
	V_{21}	0 to 6	
	V_{22}	0 to 6	
	V_{27}	0 to 10.5	
	V_{30}	0 to 10.5	
	V_{48}	0 to V_{14}	
	V_{50}	0 to V_{47}	
	V_{55}	0 to 2	
	V_{59}	0 to V_{14}	
Supply current	I_{51}	10 to 25	mA
Circuit current	I_{15}	−3.2 to +0.6	mA
	I_{16}	−3.2 to +0.6	
	I_{17}	−3.2 to +0.6	
	I_{41}	− 0.8 to +0.8	
	I_{44}	−1.1 to +0.4	
	I_{46}	− 0.8 to +0.1	

■ Recommended Operating Range (continued)

Parameter	Symbol	Range	Unit
Circuit current	I_{56}	−6.4 to +0.1	mA
	I_{58}	− 0.8 to +0.1	
	I_{59}	− 0.3 to +0.1	

Note) Do not apply external currents or voltages to any pins not specifically mentioned.
For circuit currents, '+' denotes current flowing into the IC, and '−' denotes current flowing out of the IC.

■ Electrical Characteristics at T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply						
Supply current 1	I_{14}	Current at V_{14} = 9 V	39	48	57	mA
Supply current 2	I_{23}	Current at V_{23} = 5 V	7	10	13	mA
Supply current 3	I_{47}	Current at V_{47} = 5 V	49	63	77	mA
Stabilized supply voltage	V_{51}	Voltage at I_{51} = 15 mA	5.8	6.5	7.2	V
Stabilized supply current	I_{51}	Current at V_{51} = 5 V	2	5	7	mA
Stabilized supply input resistance	R_{51}	DC measurement, slant between at I_{51} = 10 mA and 25 mA	1	5	10	Ω
VIF circuit Typical input; f_P = 38.9 MHz, V_{IN} = 90 dBμ, DAC data are typical						
Video detection output (typ.)	V_{PO}	Modulation m = 87.5%, data 0B = 44	1.7	2.1	2.5	V[p-p]
Video detection output (max.)	V_{POmax}	0B = 74	1.9	2.6	3.3	V[p-p]
Video detection output (min.)	V_{POmin}	0B = 04	1.1	1.6	2.1	V[p-p]
Video detection output-frequency characteristic	f_{PC}	Frequency which becomes −3 dB for 1 MHz output	5.5	8	12	MHz
Synchronous peak value voltage	V_{SP}	Synchronized peak value voltage at V[p-0] measurement	1.6	2.0	2.4	V
APC high-level pull-in range	f_{PPH}	High-pass side pull-in range (difference from f_P = 38.9 MHz)	1.0	2.0	—	MHz
APC low-level pull-in range	f_{PPL}	Low-pass side pull-in range (difference from f_P = 38.9 MHz)	—	−2.0	−1.0	MHz
RF AGC delay point adjustable range *1	ΔV_{RFDP}	Delay point in which data are 0A = 00 to 3F (input at V_{27} = approx. 6.5 V)	75	—	95	dBμ
VCO free-running frequency	Δf_P	Dispersion without V_{IN} V_{37} (IF AGC) = 0 V (measurement of the difference from 38.9 MHz)	−1.2	0	1.2	MHz
RF AGC maximum sink current	I_{RFmax}	Max. current IC can sink when pin 27 is low	1.5	3.0	—	mA
RF AGC minimum sink current	I_{RFmin}	IC leak current at which pin 27 is high	− 50	0	50	μA

Note) ∗1 to ∗9: Refer to "Explanation of test methods".

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VIF circuit (continued) Typical input; f_P = 38.9 MHz, V_{IN} = 90 dBμ, DAC data are typical						
AFT discrimination sensitivity *2	μ_{AFT}	Δf = ±25 kHz	40	57	75	mV/kHz
AFT center voltage	V_{AFT}	V_{30} at V_{IN} without input	4.0	4.5	5.0	V
AFT maximum output voltage	V_{AFTmax}	V_{30} at f = f_P −500 kHz	7.8	8.1	8.7	V
AFT minimum output voltage	V_{AFTmin}	V_{30} at f = f_P +500 kHz	0.3	0.8	1.0	V
Detection output resistance	R_{O41}	DC measurement, I_O = − 0.4 V to −1.0 mA	70	120	170	Ω
SIF circuit Typical input; f_S = 6.0 MHz, f_M = 400 Hz, V_{IN} = 90 dBμ						
Audio detection output (PAL, SIF1)	V_{SOP36}	Δf = ±50 kHz 0B-D3 = 0	0.90	1.15	1.40	V[rms]
Audio detection output (PAL, SIF2)	V_{SOP35}	Δf = ±50 kHz 0B-D3 = 0	0.90	1.15	1.40	V[rms]
Audio detection output (PAL, SIF3)	V_{SOP33}	Δf = ±50 kHz 0B-D3 = 0	0.90	1.15	1.40	V[rms]
Audio detection output NTSC/PAL	$R_{SN/P}$	Δf = ±25 kHz 0B-D3 = 1, ratio to PAL (V_{SOP36})	−2.5	− 0.5	1.5	dB
Audio detection output linearity	ΔV_{SOP}	f_S = 5.5 MHz and 6.0 MHz ratio to 6.5 MHz	−3	0	3	dB
SIF pull-in range NTSC (4.5 MHz)	f_{SNH} (4.5M)	Pull-in range of high-pass side	4.8	5.0	—	MHz
SIF pull-in range NTSC (4.5 MHz)	f_{SNL} (4.5M)	Pull-in range of low-pass side	—	4.0	4.2	MHz
SIF pull-in range PAL (5.5 MHz)	f_{SPH} (5.5M)	Pull-in range of high-pass side	5.8	6.0	—	MHz
SIF pull-in range PAL (5.5 MHz)	f_{SPL} (5.5M)	Pull-in range of low-pass side	—	5.0	5.2	MHz
SIF pull-in range PAL (6.0 MHz)	f_{SPH} (6.0M)	Pull-in range of high-pass side	6.3	6.5	—	MHz
SIF pull-in range PAL (6.0 MHz)	f_{SPL} (6.0M)	Pull-in range of low-pass side	—	5.5	5.7	MHz
SIF pull-in range PAL (6.5 MHz)	f_{SPH} (6.5M)	Pull-in range of high-pass side	6.8	7.0	—	MHz
SIF pull-in range PAL (6.5 MHz)	f_{SPL} (6.5M)	Pull-in range of low-pass side	—	6.0	6.2	MHz
De-emphasis terminal output resistance (PAL)	R_{29P}	Impedance of pin 29 at PAL	32	40	48	kΩ
De-emphasis terminal output resistance (NTSC)	R_{29N}	Impedance of pin 29 at NTSC	48	60	72	kΩ

Note) ∗1 to ∗9: Refer to "Explanation of test methods".

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
AV SW circuit						
Video SW voltage gain	G_{VSW}	f = 1 MHz, V_{IN} = 1 V[p-p]	5.7	6.7	7.7	dB
Video SW-frequency characteristic	f_{VSW}	Frequency to become −3 dB from f = 1 MHz, V_{IN} = 0.714 V[0-p]	8	10	—	MHz
Video SW external input terminal voltage	V_{31}	DC measurement	1.7	2.0	2.3	V
Video SW external output DC voltage	V_{44E}	DC measurement, 03-D7 = 1, 0B-D7 = 1	4.2	4.8	5.4	V
Video SW external input resistance	R_{I31}	DC measurement	44	56	68	kΩ
Video SW output resistance	R_{O44}	DC measurement, I_O = − 0.6 mA to −1.0 mA	110	150	190	Ω
Video SW internal clamp terminal voltage	$V_{38, 40}$	DC measurement, I_{IN} = −1.0 mA	1.4	1.7	2.0	V
Video SW internal output DC voltage	V_{44I}	DC measurement	3.7	4.3	4.9	V
Audio SW voltage gain	G_{ASW}	Data 03-D7 = 1, 0B-D7 = 1, (input from outside) f = 400 Hz, V_{IN} = 1 V[p-p]	−1	0	1	dB
Audio SW output DC voltage	V_{28}	DC measurement	3.7	4.2	4.7	V
Audio SW output resistance	R_{O28}	DC measurement	350	450	550	Ω
Video signal processing circuit	Typical input; 0.6 V[p-p] (V_{BW} = 0.42 V[p-p] stair-step) at G-out					
Video output (typ.)	V_{YO}	Data 03 = 20 (typ.) (contrast)	2.0	2.5	3.0	V[0-p]
Video output (max.)	V_{YOmax}	Data 03 = 3F (max.)	4.1	5.0	5.9	V[0-p]
Video output (min.)	V_{YOmin}	Data 03 = 00 (min.)	0.15	0.50	1.00	V[0-p]
Contrast variable range	$Y_{Cmax/min}$	$\frac{03 = 3F}{03 = 00}$	15	20	25	dB
Video frequency characteristic	f_{YC}	Pin 33 = 5 V (sharpness), frequency to become −3 dB from f = 0.2 MHz	5.5	6.0	—	MHz
Picture quality variable range	$Y_{Smax/min}$	$\frac{V_{33} = 7V}{V_{33} = 5V}$ f = 3.8 MHz	9	13	17	dB
Pedestal level (typ.)	V_{PED}	Data 02 = 40 (typ.) (brightness)	2.0	2.5	3.0	V
Pedestal variable width	ΔV_{PED}	Difference between data 02 = 00 and 7F	2.15	2.75	3.35	V
Brightness control sensitivity	ΔV_{BRT}	Average amount of change per 1-step between data 02 = 30 and 50	14	20	26	mV/Step
Video input clamp voltage	V_{YCLP}	Pin 45 clamp voltage	3.2	3.7	4.2	V
ACL sensitivity	ACL	Amount of change of Y-out, when V_{20} = 3.0 V → 3.5 V	2.7	3.2	3.7	V/V
Blanking level	V_{YBL}	Blanking pulse DC voltage	—	1.0	1.5	V

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Video signal processing circuit (continued)		Typical input; 0.6 V[p-p] (V_{BW} = 0.42 V[p-p] stair-step) at G-out				
Service SW * threshold voltage	V_{STH}	Voltage at which vertical output stops when pin 20 (ACL) voltage is decreased	—	—	0.3	V
DC restoration ratio	T_{DC}	APL10% to 90% $T_{DC} = \frac{\Delta AC - \Delta DC}{\Delta AC} \times 100$	90	100	110	%
Video input clamp current	I_{YCLP}	DC measurement; Sink current inside of IC	6	11	16	µA
Pedestal difference voltage	ΔV_{IPL}	Pedestal difference voltage of R, G, B-out	– 0.2	0	0.2	V
Brightness voltage tracking	ΔT_{BL}	Ratio of R, G, B-out fluctuation level for data 02 (bright) = 20 to 60	0.9	1.0	1.1	Time
Video voltage gain relative ratio	ΔG_{YC}	Output ratio of R, B-out against G-out	0.8	1.0	1.2	Time
Video voltage gain tracking	ΔT_{CONT}	Ratio of gain of R, G, B-out for data 03 (contrast) = 10 to 30	0.9	1.0	1.1	Time/ Time
Color signal processing circuit		Burst 150 mV[p-p] (PAL), reference is B-out				
Color-difference output (typ.)	V_{CO}	Input; Color bar Data 00 = 20 (typ.), 03 = 20 (typ.)	2.9	3.7	4.5	V[p-p]
Color-difference output (max.)	V_{COmax}	Data 03 = 3F, amplitude of one side 03 = 20	2.6	3.3	—	V[0-p]
Color-difference output (min.)	V_{COmin}	Data 00 = 00, 03 = 20	—	—	100	mV[p-p]
Contrast adjustable range	$C_{Cmax/min}$	$\frac{03 = 3F}{03 = 00}$ 00 = 20	15	20	25	dB
ACC characteristic 1	ACC1	Burst 150 mV[p-p] → 300 mV[p-p]	0.9	1.0	1.2	Time
ACC characteristic 2	ACC2	Burst 150 mV[p-p] → 30 mV[p-p]	0.8	1.0	1.2	Time
NTSC tint center	$\Delta\theta_C$	The difference from data 01 = 20 at which tint is adjusted to center	–7	0	7	Step
NTSC tint adjustable range 1	$\Delta\theta_1$	Input; Rainbow data 01 = 3F	30	50	65	deg
NTSC tint adjustable range 2	$\Delta\theta_2$	Input; Rainbow data 01 = 00	– 65	– 50	– 30	deg
Color-difference output ratio (R)	R/B	Input; Rainbow for both PAL/NTSC	0.46	0.56	0.66	Time
Color-difference output ratio (G)	G/B	Input; Rainbow for both PAL/NTSC	0.28	0.34	0.40	Time
Color-difference output angle (R)	∠R	Input; Rainbow for both PAL/NTSC	78	90	102	deg
Color-difference output angle (G)	∠G	Input; Rainbow for both PAL/NTSC	224	236	248	deg
PAL color killer tolerance	V_{KILLP}	0 dB = 150 mV[p-p]	– 57	– 44	– 34	dB
NTSC color killer tolerance	V_{KILLN}	0 dB = 150 mV[p-p]	– 57	– 44	– 34	dB
APC high-lebel pull-in range	f_{CPH}	Both PAL/NTSC	450	700	—	Hz
APC low-lebel pull-in range	f_{CPL}	Both PAL/NTSC	—	–700	– 450	Hz
Color killer detection output voltage (color)	V_{KC}	V_5 , killer out at which chroma input data 0A-D6 = 0, 0A-D7 =1	4.5	5.0	—	V

Note) *: Since pin 20 is also used partly as service SW when used as ACL, a sufficient care must be taken so as not to become V_{20} < 0.9 V in carrying out set design.

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Color signal processing circuit (continued) Burst 150 mV[p-p] (PAL), reference is B-out						
Color killer detection output voltage (B & W)	V_{KBW}	V_5 , killer out at which chroma input data 0A-D6 = 0, 0A-D7 =1	0	0.1	0.5	V
Demodulation output -(B-Y)	V_{DB}	Input; Color bar measured at pin 60 for both PAL/NTSC	555	695	835	mV[p-p]
Demodulation output -(R-Y)	V_{DR}	Input; Color bar measured at pin 61 for both PAL/NTSC	430	540	650	mV[p-p]
Demodulation output angle ∠(B-Y)	$\angle R_{DB}$	B-Y axis out of phase	– 6	0	6	deg
Demodulation output angle ∠(R-Y)	$\angle R_{DR}$	B-Y axis phase difference	84	90	96	deg
CW output level (4.43 MHz) *3	V_{CWP}	AC component, when VCO is set at 4.43 MHz	250	350	450	mV[p-p]
CW output level (3.58 MHz) *3	V_{CWN}	AC component, when VCO is set at 3.58 MHz	—	—	50	mV[p-p]
CW output level period (SECAM) *3	t_{CW}	Period in which CW is outputted at SECAM, PAL	1.31	1.41	1.51	ms
SECAM judgment current	I_{SECAM}	The minimum value to take out current from pin 59 to discriminate as SECAM	50	100	150	µA
SECAM judgment output	V_{SE}	V_5 , det. out, when SECAM signal input data 0A-D6 = 1, 0A-D7 = 0, SECAM	4.5	5.0	—	V
PAL/NTSC DC level	V_{59PN}	V_{59} DC level at PAL/NTSC	0.8	1.3	1.65	V
SECAM DC level	V_{59S}	V_{59} DC level at SECAM	4.1	4.6	5.1	V
RGB processing circuit DAC data are typicals						
Drive adjusting range	G_{DV}	AC change amount for R, B-out between drive adjustment max. and min.	5	6	7	dB
Offset adjusting range	$V_{CUT-OFF}$	DC change amount for R, G, B-out between offset adjustment max. and min.	2.2	2.5	2.8	V
Y_S threshold voltage	V_{YSON}	Minimum DC voltage at which Y_S turns on	1.0	—	—	V
Y_S threshold voltage	V_{YSOF}	Maximum DC voltage at which Y_S turns off	—	—	0.4	V
External R, G, B pedestal difference voltage	ΔV_{EPL}	Y_S = 1 V is applied	– 200	0	200	mV
Internal and external pedestal difference voltage	$\Delta V_{PL/IE}$	Internal part — external part	– 200	0	200	mV
External R, G, B output voltage	V_{ERGB}	Input 0.7 V[p-p], contrast 03 = 20 (typ.)	1.8	2.2	2.7	V[p-p]
External R, G, B output difference voltage	ΔV_{ERGB}	Input 0.7 V[p-p], contrast 03 = 20 (typ.)	0.8	1.0	1.2	Time
External R, G, B contrast variable range	$EC_{max/min}$	03 = 3F / 03 = 00	12	17	22	dB

Note) ∗1 to ∗9: Refer to "Explanation of test methods".

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
RGB processing circuit (continued) DAC data are typicals						
External R, G, B frequency characteristic	f_{RGBC}	Input 0.2 V[p-p]	8	10	—	MHz
Internal and external R, G, B output voltage ratio	$V_{E/I}$	External part 0.7 V[p-p]/internal part 0.6 V[p-p] input, contrast 03 = 20 (typ.)	0.78	0.92	1.06	Time
Synchronizing signal processing circuit						
Horizontal free run frequency	f_{HO}	Without sync. signal input	15.33	15.63	15.93	kHz
Horizontal output pulse duty cycle	τ_{HO}	Upward pulse duty cycle	31	37	43	%
Horizontal pull-in range	f_{HP}	Difference from f_H = 15.625 kHz	± 500	± 650	—	Hz
PAL horizontal free run frequency	f_{VO-P}	Data 01-D7 = 1, 02-D7 = 0, forced 50 Hz mode, without sync. signal input	48	50	52	Hz
NTSC vertical free run frequency	f_{VO-N}	Data 01-D7 = 1, 02-D7 = 1, forced 60 Hz mode, without sync. signal input	58	60	62	Hz
Vertical output pulse width	τ_{VO}	For both PAL/NTSC	9	10	11	1/fH
PAL vertical pull-in range	f_{VPP}	f_H = 15.625 kHz, forced 50 Hz mode	46	—	54	Hz
NTSC vertical pull-in range	f_{VPN}	f_H = 15.75 kHz, forced 60 Hz mode	56	—	64	Hz
Horizontal high-level output voltage	V_{56H}	High-level DC voltage	2.8	3.1	3.4	V
Horizontal low-level output voltage	V_{56L}	Low-level DC voltage	—	—	0.3	V
Vertical high-level output voltage	V_{58H}	High-level DC voltage	3.9	4.2	4.5	V
Vertical low-level output voltage	V_{58L}	Low-level DC voltage	—	—	0.3	V
Screen center variable range	ΔT_{HC}	Change amount of phase difference between sync. and H-out of data 0B = 40 to 47	2.6	3.2	4.4	µs
Overvoltage protection operation voltage	V_{X-RAY}	The pin 55 minimum voltage at which H-out does not appear any longer	0.60	0.68	0.76	V
Vertical frequency discrimination (50)	f_{50}	Vertical frequency at which V_5 becomes low (< 0.5 V)	47	—	55	Hz
Vertical frequency discrimination (60)	f_{60}	Vertical frequency at which V_5 becomes high (> 4.5 V)	57	—	63	Hz
Synchronous signal clamp voltage	V_{46}	V_{46} clamp voltage	1.1	1.4	1.7	V
Horizontal output start voltage	V_{fHS}	The minimum V_{50} at f_0 > 10 kHz and horizontal oscillation output is higher than 1 V[p-p]	3.4	4.2	5.0	V
I^2C interface						
Sink current when ACK	I_{ACK}	The maximum value of pin 21 sink current at ACK	1.5	2.0	5.0	mA
SCL, SDA signal high level input	V_{IHI}		3.1	—	—	V
SCL, SDA signal low level input	V_{ILO}		—	—	0.9	V
Allowable maximum input frequency	f_{Imax}		—	—	100	kbit/s

■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VIF circuit Typical input; f_P = 38.9 MHz, V_{IN} = 90 dBμ						
Input sensitivity	V_{PS}	Input level at which V_{PO1} becomes –3 dB	—	45	—	dBμ
Maximum allowable input	V_{Pmax}	Input level at which V_{PO1} becomes +1 dB	—	110	—	dBμ
SN ratio	SN_P		50	—	—	dB
Differential gain	DG_P		—	—	5	%
Differential phase	DP_P		—	—	5	deg
Black-noise detection level *4	ΔV_{BN}	Difference from sync. peak value	—	– 45	—	IRE
Black-noise clamp level *4	ΔV_{BNC}	Difference from sync. peak value	—	45	—	IRE
RF-AGC operation sensitivity	G_{RF}	Input level difference, when V_{27} = 1 V goes to 7 V	0.5	—	3.0	dB
VCO switch-on drift	Δf_{PD}	Frequency drift from 5 sec. to 5 min. after SW-on	—	—	200	kHz
Inter modulation *5	IM	$V_{fC} - V_{fP}$ = –2 dB, $V_{fS} - V_{fP}$ = –12 dB	46	—	—	dB
RF-AGC adjustment sensitivity	S_{RF}	Output voltage in data 1-step, average change amount of V_{27}	1	—	4	V/step
AFT offset adjustment sensitivity	S_{AFT}	Output voltage in data 1-step, average change amount of V_{30}	0.1	—	0.3	V/step
Video detection output fluctuation with V_{CC}	$\Delta V_{P/V}$	V_{CC} = ±10%	—	—	±15	%
Video detection output-temperature characteristics	$\Delta V_{P/T}$	T_a = –20°C to +70°C	—	—	±10	%
Input resistance (pin 24, pin 25)	$R_{I24,25}$	f = 38.9 MHz	—	1.2	—	kΩ
Input capacitance (pin 24, pin 25)	$C_{I24,25}$	f = 38.9 MHz	—	4.0	—	pF
Sound-IF output level	V_{SIF}	f_S = 38.9 MHz – 6.0 MHz, P/S = 20 dB	90	—	110	dBμ
VCO control sensitivity	β_P	ΔV_{42} = ±0.1 V	2.0	—	3.5	kHz/mV
VCO adjustment range	f_{VCO}	Free-running frequency change width at data 0C = 00 to 7F	3	—	5	MHz
RF-AGC delay point-temperature characteristics	$\Delta V_{DP/T}$	T_a = –20°C to +70°C	—	—	5	dB
VCO free-running frequency-temperature characteristics	$\Delta f_{P/T}$	T_a = –20°C to +70°C	—	300	—	kHz
AFT center frequency-temperature characteristics	$\Delta f_{AFT/T}$	Input frequency at which AFT output voltage becomes 4.5 V, T_a = –20°C to +70°C	—	300	—	kHz
External mode output DC voltage	V_{41EXT}	Output DC voltage at AV-SW outside mode	0.5	1.0	1.8	V

Note) ∗1 to ∗9: Refer to "Explanation of test methods".

■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SIF circuit Typical input; f_S = 6.0 MHz, f_M = 400 Hz, V_{IN} = 90 dBμ						
Input limiting level	V_{LIM}	Input level, when V_{SOP} becomes –3 dB	—	—	50	dBμ
AM rejection ratio	AMR	AM = 30%	55	—	—	dB
Total harmonic distortion	THD	Δf = ±50 kHz	—	—	1.0	%
SN ratio	SN_A	Δf = ±50 kHz, f_M = 400 Hz, on/off	55	—	—	dB
Audio output fluctuation with V_{CC}	$\Delta V_{S/V}$	V_{CC} = ±10%	—	—	±10	%
Audio output - temperature characteristics	$\Delta V_{S/T}$	T_a = –20°C to +70°C	—	—	±10	%
SIF input resistance	R_{I35}	DC measurement	—	31.5	—	kΩ
SIF input resistance	R_{I36}	DC measurement	—	31.5	—	kΩ
AV-SW circuit						
Video-SW crosstalk (inside → inside)	C_{TVII}	f = 1 MHz, V_{IN} = 1 V[p-p], inside → inside	—	—	– 55	dB
Video-SW crosstalk (outside → inside)	C_{TVEI}	f = 1 MHz, V_{IN} = 1 V[p-p], inside → outside, outside → inside	—	—	– 55	dB
Audio-SW crosstalk (inside → inside)	C_{TAII}	f_S = 6.5 MHz, f_M = 400 Hz, V_{IN} = 1 V[p-p], f_S = 6.5 MHz, f_M = 1.0 kHz, V_{IN} = 1 V[p-p]	—	—	– 60	dB
Video signal processing circuit Typical input; 0.6 V[p-p] (V_{BW} = 0.42 V[p-p] stair-step) at G-out						
Black level expansion 1 *6	V_{BL1}	Input: All black, difference between pin 9 = 9 V and open (with RC)	–100	0	100	mV
Black level expansion 2 *6	V_{BL2}	Input: All black, difference between pin 9 = 3 V and 9 V	400	700	1000	mV
Black level expansion 3 *6	V_{BL3}	Input: Approx. 20 IRE, voltage difference between pin 9 = open and 9 V at 03 (contrast) = 3F (max.)	100	300	500	mV
Contrast change by sharpness	ΔV_{CS}	Y-out output difference at sharpness between max. and min.	– 300	0	300	mV
Brightness change by sharpness	ΔV_{BS}	Pedestal level DC difference at sharpness between max. and min.	– 250	0	250	mV
Input dynamic change	V_{Imax}	03 (contrast) = 20 (typ.)	—	—	1.6	V[p-p]
Y-signal SN-ratio	SN_Y	03 (contrast) = 3F (max.)	53	—	—	dB
Black level expansion start point *6	V_{BLS}	Start point at V_{48} = 4.5 V	37	42	47	IRE
Video output fluctuation with V_{CC}	$\Delta V_{Y/V}$	V_{CC1} = 9 V (allowance: ±10%)	—	—	±15	%
Video output - temperature characteristics	$\Delta V_{Y/T}$	T_a = –20°C to +70°C	—	—	±10	%
ACL start point	V_{ACL}	V_{20} at which the output amplitude becomes 90% when ACL terminal (V_{20}) is decreased from 5 V	3.4	3.7	4.0	V

Note) *1 to *9: Refer to "Explanation of test methods".

■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Color signal processing circuit		Burst 150 mV[p-p] (PAL), reference is B-out				
Demodulation output residual carrier	V_{CAR1}	$2f_{SC}$ level of pin 60 and pin 61	—	—	30	mV
Color-difference output residual carrier	V_{CAR2}	$2f_{SC}$ level of pin 15, pin 16 and pin 17	—	—	50	mV
VCO free-running frequency (PAL)	f_{CP}	Difference from f = 4.433619 MHz	−300	—	300	Hz
VCO free-running frequency (NTSC)	f_{CN}	Difference from f = 3.579545 MHz	−300	—	300	Hz
f_{CO} fluctuation with V_{CC}	$\Delta f_C / V_{CC}$	V_{CC1} = 9 V (allowance: ±10%), V_{CC3} = 5 V (allowance: ±10%)	−300	—	300	Hz
Static phase error (PAL)	$\Delta\theta_P$	Tint gap at Δf_C = −300 Hz to +300 Hz change	—	—	5	deg/ 100 Hz
Static phase error (NTSC)	$\Delta\theta_N$	Tint gap at Δf_C = −300 Hz to +300 Hz change	—	—	5	deg/ 100 Hz
PAL/NTSC ratio	$R_{P/N}$	Output amplitude ratio between PAL and NTSC	0.7	1.0	1.3	Time
Line crawling	ΔV_{PAL}	Pin 61: Output amplitude difference per 1H at -(R-Y) terminal	—	—	50	mV
Color-difference output bandwidth	f_{CC}	Band to become −3 dB	1.0	—	—	MHz
Color-difference output fluctuation with V_{CC}	$\Delta V_{C/V}$	V_{CC1} = 9 V (allowance: ±10%), V_{CC3} = 5 V (allowance: ±10%)	—	—	±15	%
Color-difference output - temperature characteristics	$\Delta V_{C/T}$	T_a = −20°C to 70°C	—	—	±15	%
PAL/NTSC output impedance	$R_{O60,61PN}$	DC measurement	400	510	620	Ω
SECAM output impedance	$R_{O60,61S}$	DC measurement	100	—	—	kΩ
Color, black & white DC difference voltage	ΔV_{CBW}	Pedestal voltage difference between with and without burst signal	− 60	0	60	mV
(C-Y)/Y ratio *7	$R_{C/Y}$	Color bar input, B-out contrast typ. color data 00 = 30	0.9	1.2	1.5	V[0-p]/ V[0-p]
RGB processing circuit						
Y_S change-over speed	f_{YS}	f_{YS} , when Y_S input is 3 V[0-p] and output level is −3 dB	7	—	—	MHz
Outside R, G, B input dynamic range	V_{DEXT}	Contrast max. data 03 = 3F	1.0	—	—	V[p-p]
Inside and outside crosstalk	CT_{RGB}	Leakage at f = 1 MHz, 1 V[p-p], Y_S = 5 V	—	—	−50	dB
Synchronizing signal processing circuit						
Lock detection output voltage	V_{LD}	V_{18} at horizontal AFC lock	5.7	6.3	6.9	V
Lock detection charge and discharge current	I_{LD}	DC measurement	±0.6	±0.8	±1.1	mA

Note) ∗1 to ∗9: Refer to "Explanation of test methods".

■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Synchronizing signal processing circuit (continued)						
FBR (R, G, B) slice level	V_{FBP}	Pin 50 minimum voltage at which blanking is applied to R, G, B output	0.4	0.75	1.1	V
FBP (AFC2) slice level	V_{FBPH}	Pin 50 minimum voltage in which AFC2 operates	1.5	1.9	2.3	V
Horizontal AFC μ	μ_H	DC measurement	30	37	44	μA/μs
Horizontal VCO β	β_H	β curve slant near f = 15.75 kHz	1.4	1.9	2.4	Hz/mV
Burst gate pulse position *8	P_{BGP}	Delay from H sync. rise for both PAL/NTSC	0.2	0.4	0.6	μs
PAL burst gate pulse width *8	W_{BGPP}		3.4	4.0	4.6	μs
NTSC burst gate pulse width *8	W_{BGPN}		2.5	3.0	3.5	μs
Burst gate pulse output voltage	V_{BGP}	Pin 62 DC voltage during BGP period	4.5	4.7	4.9	V
H blanking pulse output voltage	V_{HBLK}	Pin62 DC voltage during H blanking pulse period	2.1	2.4	2.7	V
V blanking pulse output voltage	V_{VBLK}	Pin62 DC voltage during V blanking pulse period	2.1	2.4	2.7	V
PAL V blanking pulse width	W_{VP}	Pulse width at f = 15.625 kHz	1.31	1.41	1.51	ms
NTSC V blanking pulse width	W_{VN}	Pulse width at f = 15.73 kHz	1.01	1.11	1.21	ms
FBP allowable range *9	T_{FBP}	Time from H-out rise to FBP center	12	—	19	μs
FBP maximum allowable input voltage	V_{AFBP}		2.5	—	5.0	V
I^2C interface						
Bus free before start	t_{BUF}		4.0	—	—	μs
Start condition set-up time	$t_{SU, STA}$		4.0	—	—	μs
Start condition hold time	$t_{HD, STA}$		4.0	—	—	μs
Low period SCL, SDA	t_{LOW}		4.0	—	—	μs
High period SCL	t_{HIGH}		4.0	—	—	μs
Rise time SCL, SDA	t_r		—	—	1.0	μs
Fall time SCL, SDA	t_f		—	—	0.35	μs
Data set-up time (write)	$t_{SU, DAT}$		0.25	—	—	μs
Data hold time (write)	$t_{HD, DAT}$		0	—	—	μs
Acknowledge set-up time	$t_{SU, ACK}$		—	—	3.5	μs
Acknowledge hold time	$t_{HD, ACK}$		0	—	—	μs
Stop condition set-up time	$t_{SU, STO}$		4.0	—	—	μs

Note) ∗1 to ∗9: Refer to "Explanation of test methods".

■ Electrical Characteristics at T_a = 25°C (continued)

- Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DAC						
3-bit, 6-bit, 7-bit DAC DNLE	$L_{3,6,7}$	1LSB = {data (max.) – data (00)} /7, 63, 127	0.1	1.0	1.9	LSB/ Step
8-bit DAC DNLE	L_8	1LSB = {data (FF) – data (00)} /255 (7F → 80 excluded)	0.1	1.0	1.9	LSB/ Step
8-bit DAC DNLE (80)	$L_{8\text{-}80}$	LSB = {data (FF) – data (00)} /255 (7F → 80)	0.1	1.0	2.9	LSB/ Step
AFT DAC overlap	ΔStep	8-bit of AFT double-stage changeover overlap	27	32	37	Step

- Explanation of test methods

∗1: RF AGC delay point adjusting range: ΔV_{RFdp}

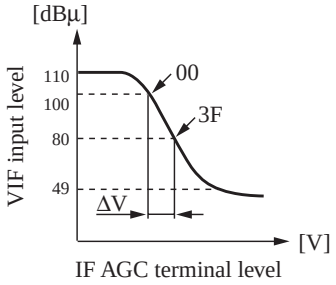


Figure 1. Gain reduction curve

In the case of VIF gain reduction curve (figure 1), if the RF AGC delay point adjustment DAC (0 A) goes 00 to 3F, the internal comparison voltage changes by ΔV, and the delay point adjustment range is determined.

∗2: AFT discrimination sensitivity: μAFT

Adjust DAC (0C-D7) and DAC (09) so that the AFT output voltage (V_{30}) becomes approx. 4.5 V when f_P = 38.9 MHz.

Measure ΔV_{30} when f_P = 38.9 MHz ±25 kHz.

∗3: Refer to "■ Technical Information 4. 7) PAL/NTSC, SECAM interface".

∗4: Black noise detection level: ΔV_{BN}

Black noise clamp level: ΔV_{BNC}

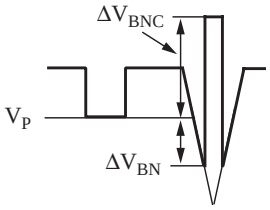


Figure 2. Black noise rejection characteristic

∗5: Inter modulation: IM

Apply the signal of f_P = 38.9 MHz, 90 dBμ and fix the voltage of pin 37 (IF AGC) under that condition.

f_P = 38.9 MHz, 82 dBμ
f_P = 38.9 MHz – 4.43 MHz, 80 dBμ
f_P = 38.9 MHz – 6.0 MHz, 70 dBμ

} Input those 3 signals and measure 1.57 MHz component of the detection output.

$$IM = 20\text{Log}\ \frac{\text{vieo component [rms]}}{V_{1.57\ MHz}\ [\text{rms}]}$$

■ Electrical Characteristics at T_a = 25°C (continued)

• Explanation of test methods (continued)

∗6: Black level extension: V_{BL}

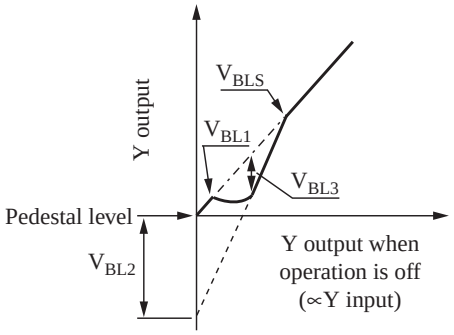


Figure 3. Black level expansion characteristics

In the black level extension characteristics (figure 3), when the voltage of pin 9 (black level detection filter) is V_{CC1} = 9 V, the operation of the black level extension circuit is turned off and the characteristic becomes as shown by the line - - - - -. Also, if the voltage of pin 9 is set at 3 V, the black level extension forcibly comes to start and the characteristic becomes as shown by the line ------. When pin 9 is set by only R, C filter, the black level extension characteristic as shown by the line ——— can be obtained.

V_{BL3} shows an output level difference between the black extension is off and the normal operation when the video input level is constant in 20 IRE.

V_{BLS} is a point where the black extension comes to start and can be adjusted by the DC voltage of pin 48 (C_{IN}).

V_{48}	2.5 V	4.5 V	6.5 V
Start point	52 IRE	42 IRE	32 IRE

∗7: (C-Y)/Y ratio: RC/Y

C-Y is the voltage from 0 level to the peak of B-out when color is typ. (00 = 20) and contrast is typ. (03 = 20). Y is the voltage from the pedestal of contrast at typ. to 100 IRE white level.

∗8: Burst gate pulse

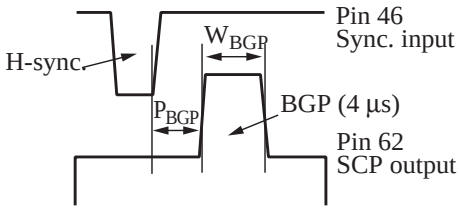


Figure 4. Burst gate pulse

As shown in figure 4, the position of the burst gate pulse is the period from the rise time of the H-sync. signal of pin 46 to the rise time of BGP.

∗9: FBP allowable range : t_{FBP}

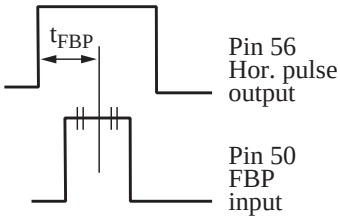
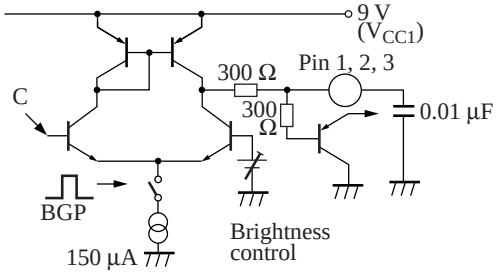
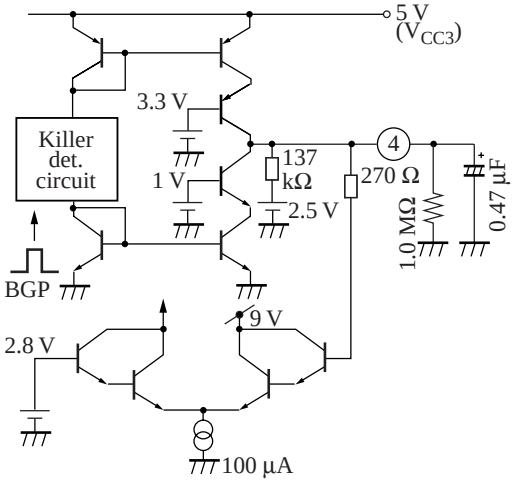
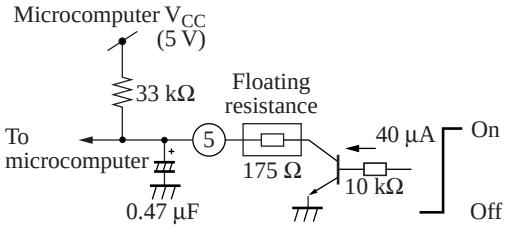
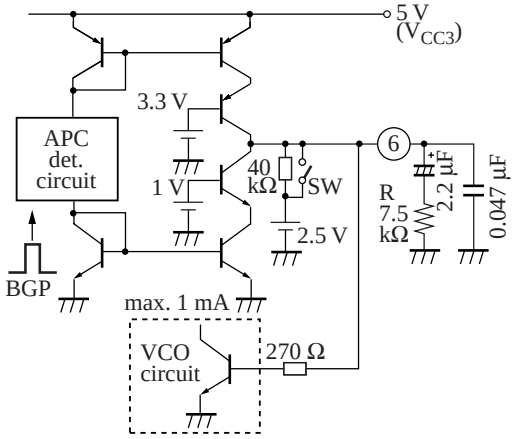
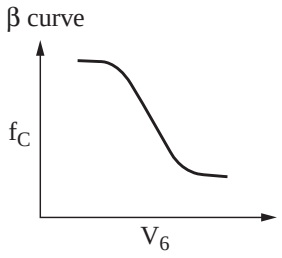


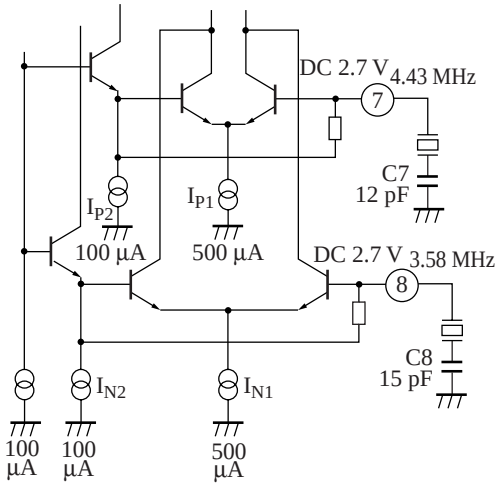
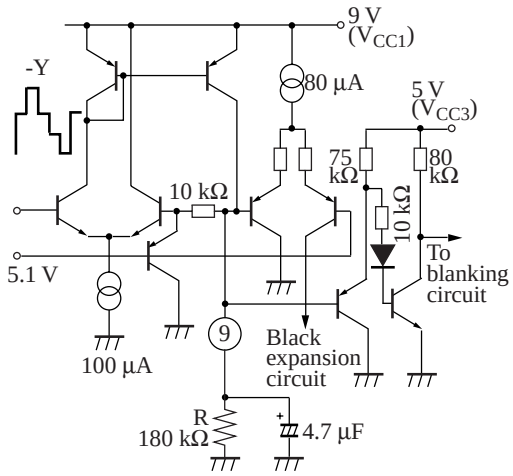
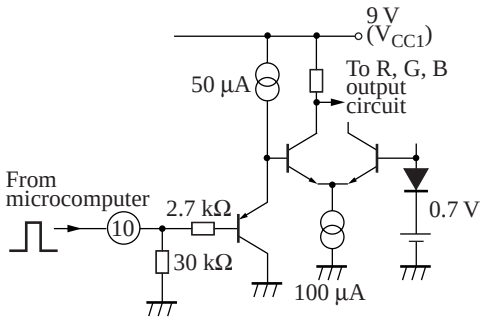
Figure 5. FBP allowable range

Figure 5 shows the relationship between Hor. pulse and FBP. The phase delay from Hor. pulse to FBP differs from set to set. This IC has an adjusting function for the screen center position. The phase range in which this function normally operate is t_{FBP}.

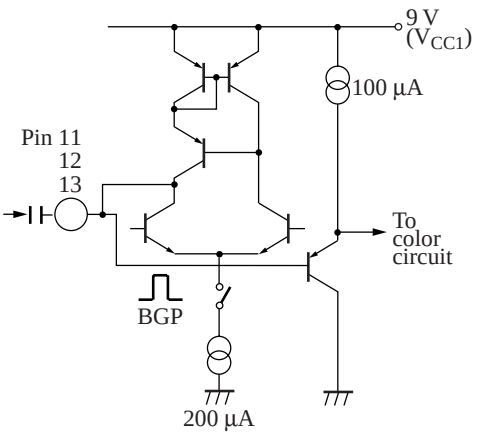
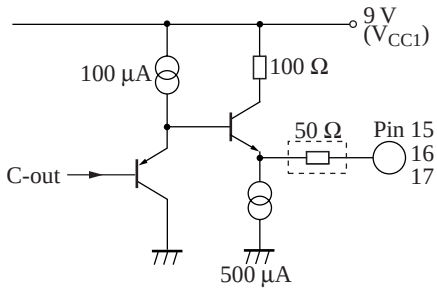
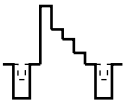
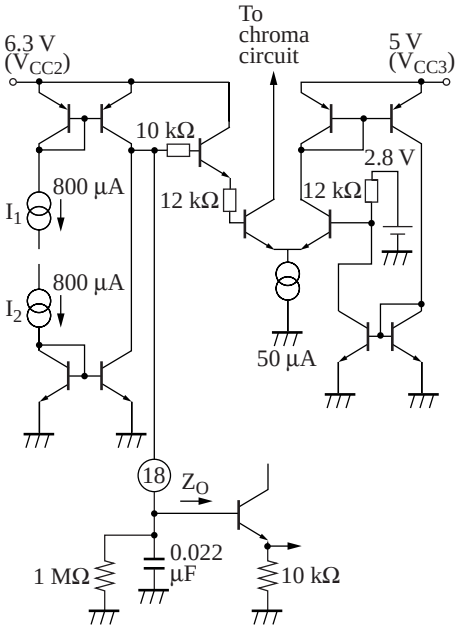
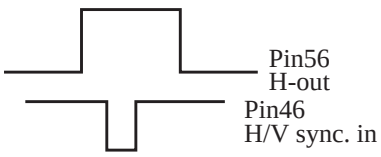
■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	voltage
1 2 3		Pin 1; Primary color signal clamp pin (R) Pin 2; Primary color signal clamp pin (G) Pin 3; Primary color signal clamp pin (B): For the clamp pulse, the internal clamp pulse (BGP) is used.	DC approx. 7 V
4		Killer filter pin: Filter pin of killer detection circuit (operates for BGP period). Killer turns on (without color output) at a voltage of 2.8 V or lower.	DC approx. 3.3 V
5		Killer, 50 Hz/60 Hz, SECAM det. output pin: Selective output by SW (I^2C bus). The load resistance 33 kΩ should be connected to microcomputer V_{CC} .	DC Low level 0.2 V High livel 5 V
6		APC filter pin: Filter pin of APC detection circuit (operates for BGP period). The detection sensitivity becomes high when the external resistance is high, (tend to be pulled-in easily. tend to be influenced by noise).  Stop APC circuit by short-circuiting 40 kΩ at SECAM.	DC approx. 2.5 V

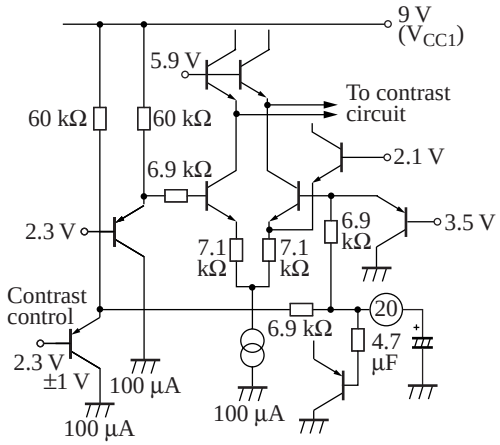
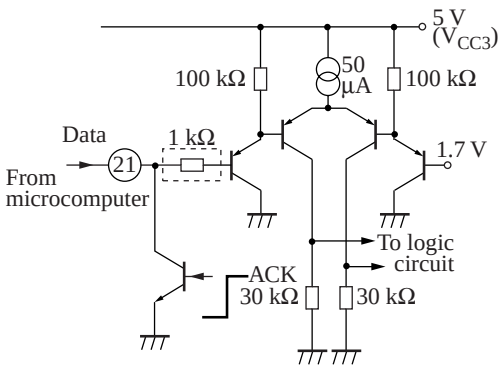
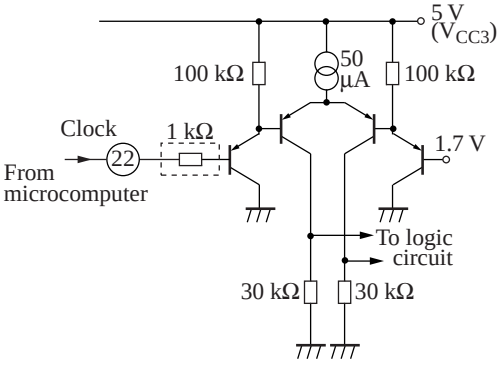
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	voltage
7 8		Pin 7; Chroma. oscillation pin (4.43 MHz) Pin 8; Chroma. oscillation pin (3.58 MHz): Either one of the oscillations of 4.43 MHz or 3.58 MHz is performed by chroma. oscillation pin. Frequency changeover is carried out by 08-D7 bit of I^2C bus. When 08-D7 = 0; I_{P1} , I_{P2} turn on, and 4.43 MHz oscillates When 08-D7 = 0; I_{N1}, I_{N2} turn on and 3.58 MHz oscillates The pattern from pin to oscillator should be as short as possible.	AC $f = f_C$ approx. 0.7 V[p-p]
9		Black level detection pin Blanking off SW pin: Black level detection filter pin for black extension circuit. Excluding the blanking period, holds the most black Y level. The sensitivity that the black extension (area judged as black) comes work is variable by means of external R. When R is large, it responds to a small area. Apply V_{CC} (9 V) to pin 9 when stopping the black extension circuit. Blanking is turned off when pin 9 is GND (black extension is also off).	DC approx. 5.1 V
10		Y_S input pin: Fast-blanking pulse input pin for external analog R, G, B. On at a voltage over 1 V. Off at a voltage under 0.4 V.	AC (pulse)

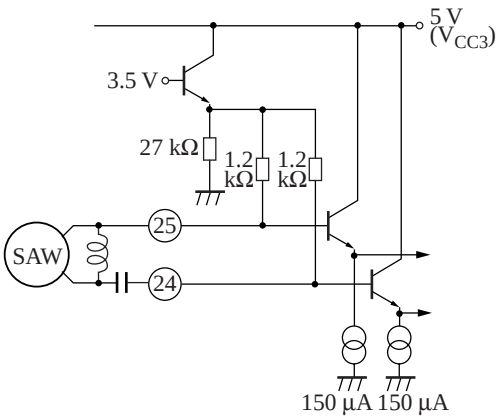
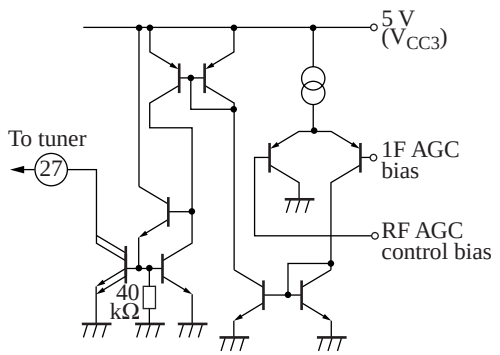
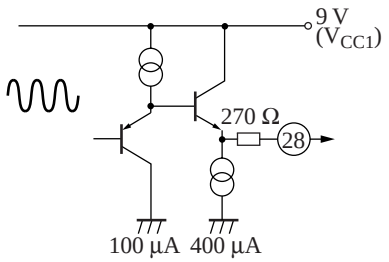
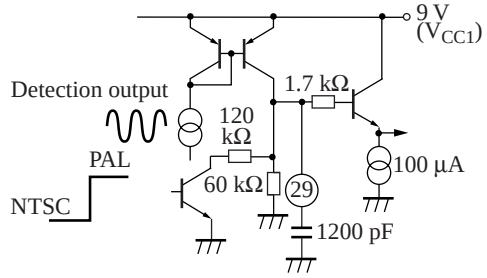
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	voltage
11 12 13		Pin11; External R input pin Pin12; External G input pin Pin13; External B input pin: The output will change linearly depending on the input level.	AC
14	—	V_{CC1} (9 V typ.): Output block of VIF, SIF circuit. AV SW circuit. Video circuit. RGB circuit.	DC 9 V
15 16 17		Pin15; R-out pin Pin16; G-out pin Pin17; B-out pin: BLK level approx. 0.9 V. Black (pedestal) level approx. 2.2 V. Blanking can be released by setting pin 9 (black level detection pin) at 0 V.	AC 
18		Horizontal synch. detection pin: The phase of horizontal sync. signal and horizontal output pulse is detected and outputted. Pin 18 becomes low if out of synchronization. Color control becomes minimum and chroma signal disappears in asynchronous state. Pay attention to impedance when the voltage of pin 18 is utilized for microcomputer. (500 kΩ or higher Z_O is required)  H Sync. period When pin 56 is high: I_1 on When pin 56 is low: I_2 on	DC When synchronous approx. 6 V When asynchronous approx. 0.3 V

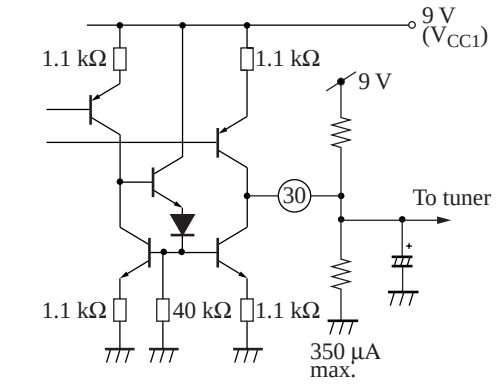
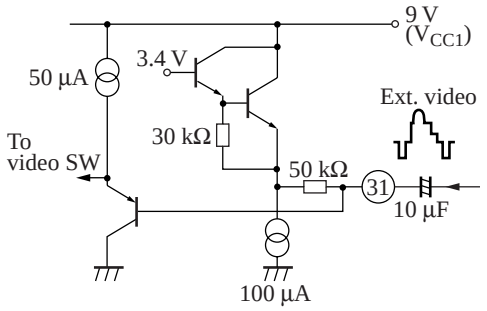
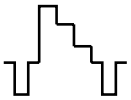
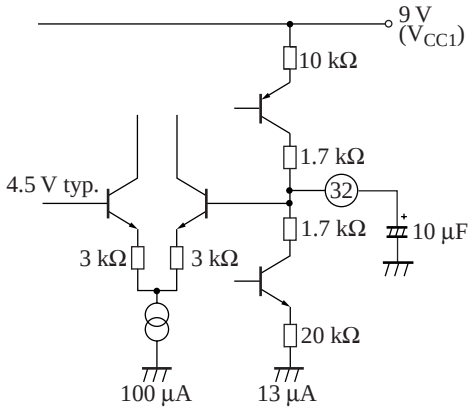
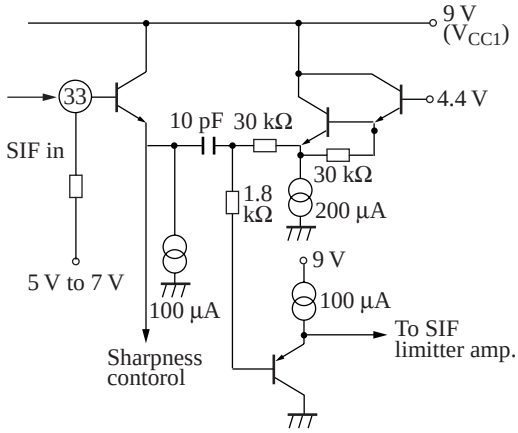
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	voltage
19	—	GND: R, G, B circuit. DAC, I^2C circuit.	—
20		ACL pin: If DC voltage of pin 20 is decreased from the outside, the contrast is turned down. Service SW. Note) Since pin 20 also serves as the service SW when used as ALC, design the set so as not to allow V_{20} < 0.9 V.	DC approx. 3 V
21		I^2C bus data input pin	AC (pulse)
22		I^2C clock input pin	AC (pulse)
23	—	V_{CC3}-1 (5 V typ.): For VIF and SIF circuitr.	DC 5 V

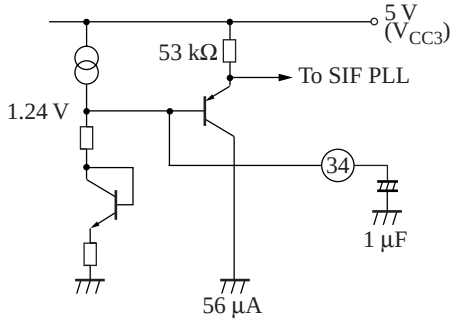
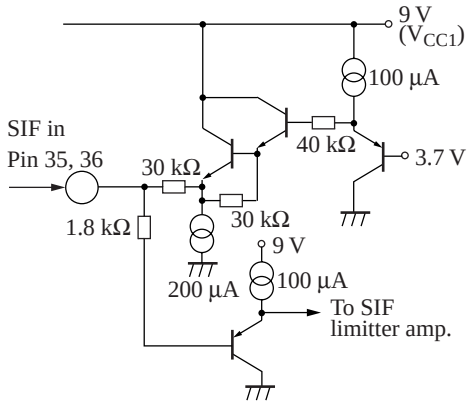
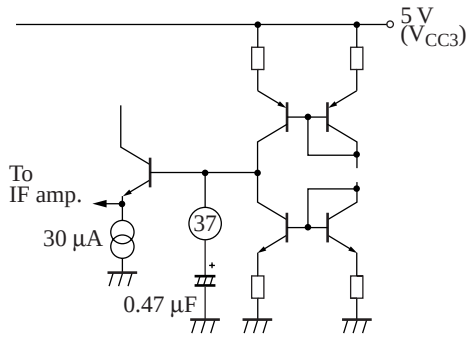
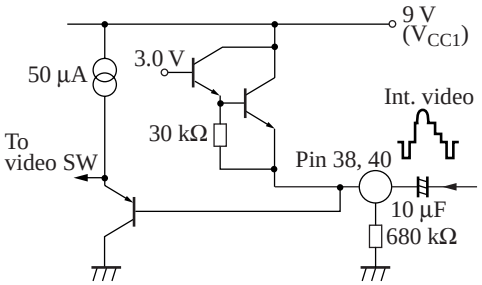
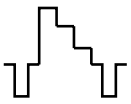
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	voltage
24 25		Pin24; VIF input pin-1 Pin25; VIF input pin-2: Balanced input by VIF amp. input.	AC $f = f_P$ DC level approx. 2.7 V
26	—	GND: For VIF and SIF circuit.	DC
27		RF AGC output pin: Open collector output and usable at any bias value (12 V max.).	DC
28		Audio output pin	AC 0 kHz to 20 kHz
29		De-emphasis pin: De-emphasis filter pin for sound detection signal. External C for PAL/NTSC is the same (internal impedance changes). PAL: 12 kΩ//60 kΩ × 1 200 pF = 48 µs NTSC: 60 kΩ × 1 200 pF = 72 µs	AC 0 kHz to 20 kHz

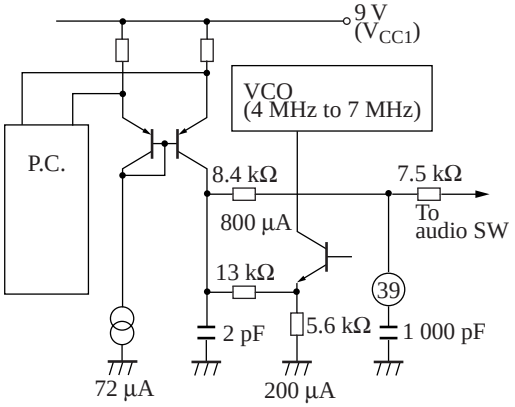
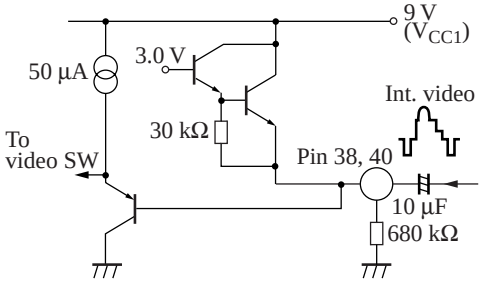
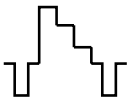
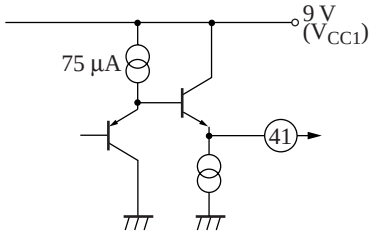
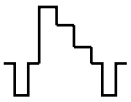
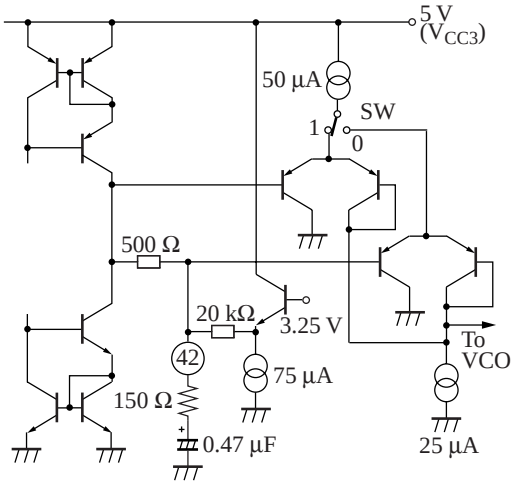
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	voltage
30		AFT output pin: Offset of center voltage is adjusted by using bus. When AFT defeat SW is turned on (09 = 00), V_{30} becomes a value determined by external resistor-divider. µ of AFT is variable by impedance of external resistor.	DC
31		External video input signal pin: External video signal input pin and DC cut input. Typical 1 V[p-p].	AC 1 V[p-p] (compost)  DC approx. 2.0 V
32		Decoupling pin: S-curve inside the IC is broad-band. However, DC feedback should be applied so that DC voltage of output signal becomes constant. DC level (4.5 V typ.). $f_S \rightarrow$ high: $V_{32} \rightarrow$ low	DC
33		SIF signal input pin: Used in common as DC input pin for sharpness control. DC bias is applied from outside (for sharpness control DC: 5 V to 7 V).	AC+DC AC $f = f_S$

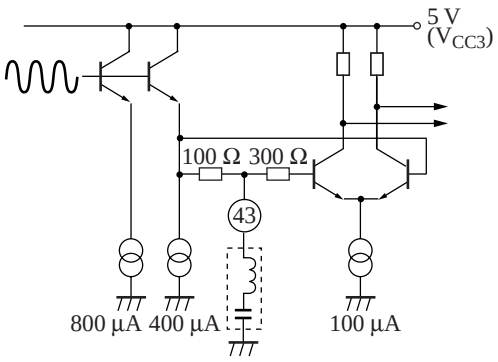
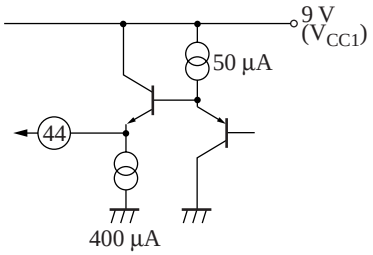
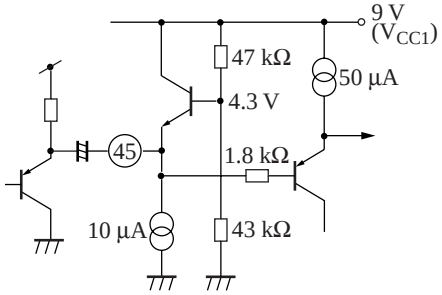
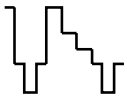
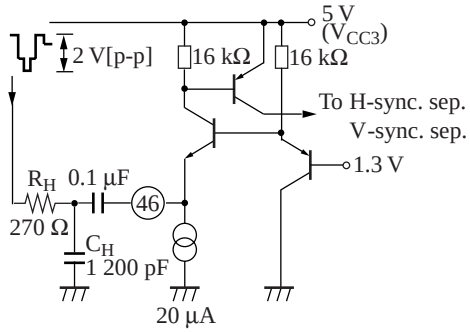
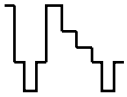
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	voltage
34		SIF internal power supply stabilization filter pin	DC 1.24 V
35		SIF signal input pin: Input pin for SIF2 and internally biased.	AC+DC AC $f = f_S$ DC 3.0 V
36		SIF signal input pin: Input pin for SIF1 and internally biased.	
37		IF AGC filter pin: IF AGC filter pin. The current obtained from peak AGC circuit is smoothed by an external capacitor. When C goes smaller, the respons charaeteristic becomes faster but the sag tends to appear easily.	DC approx. 2 V
38		Internal video input pin 1: Input pin for the signal detected by VIF circuit (internal video signal). DC cut input. Typical 1 V[p-p]	AC 1 V[p-p] (compost)  DC level approx. 1.6 V

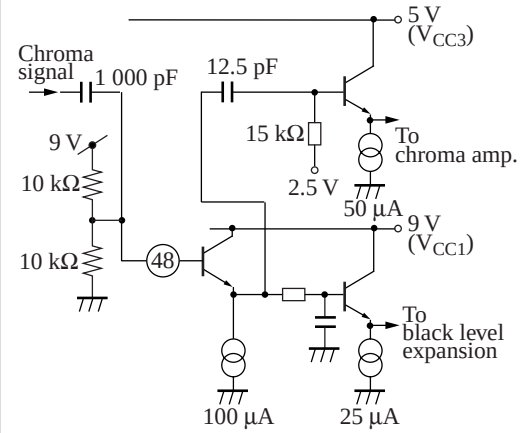
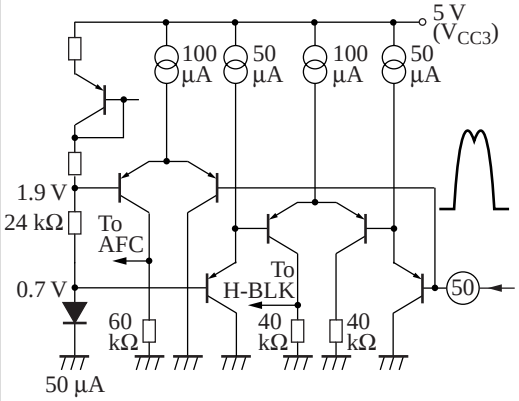
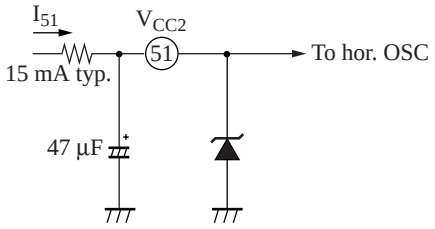
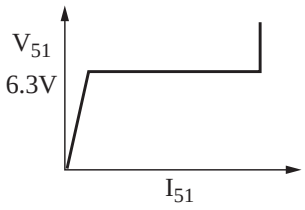
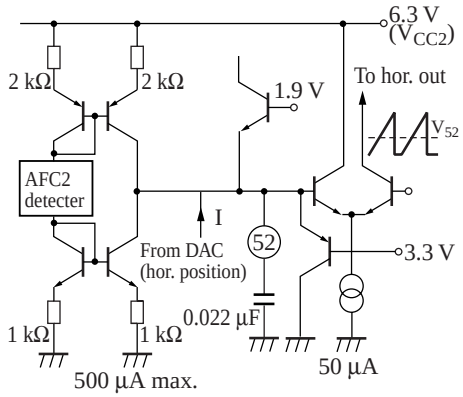
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	voltage
39		SIF APC filter pin: Filter pin for SIF APC circuit.	DC
40		Internal video input pin 2: Input pin for the signal detected by VIF circuit (internal video signal). DC cut input. Typical 1 V[p-p].	AC 1 V[p-p] (compost)  DC level approx. 1.6 V
41		VIF detection output pin: Adjust at 2 V[p-p] by I^2C bus (upper 4-bit of 0 A is used). Note) At AV mode, VIF detection signal output is not given.	AC 2 V[p-p] 
42		APC1 filter pin: Filter pin for APC1 circuit of VIF. Lock detection circuit of VCO is built in the IC inside and the time constant of APC filter is changed over. When locked SW: 0 When not locked SW: 1	DC approx. 2.5 V

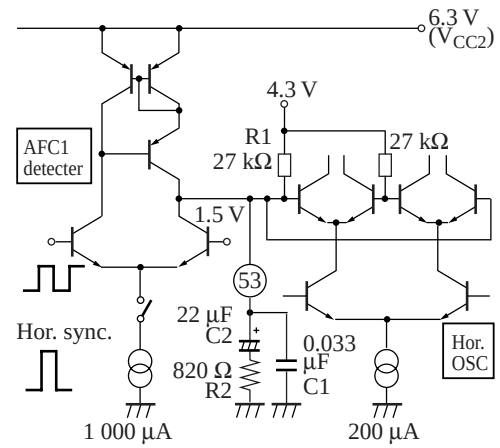
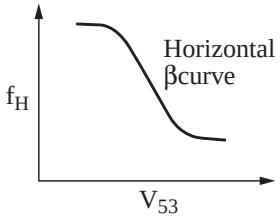
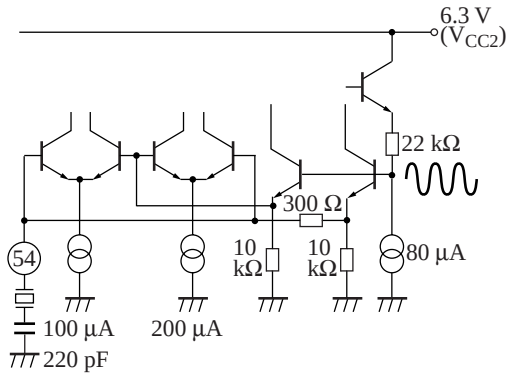
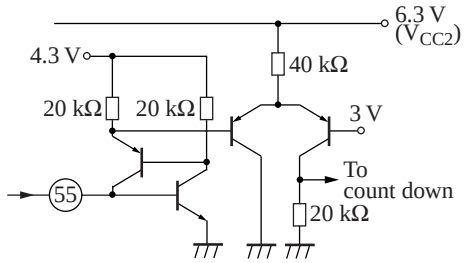
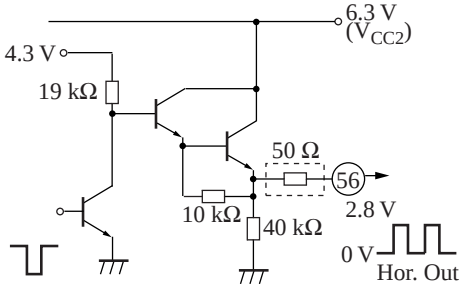
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	voltage
43		VIF oscillation pin: Depending on VIF frequency, change oscillation coil. The oscillation frequency is 1/2 of f_P .	AC $f = f_P /2$ approx. 0.7 V[p-p] DC level approx. 3.9 V
44		Video output pin: This pin outputs int.video 1, int. video 2 or ext. video signal selected by AV SW.	AC 2 V[p-p]  DC level approx. 4.5 V
45		Video input pin: Input pin for video signal (composite video also available). Typical input 0.6 V[p-p]. Sync. top is clamped at 3.5 V. The video signal should be inputted with low impedance.	AC 0.6 V[p-p] 
46		Vertical and horizontal sync. separation input pin: Sync. top is clamped at 1.3 V.	AC 2 V[p-p] 
47	—	V_{CC3-2} (5 V typ.) For chroma jungle circuit.	DC 5 V

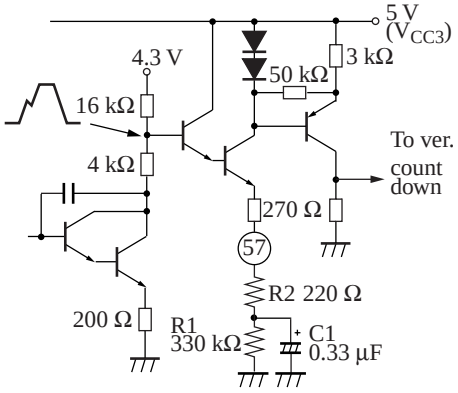
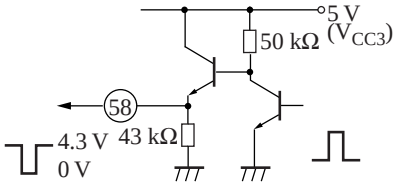
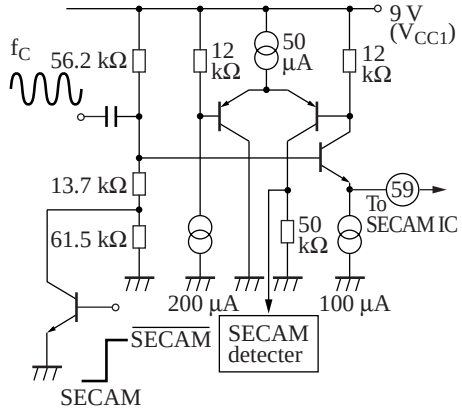
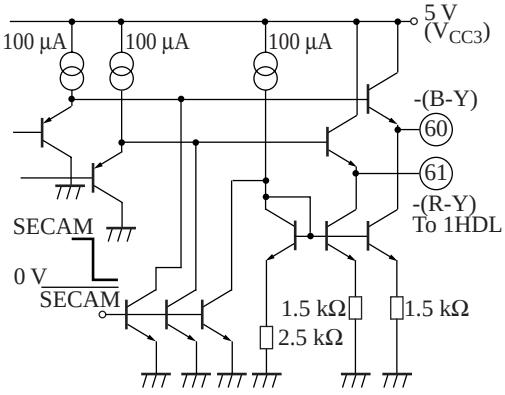
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	voltage
48		Chroma signal input pin Black extension start point adjusting pin: Pin 48 is chroma signal input pin, and the black extension start point is adjusted by DC voltage applied from the outside.	AC+DC burst 150 mV[p-p] typ. DC 4.5 V typ.
49		GND: For video chroma jungle circuit.	DC 0 V
50		FBP input pin: FBP input pin for horizontal blanking and AFC circuit. Threshold level H-BLK: 0.7 V AFC: 1.9 V It becomes all blanking when DC 1.3 V is applied from the outside.	AC FBP 
51		Horizontal stabilized power supply pin: Stabilized power supply for starting up the horizontal circuit that has a zener circuit inside. 	DC 6.3 V
52		Horizontal AFC2 filter pin: Comparing the phase of FBP and that of inside pulse of the IC, charge to and discharge from the capacitor connected to pin 52 are done. Performed by charging and discharging in DC current by the screen center position adjusting DAC. V_{52} changes depending on the time from H-out to FBP, and the slice level of internal sawtooth waveform changes.	DC 1.5 V to 3.5 V

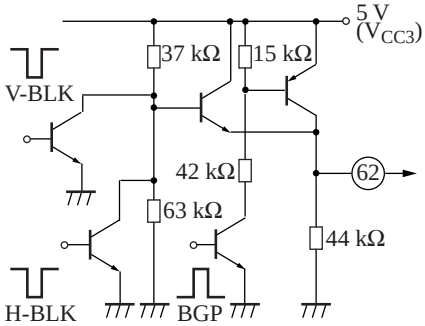
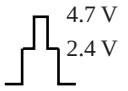
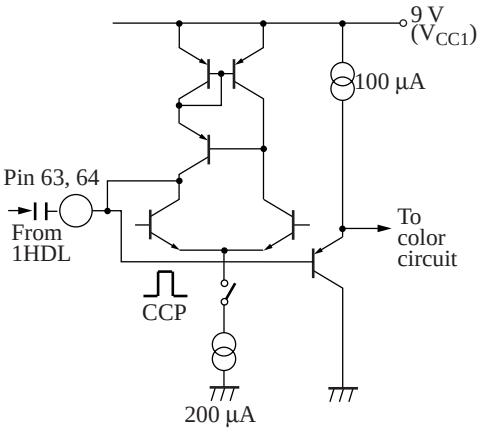
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	voltage
53		Horizontal AFC1 filter pin: Comparing the phase of horizontal sync. signal and that of inside pulse of the IC, charge to and discharge from the capacitor connected to pin 53 are done. R1, R2, C1, and C2 are lag-lead filter for AFC1. 	DC 4.3 V typ.
54		Horizontal oscillation pin: Oscillate at $32 \times f_H \approx 503$ kHz by means of ceramic oscillator. Horizontal and vertical pulse are generated by means of count down circuit in the IC.	AC $f = 32\ f_H$ (approx. 503 kHz)
55		Overvoltage protection input pin: Input pin for the protect circuit against X-ray due to overvoltage. Shut-down is started by internal logic circuit when H-out pulse is low. (Prevent the horizontal drive Tr destruction.)	DC normally 0 V
56		Horizontal pulse output pin: Duty cycle is approx. 36%.	AC pulse 

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	voltage
57		Vertical sync. signal clamp pin: Peak clamp pin for separating vertical sync. signal. Although the integral amount of vertical sync. signal itself has been determined by the internal time constant, the trigger application timing is determined by selecting external constant R1, C1. R1 must be used at higher than 200 kΩ. R2 is resistor for emitter current restriction.	AC $f = f_V$ 
58		Vertical pulse output pin: Negative polarity, pulse width of 10H.	AC pulse 
59		SECAM interface pin: Input and output pin for interfacing with SECAM IC. It becomes the SECAM mode when the current sink from pin 59 is 100 µA or more. At SECAM DC 4.4 V + AC 250 mV[p-p] At non-SECAM DC 1.1 V + AC 250 mV[p-p]: 4.43 MHz or 0 mV[p-p]: 3.58 MHz	AC+DC AC 250 mV[p-p] or 0 mV[p-p] DC 4.4 V or 1.1 V
60 61		Pin60; -(B-Y) output pin Pin61; -(R-Y) output pin: The output circuit turns off at SECAM and becomes a high impedance state. Outputs to 1HDL.	AC -(B-Y)  -(R-Y)  DC level approx. 2.1 V

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	voltage
62		Sand-castle pulse output pin: The sand-castle pulse is outputted to 1HDL and SECAM IC.	AC pulse 
63 64		Pin63; -(B-Y) input pin Pin64; -(R-Y) input pin: The color difference signal outputted from 1HDL is inputted. The pedestal level is clamped at 4 V by means of clamp circuit.	AC -(B-Y)  -(R-Y)  DC level 4 V

■ Usage Notes

1. The following terminals are not strongly resistant to surge latch-up. The precautions should be observed when using the IC.

   1) Serge

   The + side breakdown voltage of pin 22 and pin 23 is approx. 190 V if the surge source capacitance is 200 pF. The + side breakdown voltage of pin 45 is approx. 160 V if the surge source capacitance is 200 pF. Therefore, do not apply a surge stronger than that.

   2) Latch-up

   For pin 18, pin 21, pin 22, pin 51, pin 54, pin 55 and pin 56, the latch-up occurs by the + side surge of approx. 150 V (surge source capacitance 200 pF). Therefore, do not apply a surge stronger than each voltage indicated for each pin.

   Note) The stronger surge common to the above 1) and 2) means that the establishment of either one of the following two cases; the surge source capacitance is larger than the indicated value or the surge voltage is higher than the indicated value.

■ Usage Notes (continued)

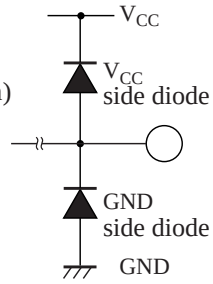
2. The protection diode of each Pin is as shown in the following table;

	Pin	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
With (●) or Without	V_{CC}	●	●	●	●	●	●	●	●	●	●	●	●	●	×	●	●	●	●	×	●	×	×	×	●	●	×
(×) Surge diode	GND	●	●	●	●	●	●	●	●	●	●	●	●	●	×	●	●	●	●	×	●	×	×	×	●	●	×
V_{CC} node being connected		1	1	1	3	3	3	3	3	1	1	1	1	1	/	1	1	1	2	/	1	/	/	/	3	3	/

	Pin	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52
With (●) or Without	V_{CC}	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	×	●	×	●	×	●
(×) Surge diode	GND	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	×	●	×	●	×	●
V_{CC} node being connected		1	1	1	1	1	1	1	3	1	1	3	1	1	1	1	3	3	3	1	1	/	3	/	3	/	2

	Pin	53	54	55	56	57	58	59	60	61	62	63	64
With (●) or Without	V_{CC}	●	●	●	●	●	●	●	●	●	●	●	●
(×) Surge diode	GND	●	●	●	●	●	●	●	●	●	●	●	●
V_{CC} node being connected		2	2	2	2	3	3	1	3	3	3	1	1

V_{CC} node
1 → V_{CC1} (9 V system)
2 → V_{CC2} (6.5 V system)
3 → V_{CC3} (5 V system)



■ Technical Information

• Explanation of each block

1. VIF
   1) Adapting the inter carrier PLL coherent detection method.
   2) The VCO of VIF is controlled by I²C bus (7-bit): Oscillation at 1/2 of the f_P frequency. (2 times multiplier circuit is inside.) Built-in double APC circuit of frequency and phase.
   3) AFT without coil: It is applicable to both VS and FS tuners by amplifying the error voltage of APC and making S-curve to obtain AFT output. The DC offset is controlled by I²C bus (9-bit). The AFT defeat is also possible.
   4) Since the VCO oscillates at 1/2 frequency, a high-frequency disturbance such as tweet is reduced.
   5) The video detection output is 2.0 V[p-p] typical: The level adjustment is carried out by I²C bus .
   6) The built-in lock detection circuit realizes a stable pulling by the changeover of time constant for APC.
   7) The delay point of RF AGC is adjusted by I²C bus (6-bit).

2. SIF
   1) The SIF detection uses PLL coherent detection method.
   2) 4 frequencies are changed over for use as the VCO oscillation frequency.
      At NTSC; 4.5 MHz
      At PAL; 5.0 MHz, 5.5 MHz, 6.5 MHz
   3) It is possible for the SIF detection output to deal with the difference in deviation of PAL/NTSC by changing over an amplifier of +6 dB.
   4) Built-in video/SIF SW.
      Video SW; 2 systems (with 6 dB amp.)
      SIFSW; 3 systems

■ Technical Information (continued)

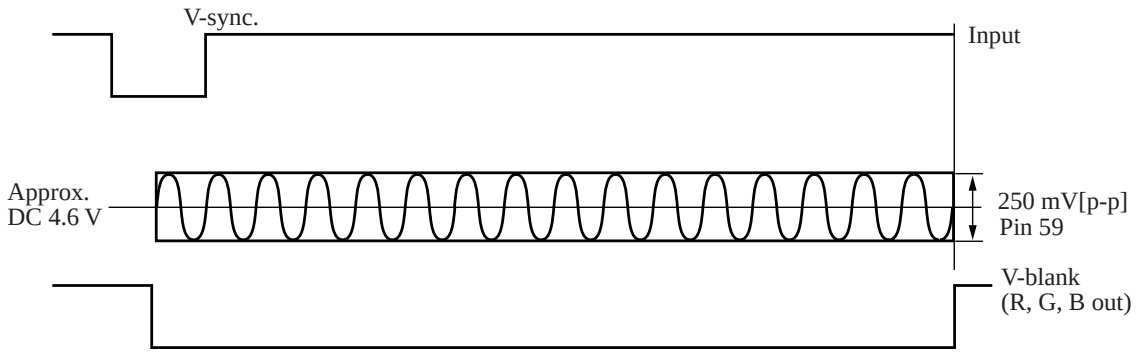
- Explanation of each block (continued)

3. Video
   1) The delay line aperture control (contours emphasis type) is used for sharpness control. The circuit as well as the black extension circuit realizes a high picture quality.
   2) Built-in pedestal clamp filter.
   3) Service SW: (Y contrast min., vertical output stop).

4. Chroma
   1) The circuit realizes an adjustment free condition by using base band 1HDL (externally attached).
   2) Incorporation of ACC filter reduces the number of external components.
   3) It is possible to support the other systems by the mode changeover I^2C bus (1) PAL/NTSC, (2) 4.43 MHz/3.58 MHz, (3) Forced PN/ForcedSECAM.
   4) Equipped with the killer output terminal for system discrimination by microcomputer. (When killer is on → 0 V, killer is off → 5 V)
   5) The color difference output terminal becomes a high impedance state at SECAM.
   6) Since the circuit is provided with the color difference input terminal, the features of ICs such as the AN5244 (IC for color signal compensation) can be connected.
   7) PAL/NTSC, SECAM interface (pin 59)

Mode	DAC(3.58 MHz/4.43 MHz)	Pin59 output	f_C	AC level	
PAL/NTSC	3.58 MHz	Approx. 1.3 V	3.58 MHz	×	CW output
	4.43 MHz	Approx. 1.3 V	4.43 MHz	250 mV[p-p]	
SECAM	3.58 MHz	Approx. 4.6 V	4.43 MHz	250 mV[p-p]	Output for V-blank
	4.43 MHz	Approx. 4.6 V	4.43 MHz	250mV[p-p]	period only *

Note) *: AC component of 4.43 MHz is outputted in the vertical sweep period only.



5. RGB
   1) It supports not only the OSD but also the teletext signal in an analog input system. (The output level is interlocked with the contrast of TV signal side.)
   2) The white balance (drive, cut-off) adjustment is performed by I^2C bus.

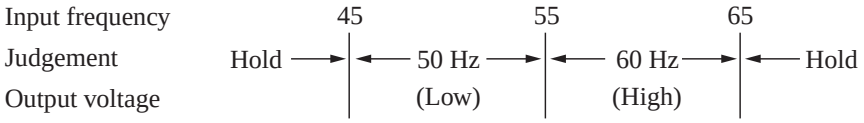
6. Jungle
   1) The horizontal circuit uses the count down method by 32 f_H ceramic oscillator. The AFC circuit uses double method.
   2) By the adaption of trigger method count down circuit, the vertical circuit can obtain a stable vertical synchronization without adjustment at all times. The output is pulse signal, so that there is no degradation of interface due to the influence of pattern layout.

■ Technical Information (continued)

• Explanation of each block (continued)

6. Jungle (continued)

3) Built-in frequency discrimination circuit: The circuit outputs the judgment results of 50 Hz/60 Hz in accordance with the frequency of the vertical synchronizing signal.
(60 Hz → high)



4) The output holds the previous state when the input frequency is 45 Hz or less and 65 Hz or more, and the output changes for the first time when judged as 50 Hz or 60 Hz for 3 consecutive vertical periods.

5) The horizontal detection circuit and X-ray protection circuit (shut-down method) are built in.

6) The screen center position is adjustable by the I^2C bus. (±1.6 µs)

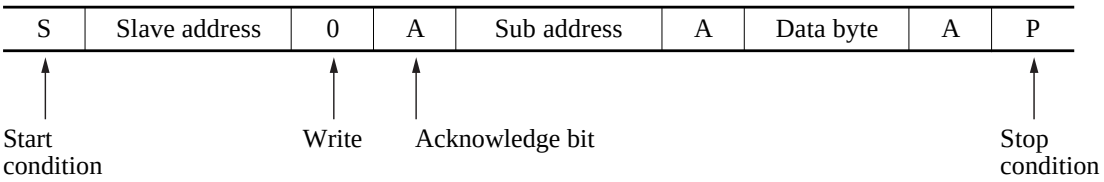
7) For the blue-back in a weak electric field, the stable screen image is held by the vertical trigger off mode (I^2C bus).

7. I^2C bus

1) Incorporating 14 DAC controls and 12 SWs for eliminating the need for the adjustment of set mechanism.

2) Provided with automatic increment function.
- Sub address 0 *: Automatic increment mode.
(When data are sent in regular succession, sub address changes successively and data are inputted.)
- Sub address 8 *:
(When data are sent in regular succession, data are inputted with the same sub address.)

3) I^2C Bus Protocol
- Slave address: 10 001 010 (8AH)
- Slave address format



4) Sub address byte and data byte format
The description in ( ) shows the initial state.

Sub address	Data byte							
	D7	D6	D5	D4	D3	D2	D1	D0
00 (21H)	P/N (0 → P)	PN/S (0 → PN)	←		Color			→
01 (21H)	Ver. auto (0 → auto)	Ver. TRG (0 → normal)	←		Tint			→
02 (41H)	Ver. OSC (0 → 50)	←			Brightness			→
03 (21H)	SIF SW	Video SW	←		Contrast			→
04 (81H)	←				Cut off R			→
05 (81H)	←				Cut off G			→
06 (81H)	←				Cut off B			→

■ Technical Information (continued)

- Explanation of each block (continued)

7. I^2C bus (continued)

4) Sub address byte and data byte format (continued)

The description in ( ) shows the initial state.

Sub address	Data byte							
	D7	D6	D5	D4	D3	D2	D1	D0
07 (41H)	SIF VCO SW1	←	←	←	Drive R	→	→	→
08 (41H)	Chroma VCO (0 → 4.43)	←	←	←	Drive B	→	→	→
09 (01H)	←	←	←	←	AFT offset	→	→	→
0A (21H)	50 Hz/60 Hz killer out SW	SECAM det. SW	←	←	RF AGC delay	→	→	→
0B (45H)	SIF/ext. SW	←	Video adjust	→	SIF VCO SW2	←	H center	→
0C (C1H)	AFT offset SW	←	←	←	VIF VCO	→	→	→

5) Contents of I^2C bus control

(1) The control information is in the direction that the output increases when the datum increases.
(Example: Contrast 00 → contrast min. , 3F → max. , brightness 00 → pedestal level low, 7F → high)

(2) Supplement of other control

a. 00: Color
When data are 00, the color becomes off since the chroma output is decreased completely .

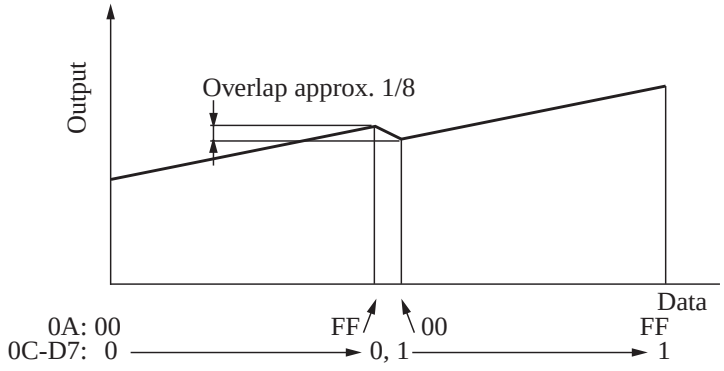
b. 01: Tint
Data 00 → Skin color tends to become reddish, 3F → skin color tends to become greenish.

c. 04, 05, 06: Cut off R, G, B
8-bit DAC

d. 07, 08: Driver R, B
7-bit DAC

e. 09: AFT offset adjustment
The DC offset of S-curve of AFT output is corrected.
Data 01 → S-curve falls (DC voltage of center frequency drops).
Data FF → S-curve rises.
It becomes AFT defeat mode when data 00, the voltage of AFT out (pin 30) becomes the value in accordance with the external resistor.
AFT changes over 8-bit DAC into 2 stages for variable range and improvement of precision for per 1-bit.

Example: In the case of AFT



■ Technical Information (continued)

• Explanation of each block (continued)

7. I^2C bus (continued)

5) Contents of I^2C bus control (continued)

(2) Supplement of other control (continued)

f. 0A: RF AGC delay point adjustment
The same operation as when bias is applied from outside conventionally.
Data 00 → DC-applied bias drops → delay point rises
Data 3F → DC-applied bias drops → delay point down

g. 0B: Video adjustment
Data 0* → detection output min. 7* → max. to be used for correcting the dispersion of detection output inside the IC.

h. 0B: Hor. screen image position
Data *0 → screen image goes to the left 7 * → screen image shifts to the right.

i. 0C: VCO control
Fine control for the oscillation frequency of VCO (1/2 frequency of f_p) of VIF.

8. Supplementary explanation of SW operation

Data-bit	SW contents	Concrete contents
00-D7	PAL/NTSC mode SW (0 → PAL) (1 → NTSC)	1) BGP width changeover (PAL: Wide) 2) CW changeover to killer (PAL: 90 deg./270 deg.) 3) Tint operation changeover (PAL: Tint off) 4) Ident operation changeover (PAL: With operation)
00-D6	PAL, NTSC/SECAM mode SW (1 → forced SECAM) (0 → normal discrimination mode)	1) Demodulation output mode changeover. The color difference output terminal becomes high impedance at forced SECAM.
01-D7	Ver. auto SW (0 → auto changeover) (1 → manual changeover)	1) Vertical frequency discrimination circuit changeover. Auto changeover: Automatic discrimination mode by internal counter. Manual changeover: Forcibly changeover 50 Hz/60 Hz by 02-D7 data.
01-D6	Ver. TRG stop SW (0 → normal) (1→ trigger off)	1) Vertical trigger input inhibit SW. 1 → trigger input-off is the mode to protect from the vertical dancing caused by noise at blue-back .
02-D7	Ver. OSC SW (0 → 50 Hz) (1→ 60 Hz)	1) Vertical frequency changeover SW. Valid only when 01-D7 is 1.
03-D7 0B-D7	SIF, external AV input changeover switch	

03-D7	0B-D7	Output signal	
0	0	SIF1 (int.)	Power on time
0	1	SIF2 (int.)	
1	0	SIF3 (int.)	
1	1	Ext. (video)	Int. is set at SIF1

■ Technical Information (continued)

- Explanation of each block (continued)

8. Supplementary explanation of SW operation (continued)

<table>
<tr><th>Data-bit</th><th>SW contents</th><th>Concrete contents</th></tr>
<tr><td>03-D6</td><td colspan="2">Video input changeover switch
<table>
<tr><th>03-D6</th><th>Input signal</th><th></th></tr>
<tr><td>0</td><td>Video1</td><td>Power on time</td></tr>
<tr><td>1</td><td>Video2</td><td></td></tr>
</table></td></tr>
<tr><td>08-D7</td><td>Chroma VCO SW
(0 → 4.43 MHz)
(1 → 3.58 MHz)</td><td>1) Chroma oscillation circuit changeover.</td></tr>
<tr><td>0A-D7
0A-D6</td><td colspan="2">50 Hz/60 Hz, killer, SECAM det. out switch
<table>
<tr><th>0A-D6</th><th>0A-D7</th><th>Output signal</th><th></th></tr>
<tr><td>0</td><td>0</td><td>50 Hz/60 Hz out</td><td>Power on time</td></tr>
<tr><td>0</td><td>1</td><td>Killer out</td><td></td></tr>
<tr><td>1</td><td>0</td><td>SECAM det. out</td><td></td></tr>
</table>
<table>
<tr><th>Mode / Output</th><th>50 Hz/60 Hz out</th><th>Killer out</th><th>SECAM det. out</th></tr>
<tr><td>H (5 V)</td><td>60 Hz</td><td>Off (color)</td><td>SECAM</td></tr>
<tr><td>L (0 V)</td><td>50 Hz</td><td>On (B/W)</td><td>No SECAM</td></tr>
</table></td></tr>
<tr><td>07-D7
0B-D3</td><td colspan="2">SIF VCO free-running frequency, de-emphasis
Detection output gain changeover switch
<table>
<tr><th>07-D7</th><th>0B-D3</th><th>De-emphasis/gain</th><th>Oscillation frequency of VCO</th><th>SIF input terminal</th></tr>
<tr><td>1</td><td>0</td><td>NTSC</td><td>4.5 MHz (power on time)</td><td>—</td></tr>
<tr><td>1</td><td>1</td><td>PAL</td><td>5.5 MHz</td><td>—</td></tr>
<tr><td>0</td><td>0</td><td>PAL</td><td>6.0 MHz</td><td>—</td></tr>
<tr><td>0</td><td>1</td><td>PAL</td><td>6.5 MHz</td><td>—</td></tr>
</table></td></tr>
<tr><td>0C-D7</td><td>AFT offset SW
(0 → without offset)
(1 → with offset)</td><td>1) For AFT 2-stage changeover.
(Power on preset: AFT offset SW → 1)
2) AFT defeat.
Defeat comes ettective only when 0C-D7 = 0,
DAC(09) = 00.</td></tr>
</table>

■ Application Circuit Example