SkyPHY
DVB S2 RECEIVER

ECC3100EP -
ECC3100 SkyPHY Receiver
Evaluation Board Data Sheet

Version 1.0

Revision History

Revision Number	Date	Company	Comments
1.0	5/22/06	Efficient Channel Coding, Inc.	Initial Release

Table of Contents

1 Overview

The ECC3100 evaluation board design provides a platform for evaluation and demonstration of the ECC3100 SkyPHY Receiver ASIC in a DVB-S2 forward link receiver sub-system.

The evaluation board provides three analog signal inputs:

- 75Ω RF input to Analog Devices AD8347 Direct Conversion Quadrature Demodulator
- 75Ω RF input to Zarlink ZL10038 Advanced Modulation Satellite Tuner
- Baseband I & Q analog inputs (direct input to ADCs)

The evaluation board provides four digital data outputs:

- MPEG-2 TS Synchronous Parallel Interface (SPI)
- ASI serial output based on a Cypress Hotlink II transceiver
- Serial BERT clock and data output
- NEC processor local bus

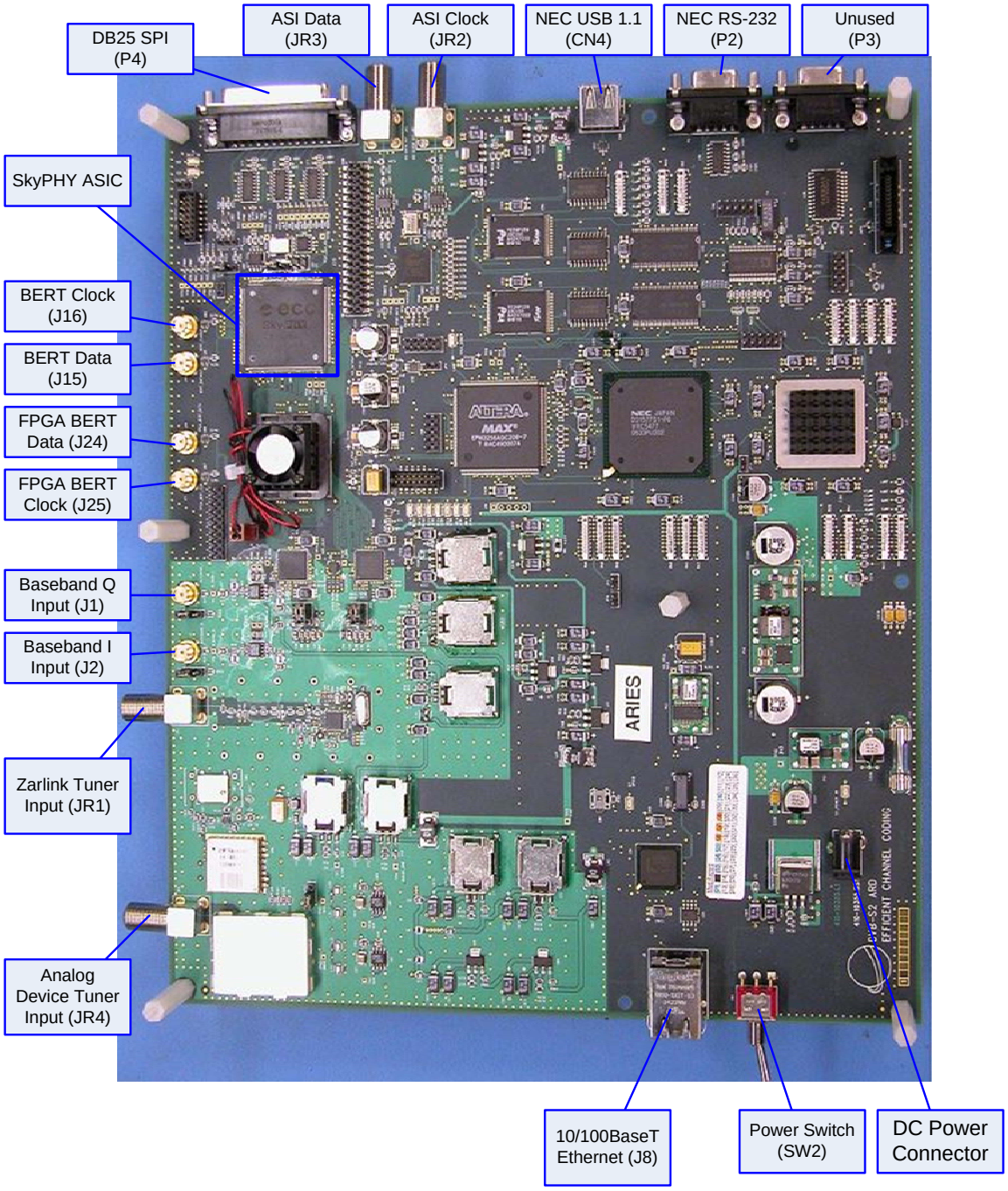
This platform processor is the NEC VR5500 with VRC5477 companion chip. The processor is supported with 32MB of SDRAM, 32MB of FLASH memory and interfaces to Ethernet, USB & RS232 Serial ports.

The processor is running an ASIC device driver that provides for the initial configuration of the ASIC, periodic ASIC maintenance, and tuning of the Analog Devices demodulator.

The processor is also running an embedded Java applet that provides the user with a GUI for ASIC configuration and status monitoring. The GUI can be accessed by connecting the evaluation board to your local area network and pointing a web browser to the IP address of the board.

The evaluation platform contains a single FPGA which is currently used to translate the 1.8V signal voltage level out of the ADCs to 3.3V for the ASIC. Future releases of the FPGA image will allow for on-board testing of the ASIC's demodulator bypass mode.

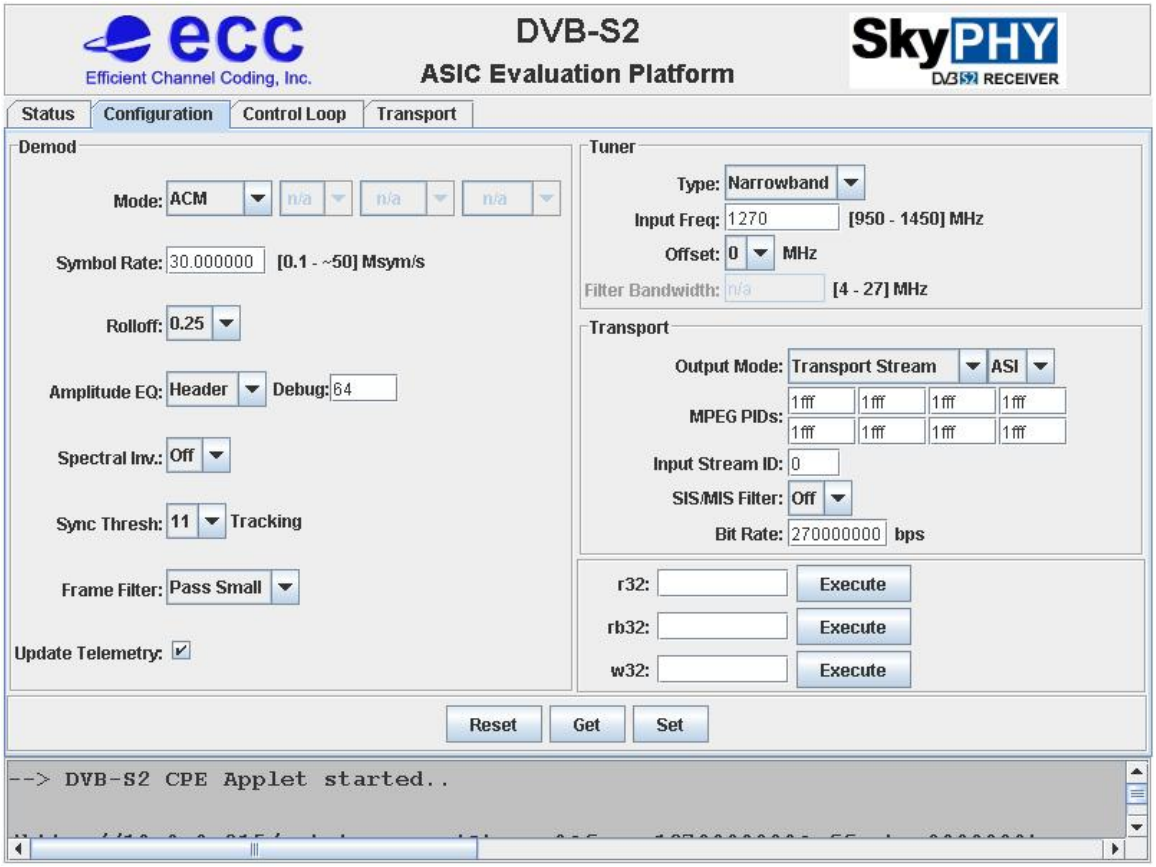
The picture on the following page shows the evaluation board and its various inputs and outputs.



The evaluation board is designed for use in a lab environment. Care should be taken to ensure antistatic precautions are taken when handling the board. Electrostatic shock, excessive heat and moisture may cause damage to the board and attached components.

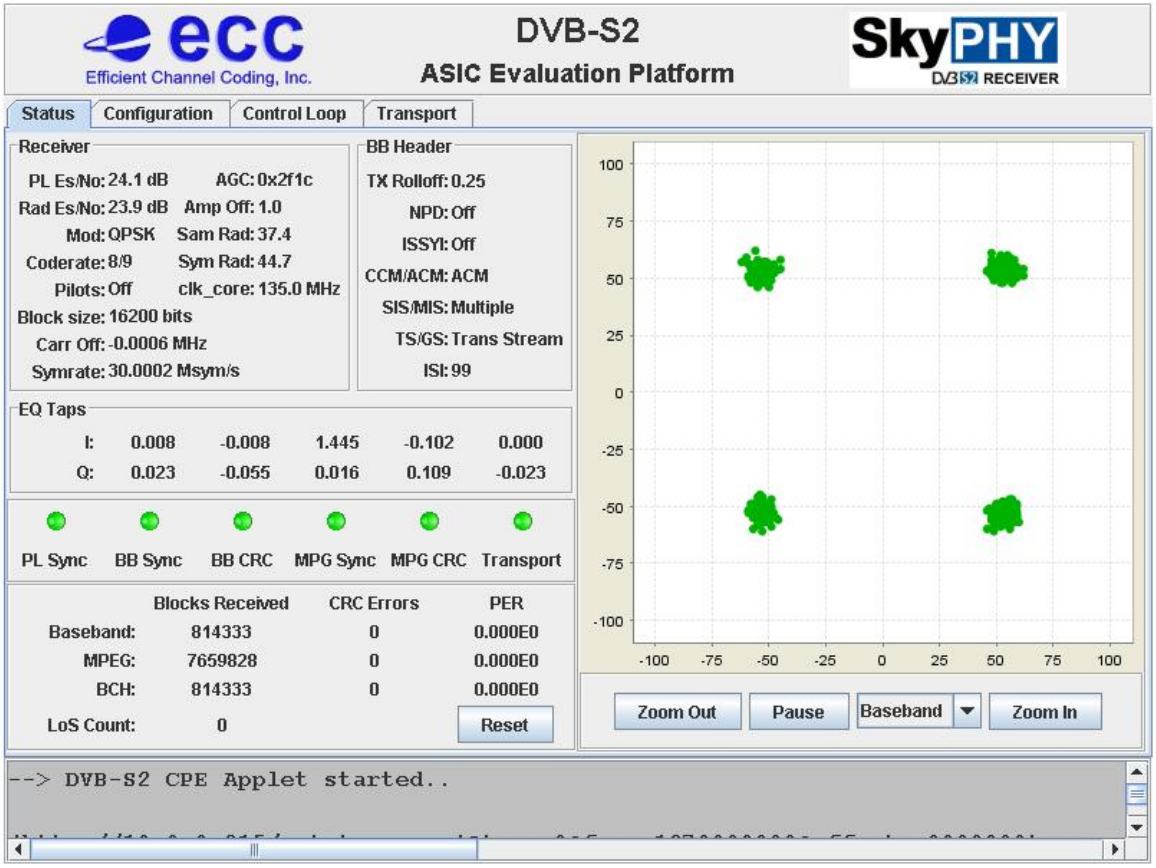
2 Configuration Tab

The figure below shows the GUI Configuration tab. This tab displays panes for configuration of the evaluation platform.



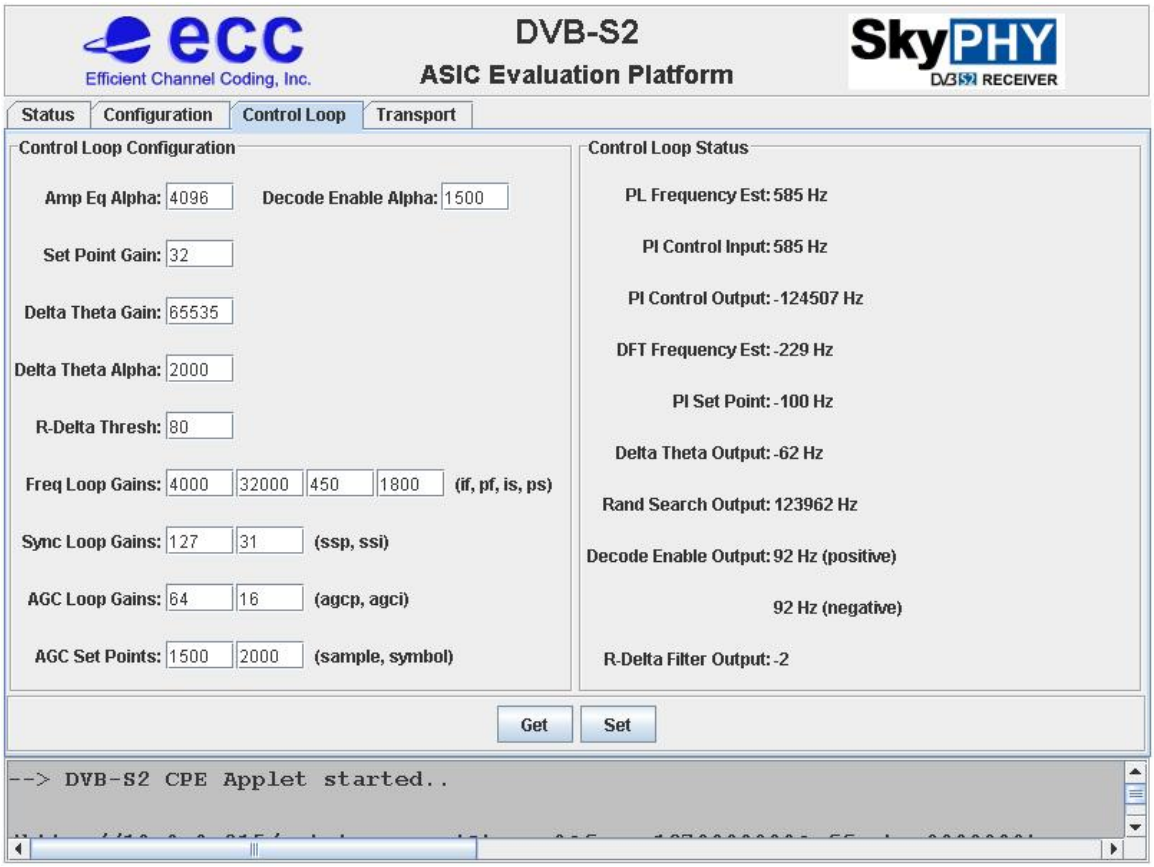
3 Status Tab

The Status Tab displays demodulator and transport telemetry information, a constellation plot, and status of blocks being received.



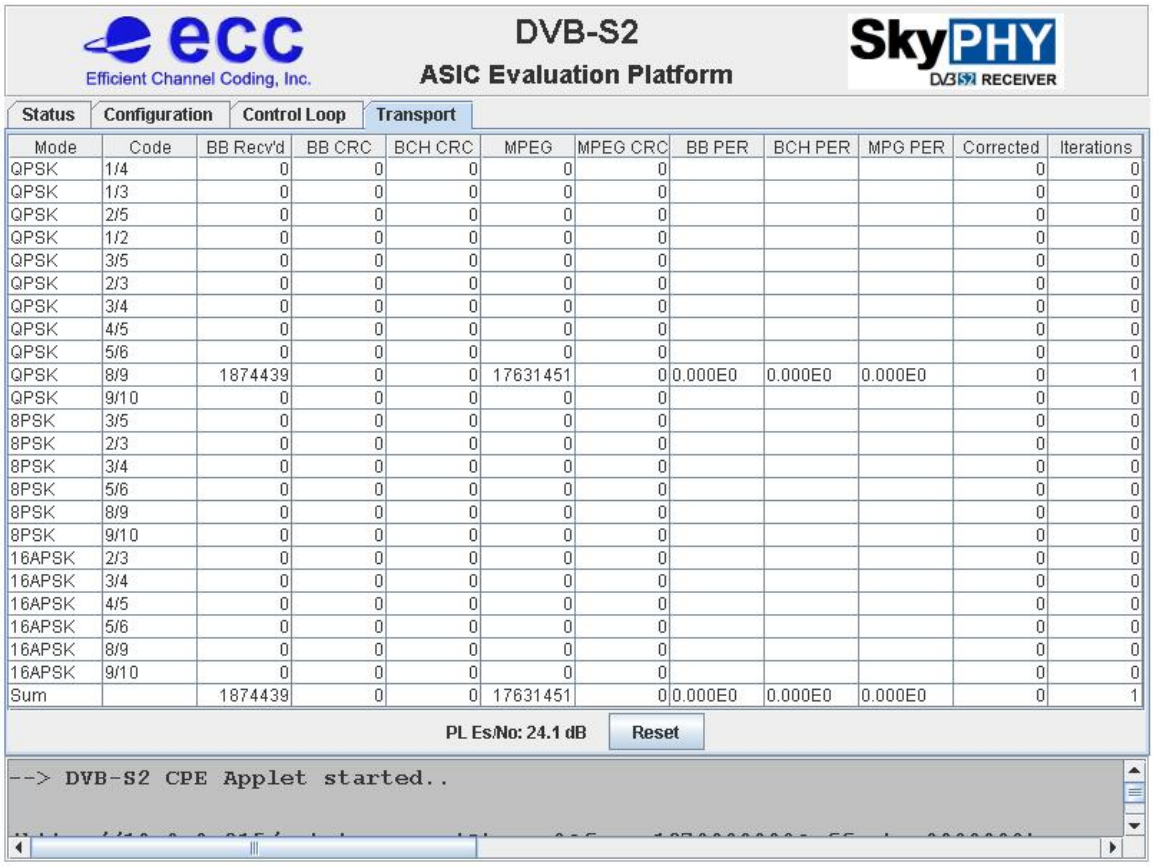
4 Control Loop Tab

The control loop tab displays the current status of several demodulator control loops and allows the user to modify some of the demodulator control loop parameters.



5 Transport Tab

The transport tab displays the packet processing statistics for all modulation and code pairs. The table does not distinguish between normal and small frames or between pilot on and pilot off modes. The last row of the table shows the sum of the statistics in each column.



Mode	Code	BB Recv'd	BB CRC	BCH CRC	MPEG	MPEG CRC	BB PER	BCH PER	MPG PER	Corrected	Iterations
QPSK	1/4	0	0	0	0	0				0	0
QPSK	1/3	0	0	0	0	0				0	0
QPSK	2/5	0	0	0	0	0				0	0
QPSK	1/2	0	0	0	0	0				0	0
QPSK	3/5	0	0	0	0	0				0	0
QPSK	2/3	0	0	0	0	0				0	0
QPSK	3/4	0	0	0	0	0				0	0
QPSK	4/5	0	0	0	0	0				0	0
QPSK	5/6	0	0	0	0	0				0	0
QPSK	8/9	1874439	0	0	17631451	0	0.000E0	0.000E0	0.000E0	0	1
QPSK	9/10	0	0	0	0	0				0	0
8PSK	3/5	0	0	0	0	0				0	0
8PSK	2/3	0	0	0	0	0				0	0
8PSK	3/4	0	0	0	0	0				0	0
8PSK	5/6	0	0	0	0	0				0	0
8PSK	8/9	0	0	0	0	0				0	0
8PSK	9/10	0	0	0	0	0				0	0
16APSK	2/3	0	0	0	0	0				0	0
16APSK	3/4	0	0	0	0	0				0	0
16APSK	4/5	0	0	0	0	0				0	0
16APSK	5/6	0	0	0	0	0				0	0
16APSK	8/9	0	0	0	0	0				0	0
16APSK	9/10	0	0	0	0	0				0	0
Sum		1874439	0	0	17631451	0	0.000E0	0.000E0	0.000E0	0	1