PROGRAMMABLE UNIVERSAL COUNTER

Description

ZENIC INC. ZEN2002AP is a 24 bit programmable universal counter LSI .

THE ZEN2002AP counts phase-shifted signals and up/down pulse signals, generated from rotary encoders or linear scales.

Since the counter response speed is as high as 20MHz(MAX),the ZEN2002AP is used in a variety of high speed services including digital servo control and precision measurement.

THE ZEN2002AP is provided with a function which monitors the input signals and detects any abnormal input accompanied with noise or other disturbances, so that the reliability of counted values are secured.

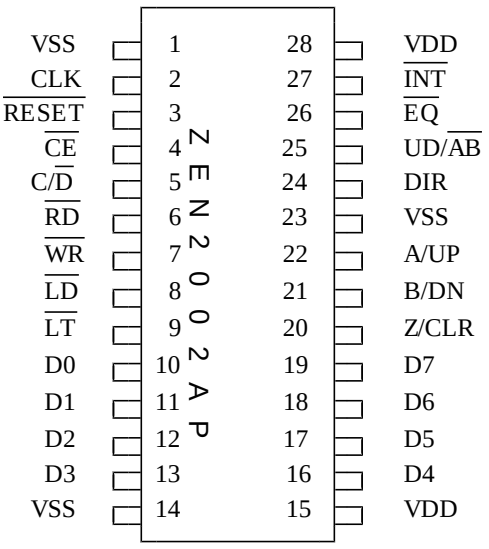
1, Features

- 24 bit binary up/down counter.
- Counter response speed:
  20MHz.(MAX.) (CLK f_0 = 20MHz at 50% duty)
- Input frequency of count pulse.
- Phase-shifted signal input:
  A/B phase input DC ~ 5MHz.
  (less than f_0 ×1/4)
- Up/down pulse signal input:
  Up/down input DC ~ 10MHz
  (less than f_0 ×1/2)
- CLK frequency DC ~ 20MHz.
  (MAX.: duty ratio 50%)
- Direction recognition for up/down counting.
- Abnormal input detection circuit.
- Preload register for the up/down counter.
- Latch register for the up/down counter.
- Reference value - count value coincidence detection function.
- Momentary output : TTL
- Interrupt output(latched) : open collector
- On-chip status register.
- Counter operation mode.
  Edge evaluation selection : single/double/quad
  (only for phase-shifted signal input)
  Count direction selection.
  Counter clear control:synchronous/
  asynchronous clear.
  Fixed/variable edge clear.
- 8 bit data bus.
- Low power CMOS technology.
- TTL compatible.
- Single 5V power supply.
- 28 pin DIP.

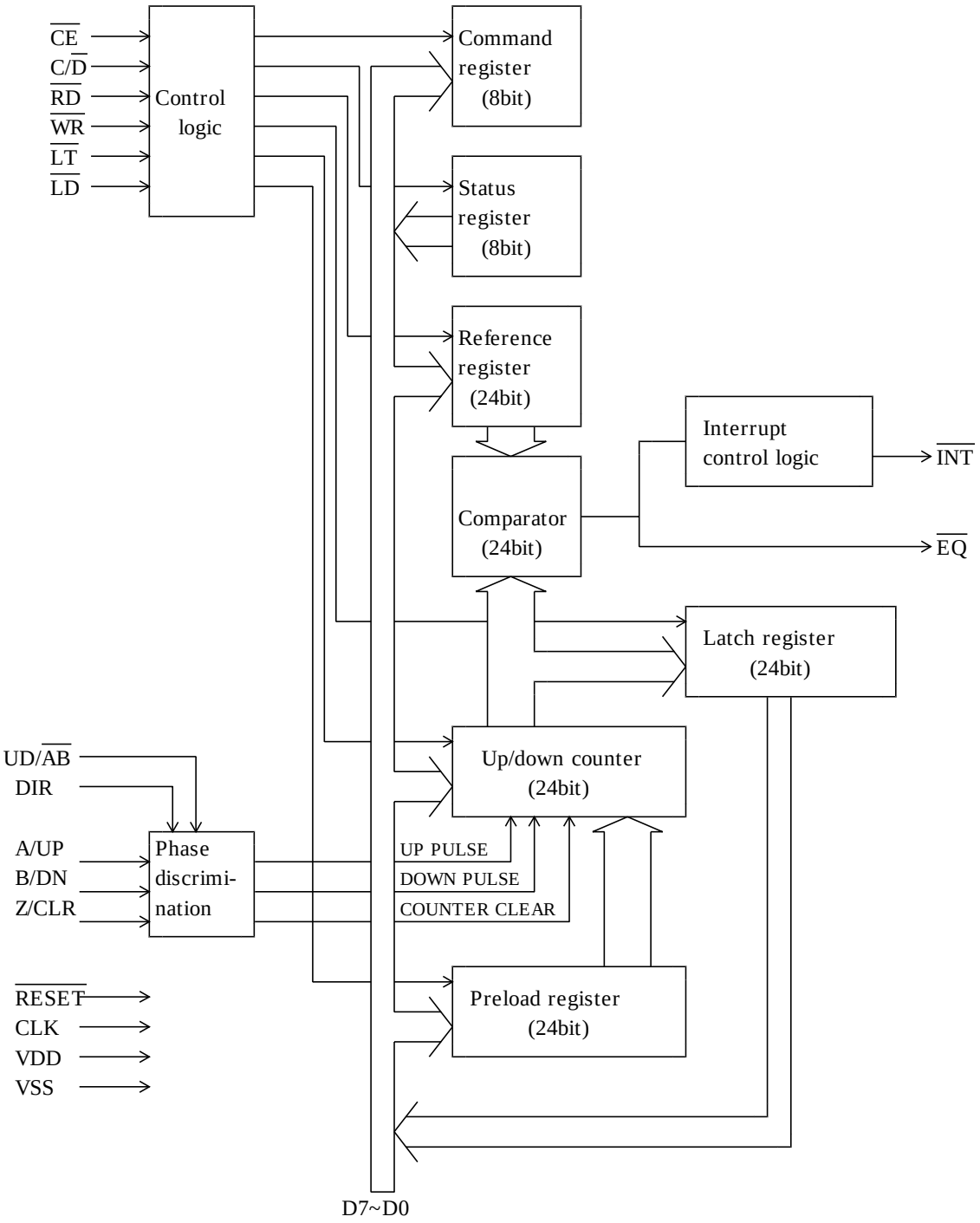
2, Typical Applications

- NC machine tools
- Precision positioners
- Robot arm controllers
- Speed controllers for rotating machines
- Electronic gauges
- Frequency counters

Pin configuration
(Top view)



3, Block Diagram



4, Block function

1) Up/down counter
It is presettable up/down binary counter of 24 bit length.
The count value can be read out from the latch register via the data bus without influencing to the count operation.
The counter value is initialized by loading the preload register(24bits) or via the data bus every 8 bits.

2) Reference register
It is a writing register of 24 bit length.
The written data is compared by the comparator with the count value of the up/down counter.

3) Comparator
It is a digital comparator of 24 bit length.
The data of the reference register is always compared with the counter value of the up/down counter and the result is output to EQ(26Pin), the status register, and the interruption control logic.

4) Preload register
It is a data register of 24 bit length.
Its data is loaded into the up/down counter by the external signal LD(8Pin) or the command(load instruction).

5) Latch register
It is a data register only for reading 24 bit length.
It latch the count value of the up/down counter by the external signal LT(9Pin) or the command(latch instruction).

6) Command register
It is a register for the command writing. (8 bits)
The controls of loading instruction, latch instruction, count clear control, and register (byte) selection and count mode changes, etc. are done by using this register.

7) Status register
It is a register for the status reading. (8 bits)
It monitors the state of abnormal input detection, the state of input signal(A,B,Z), the state of the latch register, count direction, the state of coincidence detection(count value = preset value), and the state of interruption output (INT).

8) Phase distcrimination logic
The count pulse for the up/down counter is generated from the input signal of A/UP(22Pin) and B/DN(21Pin).

9) Control logic
The read/write timing control, the decoding about the command data, and the status flag control.

5, Pin Description

Pin No.	Signal	I/O	Function
2	CLK	I	System clock
3	$\overline{\text{RESET}}$	I	System reset Up/down counter, phase discrimination logic, command register and the status register are initialized.
4	$\overline{\text{CE}}$	I	Chip enable
5	C/$\overline{\text{D}}$	I	Command/data select "High":command/status "Low":data
6	$\overline{\text{RD}}$	I	Read strobing
7	$\overline{\text{WR}}$	I	Write strobing
8	$\overline{\text{LD}}$	I	Data loading The data of the preload register is loaded to the up/down counter
9	$\overline{\text{LT}}$	I	Count data latch The count value of the up/down counter is latched to the latch register.
10 11 12 13 16 17 18 19	D0 D1 D2 D3 D4 D5 D6 D7	I/O	Data bus Bidirectional data bus (8 bits). It is used to transmit and receive the command, status and data.
20	Z/CLR	I	Counter clear
21	B/DN	I	Count pulse input B
22	A/UP	I	Count pulse input A
24	DIR	I	Count direction selection
25	UD/$\overline{\text{AB}}$	I	Input signal selection Selection up/down or phase-shifted pulse
26	$\overline{\text{EQ}}$	O	Coincidence detection output Coincidence detection output of count value and preset value of reference register.
27	$\overline{\text{INT}}$	O	Interruption output When the coincidence of the count value and the preset value is detected, it outputs. It maintains to reset or the reset command execution.
1	VSS		Power supply (5v)
15	VDD		Ground (0v)

6, Basic operation

The read/write operation is selected according to CE, C/D, RD, and WR.

$\overline{CE}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	Operation
H	-	-	-	Disable
L	L	L	H	The data reading
L	L	H	L	The data writing
L	H	L	H	Status reading
L	H	H	L	Command writing

1) Selection of count pulse input

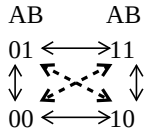
UD/$\overline{AB}$	Input pulse signal	A/UP	B/DN
H	Up/down pulse	Up pulse	Down pulse
L	Phase-shifted pulse	Phase-A pulse	Phase-B pulse

2) Access pointer

The internal register is selected by setting the access pointer of the command register. Once setting the pointer, it is incremented automatically after reading or writing 1 byte data. (automatical increment function)

3) Abnormal input detection

The function is to check whether it is normal state transition () when the phase-shifted pulse is input.
When the abnormal state transition happens , D7 of the status register becomes "H".



⟷ : noamal transition
<---> : abnormal transition

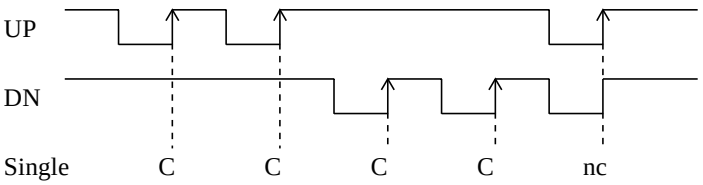
Example of causing abnormal

a. When it is not possible to sample signal accurately
because the pulse input frequency exceeded 1/4 of the system clock frequency.

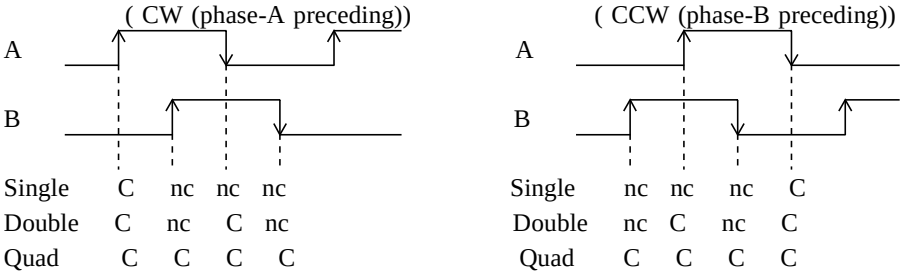
b. When you pick up noise.

4) Selection of count edge (C = count , nc = no count)

Up/down pulse input



Phase-shifted pulse input



7, Command register

```
D7  D6  D5  D4  D3  D2  D1  D0
 |   |  (command ID)
 0   0 =  Load/latch and register selection
 0   1 =  Phase-Z input control
 1   0 =  Edge evaluation and clearness timing control
 1   1 =  Interruption output control
```

(1) Latch and loading/register selection

```
D7  D6  D5  D4  D3  D2  D1  D0
 0   0   LD  LT RS1 RS0 BS1 BS0
             |   |   |   |   0   0  -- Lower 8 bits.  (D)     ( the pointer is automatically incremented )
             |   |   |   |   0   1  -- Middle 8 bits.                    Π
             |   |   |   |   1   0  -- Upper 8 bits.                     Π
             |   |   0   0  ---------- Up/down counter  (D)    ( the pointer is automatically incremented )
             |   |   0   1  ---------- Comparison register              Π
             |   |   1   -  ---------- Preload register                 Π
             |   1      ------------------------ The data latch instruction
             1  ---------------------------------- The data loading instruction
```

(2) Phase-Z input control

```
D7  D6  D5  D4  D3  D2  D1  D0
 0   1   0   0   -   -  ZE1 ZE0
                        0   0  --  No operation
                        0   1  --  Phase-Z input invalidity (D)
                        1   0  --  Limiting phase-Z input next effective
                        1   1  --  Every time, phase-Z input is effective.
```

(3) Edge evaluation and clear timing

```
D7  D6  D5  D4  D3  D2  D1  D0
 1   0   0   0 SYNC ZC  MS1 MS0
                 |   |   0   0  --  Single
                 |   |   0   1  --  Double
                 |   |   1   -  --  Quad      (D)
                 |   0  ----------  A changeable edge is clear.
                 |   1  ----------  A fixed edge is clear (D).
                 0  ----------  Asynchronous clearness (D)
                 1  ----------  Synchronous clearness
```

(4) Interruption output control

```
D7  D6  D5  D4  D3  D2  D1  D0
 1   1   0   0   -   -   -  INT
                            0 ---- Interruption output disable (D)
                            1 ---- Interruption output enable
```

(D): Default

8 , Status register

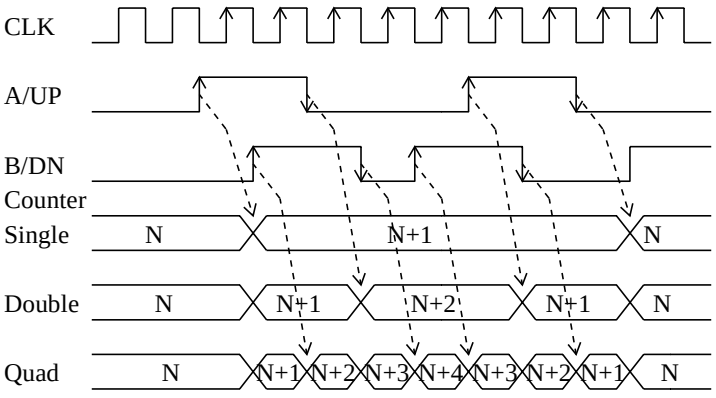
D7	D6	D5	D4	D3	D2	D1	D0	
AI	Z	A	B	DTR	U/$\overline{D}$	$\overline{EQ}$	$\overline{INT}$	
							0	$\overline{INT}$ = "L"
							1	" = "H"
						0		Count value = preset value
						1		" 1 "
					0			Down count
					1			Up count
				0				Latch register Not ready
				1				" Data ready
			0					B/DN = "L"
			1					= "H"
		0						A/UP = "L"
		1						= "H"
	0							Z/CLR = "L"
	1							= "H"
0								Abnormal input undetection
1								" detection

AI is reset after the status reading and DTR is after reading the data of one byte in "0".

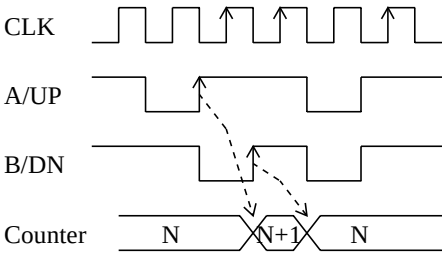
9 , Operation timing

(1) Count operation

Phase-shifted pulse input



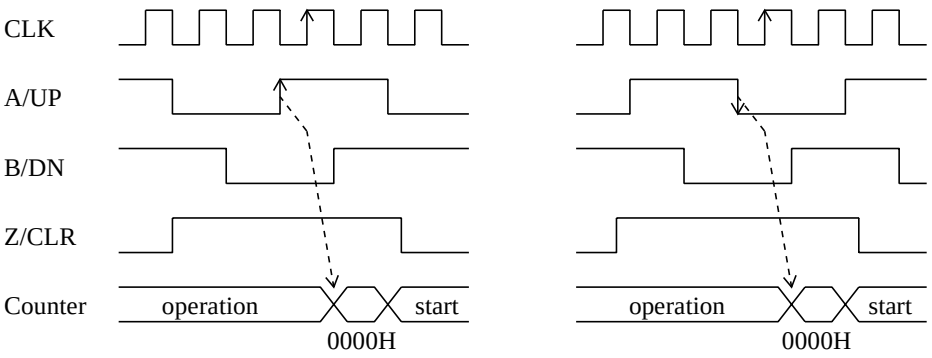
Up/down pulse input



(2) Clear operation

Synchronous clear (Only phase-shifted pulse input).

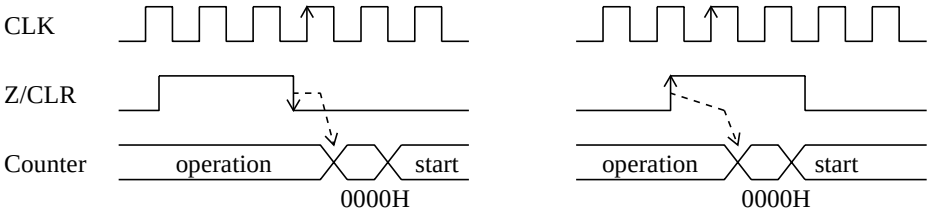
direction CW (phase-A preceding) direction CCW (phase-B preceding)



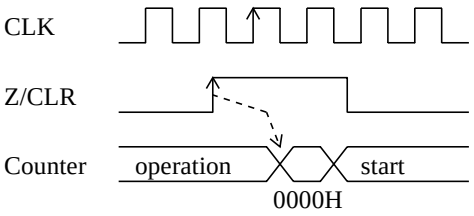
Asynchronous clear

Variable edge

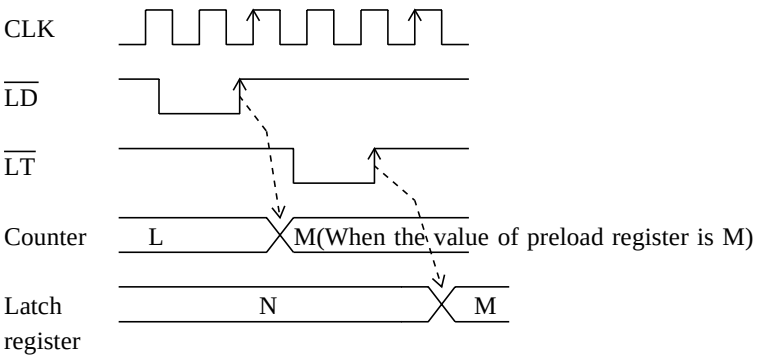
direction CW (phase-A preceding) direction CCW (phase-B preceding)



Fixed edge



(3) The data loading and latch operation timing



10, Electric characteristic

1) Absolute maximum ratings (V_{SS} = 0v)

Item	Sign	Values	Unit
Supply voltage	V_{DD}	-0.3 ~ 7.0	V
Input voltage	V_I	V_{SS}-0.3 ~ V_{DD}+0.3	V
Output voltage	V_O	V_{SS}-0.3 ~ V_{DD}+0.3	V
Peak output current	I_{OL}	+40	mA
	I_{OH}	-20	mA
Permissible loss	PT	495	mW
Operation temperature	T_{opr}	0 ~ 70	C
Reservation temperature	T_{stg}	-55 ~ 150	C

2) Recommended operating conditions (V_{SS} = 0v)

Item	Sign	Min.	Typical	Max.	Unit
Supply voltage	V_{DD}	4.75	5.00	5.25	V
Operation temperature	Ta	0		70	C

3) I/O capacity (V_{DD}=V_I=0v f=1MHz Ta=25 C)

Item	Sign	Min.	Typical	Max.	Unit
Input terminal	C_{IN}		10	20	pF
Output terminal	C_{OUT}		10	20	pF
I/O terminal	$C_{I/O}$		10	20	pF

4) DC characteristics (at the recommended operating conditions)

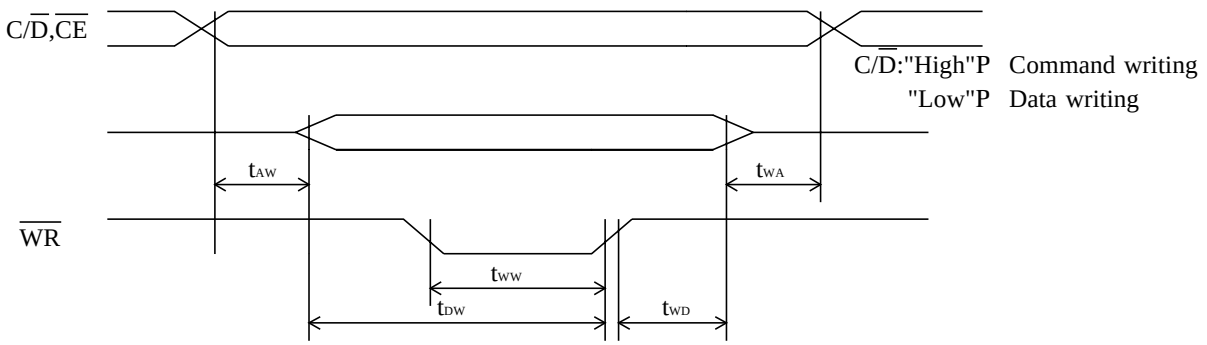
Item		Sign	conditions	Min.	Typical	Max.	Unit
Standby current		I_{DDS}	V_I=V_{DD} or V_{SS}			100	μA
Operation current		I_{DDO}	V_I=V_{DD} or V_{SS} f=20MHz Output open			30	mA
Input voltage	H level	V_{IH}	(group A,D,E)	2		VDD	V
	L level	V_{IL}	(group A,D,E)	0		0.8	V
Input leakage current		I_{LI}	V_I=V_{DD} or V_{SS} (group A,B)	-10		10	A
		I_{PLPU}	V_I=V_{DD} (group E)	-20		20	μA
Input threthold		V_{T+T4}	V_{DD}=5.0V (group B)		1.7	2.4	V
		V_{T-T4}		0.6	1.2		V
Hysteresis width		ΔV_{t4}	V_{DD}=5.0V (group B)	0.2	0.5		V
Output voltage	H level	V_{OH}	I_O=-1.6mA V_I=V_{DD} or V_{SS} (group D,F)	VDD - 0.6			V
	L level	V_{OL}	I_O=12mA V_I=V_{DD} or V_{SS} (group C)			0.4	V
			I_O=4mA V_I=V_{DD} or V_{SS} (group D,F)			0.4	V
Output leakage current		I_{OZ}	V_O=HI-Z V_I=V_{DD} or V_{SS} V_O=V_{DD} (group C)	-10		10	μA
			V_O=HI-Z V_I=V_{DD} or V_{SS} V_O=V_{DD} or V_{SS} (group D)	-10		10	μA
Pullup register		R_{PU1}	V_I=0.0V V_{DD}=5.0V (group E)	12	30	75	KΩ

group A:$\overline{CE}$,C/$\overline{D}$,$\overline{RD}$,$\overline{WR}$,CLK,$\overline{RESET}$
group B:$\overline{LT}$,$\overline{LD}$,Z/CLR,B/DN,A/UP
group C:$\overline{INT}$
group D:D0,D1,D2,D3,D4,D5,D6,D7
group E:DIR,UD/$\overline{AB}$
group F:$\overline{EQ}$

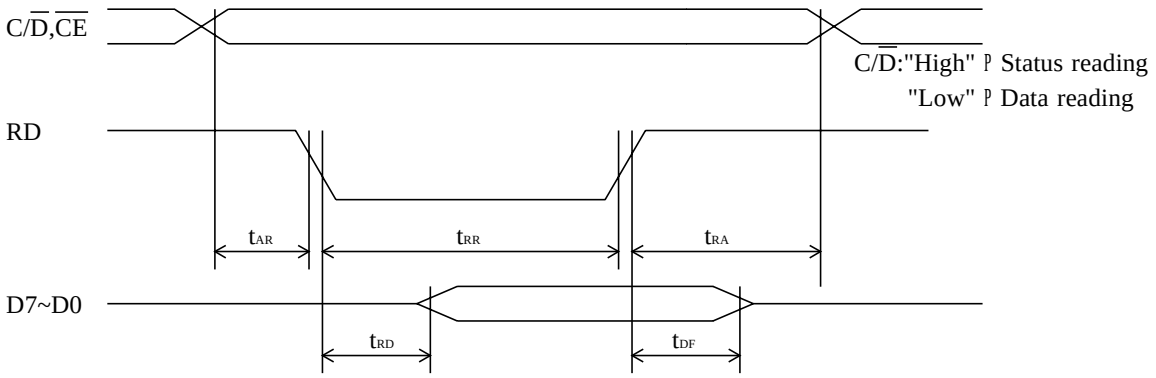
11，AC characteristics (Ta=0-70℃ Vcc=5v±5%)

Item	Sign	Condition	Min	Max	Unit
C/D,CE setup time(D7-D0)	t_{AW}		0		nS
C/D,CE hold time(D7-D0)	t_{WA}		0		nS
Data setup time (WR-)	t_{DW}		25		nS
Data hold time (WR-)	t_{WD}		10		nS
WR pulse width	t_{WW}		50		nS
C/D,CE setup time (RD↑)	t_{AR}		50		nS
C/D,CE hold time (RD-)	t_{RA}		30		nS
RD pulse width	t_{RR}		50		nS
Data access time (RD↑)	t_{RD}			50	nS
Data float delay time(RD-)	t_{DF}			20	nS
Clock H/L pulse width	ϕ		22		nS
Clock rise up time	ϕ_r			3	nS
Clock fall down time	ϕ_f			3	nS
Clock cycle time	ϕ_{cy}		50		nS
Reset pulse width	t_{RST}		ϕ_{cy} /2+50		nS
LD pulse width	t_{LDW}		50		nS
LT pulse width	t_{LDW}		50		nS
CLK--EQ↑delay time	t_{EQF}			20	nS
CLK--EQ-delay time	t_{EQR}			20	nS
A,B high level width	t_{PWABH}		ϕ_{cy} /2+20		nS
A,B low level width	t_{PWABL}		ϕ_{cy} /2+20		nS
A,B phase difference time	t_{SAB}		ϕ_{cy}+10		nS
Z high level width	t_{SZ}	Synchronous clear	ϕ_{cy} /2+20		nS
Z pulse width	t_{ZZ}	Asynchronous clear	ϕ_{cy}+20		nS
UP high level time	t_{UPH}	Up/down mode	ϕ_{cy}+20		nS
UP low level time	t_{UPL}	"	ϕ_{cy}+20		nS
DN high level time	t_{DNH}	"	ϕ_{cy}+20		nS
DN low level time	t_{DNL}	"	ϕ_{cy}+20		nS
UP--DN- set time	t_{UDS}	"	0		nS
CLK--INT↑delay time	t_{INTF}	load capacity 75pF		121	nS

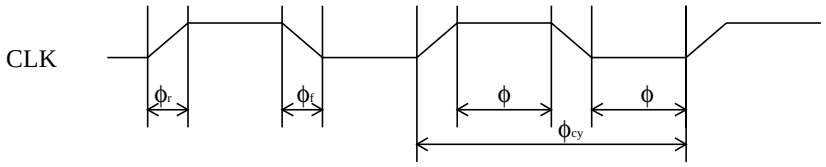
Write cycle



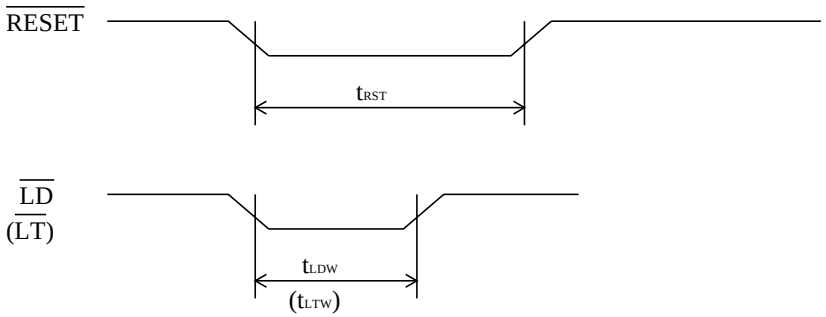
Read cycle



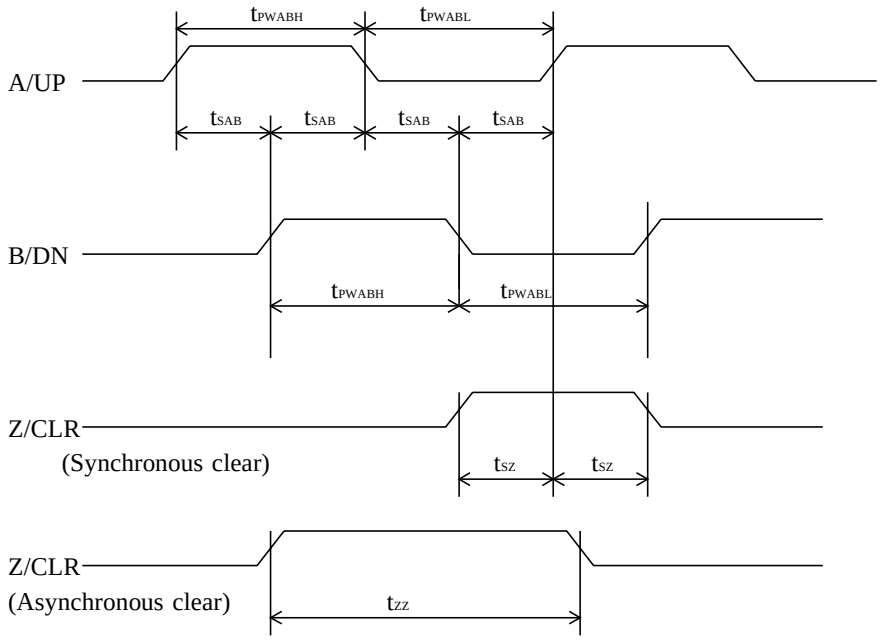
Clock waveform



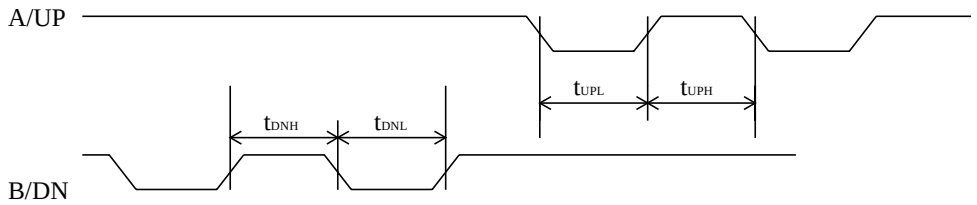
Reset waveform



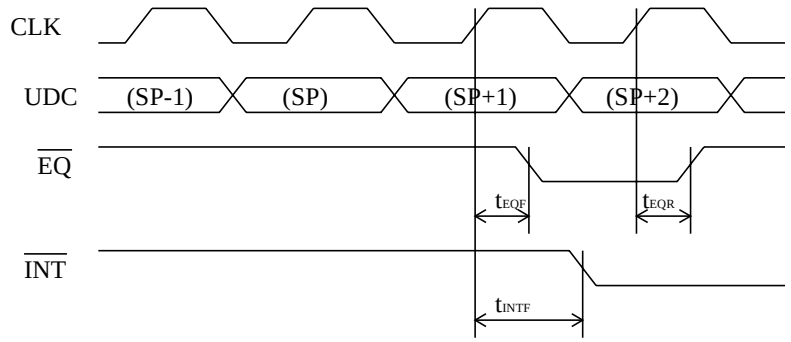
Phase-shifted pulse input



Up/down pulse input



Output timing of $\overline{EQ}$,$\overline{INT}$ signal

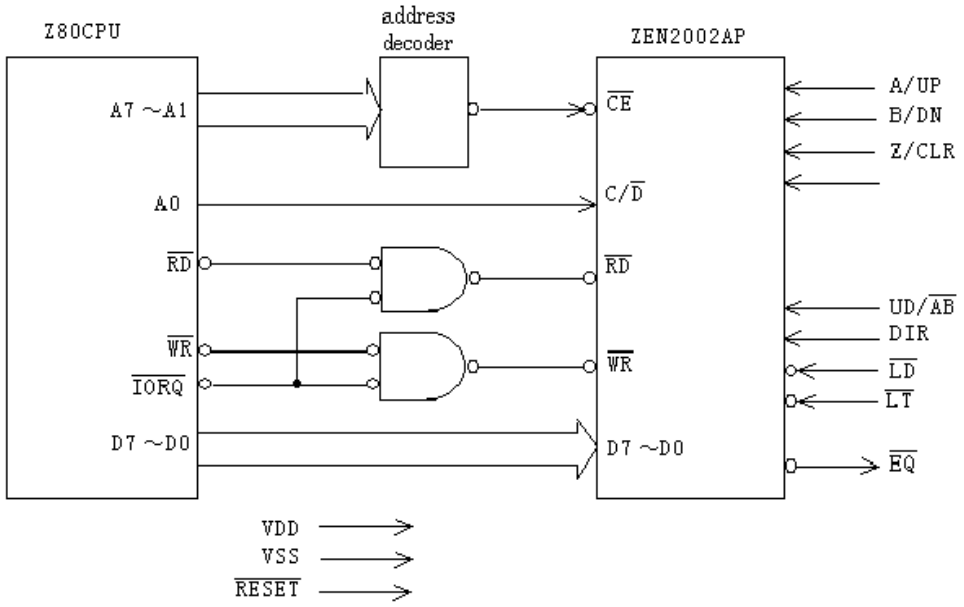


UDC:count value of up/down counter

(SP):set value of reference register

12, Application note

Z80



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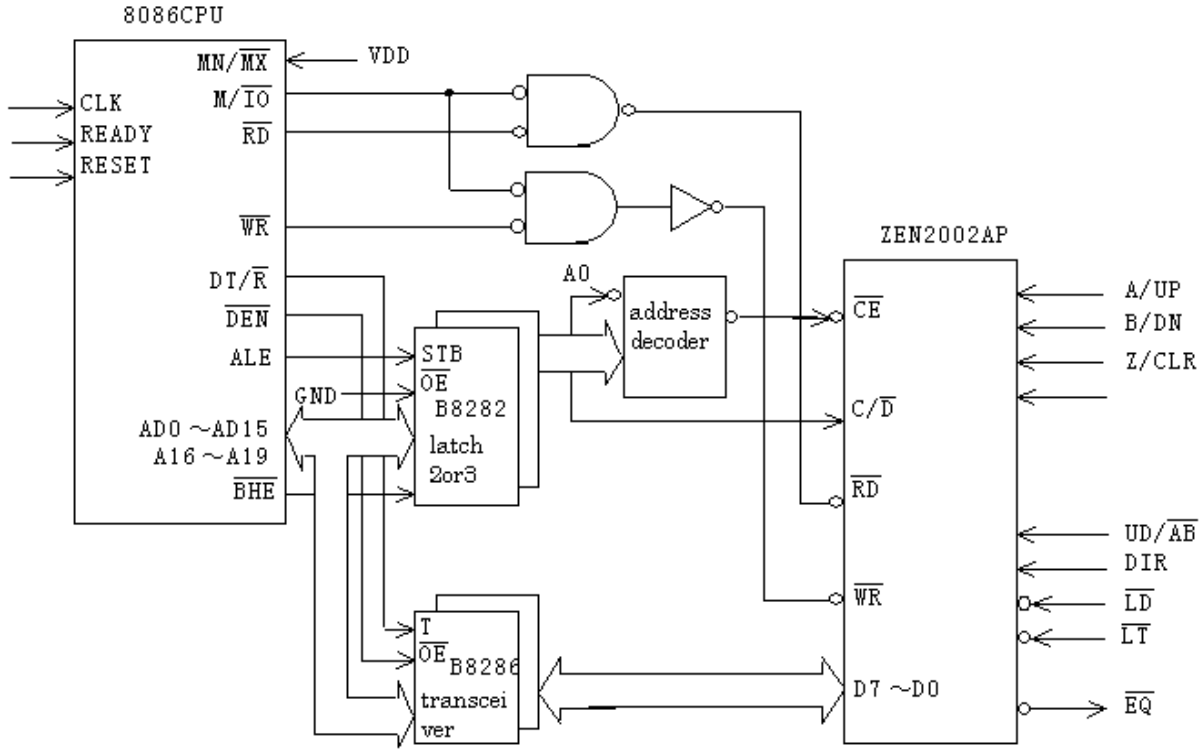
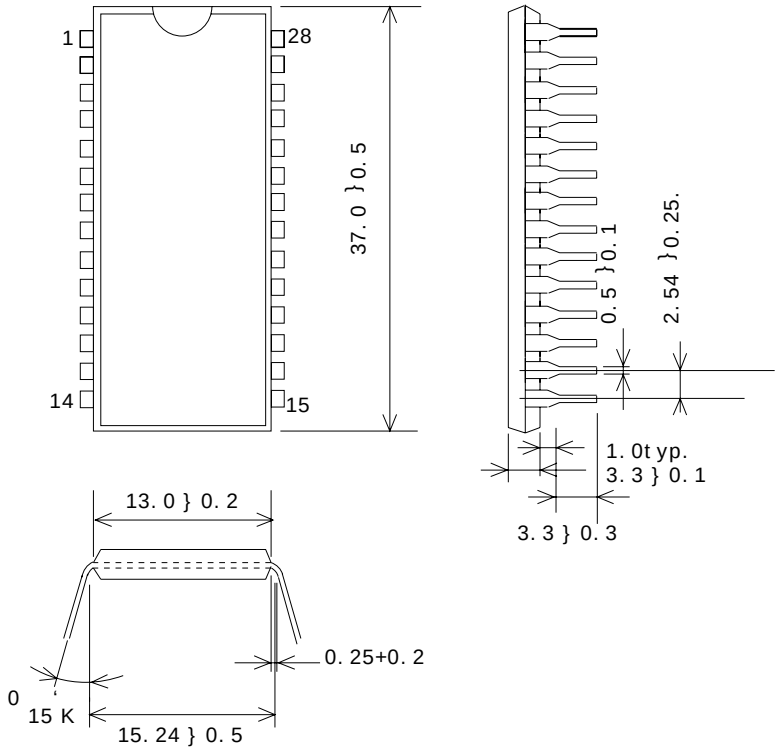


13, Package Outlines(dimensions in mm)



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