RC2211

FSK Demodulator/Tone Decoder

Features

- Wide frequency range – 0.01 Hz to 300 kHz
- Wide supply voltage range – 4.5V to 20V
- DTL/TTL/ECL logic compatibility
- FSK demodulation with carrier-detector
- Wide dynamic range – 2 mV to 3 V_{RMS}
- Adjustable tracking range – ±1% to ±80%
- Excellent temperature stability – 20 ppm/°C typical

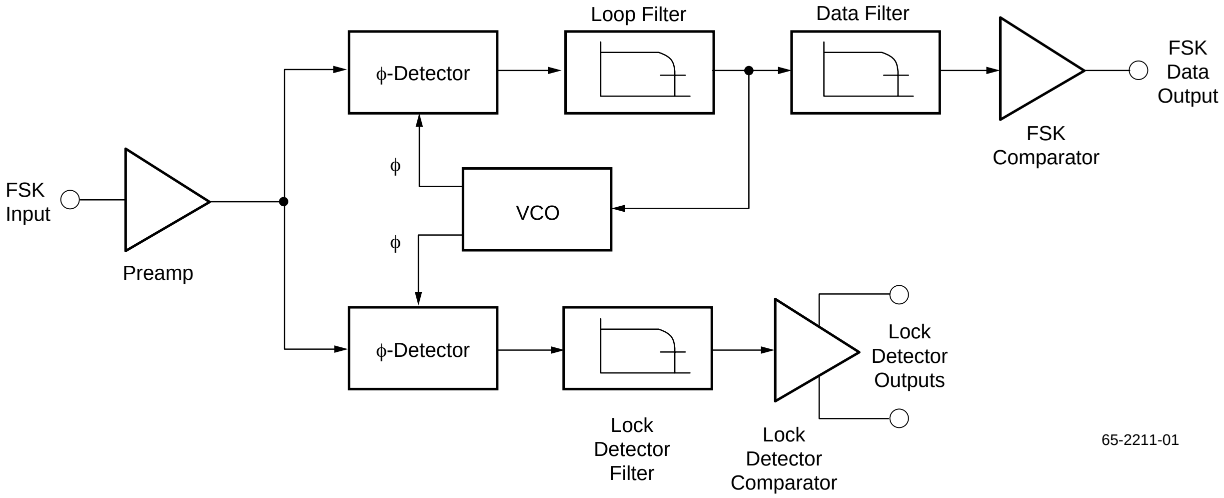
Applications

- FSK demodulation
- Data synchronization
- Tone decoding
- FM detection
- Carrier detection

Description

The RC2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications. It is particularly well-suited for FSK modem applications, and operates over a wide frequency range of 0.01 Hz to 300 kHz. It can accommodate analog signals between 2 mV and 3V, and can interface with conventional DTL, TTL and ECL logic families. The circuit consists of a basic PLL for tracking an input signal frequency within the passband, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set carrier frequency, bandwidth and output delay.

Block Diagram



Description of Circuit Controls

Signal Input (Pin 2)

The input signal is AC coupled to this terminal. The internal impedance at pin 2 is 20 kΩ. Recommended input signal level is in the range of 10 mV_{RMS} to 3 V_{RMS}.

Quadrature Phase Detector Output, Q (Pin 3)

This is the high impedance output of the quadrature phase detector, and is internally connected to the input of lock detector voltage comparator. In tone detection applications, pin 3 is connected to ground through a parallel combination of R_D and C_D (see Figure 1) to eliminate chatter at the lock detector outputs. If this tone detector section is not used, pin 3 can be left open circuited.

Lock Detector Output, Q (Pin 5)

The output at pin 5 is at a “high” state when the PLL is out of lock and goes to a “low” or conducting state when the PLL is locked. It is an open collector output and requires a pull-up resistor, R_L, to $+V_S$ for proper operation. In the “low” state it can sink up to 5 mA of load current.

Lock Detector Complement, $\overline{Q}$ (Pin 6)

The output at pin 6 is the logic complement of the lock detector output at pin 5. This output is also an open collector type stage which can sink 5 mA of load current in the low or “on” state.

FSK Data Output (Pin 7)

This output is an open collector stage which requires a pull-up resistor, R_L, to $+V_S$ for proper operation. It can sink 5 mA of load current. When decoding FSK signals the FSK data output will switch to a “high” or off state for low input frequency, and will switch to a “low” or on state for high input frequency. If no input signal is present, the logic state at pin 7 is indeterminate.

FSK Comparator Input (Pin 8)

This is the high impedance input to the FSK voltage comparator. Normally, an FSK post detection or data filter is connected between this terminal and the PLL phase detector output (pin 11). This data filter is formed by R_F and C_F of Figure 1. The threshold voltage of the comparator is set by the internal reference voltage, V_R, available at pin 10.

Reference Bypass (Pin 9)

This pin can have an optional 0.1, µF capacitor connected to the ground.

Reference Voltage, V_R (Pin 10)

This pin is internally biased at the reference voltage level, V_R; $V_R = +V_S/2 - 650$ mV. The DC voltage level at this pin forms an internal reference for the voltage levels at pin 3, 8, 11 and 12. Pin 10 must be bypassed to ground with a 0.1 µF capacitor.

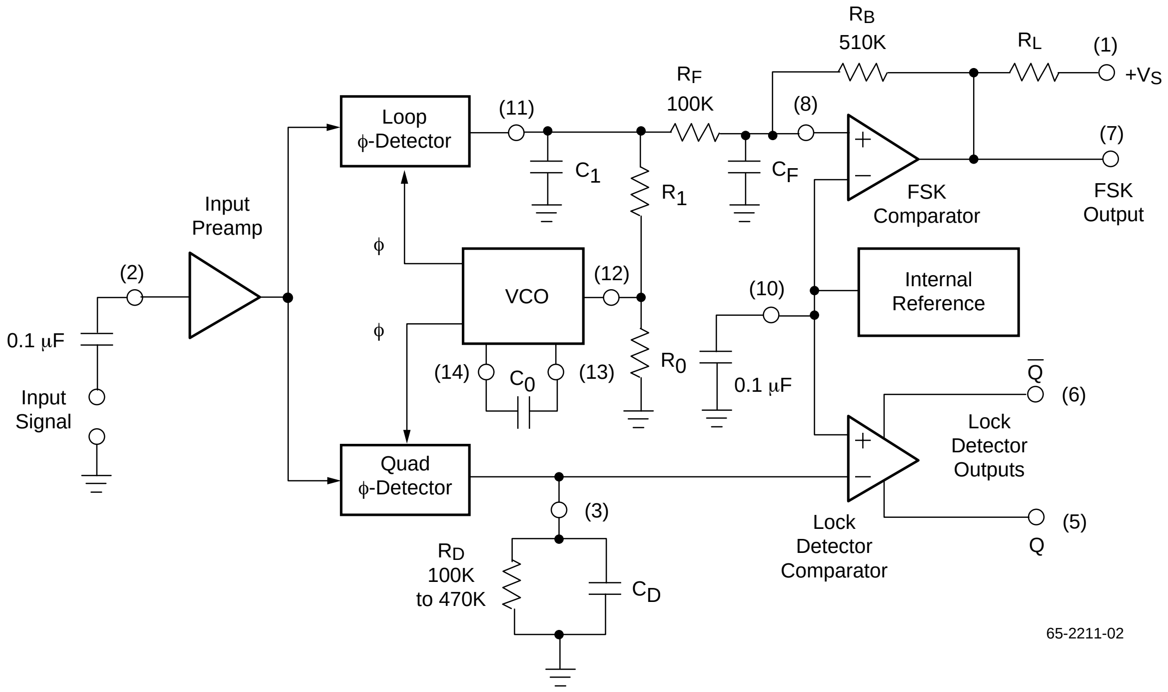


Figure 1. Generalized Circuit Connection for FSK and Tone Detection

Loop Phase Detector Output (Pin 11)

This terminal provides a high impedance output for the loop phase detector. The PLL loop filter is formed by R1 and C1 connected to pin 11 (see Figure 1). With no input signal, or with no phase error within the PLL, the DC level at pin 11 is very nearly equal to V_R. The peak voltage swing available at the phase detector output is equal to $\pm V_R$.

VCO Control Input (Pin 12)

VCO free running frequency is determined by external timing resistor, R0, connected from this terminal to ground. The VCO free running frequency, F_0 is given by:

$$F_0\,(\mathrm{Hz}) = \frac{1}{R_0 C_0}$$

where C_0 is the timing capacitor across pins 13 and 14. For optimum temperature stability R_0 must be in the range of 10 kΩ to 100 kΩ (see Typical Performance Characteristics).

This terminal is a low impedance point, and is internally biased at a DC level equal to V_R. The maximum timing current drawn from pin 12 must be limited to ≤3 mA for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14)

VCO frequency is inversely proportional to the external timing capacitor, C_0, connected across these terminals. C_0 must be non-polarized, and in the range of 200 pF to 10 µF.

VCO Frequency Adjustment

VCO can be fine tuned by connecting a potentiometer, R_x, in series with R_0 at pin 12 (see Figure 2).

VCO Free-Running Frequency, F_0

The RC2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase detector sections of the circuit. However, for set-up or adjustment purposes, the VCO freerunning frequency can be measured at pin 3 (with C_D disconnected) with no input and with pin 2 shorted to pin 10.

Design Equations

See Figure 1 for Definitions of Components.

1. VCO Center Frequency, F_0:

$$F_0\,(\mathrm{Hz}) = \frac{1}{R_0 C_0}$$

2. Internal Reference Voltage, V_R (measured at pin 10)

$$V_R = \left(\frac{+V_S}{2}\right)\text{-650 mV}$$

3. Loop Lowpass Filter Time Constant, τ

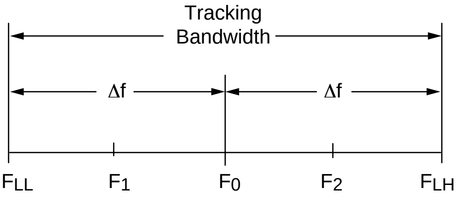
$$\tau = R_1 C_1$$

4. Loop Dampening, ζ:

$$\zeta = \left(\sqrt{\frac{C_0}{C_1}}\right)\left(\frac{1}{4}\right)$$

5. Loop Tracking Bandwidth, $\pm\Delta F/F_0$:

$\Delta f/F_O = R0/R1$



65-2211-03

6. FSK Data Filter Time Constant, τ_F:

$$\tau_F = R_F C_F$$

7. Loop Phase Detector Conversion Gain, $K\phi$ ($K\phi$ is the differential DC voltage across pins 10 and 11, per unit of phase error at phase-detector input):

$$k\phi\,(\text{in volts per radian}) = \frac{(-2)\,(V_R)}{\pi}$$

8. VCO Conversion Gain, K_0 is the amount of change in VCO frequency per unit of DC voltage change at pin 11:

$$K0\,(\text{in Hertz per volt}) = \frac{-1}{C_0 R_1 V_R}$$

9. Total Loop Gain, K_T:

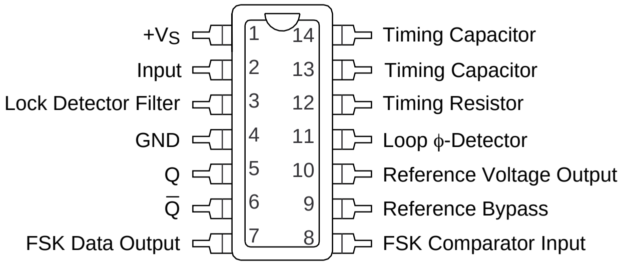
K_T (in radians per second per volt)= $2\,\pi K\phi K0$

$$= \frac{4}{C_0 R_1}$$

10. Peak Phase Detector Current, I_A:

$$I_A\,(\mathrm{mA}) = \frac{V_R}{25}$$

Pin Assignments



65-2211-04

Absolute Maximum Ratings

Parameter		Min	Max	Unit
Supply Voltage		-20	+20	V
Input Signal Level			3	V_{RMS}
Storage Temperature Range		-65	+150	°C
Operating Temperature Range	RM2211D	-55	+125	°C
	RV2211N	-25	+85	°C
	RC2211N	-0	+70	°C
Junction Temperature	PDIP		+125	°C
	CerDIP		+175	°C
Lead Soldering Temperature (60 sec.)			+300	°C
Max. P_D T_A<50°C	PDIP		468	mW
	CerDIP		1042	mW

Thermal Characteristics

Parameter	14 Lead Plastic DIP	14 Lead Ceramic DIP
Therm. Res θ_{JC}	—	60°C/W
Therm. Res. θ_{JA}	160°C/W	120°C/W
For T_A > 50°C Derate at	6.5 mW/°C	8.33 mW/°C

Electrical Characteristics

(Test Conditions $+V_S$ = +12V, T_A +25°C, R0 = 30 kΩ, C0 = 0.033 µF. See Figure 1 for component designations.)

Parameters	Test Conditlons	RV/RM2211			RC2211			Units
		Min	Typ	Max	Min	Typ	Max	
General								
Supply Voltage[2]		4.5		20	4.5		20	V
Supply Current	$R_0 \geq 10$ kΩ		4.0	9.0		5.0	11	mA
Oscillator								
Frequency Accuracy	Deviation from $f_0 = 1/R_0C_0$		±1.0	±3.0		±1.0		%
Frequency Stability[1]								
Temperature Coefficient	$R_1 = \infty$		±20	±50		±20		ppm/°C
Power Supply Rejection	$+V_S$ = 12 ±1V		0.05	0.5		0.05		%/V
	$+V_S$ = 5 ±0.5V		0.2		0.2			%/V
Upper Frequency Limit	R_0 = 8.2 kΩ, C_0 = 400 pF	100	300			300		kHz
Lowest Practical Operating Frequency[1]	R_0 = 2 MΩ, C_0 = 50 µF			0.01		0.01		Hz
Timing Resistor, R_0								
Operating Range		5.0		2000	5.0		2000	kΩ
Recommended Range		15		100	15		100	kΩ
Loop Phase Detector								
Peak Output Current	Measured at pin 11	±150	±200	±300	±100	±200	±300	µA
Output Offset Current			±1.0			±2.0		µA
Output Impedance			1.0			1.0		MΩ
Maximum Swing	Ref. to pin 10	±4.0	±5.0		±4.0	±5.0		V
Quadrature Phase Detector								
Peak Output Current[3]	Measured at pin 3	100	150			150		µA
Output Impedance			1.0			1.0		MΩ
Maximum Swing			11			11		V_{P-P}
Input Preamp								
Input Impedance	Measured at pin 2		20			20		kΩ
Input Signal Voltage Required to Cause Limiting[3]			2.0	10		2.0		mV_{RMS}
Voltage Comparator								
Input Impedance	Measured at pins 3 & 8		2.0			2.0		MΩ
Input Bias Current			100			100		nA
Voltage Gain[1]	R_L = 5.1 kΩ	55	70		55	70		dB
Output Voltage Low	I_C = 3mA		300			300		mV
Output Leakage Current	V_0 = 12V		0.01			0.01		µA
Internal Reference								
Voltage Level	Measured at pin 10	4.9	5.3	5.7	4.75	5.3	5.85	V
Output Impedance			100			100		Ω

Notes:

1. Guaranteed by design.
2. Individual applications may need special circuitry to function at <12V.
3. Sample tested.

Applications

FSK Decoding

Figure 2 shows the basic circuit connection for FSK decoding. With reference to Figures 1 and 2, the functions of external components are defined as follows: R_0 and C_0 set the PLL center frequency, R_1 sets the system bandwidth, and C_1 sets the loop filter time constant and the loop damping factor. C_F and R_F form a one pole post-detection filter for the FSK data output. The resistor R_B (510 kΩ) from pin 7 to pin 8 introduces positive feedback across FSK comparator to facilitate rapid transition between output logic states.

Recommended component values for some of the most commonly used FSK bauds are given in Table 1.

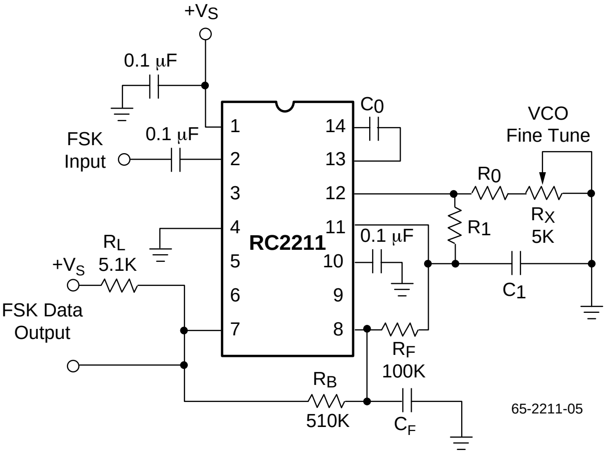


Figure 2. Circuit Connectbn for FSK Decoding

Table 1. Recommended Component Values for Commonly Used FSK Bands
(see Circuit of Figure 2)

FSK Band	Component Values
300 Baud	C_0 = 0.039 µF, C_F = 0.005 µF
F_1 = 1070 Hz	C_1 = 0.01 µF, R_0 = 18 kΩ
F_2 = 1270 Hz	R_1 = 100 kΩ
300 Baud	C_0 = 0.022 µF, C_F = 0.005 µF
F_1 = 2025 Hz	C_1 = 0.0047 µF, R_0 = 18 kΩ
F_2 = 2225 Hz	R_1 = 200 kΩ
1200 Baud	C_0 = 0.027 µF, C_F = 0.0022 µF
F_1 = 1200 Hz	C_1 = 0.01 µF, R_0 = 18 kΩ
F_2 = 2200 Hz	R_1 = 30 kΩ

Design Instructions

The circuit of Figure 2 can be tailored for any FSK decoding application by the choice of five key circuit components: R_0, R_1, C_0, C_1 and C_F. For a given set of FSK mark and space frequencies, F_1 and F_2, these parameters can be calculated as follows:

1. Calculate PLL center frequency, F_0

   $$F_0 = \frac{F_1 + F_2}{2}$$

2. Choose a value of timing resistor R_0 to be in the range of 10 kΩ to 100 kΩ. This choice is arbitrary. The recommended value is R_0 = 20 kΩ. The final value of R_0 ios normally finetuned with the series potentiometer, R_X.

3. Calculate value of C_0 from Design Equation No. 1 or from Typical Performance Characteristics:

   $C_0 = 1/R_0F_0$

4. Calculate R_1 to give a Δf equal to the markspace deviation:

   $R_1 = R_0 [F_0/(F_1 - F_2)]$

5. Calculate C_1 to set loop damping. (See Design Equation No. 4)

   Normally, $\zeta \approx 1/2$ is recommended
   Then: $C_1 = C_0/4$ for $\zeta = 1/2$

6. Calculate Data Filter Capacitance, C_F:
   For R_F = 100 kΩ, R_B = 510 kΩ, the recommended value of C_F is:

   $$C_F \text{ (in µF)} = \frac{3}{\text{Baud Rate}}$$

Note: All calculated component values except RO can be rounded off to the nearest standard value, and R0 can be varied to fine-tune center frequency through a series potentiometer, R_X (see Figure 2).

Design Example

75 Baud FSK demodulator with mark space frequencies of 1110/1170 Hz:

Step 1: Calculate F_0:
F_0=(1110+1170)(1/2)= 1140Hz

Step 2: Choose R_0 = 20 kΩ (18 kΩ fixed resistor in series with 5 kΩ potentiometer)

Step 3: Calculate C_0 from VCO Frequency vs. Timing Capacitor: C_9 = 0.044µF

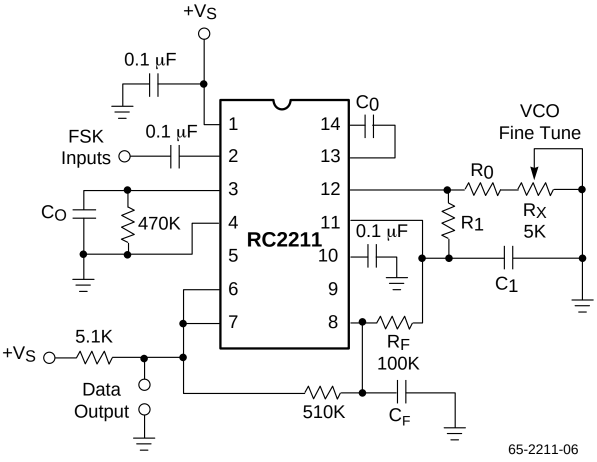
Step 4: Calculate R_1: $R_1 = R_0$ (1140/60) = 380 kΩ

Step 5: Calculate C_1: $C_1 = C_0/4$ = 0.011 µF

Note: All values except R_0 can be rounded off to nearest standard value.

FSK Decoding with Carrier Detector

The lock detector section of the RC2211 can be used as a carrier detector option for FSK decoding. The recommended circuit connection for this application is shown in Figure 3. The open-collector lock detector output, pin 6, is shorted to the data output (pin 7). Thus, the data output will be disabled at "low" state, until there is a carrier within the detection band of the PLL, and the pin 6 output goes "high" to enable the data output.



Note: Data output is "low" when no carrier is present.

Figure 3. External Connections for FSK Demodulation with Carrier Detector Capability

The minimum value of the lock detector filter capacitance C_D is inversely proportional to the capture range, $\pm\Delta f_C$. This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by C_1. For most applications, $\Delta F_C < \Delta F/2$. For $R_D = 470\ k\Omega$, the approximate minimum value of C_D can be determined by:

$$C_D(\mu F) \geq 16/\text{capture range in Hz}$$

With values of C_D that are too small, chatter can be observed on the lock detector output as an incoming signal frequency approaches the capture bandwidth. Excessively large values of C_D will slow the response time of the lock detector output.

Tone Detection

Figure 4 shows the generalized circuit connection for tone detection. The logic outputs, Q and $\overline{Q}$ at pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs becomes reversed to the duration of the input tone. Each logic output can sink 5 mA of load current.

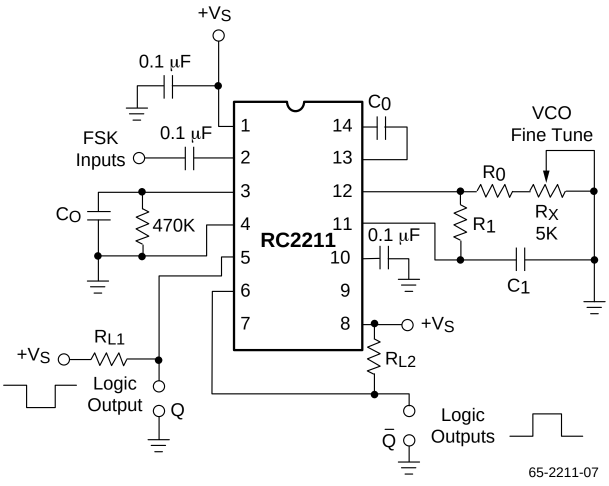


Figure 4. Circuit Connection for Tone Detection

Both logic outputs at pins 5 and 6 are open-collector type stages, and require external pull-up resistors R_{L1} and R_{L2} as shown in Figure 4.

With reference to Figures 1 and 4, the function of the external circuit components can be explained as follows: R_0 and C_0 set VCO center frequency, R_1 sets the detection bandwidth, C_1 sets the lowpass-loop filter time constant and the loop dampening factor, and R_{L1} and R_{L2} are the respective pull-up resistors for the Q and $\overline{Q}$ logic outputs.

Design Instructions

The circuit of Figure 4 can be optimized for any tone-detection application by the choice of five key circuit components: R_0, R_1, C_0, C_1 and C_D. For a given input tone frequency, F_S, these parameters are calculated as follows:

1. Choose R_0 to be in the range of 15 kΩ to 100 kΩ. This choice is arbitrary.
2. Calculate C_0 to set center frequency, f_0 equal to F_S: $C_0 = 1/R_0F_S$.
3. Calculate R_1 to set bandwidth $\pm\Delta F$ (see Design Equation No. 5): $R_1 = R_0(F_0/\Delta F)$. Note: The total detection bandwidth covers the frequency range of $F_0 \pm \Delta F$.
4. Calculate value of C_1 for a given loop damping factor:

   $C_1 = C_0/16\zeta^2$

   Normally $\zeta = 1/2$ is optimum for most tone detector applications, giving $C_1 = 0.25\ C0$.

   Increasing C_1 improves the out-of-band signal rejection, but increases the PLL capture time.
5. Calculate value of filter capacitor C_D. To avoid chatter at the logic output, with $R_D = 470\Omega$, C_D must be:

   $C_D(\mu F) \geq (16/\text{capture range in Hz})$

   Increasing C_D slows the logic output response time.

Design Examples

Tone detector with a detection band of 1 kHz ±20 Hz:

Step 1: Choose R_0 = 20 kΩ (18 kΩ in series with 5 kΩ potentiometer) .

Step 2: Choose C_0 for F_0 = 1 kHz: C_0 = 0.05 µF.

Step 3: Calculate R_1: $R_1 = (R_0)(1000/20) = 1$ MΩ.

Step 4: Calculate C_1: for $\zeta = 1/2$, C_1 = 0.25 µF, C_0 = 0.013 µF.

Step 5: Calculate C_D: $C_D = 16/38 = 0.42$ µF.

Step 6: Fine tune the center frequency with the 5 kΩ potentiometer. R_X.

Linear FM Detection

The RC2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for the application is shown in Figure 5. The demodulated output is taken from the loop phase detector output (pin 11), through a post detection filter made up of R_F and C_F, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in Figure 5.

The FM detector gain, i.e., the output voltage change per unit of FM deviation, can be given as:

$$V_{OUT} = R_1 V_R/100 R_0 \text{ Volts/\% deviation}$$

where V_R is the internal reference voltage. For the choice of external components R_1, R_0, C_0, C_1 and C_F, see the section on Design Instructions.

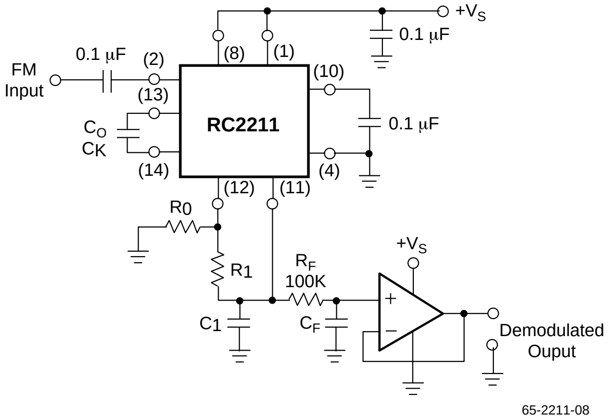


Figure 5. Linear FM Detector Using RC2211 and an External Op Amp

Typical Performance Characteristics

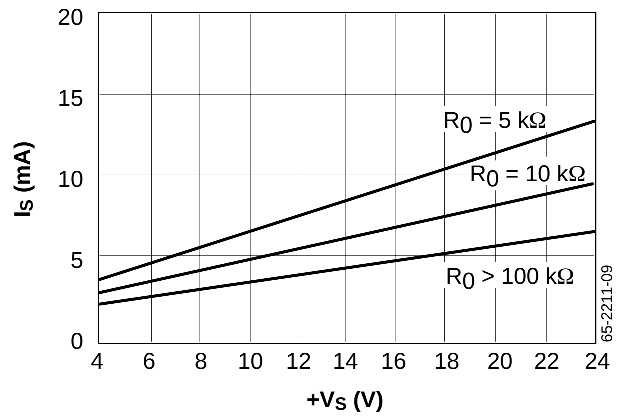


Figure 6. Supply Current vs. Supply Voltage (Logic Outputs Open Circuited)

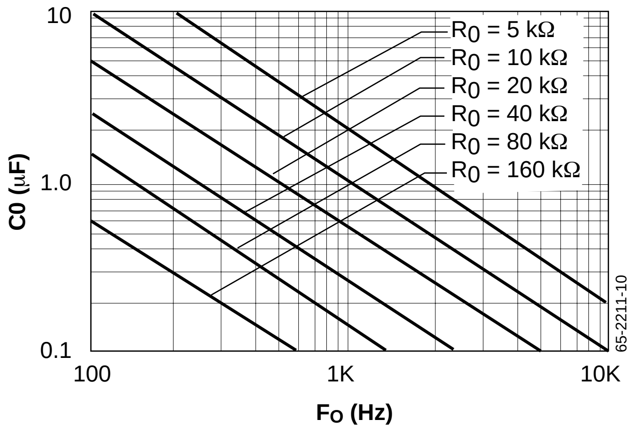


Figure 7. Timing Resistor with Timing Capacitor vs. VCO Frequency

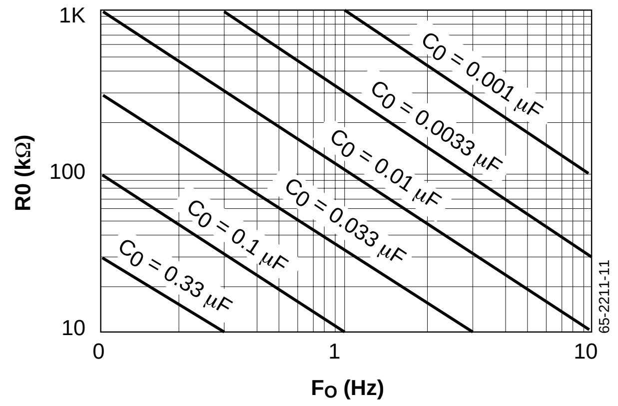


Figure 8. Timing Capacitor with Timing Resistor vs. VCO Frequency

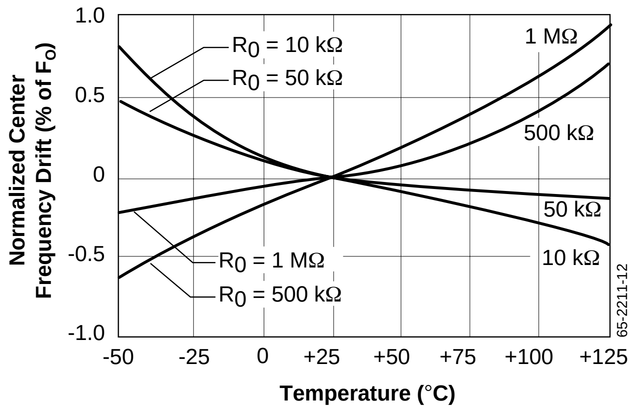
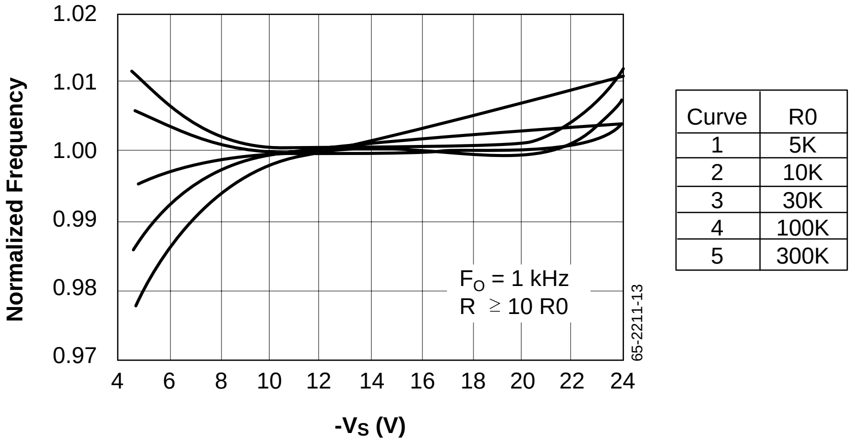


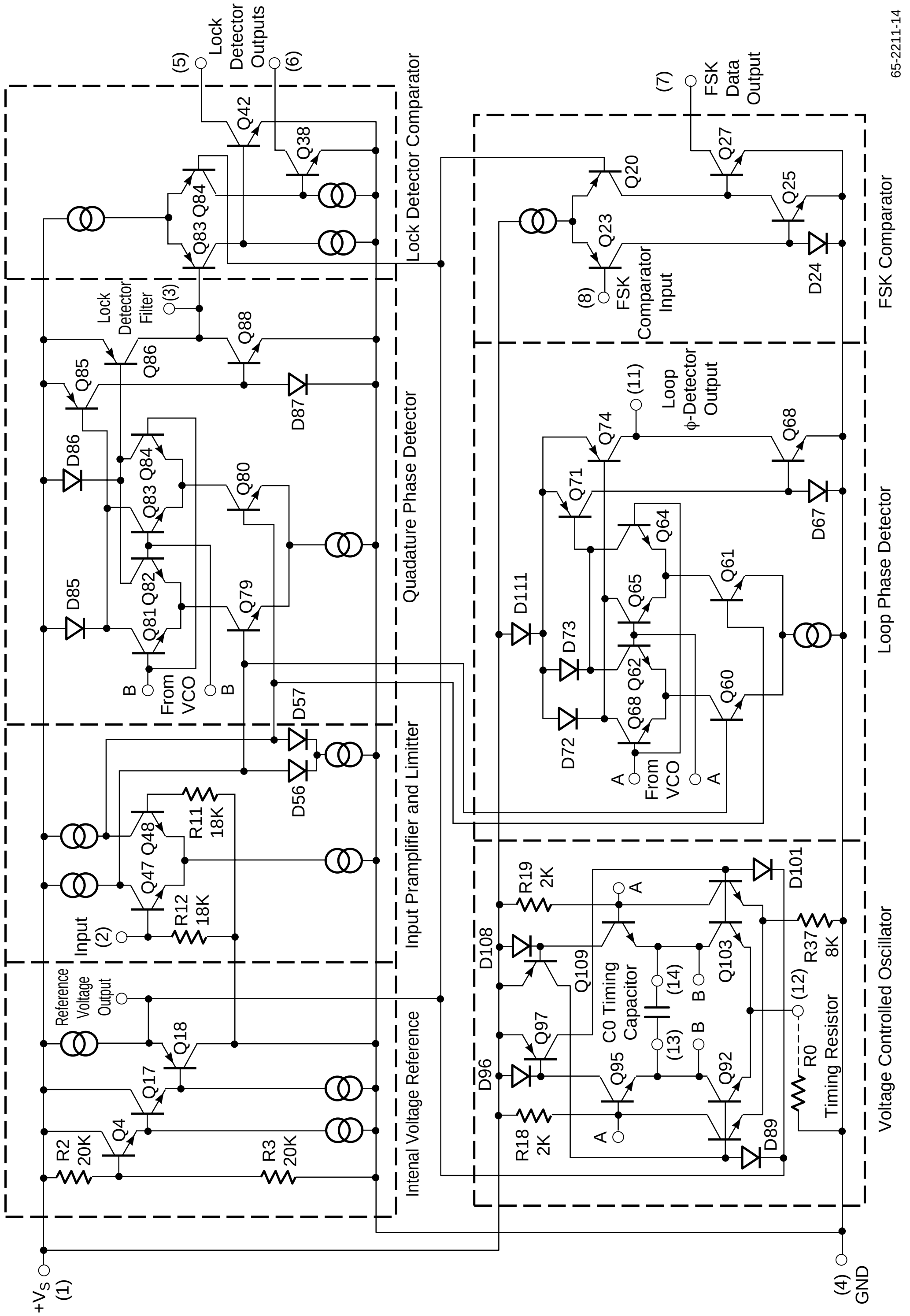
Figure 9. Center Frequency Drift vs. Temperature



Curve	R0
1	5K
2	10K
3	30K
4	100K
5	300K

Figure 10. VCO Frequency vs. Supply Voltage

Schematic Diagram



Notes:

Notes:

Notes:

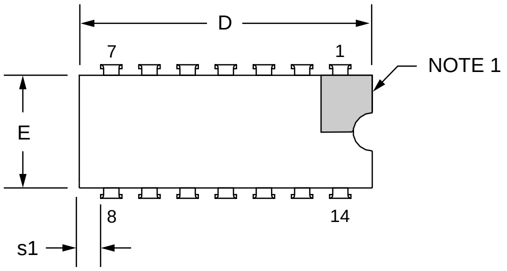
Mechanical Dimensions

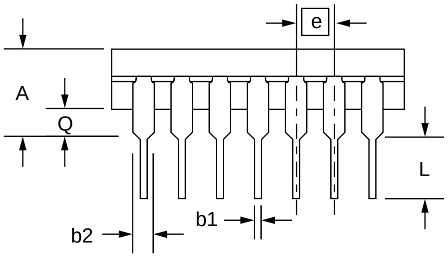
14-Lead Ceramic DIP Package

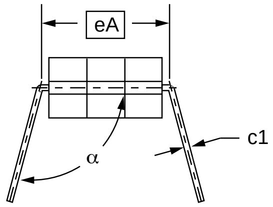
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2
c1	.008	.015	.20	.38	8
D	—	.785	—	19.94	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 7, 8 and 14 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 14.
6. Applies to all four corners (leads number 1, 7, 8, and 14).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Twelve spaces.







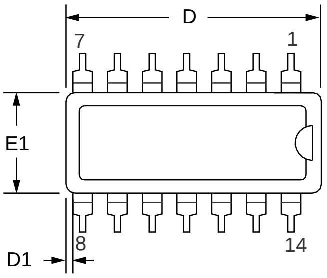
Mechanical Dimensions (continued)

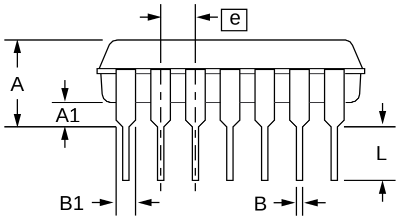
14-Lead Plastic DIP Package

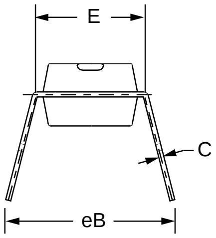
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.725	.795	18.42	20.19	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.200	2.92	5.08	
N	14		14		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







Ordering Information

Part Number	Package	Operating Temperature Range
RC2211N	N	0°C to +70°C
RV2211N	N	-25°C to +85°C
RM2211D	D	-55°C to +125°C
RM2211D/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Par 1.2.1 Compliant Devices
N = 14-Lead Plastic DIP
D = 14-Lead Ceramic DIP

LIFE SUPPORT POLICY:

Raytheon's products are not designed for use in life support applications, wherein a failure or malfunction of the component can reasonably be expected to result in personal injury. The user of Raytheon components in life support applications assumes all risk of such use and indemnifies Raytheon Company against all damages

Raytheon Electronics
Semiconductor Division
350 Ellis Street
Mountain View CA 94043
415 968 9211
FAX 415 966 7742

12/95 0.0m
Stock#DS20002211