

HM6268 Series

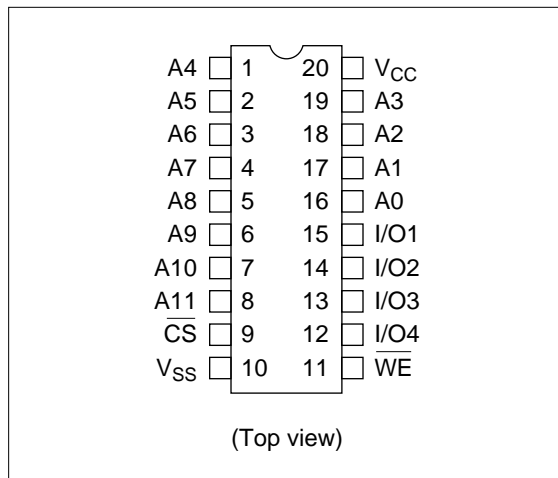
Maintenance only

4096-word × 4-bit High-Speed CMOS Static RAM

Features

- Single 5 V supply and high density 20-pin package
- High speed: fast access time 25/35/45 ns (max)
- Low power
 - Active: 250 mW (typ)
 - Standby: 100 μ W (typ), 5 μ W (typ) (L-version)
- Completely static memory: no clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible—all inputs and outputs
- Battery back-up operation capability (L-version)

Pin Arrangement

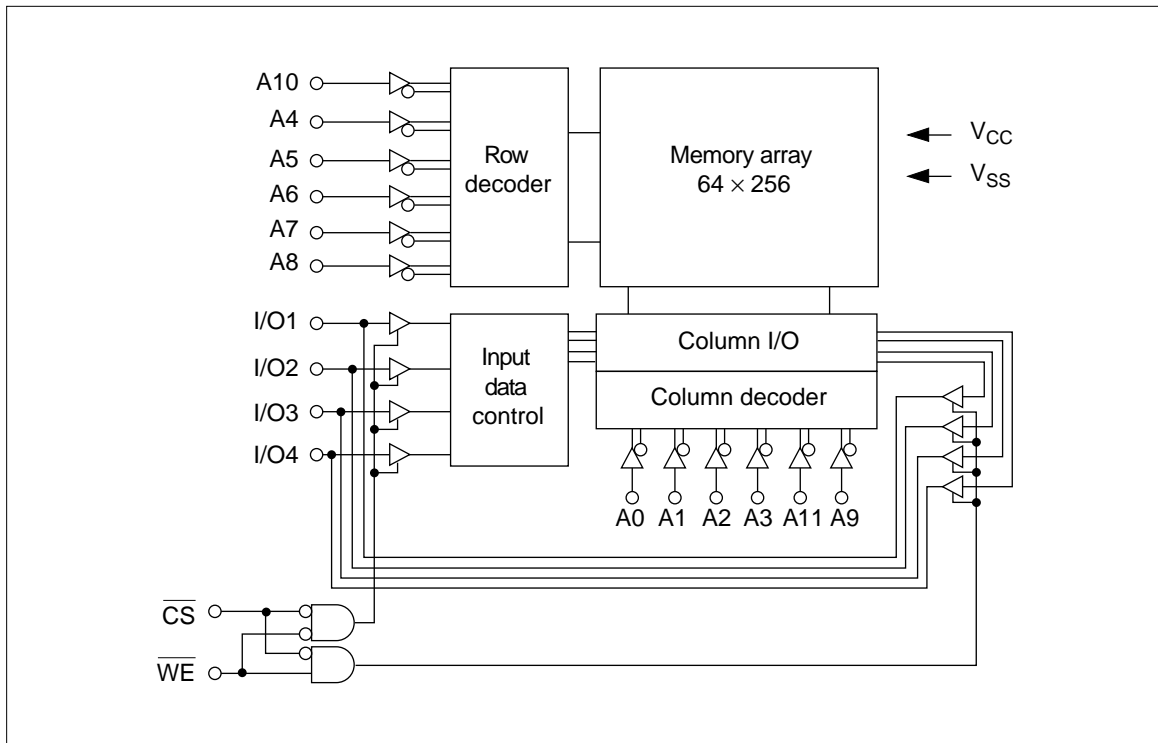


Ordering Information

Type No.	Access time	Package
HM6268P-25	25 ns	300-mil 20-pin, plastic DIP (DP-20N)
HM6268P-35	35 ns	
HM6268P-45	45 ns	
HM6268LP-25	25 ns	
HM6268LP-35	35 ns	
HM6268LP-45	45 ns	

Note: This device is not available for new application.

Block Diagram



Truth Table

\overline{CS}	\overline{WE}	Mode	V_{CC} current	I/O pin	Cycle
H	x	Not Selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	I_{CC}	Dout	Read cycle
L	L	Write	I_{CC}	Din	Write cycle

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	-0.5 ^{*1} to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to + 70	°C
Storage temperature	T_{stg}	-55 to +125	°C
Temperature under bias	T_{bias}	-10 to + 85	°C

Note: 1. -3.5 V for pulse width \leq 10 ns.

Recommended DC Operating Conditions ($T_a = 0$ to $+70^\circ\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	-0.5^{*1}	—	0.8	V

Note: 1. -3.0 V for pulse width ≤ 10 ns.

DC Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 0$ to $+70^\circ\text{C}$)

Parameter	Symbol	Min	Typ ^{*1}	Max	Unit	Test condition
Input leakage current	$ I_{LI} $	—	—	2.0	μA	$V_{CC} = 5.5\text{ V}$, $V_{in} = V_{SS}$ to V_{CC}
Output leakage current	$ I_{LO} $	—	—	2.0	μA	$\overline{CS} = V_{IH}$, $V_{I/O} = V_{SS}$ to V_{CC}
Operating power supply current	I_{CC}	—	50^{*3}	90	mA	$\overline{CS} = V_{IL}$, $I_{I/O} = 0\text{ mA}$, min. cycle
Standby power supply current	I_{SB}	—	15	25	mA	$\overline{CS} = V_{IH}$, min. cycle
Standby power supply current (1)	I_{SB1}	—	0.02	2.0	mA	$\overline{CS} \geq V_{CC} - 0.2\text{ V}$, $0\text{ V} \leq V_{IN} \leq 0.2\text{ V}$ or $V_{CC} - 0.2\text{ V} \leq V_{IN}$
		—	1^{*2}	50^{*2}	μA	
Output low voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 8\text{ mA}$
Output high voltage	V_{OH}	2.4	—	—	V	$I_{OH} = -4.0\text{ mA}$

Notes: 1. Typical limits are at $V_{CC} = 5.0\text{ V}$, $T_a = +25^\circ\text{C}$ and specified loading
 2. This characteristic is guaranteed only for L-version.
 3. 40 mA typical for 45 ns version.

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$) ^{*1}

Parameter	Symbol	Test conditions	Min	Max	Unit
Input capacitance	C_{in}	$V_{in} = 0\text{ V}$	—	6	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O} = 0\text{ V}$	—	9	pF

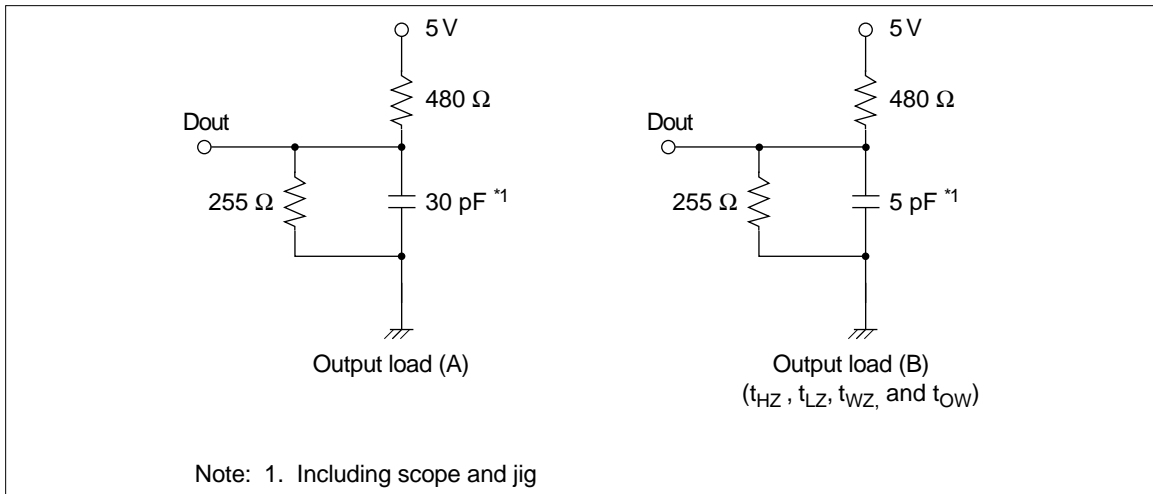
Note: 1. These parameters are sampled and not 100% tested.

AC Characteristics ($V_{CC} = 5\text{ V} + 10\%$, $T_a = 0\text{ to }+70^\circ\text{C}$, unless otherwise noted)

AC Test Conditions:

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figure

Output Load

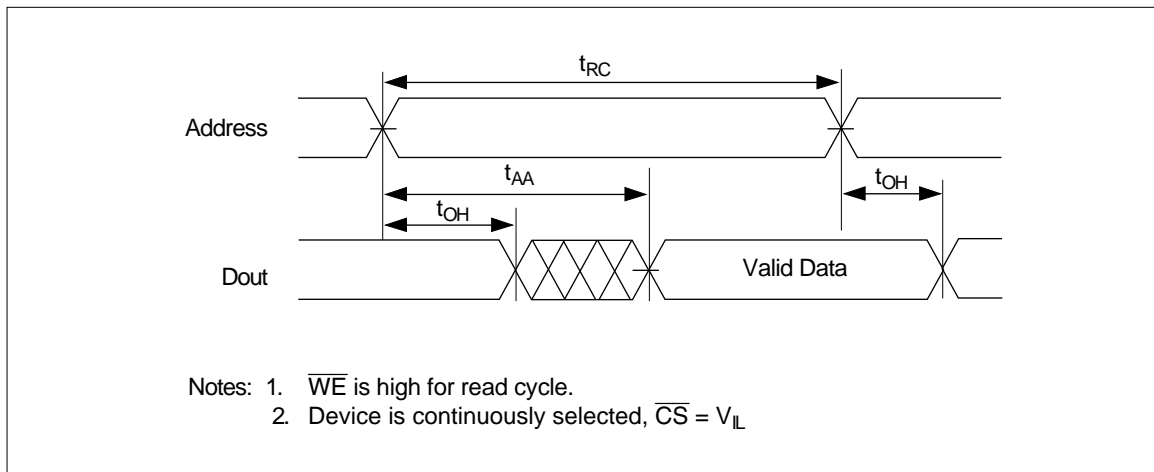


Read Cycle

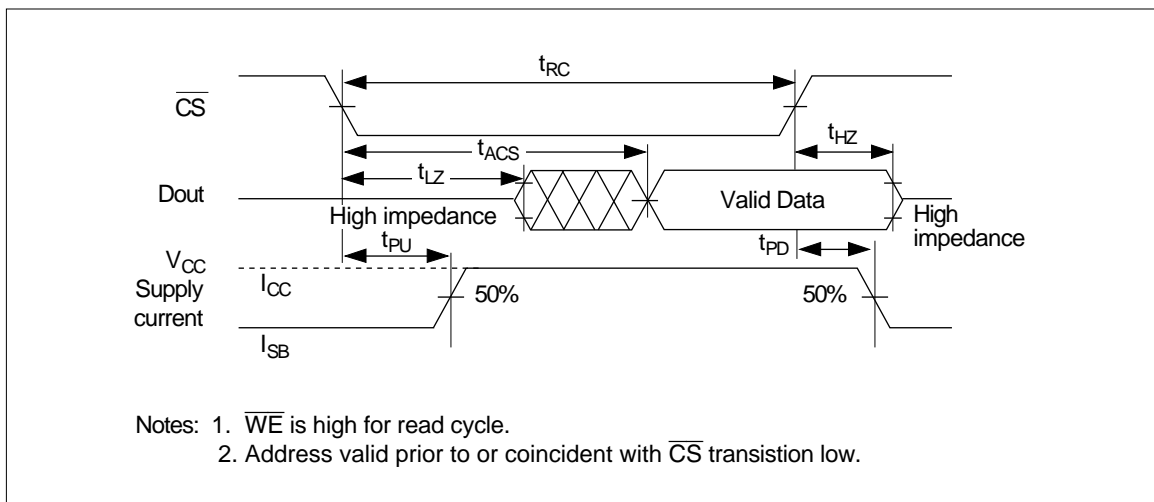
Parameter	Symbol	HM6268-25		HM6268-35		HM6268-45		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	25	—	35	—	45	—	ns
Address access time	t_{AA}	—	25	—	35	—	45	ns
Chip select access time	t_{ACS}	—	25	—	35	—	45	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip selection to output in low-Z	t_{LZ}^{*1}	10	—	10	—	10	—	ns
Chip deselection to output in high-Z	t_{HZ}^{*1}	0	15	0	20	0	20	ns
Chip selection to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	25	—	25	—	30	ns

Note: 1. Transition is measured +200 mV from steady state voltage with load (B). These parameters are sampled and not 100% tested.

Read Timing Waveform (1)



Read Timing Waveform (2)

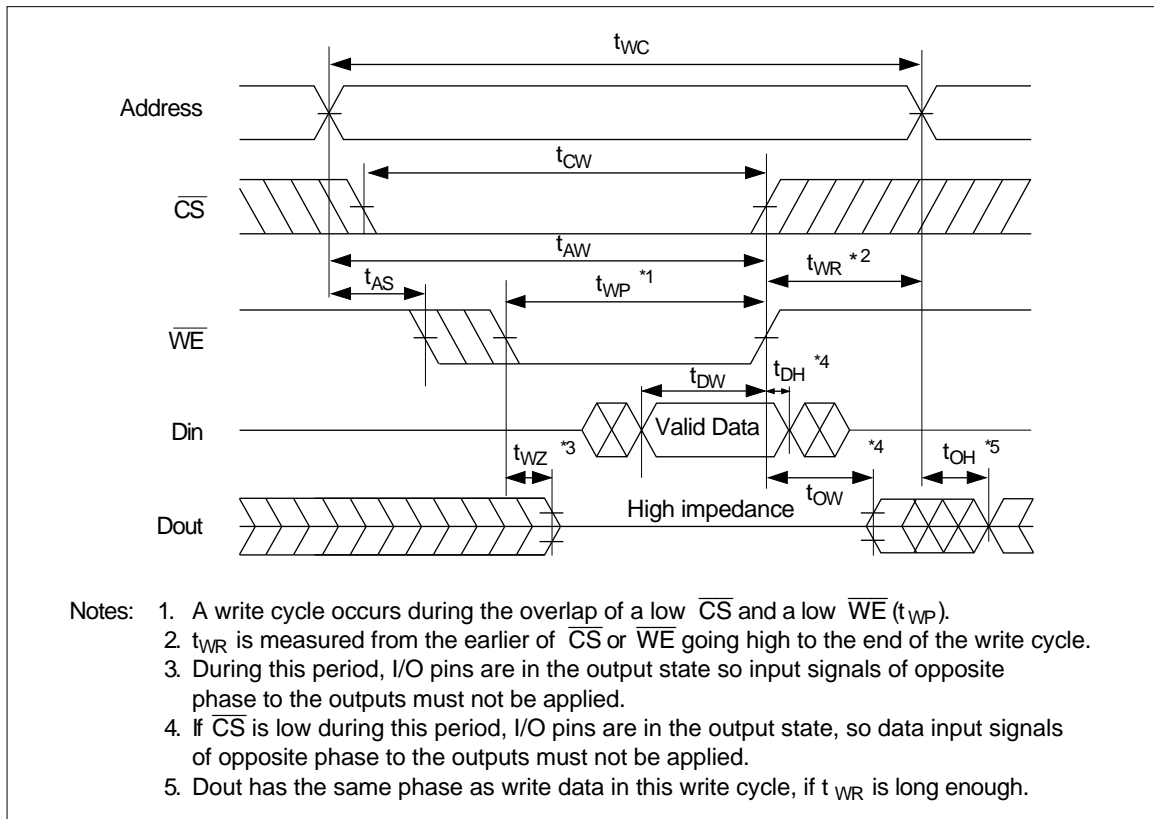


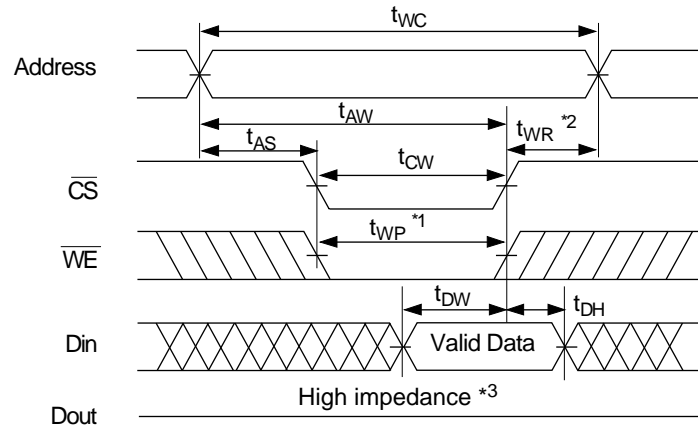
Write Cycle

Parameter	Symbol	HM6268-25		HM6268-35		HM6268-45		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	t_{WC}	25	—	35	—	45	—	ns
Chip selection to end of write	t_{CW}	20	—	30	—	40	—	ns
Address valid to end of write	t_{AW}	20	—	30	—	40	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	30	—	35	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Data valid to end of write	t_{DW}	12	—	20	—	20	—	ns
Data hold time	t_{DH}	0	—	0	—	0	—	ns
Write enabled to output in high-Z	t_{WZ}^{*1}	0	8	0	10	0	15	ns
Output active from end of write	t_{OW}^{*1}	0	—	0	—	0	—	ns

Note: 1. Transition is measured +200 mV from steady state voltage with load (B).
These parameters are sampled and not 100% tested.

Write Timing Waveform (1) (\overline{WE} Controlled)



Write Timing Waveform (2) (\overline{CS} Controlled)

- Notes:
1. A write cycle occurs during the overlap of a low \overline{CS} and a low \overline{WE} (t_{WP}).
 2. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of the write cycle.
 3. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, the output buffers remain in a high impedance state.

Low V_{CC} Data Retention Characteristics ($0^{\circ}\text{C} \leq T_a \leq 70^{\circ}\text{C}$)

These characteristics are guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$, or
Data retention current	I_{CCDR}	—	—	30^{*2} 20^{*3}	μA	$0\text{ V} \leq V_{IN} \leq 0.2\text{ V}$
Chip deselect to data retention time	t_{CDR}	2.0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}^{*1}	—	—	ns	

- Notes: 1. Read cycle time
 2. $V_{CC} = 3.0\text{ V}$
 3. $V_{CC} = 2.0\text{ V}$

Low V_{CC} Data Retention Waveform

