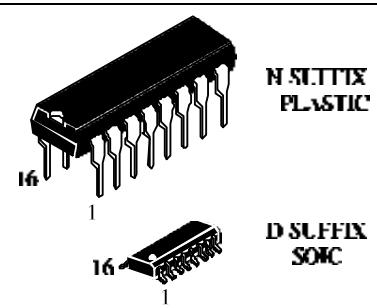


## 3-to-8-Line Decoder/Demultiplexer

This schottky-clamped TTL MSI circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay time. In high-performance memory systems this decode can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit the delay times of this decoder and the enable time of the memory are usually less than the typical access times of the memory. This means that the effective system delay introduced by the schottky-clamped system decoder is negligible.

- Designed Specifically for High Speed Memory Decoders and Data Transmission Systems
- Incorporate 3 Enabler Inputs to Simplify Cascading AND/OR Data Reception
- Schottky Clamped for High Performance



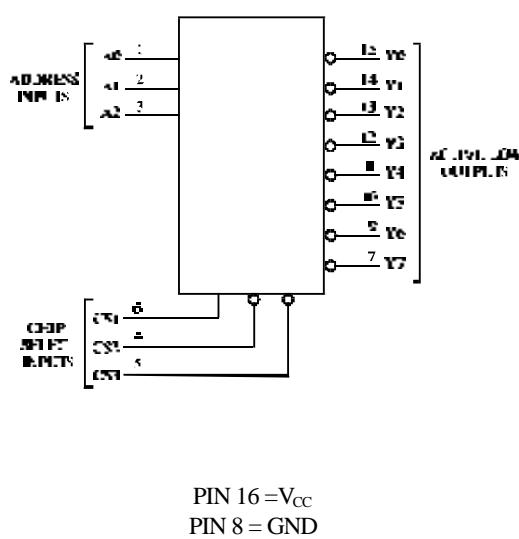
### ORDERING INFORMATION

SL74LS138N Plastic  
SL74LS138D SOIC  
 $T_A = 0^\circ \text{ to } 70^\circ \text{ C}$   
for all packages

### PIN ASSIGNMENT

A0	1 ●	16	V <sub>CC</sub>
A1	2	15	Y0
A2	3	14	Y1
CS1	4	13	Y2
CS2	5	12	Y3
CS3	6	11	Y4
Y7	7	10	Y5
GND	8	9	Y6

### LOGIC DIAGRAM



### FUNCTION TABLE

Inputs		Outputs										
CS1	CS2	CS3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6
X	X	H	X	X	X	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	L	H	H
H	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	L

H = high level (steady state)

L = low level (steady state)

X = don't care



System Logic  
Semiconductor

# SL74LS138

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## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	7.0	V
V <sub>IN</sub>	Input Voltage	7.0	V
V <sub>OUT</sub>	Output Voltage	5.5	V
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.25	V
V <sub>IH</sub>	High Level Input Voltage	2.0		V
V <sub>IL</sub>	Low Level Input Voltage		0.8	V
I <sub>OH</sub>	High Level Output Current		-0.4	mA
I <sub>OL</sub>	Low Level Output Current		8.0	mA
T <sub>A</sub>	Ambient Temperature Range	0	+70	°C

## DC ELECTRICAL CHARACTERISTICS over full operating conditions

Symbol	Parameter	Test Conditions	Guaranteed Limit		Unit
			Min	Max	
V <sub>IK</sub>	Input Clamp Voltage	V <sub>CC</sub> = min, I <sub>IN</sub> = -18 mA		-1.5	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = min, I <sub>OH</sub> = -0.4 mA	2.7		V
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = min, I <sub>OL</sub> = 4 mA		0.4	V
		V <sub>CC</sub> = min, I <sub>OL</sub> = 8 mA		0.5	
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = max, V <sub>IN</sub> = 2.7 V		20	µA
		V <sub>CC</sub> = max, V <sub>IN</sub> = 7.0 V		0.1	mA
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = max, V <sub>IN</sub> = 0.4 V		-0.4	mA
I <sub>O</sub>	Output Short Circuit Current	V <sub>CC</sub> = max, V <sub>O</sub> = 0 V (Note 1)	-20	-100	mA
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = max Outputs enabled and open		10	mA

Note 1: Not more than one output should be shorted at a time, and duration should not exceed one second.

**AC ELECTRICAL CHARACTERISTICS** ( $T_A=25^\circ\text{C}$ ,  $V_{CC} = 5.0 \text{ V}$ ,  $C_L = 15 \text{ pF}$ ,  $R_L = 2 \text{ k}\Omega$ ,  $t_r = 15 \text{ ns}$ ,  $t_f = 6.0 \text{ ns}$ )

Symbol	Parameter	Level	Min	Max	Unit
$t_{PLH}$	Maximum Propagation Delay, Input A to Output Y	2		20	ns
$t_{PHL}$	Maximum Propagation Delay, Input A to Output Y			41	ns
$t_{PLH}$	Maximum Propagation Delay, Input A to Output Y	3		27	ns
$t_{PHL}$	Maximum Propagation Delay, Input A to Output Y			39	ns
$t_{PLH}$	Maximum Propagation Delay , CS1 to Output Y	3		26	ns
$t_{PHL}$	Maximum Propagation Delay , CS1 to Output Y			38	ns
$t_{PLH}$	Maximum Output Transition Time , CS2 or CS3 to Output Y	2		18	ns
$t_{PHL}$	Maximum Output Transition Time , CS2 or CS3 to Output Y			32	ns

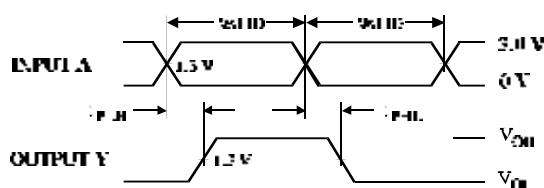


Figure 1. Switching Waveforms

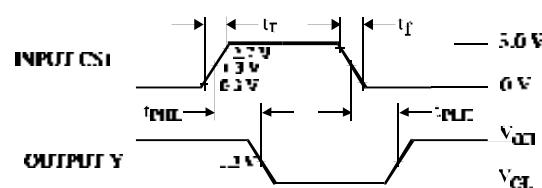


Figure 2. Switching Waveforms

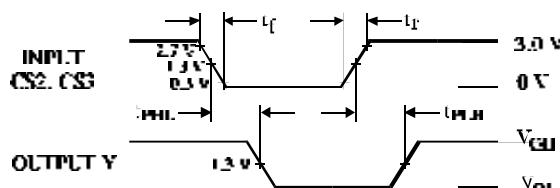
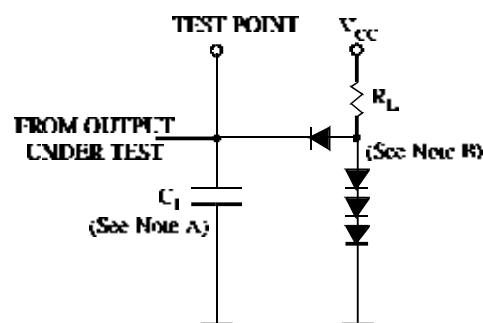


Figure 3. Switching Waveforms



NOTES A.  $C_L$  includes probe and jig capacitance.  
B. All diodes are 1N916 or 1N3064.

Figure 4. Test Circuit