# Am73/8307 • Am73/8308

## Octal Three-State Bidirectional Bus Transceivers

### DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- 3-state inputs/outputs for interfacing with bus-oriented systems
- PNP inputs reduce input loading
- $V_{CC}$ – 1.15V $V_{OH}$ interfaces with TTL, MOS, and CMOS
- 48mA, 300pF bus drive capability
- Am73/8307 has inverting tranceivers
- Am73/8308 has noninverting transceivers
- Separate $\overline{\text{TRANSMIT}}$ and $\overline{\text{RECEIVE}}$ Enables
- 20 pin ceramic and molded DIP package
- Low power – 8mA per bidirectional bit
- Advanced Schottky processing
- Bus port stays in hi-impedance state during power up/down
- 100% product assurance screening to MIL-STD-883 requirements

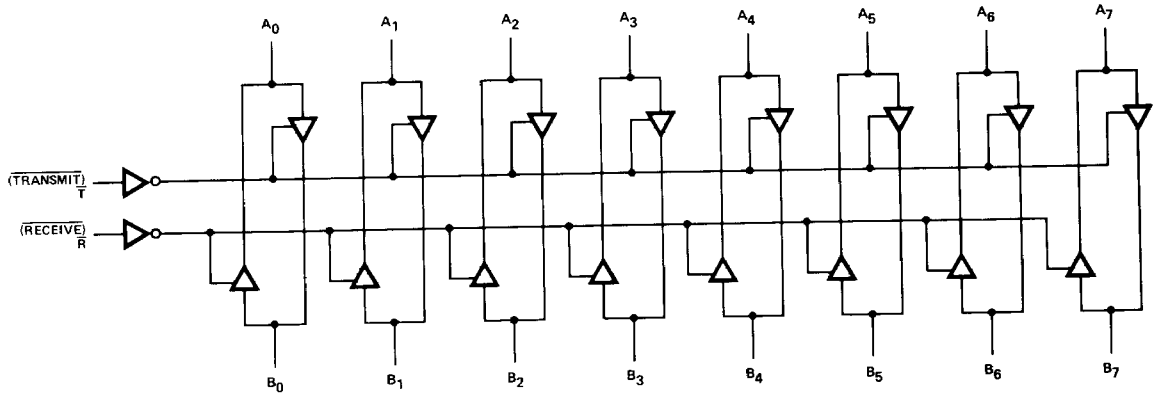
### GENERAL DESCRIPTION

The Am73/8307 and Am73/8308 are 8-bit, 3-state Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 16mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

Separate $\overline{\text{TRANSMIT}}$ and $\overline{\text{RECEIVE}}$ Enables are provided for microprocessor system with separated read and write control bus lines.

The output high voltage ($V_{OH}$) is specified at $V_{CC}$ – 1.15V minimum to allow interfacing with MOS, CMOS, TTL, ROM RAM, or microprocessors.

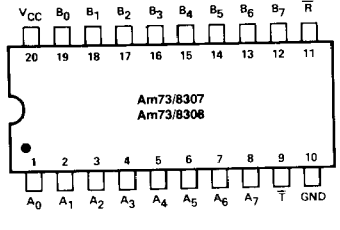
### Am73/8308 LOGIC DIAGRAM




Am73/8307 has inverting transceivers

BLI-177

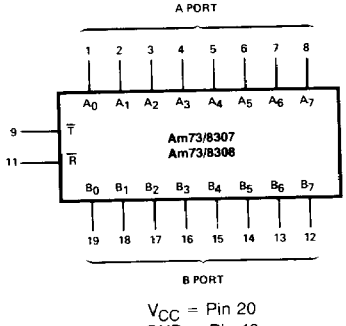
### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.
Am73/8307 is inverting from $A_i$ to $B_i$

BLI-178

### LOGIC SYMBOL




$V_{CC}$ = Pin 20
GND = Pin 10

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## ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65 to +150°C |
| Supply Voltage | 7.0V |
| Input Voltage | 5.5V |
| Output Voltage | 5.5V |
| Lead Temperature (Soldering, 10 seconds) | 300°C |

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:

| | | | |
|---|---|---|---|
| MIL | $T_A$ = −55 to +125°C | $V_{CC}$ MIN = 4.5V | $V_{CC}$ MAX = 5.5V |
| COM'L | $T_A$ = 0 to +70°C | $V_{CC}$ MIN = 4.75V | $V_{CC}$ MAX = 5.25V |

## DC ELECTRICAL CHARACTERISTICS over operating temperature range

| Parameters | Description | Test Conditions | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|
| **A PORT ($A_0$-$A_7$)** | | | | | | | |
| $V_{IH}$ | Logical "1" Input Voltage | $\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V | | 2.0 | | | Volts |
| $V_{IL}$ | Logical "0" Input Voltage | $\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V | COM'L | | | 0.8 | Volts |
| | | | MIL | | | 0.7 | |
| $V_{OH}$ | Logical "1" Output Voltage | $\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V | $I_{OH}$ = −0.4mA | $V_{CC}$−1.15 | $V_{CC}$−0.7 | | Volts |
| | | | $I_{OH}$ = −3.0mA | 2.7 | 3.95 | | |
| $V_{OL}$ | Logical "0" Output Voltage | $\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V | $I_{OL}$ = 8mA | | 0.3 | 0.4 | Volts |
| | | | COM'L $I_{OL}$ = 16mA | | 0.35 | 0.50 | |
| $I_{OS}$ | Output Short Circuit Current | $\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, $V_O$ = 0V, $V_{CC}$ = MAX, Note 2 | | −10 | −38 | −75 | mA |
| $I_{IH}$ | Logical "1" Input Current | $\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, $V_I$ = 2.7V | | | 0.1 | 80 | μA |
| $I_I$ | Input Current at Maximum Input Voltage | $\overline{T}$ = $\overline{R}$ = 2.0V, $V_{CC}$ = MAX, $V_I$ = $V_{CC}$ MAX | | | | 1 | mA |
| $I_{IL}$ | Logical "0" Input Current | $\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, $V_I$ = 0.4V | | | −70 | −200 | μA |
| $V_C$ | Input Clamp Voltage | $\overline{T}$ = $\overline{R}$ = 2.0V, $I_{IN}$ = −12mA | | | −0.7 | −1.5 | Volts |
| $I_{OD}$ | Output/Input 3-State Current | $\overline{T}$ = $\overline{R}$ = 2.0V | $V_O$ = 0.4V | | | −200 | μA |
| | | | $V_O$ = 4.0V | | | 80 | |
| **B PORT ($B_0$-$B_7$)** | | | | | | | |
| $V_{IH}$ | Logical "1" Input Voltage | $\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V | | 2.0 | | | Volts |
| $V_{IL}$ | Logical "0" Input Voltage | $\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V | COM'L | | | 0.8 | Volts |
| | | | MIL | | | 0.7 | |
| $V_{OH}$ | Logical "1" Output Voltage | $\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V | $I_{OH}$ = −0.4mA | $V_{CC}$−1.15 | $V_{CC}$−0.8 | | Volts |
| | | | $I_{OH}$ = −5.0mA | 2.7 | 3.9 | | |
| | | | $I_{OH}$ = −10mA | 2.4 | 3.6 | | |
| $V_{OL}$ | Logical "0" Output Voltage | $\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V | $I_{OL}$ = 20mA | | 0.3 | 0.4 | Volts |
| | | | $I_{OL}$ = 48mA | | 0.4 | 0.5 | |
| $I_{OS}$ | Output Short Circuit Current | $\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, $V_O$ = 0V, $V_{CC}$ = MAX, Note 2 | | −25 | −50 | −150 | mA |
| $I_{IH}$ | Logical "1" Input Current | $\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, $V_I$ = 2.7V | | | 0.1 | 80 | μA |
| $I_I$ | Input Current at Maximum Input Voltage | $\overline{T}$ = $\overline{R}$ = 2.0V, $V_{CC}$ = MAX, $V_I$ = $V_{CC}$ MAX | | | | 1 | mA |
| $I_{IL}$ | Logical "0" Input Current | $\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, $V_I$ = 0.4V | | | −70 | −200 | μA |
| $V_C$ | Input Clamp Voltage | $\overline{T}$ = $\overline{R}$ = 2.0V, $I_{IN}$ = −12mA | | | −0.7 | −1.5 | Volts |
| $I_{OD}$ | Output/Input 3-State Current | $\overline{T}$ = $\overline{R}$ = 2.0V | $V_O$ = 0.4V | | | −200 | μA |
| | | | $V_O$ = 4.0V | | | 200 | |
| **CONTROL INPUTS $\overline{T}$, $\overline{R}$** | | | | | | | |
| $V_{IH}$ | Logical "1" Input Voltage | | | 2.0 | | | Volts |
| $V_{IL}$ | Logical "0" Input Voltage | | COM'L | | | 0.8 | Volts |
| | | | MIL | | | 0.7 | |
| $I_{IH}$ | Logical "1" Input Current | $V_I$ = 2.7V | | | 0.5 | 20 | μA |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = MAX, $V_I$ = $V_{CC}$ MAX | | | | 1.0 | mA |
| $I_{IL}$ | Logical "0" Input Current | $V_I$ = 0.4V | $\overline{R}$ | | −0.1 | −0.25 | mA |
| | | | $\overline{T}$ | | −0.25 | −0.5 | |
| $V_C$ | Input Clamp Voltage | $I_{IN}$ = −12mA | | | −0.8 | −1.5 | Volts |
| **POWER SUPPLY CURRENT** | | | | | | | |
| $I_{CC}$ | Power Supply Current | Am73/8307 | $\overline{T}$ = $\overline{R}$ = 2.0V, $V_I$ = 2.0V, $V_{CC}$ = MAX | | 70 | 100 | mA |
| | | | $\overline{T}$ = 0.4V, $V_{INA}$ = $\overline{R}$ = 2.0V, $V_{CC}$ = MAX | | 100 | 150 | |
| | | Am73/8308 | $\overline{T}$ = $\overline{R}$ = 2.0V, $V_I$ = 0.4V, $V_{CC}$ = MAX | | 70 | 100 | mA |
| | | | $\overline{T}$ = $V_{INA}$ = 0.4V, $\overline{R}$ = 2.0V, $V_{CC}$ = MAX | | 90 | 140 | |

## AC ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5.0V, $T_A$ = 25°C)

| Parameter | Description | Test Conditions | Typ | Max | Units |
|---|---|---|---|---|---|
| **A PORT DATA/MODE SPECIFICATIONS** | | | | | |
| $t_{PDHLA}$ | Propagation Delay to a Logical "0" from B Port to A Port | $\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A)<br>$R_1$ = 1k, $R_2$ = 5k, $C_1$ = 30pF | 8 | 12 | ns |
| $t_{PDLHA}$ | Propagation Delay to a Logical "1" from B Port to A Port | $\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A)<br>$R_1$ = 1k, $R_2$ = 5k, $C_1$ = 30pF | 11 | 16 | ns |
| $t_{PLZA}$ | Propagation Delay from a Logical "0" to 3-State from $\overline{R}$ to A Port | $B_0$ to $B_7$ = 2.4V, $\overline{T}$ = 2.4V (Figure B)<br>$S_3$ = 1, $R_5$ = 1k, $C_4$ = 15pF | 10 | 15 | ns |
| $t_{PHZA}$ | Propagation Delay from a Logical "1" to 3-State from $\overline{R}$ to A Port | $B_0$ to $B_7$ = 0.4V, $\overline{T}$ = 2.4V (Figure B)<br>$S_3$ = 0, $R_5$ = 1k, $C_4$ = 15pF | 8 | 15 | ns |
| $t_{PZLA}$ | Propagation Delay from 3-State to a Logical "0" from $\overline{R}$ to A Port | $B_0$ to $B_7$ = 2.4V, $\overline{T}$ = 2.4V (Figure B)<br>$S_3$ = 1, $R_5$ = 1k, $C_4$ = 30pF | 25 | 35 | ns |
| $t_{PZHA}$ | Propagation Delay from 3-State to a Logical "1" from $\overline{R}$ to A Port | $B_0$ to $B_7$ = 0.4V, $\overline{T}$ = 2.4V (Figure B)<br>$S_3$ = 0, $R_5$ = 5k, $C_4$ = 30pF | 24 | 35 | ns |
| **B PORT DATA/MODE SPECIFICATIONS** | | | | | |
| $t_{PDHLB}$ | Propagation Delay to a Logical "0" from A Port to B Port | $\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A)<br>$R_1$ = 100Ω, $R_2$ = 1k, $C_1$ = 300pF | 12 | 18 | ns |
| | | $R_1$ = 667Ω, $R_2$ = 5k, $C_1$ = 45pF | 8 | 12 | ns |
| $t_{PDLHB}$ | Propagation Delay to a Logical "1" from A Port to B Port | $\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A)<br>$R_1$ = 100Ω, $R_2$ = 1k, $C_1$ = 300pF | 15 | 23 | ns |
| | | $R_1$ = 667Ω, $R_2$ = 5k, $C_1$ = 45pF | 9 | 14 | ns |
| $t_{PLZB}$ | Propagation Delay from a Logical "0" to 3-State from $\overline{T}$ to B Port | $A_0$ to $A_7$ = 2.4V, $\overline{R}$ = 2.4V (Figure B)<br>$S_3$ = 1, $R_5$ = 1k, $C_4$ = 15pF | 13 | 18 | ns |
| $t_{PHZB}$ | Propagation Delay from a Logical "1" to 3-State from $\overline{T}$ to B Port | $A_0$ to $A_7$ = 0.4V, $\overline{R}$ = 2.4V (Figure B)<br>$S_3$ = 0, $R_5$ = 1k, $C_4$ = 15pF | 8 | 15 | ns |
| $t_{PZLB}$ | Propagation Delay from 3-State to a Logical "0" from $\overline{T}$ to B Port | $A_0$ to $A_7$ = 2.4V, $\overline{R}$ = 2.4V (Figure B)<br>$S_3$ = 1, $R_5$ = 100Ω, $C_4$ = 300pF | 32 | 40 | ns |
| | | $S_3$ = 1, $R_5$ = 667Ω, $C_4$ = 45pF | 18 | 25 | ns |
| $t_{PZHB}$ | Propagation Delay from 3-State to a Logical "1" from $\overline{T}$ to B Port | $A_0$ to $A_7$ = 0.4V, $\overline{R}$ = 2.4V (Figure B)<br>$S_3$ = 0, $R_5$ = 1k, $C_4$ = 300pF | 25 | 35 | ns |
| | | $S_3$ = 0, $R_5$ = 5k, $C_4$ = 45pF | 16 | 25 | ns |

### FUNCTION TABLE

| Control Inputs | | Resulting Conditions | |
|---|---|---|---|
| $\overline{\text{Transmit}}$ | $\overline{\text{Receive}}$ | A Port | B Port |
| 1 | 0 | Out | In |
| 0 | 1 | In | Out |
| 1 | 1 | 3-State | 3-State |
| 0 | 0 | Both Active* | |

*This is not an intended logic condition and may cause oscillations.

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## AC ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5.0V, $T_A$ = 25°C)

| Parameter | Description | Test Conditions | Typ | Max | Units |
|---|---|---|---|---|---|
| **A PORT DATA/MODE SPECIFICATIONS** | | | | | |
| $t_{PDHLA}$ | Propagation Delay to a Logical "0" from B Port to A Port | $\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A)<br>$R_1$ = 1k, $R_2$ = 5k, $C_1$ = 30pF | 14 | 18 | ns |
| $t_{PDLHA}$ | Propagation Delay to a Logical "1" from B Port to A Port | $\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A)<br>$R_1$ = 1k, $R_2$ = 5k, $C_1$ = 30pF | 13 | 18 | ns |
| $t_{PLZA}$ | Propagation Delay from a Logical "0" to 3-State from $\overline{R}$ to A Port | $B_0$ to $B_7$ = 0.4V, $\overline{T}$ = 2.4V (Figure B)<br>$S_3$ = 1, $R_5$ = 1k, $C_4$ = 15pF | 11 | 15 | ns |
| $t_{PHZA}$ | Propagation Delay from a Logical "1" to 3-State from $\overline{R}$ to A Port | $B_0$ to $B_7$ = 2.4V, $\overline{T}$ = 2.4V (Figure B)<br>$S_3$ = 0, $R_5$ = 1k, $C_4$ = 15pF | 8 | 15 | ns |
| $t_{PZLA}$ | Propagation Delay from 3-State to a Logical "0" from $\overline{R}$ to A Port | $B_0$ to $B_7$ = 0.4V, $\overline{T}$ = 2.4V (Figure B)<br>$S_3$ = 1, $R_5$ = 1k, $C_4$ = 30pF | 24 | 35 | ns |
| $t_{PZHA}$ | Propagation Delay from 3-State to a Logical "1" from $\overline{R}$ to A Port | $B_0$ to $B_7$ = 2.4V, $\overline{T}$ = 2.4V (Figure B)<br>$S_3$ = 0, $R_5$ = 5k, $C_4$ = 30pF | 21 | 30 | ns |
| **B PORT DATA/MODE SPECIFICATIONS** | | | | | |
| $t_{PDHLB}$ | Propagation Delay to a Logical "0" from A Port to B Port | $\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A)<br>$R_1$ = 100Ω, $R_2$ = 1k, $C_1$ = 300pF | 18 | 23 | ns |
| | | $R_1$ = 667Ω, $R_2$ = 5k, $C_1$ = 45pF | 11 | 18 | ns |
| $t_{PDLHB}$ | Propagation Delay to a Logical "1" from A Port to B Port | $\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A)<br>$R_1$ = 100Ω, $R_2$ = 1k, $C_1$ = 300pF | 16 | 23 | ns |
| | | $R_1$ = 667Ω, $R_2$ = 5k, $C_1$ = 45pF | 11 | 18 | ns |
| $t_{PLZB}$ | Propagation Delay from a Logical "0" to 3-State from $\overline{T}$ to B Port | $A_0$ to $A_7$ = 0.4V, $\overline{R}$ = 2.4V (Figure B)<br>$S_3$ = 1, $R_5$ = 1k, $C_4$ = 15pF | 13 | 18 | ns |
| $t_{PHZB}$ | Propagation Delay from a Logical "1" to 3-State from $\overline{T}$ to B Port | $A_0$ to $A_7$ = 2.4V, $\overline{R}$ = 2.4V (Figure B)<br>$S_3$ = 0, $R_5$ = 1k, $C_4$ = 15pF | 8 | 15 | ns |
| $t_{PZLB}$ | Propagation Delay from 3-State to a Logical "0" from $\overline{T}$ to B Port | $A_0$ to $A_7$ = 0.4V, $\overline{R}$ = 2.4V (Figure B)<br>$S_3$ = 1, $R_5$ = 100Ω, $C_4$ = 300pF | 25 | 35 | ns |
| | | $S_3$ = 1, $R_5$ = 667Ω, $C_4$ = 45pF | 17 | 25 | ns |
| $t_{PZHB}$ | Propagation Delay from 3-State to a Logical "1" from $\overline{T}$ to B Port | $A_0$ to $A_7$ = 2.4V, $\overline{R}$ = 2.4V (Figure B)<br>$S_3$ = 0, $R_5$ = 1k, $C_4$ = 300pF | 24 | 35 | ns |
| | | $S_3$ = 0, $R_5$ = 5k, $C_4$ = 45pF | 17 | 25 | ns |

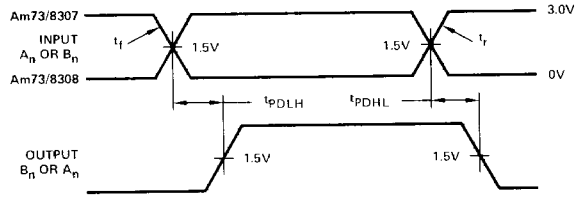
### DEFINITION OF FUNCTIONAL TERMS

**$A_0$-$A_7$** A port inputs/outputs are receiver output drivers when $\overline{Receive}$ is LOW and $\overline{Transmit}$ is HIGH, and are transmit inputs when $\overline{Receive}$ is HIGH and $\overline{Transmit}$ is LOW.

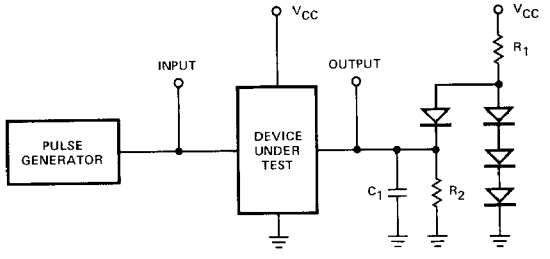
**$B_0$-$B_7$** B port inputs/outputs are transmit output drivers when $\overline{Transmit}$ is LOW and $\overline{Receive}$ is HIGH, and are receiver inputs when $\overline{Transmit}$ is HIGH and $\overline{Receive}$ is LOW.

**$\overline{Transmit}$, $\overline{Receive}$** These controls determine whether A port and B port drivers are in 3-state. With both $\overline{Transmit}$ and $\overline{Receive}$ HIGH both ports are in 3-state. $\overline{Transmit}$ and $\overline{Receive}$ both LOW activate both drivers and may cause oscillations. This is not an intended logic condition. With $\overline{Transmit}$ HIGH and $\overline{Receive}$ LOW A port is the output and B port is the input. With $\overline{Transmit}$ LOW and $\overline{Receive}$ HIGH B port is the output and A port is the input.

## SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS

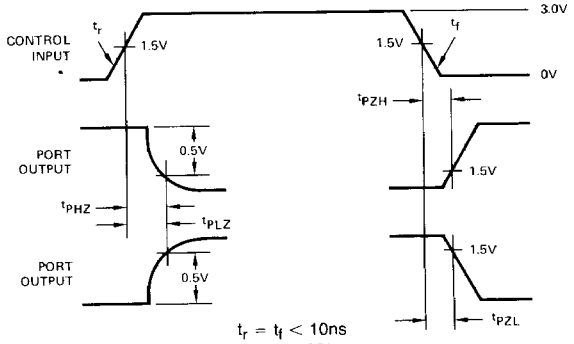



$t_r = t_f < 10ns$
10% to 90%

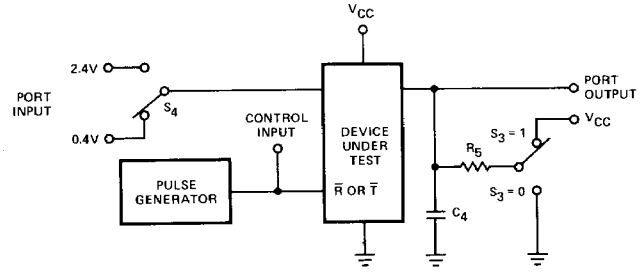



Note: $C_1$ includes test fixture capacitance.

**Figure A. Propagation Delay from A Port to B Port or from B Port to A Port**




$t_r = t_f < 10ns$
10% to 90%




Note: $C_4$ includes test fixture capacitance. Port input is in a fixed logical condition. See AC table.

**Figure B. Propagation Delay to/from Three-State from $\overline{R}$ to A Port and $\overline{T}$ to B Port**

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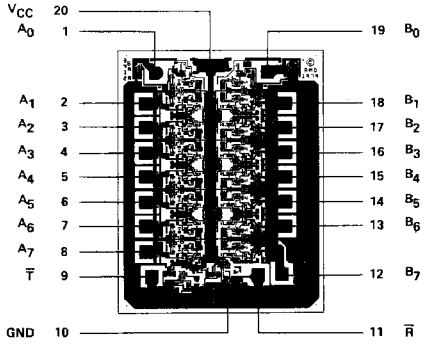
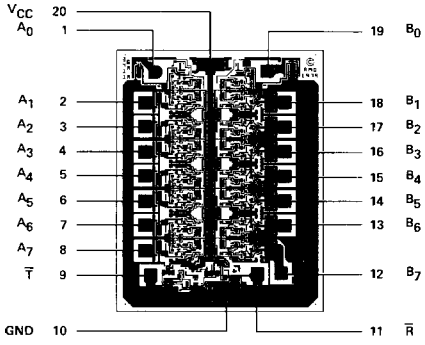
## Metallization and Pad Layouts

### Am73/8307




DIE SIZE .069" X .089"

### Am73/8308




DIE SIZE .069" X .089"

## ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

| Am73/8307 Order Number | Am73/8308 Order Number | Package Type (Note 1) | Operating Range (Note 2) | Screening Level (Note 3) |
|---|---|---|---|---|
| DP7307J | DP7308J | D-20 | M | C-3 |
| DP7307JB | DP7308JB | D-20 | M | B-3 |
| DP8307J | DP8308J | D-20 | C | C-1 |
| DP8307JB | DP8308JB | D-20 | C | B-1 |
| DP8307N | DP8308N | P-20 | C | C-1 |
| DP8307NB | DP8308NB | P-20 | C | B-1 |
| AM7307X | AM7308X | Dice | M | Visual Inspection to MIL-STD-883 Method 20103 |
| AM8307X | AM8308X | Dice | C | |

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flatpack. Number following letter is number of leads.
2. C = 0 to 70°C, $V_{CC}$ = 4.75 to 5.25V, M = −55 to +125°C, $V_{CC}$ = 4.50 to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.