

VQ7254 SERIES



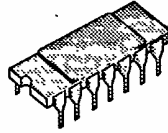
N- and P-Channel Enhancement-Mode MOS Transistor Arrays

T-43-25

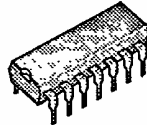
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ $Q_1 + Q_2$ or $Q_3 + Q_4$	I_D (A)	PACKAGE
VQ7254J	20/-20	3 Ω	2	Plastic
VQ7254P	20/-20	3 Ω	2	Side Braze

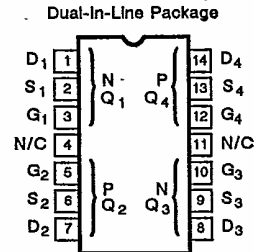
14-PIN DIP
SIDE BRAZE



14-PIN PLASTIC



TOP VIEW



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

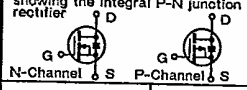
PARAMETERS/TEST CONDITIONS	SYMBOL	VQ7254J		VQ7254P		UNITS	
		N-Channel	P-Channel	N-Channel	P-Channel		
Drain-Source Voltage	V_{DS}	20	-20	20	-20	V	
Gate-Source Voltage	V_{GS}	± 30	± 30	± 20	± 20	V	
Continuous Drain Current ($T_A = 25^\circ\text{C}$)	I_D	2	-2	2	-2	A	
Pulsed Drain Current ¹	I_{DM}	± 3	± 3	± 3	± 3	A	
Power Dissipation - Single	P_D	$T_A = 25^\circ\text{C}$	1.75	1.75	1.75	1.75	W
		$T_A = 80^\circ\text{C}$	1.05	1.05	1.05	1.05	
Operating Junction	T_j	-40 to 100				°C	
Storage Temperature	T_{stg}	-40 to 150					
Lead Temperature (1/16" from case for 10 seconds)	T_L	300					
Thermal Coupling Factor - Single (K) - $Q_1 - Q_4$ or $Q_2 - Q_3$		60				%	
Thermal Coupling Factor - Single (K) - $Q_1 - Q_2 - Q_3 - Q_4$, $Q_1 - Q_3$ or $Q_2 - Q_4$		50					

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VQ7254J	VQ7254P	UNITS
Junction-to-Ambient - Single	R_{thJA}	96.2	96.2	°C/W
Junction-to-Ambient - Quad		62.5	62.5	

¹Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS ¹			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS ⁶	VQ7254			UNIT
			TYP ²	MIN	MAX	
STATIC⁴						
Drain-Source On Voltage	V _{DS(ON)}	V _{GS} = 11.4 V, I _D = 1 A (Q ₁ + Q ₂) or (Q ₃ + Q ₄)	2.5	2	3	V
Drain-Source On-Resistance ³	r _{DS(ON)}		2.5	2	3	Ω

PARAMETER	SYMBOL	TEST CONDITIONS ⁶	N-Channel			P-Channel			UNIT
			TYP ²	MIN	MAX	TYP ²	MIN	MAX	
STATIC									
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 10 μA	-40	20		-55	-20		V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} I _D = 1 mA T _J = 85°C	1.5	0.8		-3.6	-0.8		
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±12 V	±1		±100	±1		±100	nA
Zero-Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	0.1		500	-0.1		-500	μA
On-State Drain Current ³	I _{D(ON)}	V _{DS} = 10 V, V _{GS} = 10 V	1.8			-1.6			A
Forward Transconductance ³	g _{FS}	V _{DS} = 10 V, I _D = 0.5 A	500	200		290	200		mS
DYNAMIC									
Input Capacitance	C _{iss}	V _{DS} = 12 V V _{GS} = 0 V f = 1 MHz	85		175	130		190	pF
Output Capacitance	C _{oss}		80		95	75		100	
Reverse Transfer Capacitance	C _{rss}		18		25	20		60	
SWITCHING⁵									
Turn-On Time	t _{ON}	V _{DD} = 17 V, R _L = 15 Ω I _D = 1.1 A, V _{GEN} = 10 V R _G = 25 Ω	12		20	20		30	ns
Turn-Off Time	t _{OFF}		14		20	20		30	
DYNAMIC									
Continuous Source Current (Body Diode)	I _S	Modified MOSPOWER symbol showing the integral P-N junction rectifier  N-Channel P-Channel			2			-2	A
Source Current (Body Diode)	I _{SM}				3			-3	
Diode Forward Voltage	V _{SD}		V _{GS} = 0 V T _C = 25°C	I _S = 50 mA 0.6		0.75	-0.6		-0.75
		I _S = 1 A	1		1.2	-1		-1.2	

- NOTES: 1. T_A = 25 °C unless otherwise noted.
 2. For design aid only, not subject to production testing.
 3. Pulse test; PW = 300 μs, duty cycle ≤ 2%.
 4. r_{DS(ON)} and V_{DS(ON)} limits are not specified for individual transistors but are measured as the sum of a n- and p-channel pair.
 5. Switching time is essentially independent of operating temperature.
 6. Reverse polarity for p-channel devices.

6