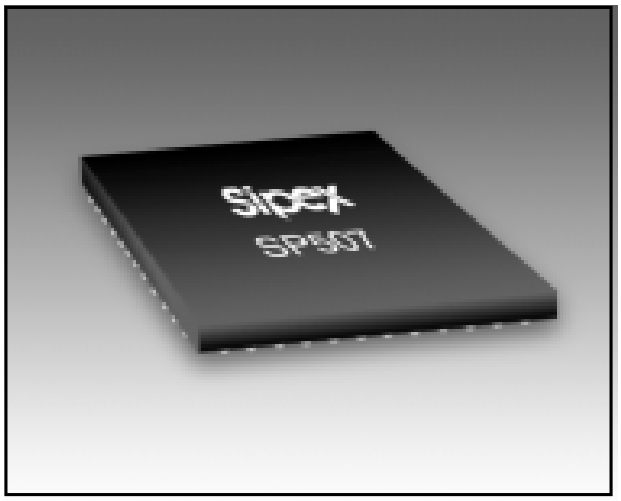
+5V, Single Chip WAN Multi-Mode Serial Transceiver

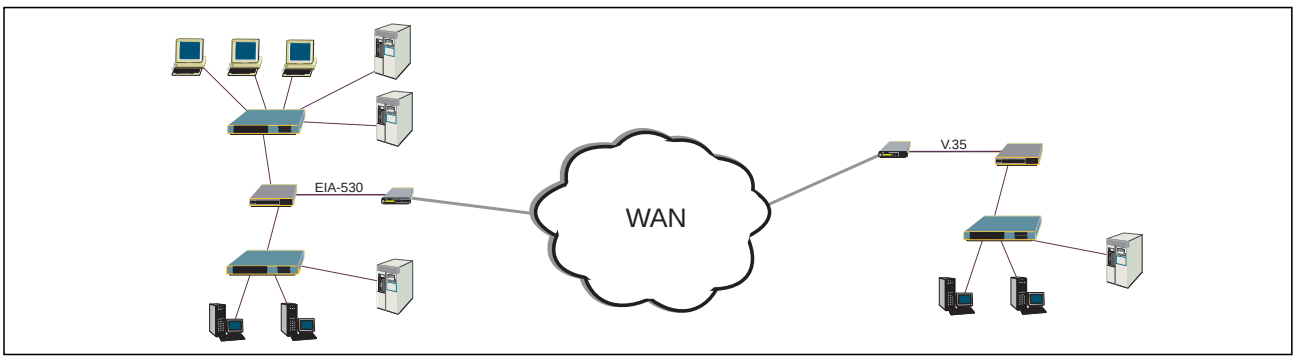
- Interface Modes Supported:
  - ✓ RS-232 **(V.28)**
  - ✓ X.21/RS-422 **(V.11)**
  - ✓ EIA-530 **(V.10 & V.11)**
  - ✓ EIA-530A **(V.10 & V.11)**
  - ✓ RS-449 **(V.10 & V.11)**
  - ✓ V.35 **(V.35 & V.28)**
- Software Selectable Protocols
- Highest Differential Transmission Rates available at over 20Mbps
- +5V Only Operation
- Seven (7) Drivers and Seven (7) Receivers
- Driver and Receiver Tri-state Control
- Internal Transceiver Termination Resistors for V.11 and V.35 Protocols
- Improved ESD Tolerance for Analog I/Os
- Compliant to NET1/2 and TBR2 Physical Layer Requirements
- Used in WAN Serial Ports in Routers Switches, DSU/CSU's and other Access Devices
- Available in small scale ball grid array and 80L QFP



DESCRIPTION

The **SP507** is a monolithic IC that supports seven (7) popular serial interface standards for DTE/DCE connectivity. The seven (7) drivers and seven (7) receivers transmit and receive signals at over 20Mbps. The **SP507** requires no additional external components for compliant operation for all seven (7) modes of operation. All necessary termination is integrated within the **SP507** and is switchable when V.35 drivers, V.35 receivers, and V.11 receivers are used. The **SP507** can operate as either a DTE or DCE.

Additional features include a latch enable pin with the driver and receiver address decoder. Tri-state ability for the driver and receiver outputs is controlled by supplying a 3-bit word into the address decoder. Four (4) drivers and four (4) receivers in the **SP507** include separate enable pins for added convenience.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC}.....+7V
Input Voltages:
Logic.....-0.3V to (V_{CC}+0.5V)
Drivers.....-0.3V to (V_{CC}+0.5V)
Receivers.....±15.5V
Output Voltages:
Logic.....-0.3V to (V_{CC}+0.5V)
Drivers.....±15V
Receivers.....-0.3V to (V_{CC}+0.5V)
Storage Temperature.....-65˚C to +150˚C
Power Dissipation per package
80-pin QFP (derate 18.3mW/˚C above +70˚C)...1500mW

STORAGE CONSIDERATIONS

Due to the relatively large package size of the 80-pin quad flat-pack, storage in a low humidity environment is preferred. Large high density plastic packages are moisture sensitive and should be stored in Dry Vapor Barrier Bags. Prior to usage, the parts should remain bagged and stored below 40°C and 60%RH. If the parts are removed from the bag, they should be used within 48 hours or stored in an environment at or below 20%RH. If the above conditions cannot be followed, the parts should be baked for four hours at 125°C in order remove moisture prior to soldering. Sipex ships the 80-pin QFP in Dry Vapor Barrier Bags with a humidity indicator card and desiccant pack. The humidity indicator should be below 30%RH.

SPECIFICATIONS

T_A = +25°C and V_{CC} = +4.75V to +5.25V unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
LOGIC INPUTS					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
LOGIC OUTPUTS					
V_{OL}			0.4	Volts	I_{OUT}= –3.2mA
V_{OH}	2.4			Volts	I_{OUT}= 1.0mA
V.28 DRIVER					
DC Parameters					
Outputs					
Open Circuit Voltage			±15	Volts	per Figure 1
Loaded Voltage	±5.0		±15	Volts	per Figure 2
Short-Circuit Current			±100	mA	per Figure 4
Power-Off Impedance	300			Ω	per Figure 5
AC Parameters					**V_{CC} = +5V for AC parameters**
Outputs					
Transition Time			1.5	µs	per Figure 6; +3V to -3V
Instantaneous Slew Rate			30	V/µs	per Figure 3
Propagation Delay					
t_{PHL}	0.5	1	5	µs	
t_{PLH}	0.5	1	5	µs	
Max. Transmission Rate	120	230		kbps	
V.28 RECEIVER					
DC Parameters					
Inputs					
Input Impedance	3		7	kΩ	per Figure 7
Open-Circuit Bias			+2.0	Volts	per Figure 8
HIGH Threshold		1.7	3.0	Volts	
LOW Threshold	0.8	1.2		Volts	
AC Parameters					**V_{CC} = +5V for AC parameters**
Propagation Delay					
t_{PHL}	50	100	500	ns	
t_{PLH}	50	100	500	ns	

SPECIFICATIONS

T_A = +25°C and V_{CC} = +4.75V to +5.25V unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V.28 RECEIVER (continued)					
AC Parameters (cont.)					
Max.Transmission Rate	120	230		kbps	
V.10 DRIVER					
DC Parameters					
Outputs					
Open Circuit Voltage	±4.0		±6.0	Volts	per Figure 9
Test-Terminated Voltage	$0.9V_{OC}$			Volts	per Figure 10
Short-Circuit Current			±150	mA	per Figure 11
Power-Off Current			±100	µA	per Figure 12
AC Parameters					**V_{CC} = +5V for AC parameters**
Outputs					
Transition Time			200	ns	per Figure 13; 10% to 90%
Propagation Delay					
t_{PHL}	50	100	500	ns	
t_{PLH}	50	100	500	ns	
Max.Transmission Rate	120			kbps	
V.10 RECEIVER					
DC Parameters					
Inputs					
Input Current	–3.25		+3.25	mA	per Figures 14 and 15
Input Impedance	4			kΩ	
Sensitivity			±0.3	Volts	
AC Parameters					**V_{CC} = +5V for AC parameters**
Propagation Delay					
t_{PHL}	50	120	250	ns	
t_{PLH}	50	120	250	ns	
Max.Transmission Rate	120			kbps	
V.11 DRIVER					
DC Parameters					
Outputs					
Open Circuit Voltage			±5.0	Volts	per Figure 16
Test Terminated Voltage	±2.0			Volts	per Figure 17
	$0.5V_{OC}$		$0.67V_{OC}$	Volts	
Balance			±0.4	Volts	per Figure 17
Offset			+3.0	Volts	per Figure 17
Short-Circuit Current			±150	mA	per Figure 18
Power-Off Current			±100	µA	per Figure 19
AC Parameters					**V_{CC} = +5V for AC parameters**
Outputs					
Transition Time			20	ns	per Figures 21 and 36; 10% to 90%
Propagation Delay					
t_{PHL}	50	65	85	ns	per Figures 33 and 36, C_L = 50pF
t_{PLH}	50	65	85	ns	per Figures 33 and 36, C_L = 50pF
Differential Skew		10	20	ns	per Figures 33 and 36, C_L = 50pF
Max.Transmission Rate	20			Mbps	per Figure 33, C_L = 50pF f_{IN} = 10MHz
V.11 RECEIVER					
DC Parameters					
Inputs					
Common Mode Range	–7		+7	Volts	
Sensitivity			±0.3	Volts	

SPECIFICATIONS

T_A = +25°C and V_{CC} = +4.75V to +5.25V unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V.11 RECEIVER (continued)					
DC Parameters (cont.)					
Input Current	–3.25		±3.25	mA	per Figure 20 and 22
Current w/ 100Ω Termination			±60.75	mA	per Figure 23 and 24
Input Impedance	4			kΩ	
AC Parameters					**V_{CC} = +5V for AC parameters**
Propagation Delay					
t_{PHL}	30	65	85	ns	per Figures 33 and 38; C_L = 50pF
t_{PLH}	30	65	85	ns	per Figures 33 and 38; C_L = 50pF
Differential Skew		10		ns	per Figure 33; C_L = 50pF
Max.Transmission Rate	20			Mbps	per Figure 33; C_L = 50pF f_{IN} = 10MHz
V.35 DRIVER					
DC Parameters					
Outputs					
Open Circuit Voltage			±1.20	Volts	per Figure 16
Test Terminated Voltage	±0.44		±0.66	Volts	per Figure 25
Offset			±0.6	Volts	per Figure 25
Source Impedance	50		150	Ω	per Figure 27; $Z_S = V_2/V_1 \times 50\Omega$
Short-Circuit Impedance	135		165	Ω	per Figure 28
AC Parameters					**V_{CC} = +5V for AC parameters**
Outputs					
Transition Time		30	40	ns	per Figure 29; 10% to 90%
Propagation Delay					
t_{PHL}	50	70	90	ns	per Figures 33 and 36; C_L = 20pF
t_{PLH}	50	70	90	ns	per Figures 33 and 36; C_L = 20pF
Differential Skew		7	10	ns	per Figures 33 and 36; C_L = 20pF
Max.Transmission Rate	20			Mbps	per Figure 33; C_L = 20pF f_{IN} = 10MHz
V.35 RECEIVER					
DC Parameters					
Inputs					
Sensitivity		±80		mV	
Source Impedance	90		110	Ω	per Figure 30; $Z_S = V_2/V_1 \times 50\Omega$
Short-Circuit Impedance	135		165	Ω	per Figure 31
AC Parameters					**V_{CC} = +5V for AC parameters**
Propagation Delay					
t_{PHL}	30	75	90	ns	per Figures 33 and 38; C_L = 20pF
t_{PLH}	30	75	90	ns	per Figures 33 and 38; C_L = 20pF
Differential Skew		10		ns	per Figure 33; C_L = 20pF
Max.Transmission Rate	20			Mbps	per Figure 33; C_L = 20pF f_{IN} = 10MHz
TRANSCEIVER LEAKAGE CURRENTS					
Driver Output 3-State Current		500		µA	per Figure 32; Drivers disabled
Rcvr Output 3-State Current		1	10	µA	Mx = 111, 0.4V ≤ V_O ≤ 2.4V

OTHER AC CHARACTERISTICS

T_A = +25°C and V_{CC} = +5.0V unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER DELAY TIME BETWEEN ACTIVE MODE AND TRI-STATE MODE					
RS-232/V.28					
t_{PZL}; Tri-state to Output LOW		0.70	5.0	µs	C_L = 100pF, Fig. 34 & 40; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.40	2.0	µs	C_L = 100pF, Fig. 34 & 40; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.20	2.0	µs	C_L = 100pF, Fig. 34 & 40; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.40	2.0	µs	C_L = 100pF, Fig. 34 & 40; S_2 closed
RS-423/V.10					
t_{PZL}; Tri-state to Output LOW		0.15	2.0	µs	C_L = 100pF, Fig. 34 & 40; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.20	2.0	µs	C_L = 100pF, Fig. 34 & 40; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.20	2.0	µs	C_L = 100pF, Fig. 34 & 40; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.15	2.0	µs	C_L = 100pF, Fig. 34 & 40; S_2 closed
RS-422/V.11					
t_{PZL}; Tri-state to Output LOW		2.80	10.0	µs	C_L = 100pF, Fig. 34 & 37; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.10	2.0	µs	C_L = 100pF, Fig. 34 & 37; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.10	2.0	µs	C_L = 15pF, Fig. 34 & 37; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.10	2.0	µs	C_L = 15pF, Fig. 34 & 37; S_2 closed
V.35					
t_{PZL}; Tri-state to Output LOW		2.60	10.0	µs	C_L = 100pF, Fig. 34 & 37; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.10	2.0	µs	C_L = 100pF, Fig. 34 & 37; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.10	2.0	µs	C_L = 15pF, Fig. 34 & 37; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.15	2.0	µs	C_L = 15pF, Fig. 34 & 37; S_2 closed
RECEIVER DELAY TIME BETWEEN ACTIVE MODE AND TRI-STATE MODE					
RS-232/V.28					
t_{PZL}; Tri-state to Output LOW		0.12	2.0	µs	C_L = 100pF, Fig. 35 & 38; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.10	2.0	µs	C_L = 100pF, Fig. 35 & 38; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.10	2.0	µs	C_L = 100pF, Fig. 35 & 38; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.10	2.0	µs	C_L = 100pF, Fig. 35 & 38; S_2 closed
RS-423/V.10					
t_{PZL}; Tri-state to Output LOW		0.10	2.0	µs	C_L = 100pF, Fig. 35 & 38; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.10	2.0	µs	C_L = 100pF, Fig. 35 & 38; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.10	2.0	µs	C_L = 100pF, Fig. 35 & 38; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.10	2.0	µs	C_L = 100pF, Fig. 35 & 38; S_2 closed

OTHER AC CHARACTERISTICS (Continued)

T_A = +25°C and V_{CC} = +5.0V unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RS-422/V.11					
t_{PZL}; Tri-state to Output LOW		0.10	2.0	µs	C_L = 100pF, Fig. 35 & 39; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.10	2.0	µs	C_L = 100pF, Fig. 35 & 39; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.10	2.0	µs	C_L = 15pF, Fig. 35 & 39; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.10	2.0	µs	C_L = 15pF, Fig. 35 & 39; S_2 closed
V.35					
t_{PZL}; Tri-state to Output LOW		0.10	2.0	µs	C_L = 100pF, Fig. 35 & 39; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.10	2.0	µs	C_L = 100pF, Fig. 35 & 39; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.10	2.0	µs	C_L = 15pF, Fig. 35 & 39; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.10	2.0	µs	C_L = 15pF, Fig. 35 & 39; S_2 closed
TRANSCEIVER TO TRANSCEIVER SKEW					(per Figures 33, 36, 38)
V.28 Driver		100		ns	$[(t_{phl})_{Tx1} - (t_{phl})_{Tx6,7}]$
		100		ns	$[(t_{plh})_{Tx1} - (t_{plh})_{Tx6,7}]$
V.28 Receiver		20		ns	$[(t_{phl})_{Rx1} - (t_{phl})_{Rx2,7}]$
		20		ns	$[(t_{plh})_{Rx1} - (t_{phl})_{Rx2,7}]$
V.11 Driver		2		ns	$[(t_{phl})_{Tx1} - (t_{phl})_{Tx6,7}]$
		2		ns	$[(t_{plh})_{Tx1} - (t_{plh})_{Tx6,7}]$
V.11 Receiver		3		ns	$[(t_{phl})_{Rx1} - (t_{phl})_{Rx2,7}]$
		3		ns	$[(t_{plh})_{Rx1} - (t_{phl})_{Rx2,7}]$
V.10 Driver		5		ns	$[(t_{phl})_{Tx2} - (t_{phl})_{Tx3,4,5}]$
		5		ns	$[(t_{plh})_{Tx2} - (t_{plh})_{Tx3,4,5}]$
V.10 Receiver		5		ns	$[(t_{phl})_{Rx2} - (t_{phl})_{Rx3,4,5}]$
		5		ns	$[(t_{plh})_{Rx2} - (t_{phl})_{Rx3,4,5}]$
V.35 Driver		4		ns	$[(t_{phl})_{Tx1} - (t_{phl})_{Tx6,7}]$
		4		ns	$[(t_{plh})_{Tx1} - (t_{plh})_{Tx6,7}]$
V.35 Receiver		6		ns	$[(t_{phl})_{Rx1} - (t_{phl})_{Rx2,7}]$
		6		ns	$[(t_{plh})_{Rx1} - (t_{phl})_{Rx2,7}]$

POWER REQUIREMENTS

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{CC}	4.75	5.00	5.25	Volts	
I_{CC} (No Mode Selected)		30		mA	All I_{CC} values are with V_{CC} = +5V
(V.28/RS-232)		65		mA	f_{IN} = 120kbps; Drivers active & loaded.
(V.11/X.21)		175		mA	f_{IN} = 10Mbps; Drivers active & loaded.
(EIA-530 & RS-449)		250		mA	f_{IN} = 10Mbps; Drivers active & loaded.
(V.35)		100		mA	V.35 @ f_{IN} = 10Mbps, V.28 @ 120kbps; Drivers active & loaded.

TEST CIRCUITS

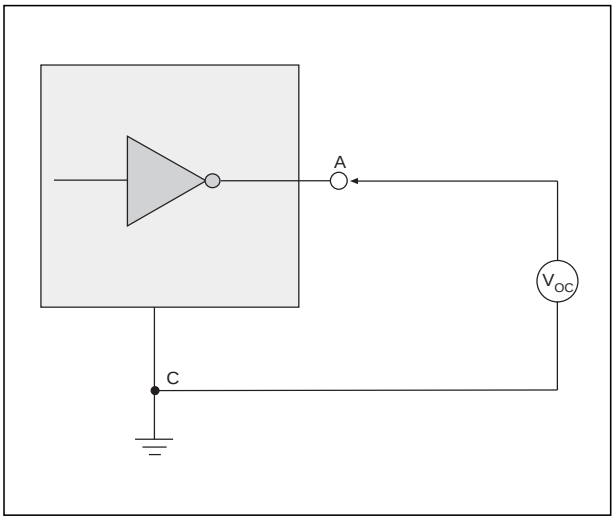


Figure 1. V.28 Driver Output Open Circuit Voltage

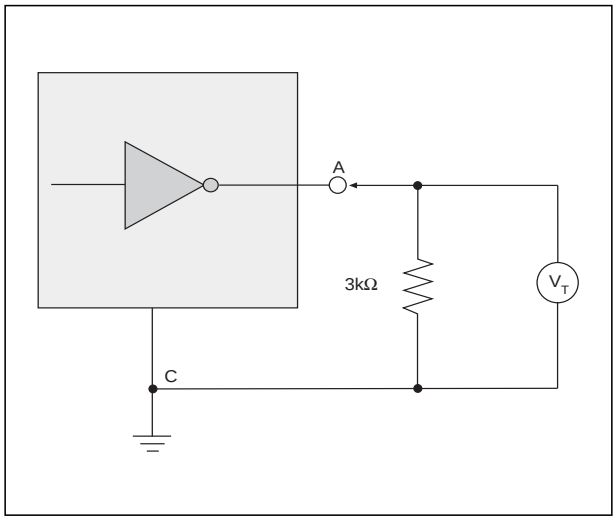


Figure 2. V.28 Driver Output Loaded Voltage

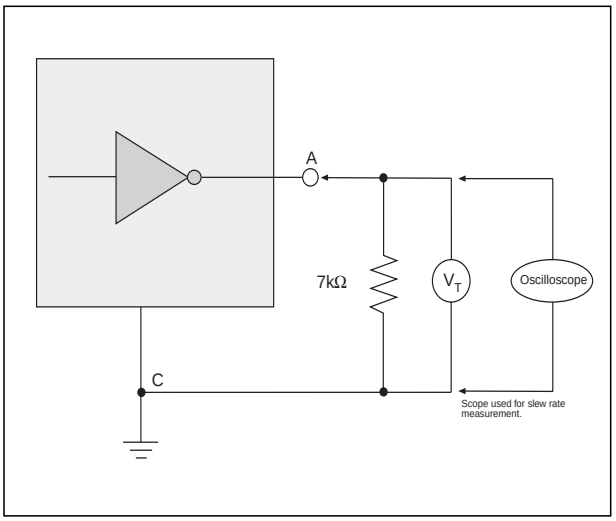


Figure 3. V.28 Driver Output Slew Rate

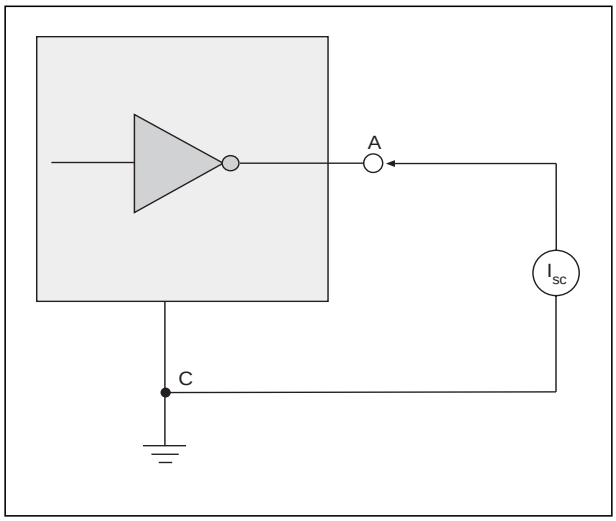


Figure 4. V.28 Driver Output Short-Circuit Current

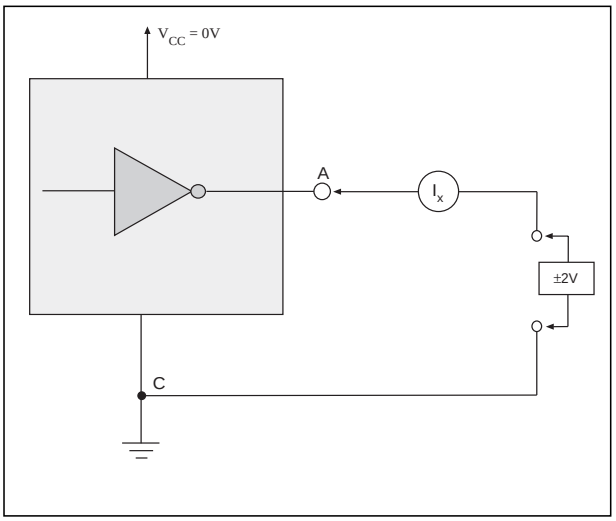


Figure 5. V.28 Driver Output Power-Off Impedance

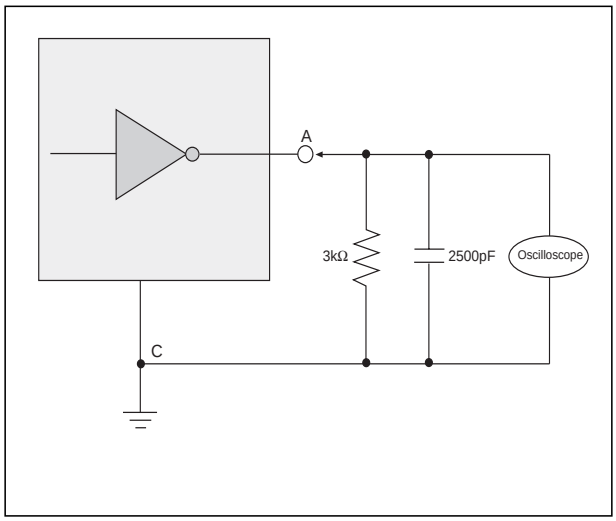


Figure 6. V.28 Driver Output Rise/Fall Times

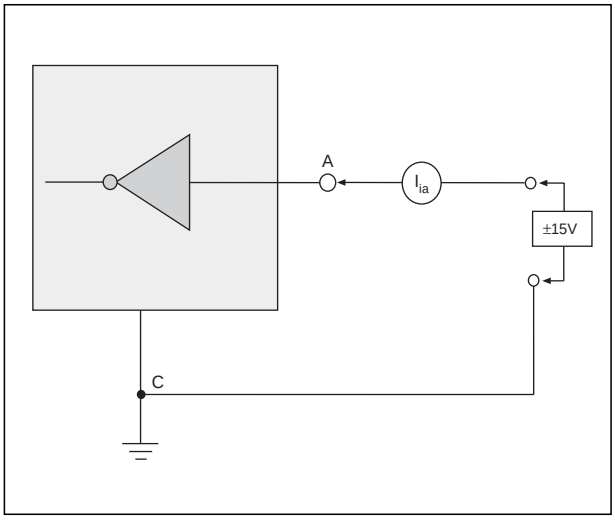


Figure 7. V.28 Receiver Input Impedance

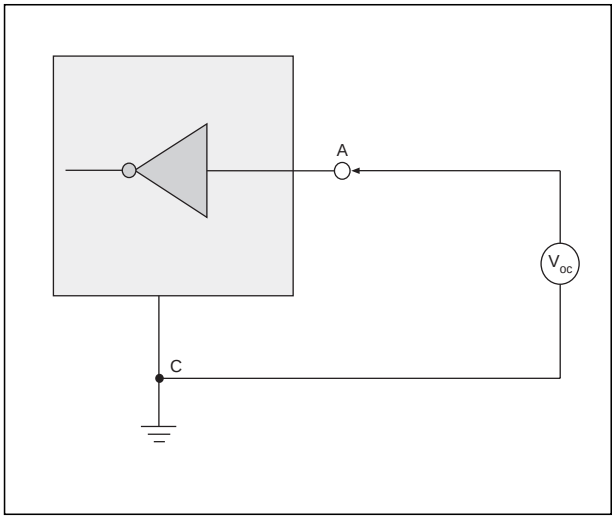


Figure 8. V.28 Receiver Input Open Circuit Bias

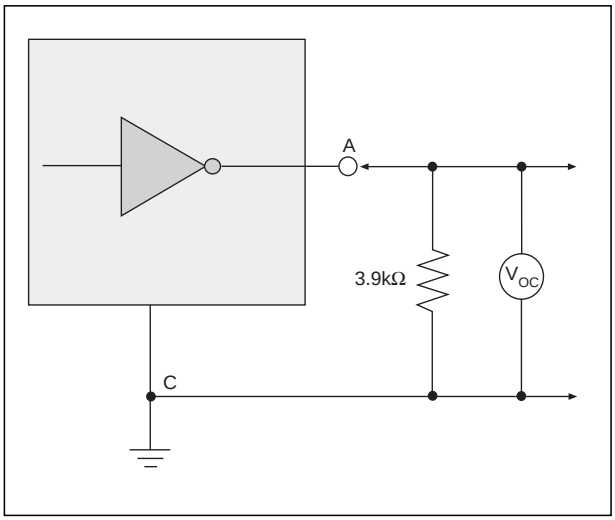


Figure 9. V.10 Driver Output Open-Circuit Voltage

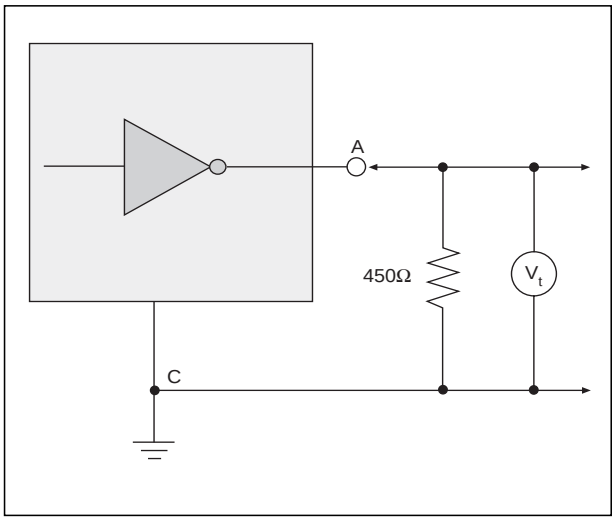


Figure 10. V.10 Driver Output Test Terminated Voltage

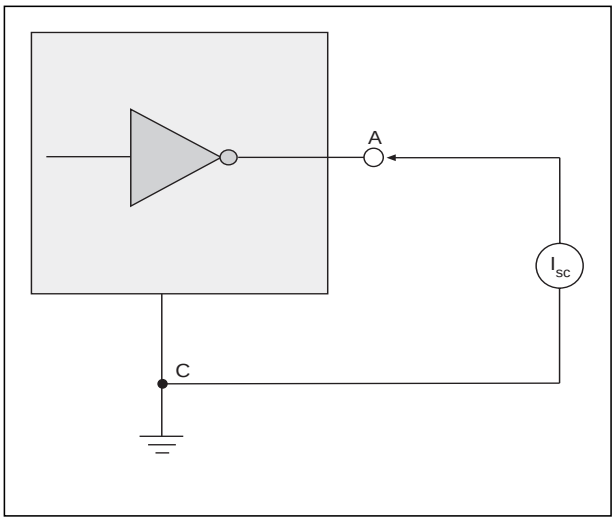


Figure 11. V.10 Driver Output Short-Circuit Current

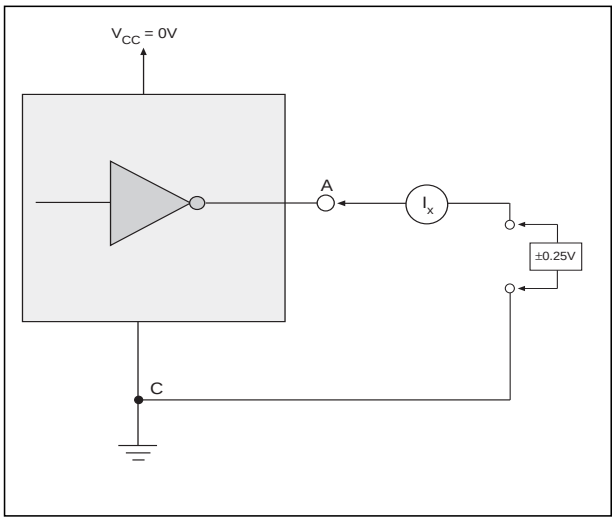


Figure 12. V.10 Driver Output Power-Off Current

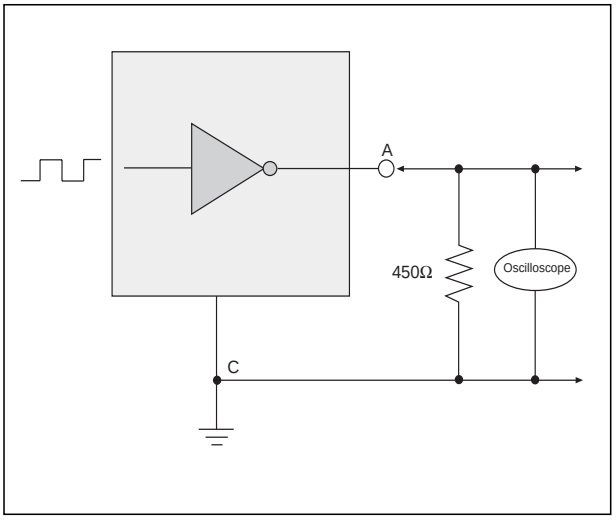


Figure 13. V.10 Driver Output Transition Time

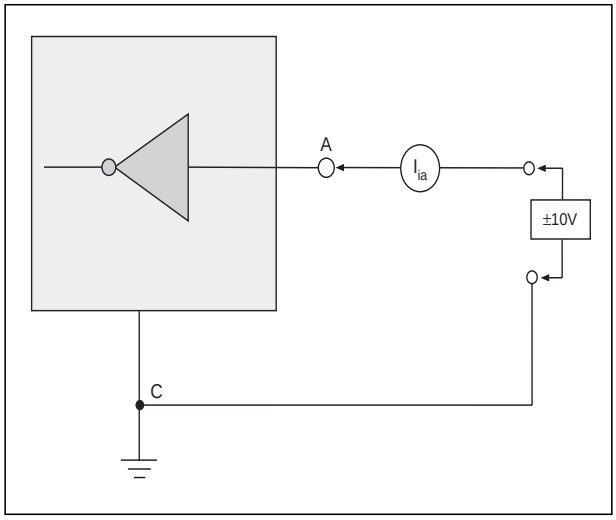


Figure 14. V.10 Receiver Input Current

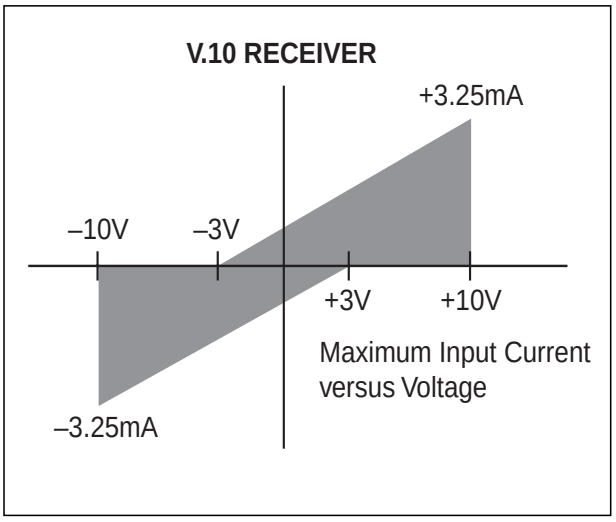


Figure 15. V.10 Receiver Input IV Graph

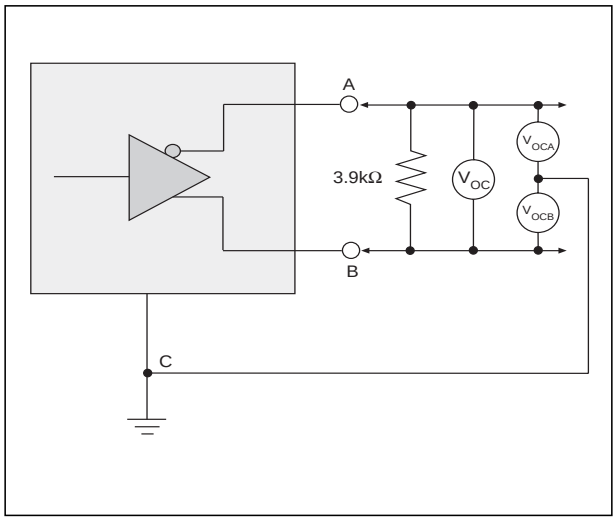


Figure 16. V.11 and V.35 Driver Output Open-Circuit Voltage

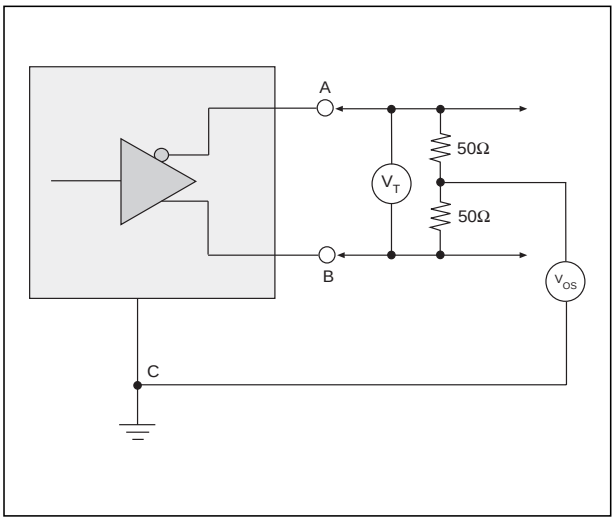


Figure 17. V.11 Driver Output Test Terminated Voltage

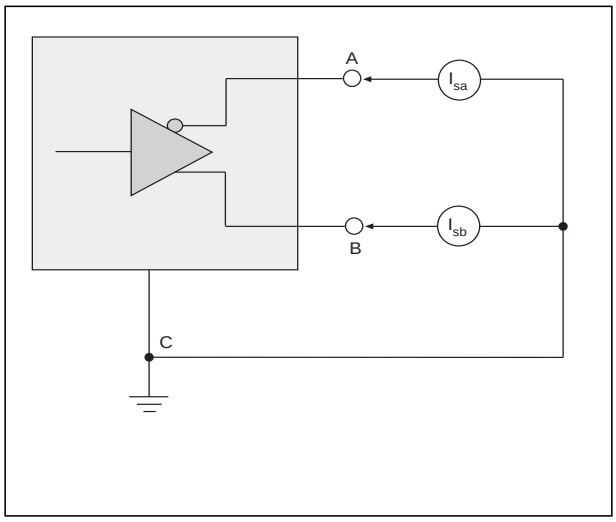


Figure 18. V.11 Driver Output Short-Circuit Current

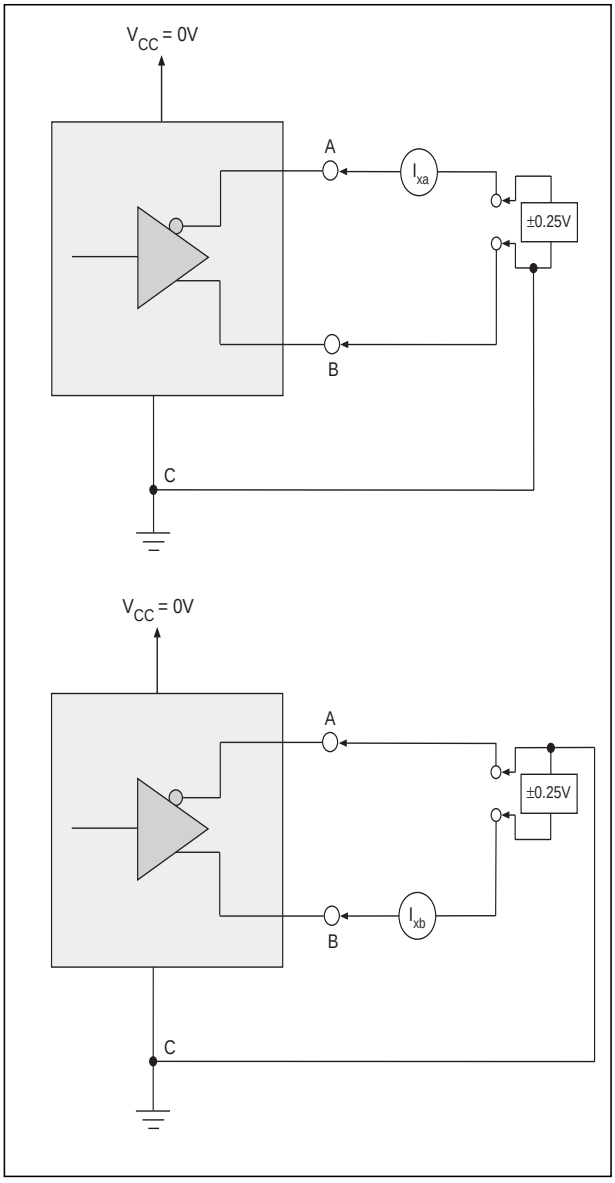


Figure 19. V.11 Driver Output Power-Off Current

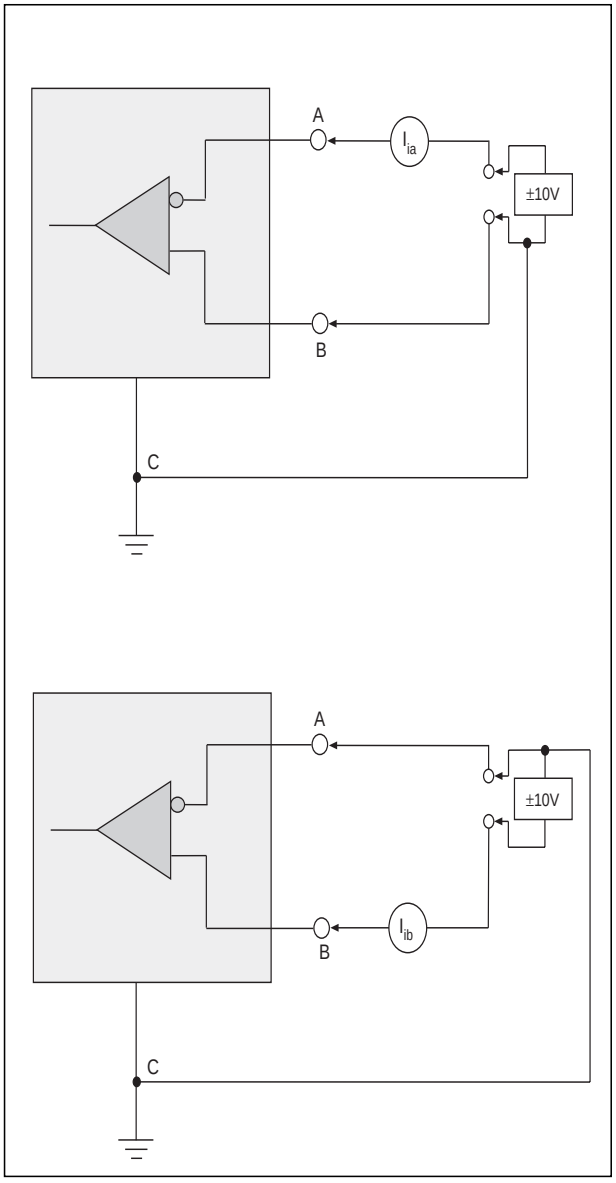


Figure 20. V.11 Receiver Input Current

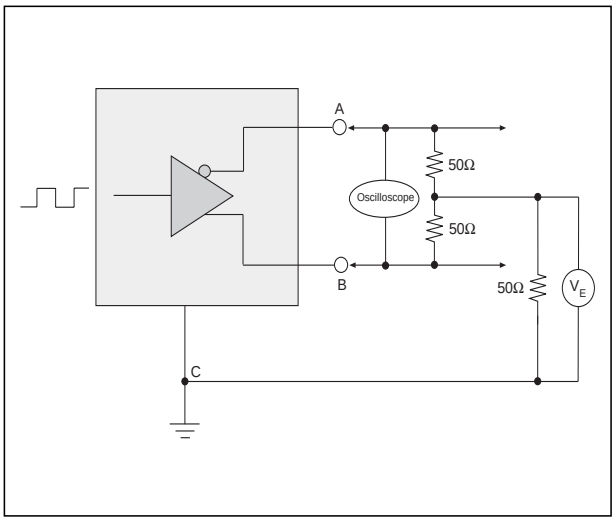


Figure 21. V.11 Driver Output Rise/Fall Time

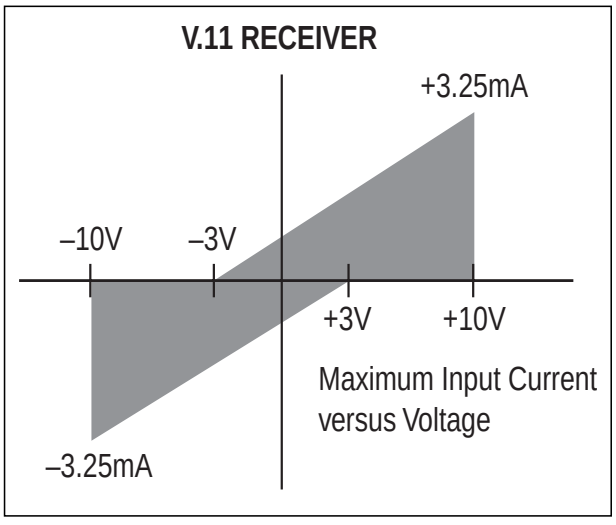


Figure 22. V.11 Receiver Input IV Graph

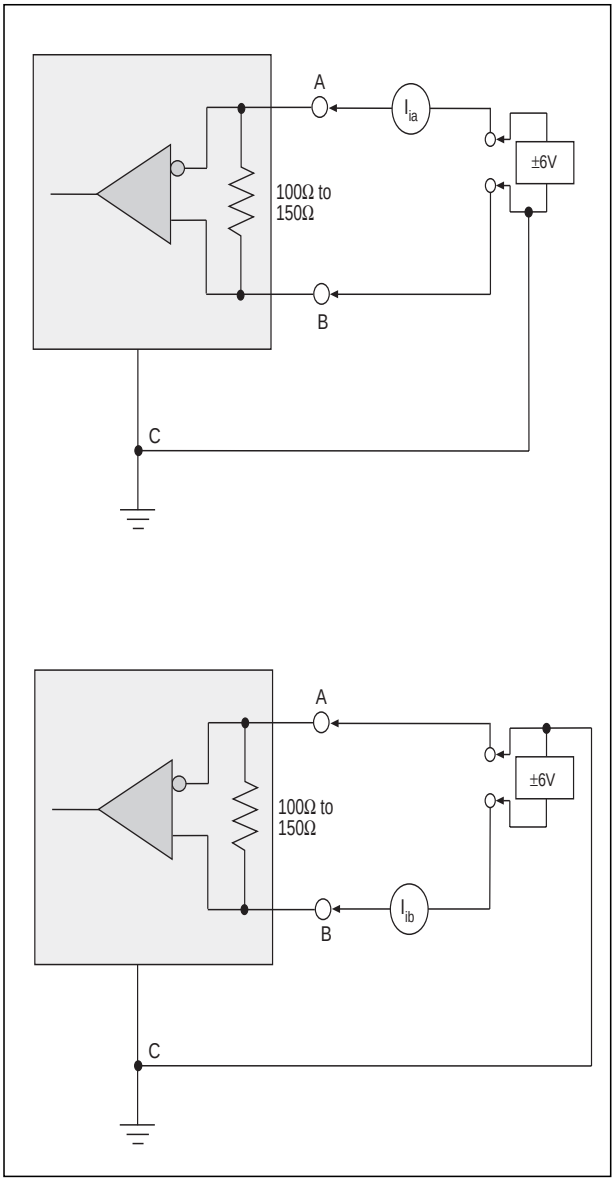


Figure 23. V.11 Receiver Input Current w/ Termination

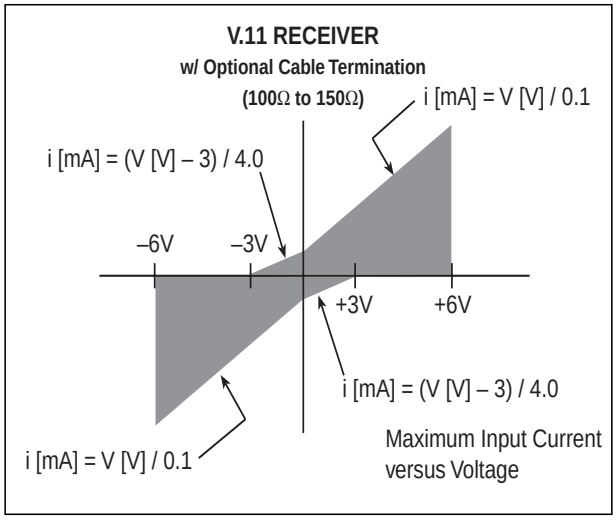


Figure 24. V.11 Receiver Input Graph w/ Termination

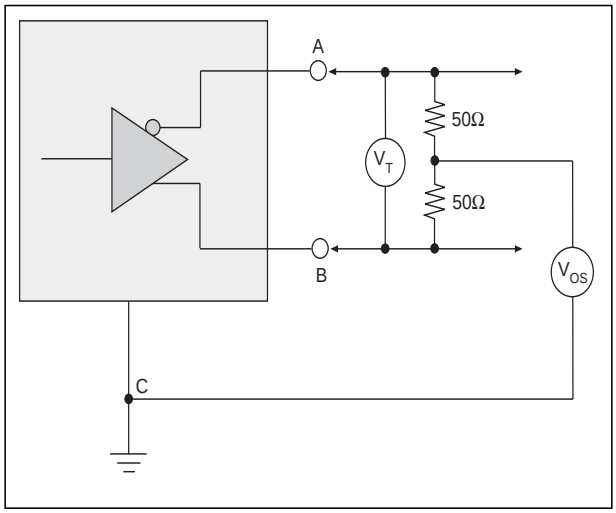


Figure 25. V.35 Driver Output Test Terminated Voltage

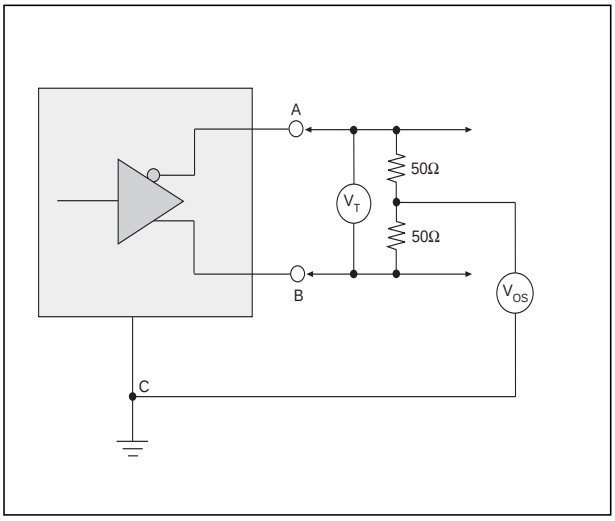


Figure 26. V.35 Driver Output Offset Voltage

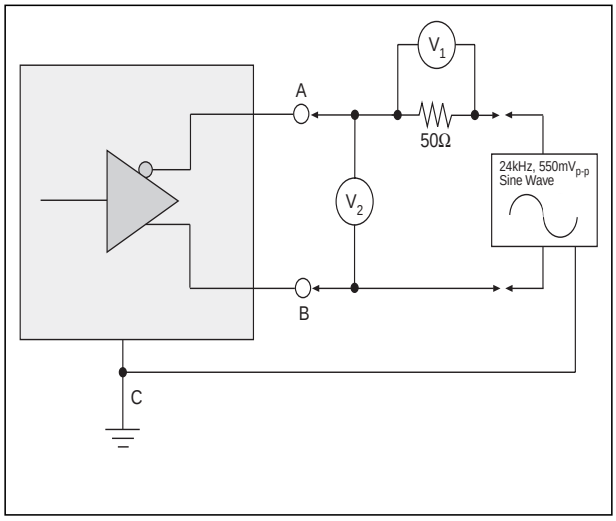


Figure 27. V.35 Driver Output Source Impedance

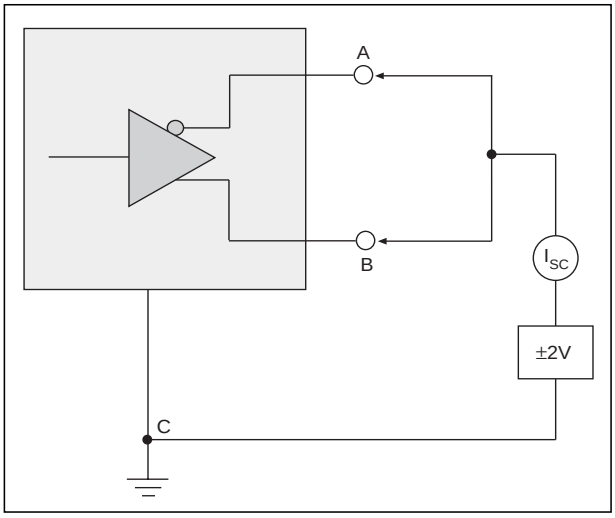


Figure 28. V.35 Driver Output Short-Circuit Impedance

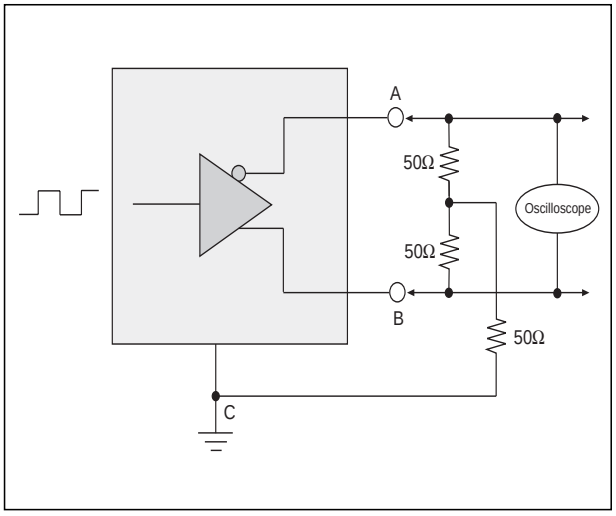


Figure 29. V.35 Driver Output Rise/Fall Time

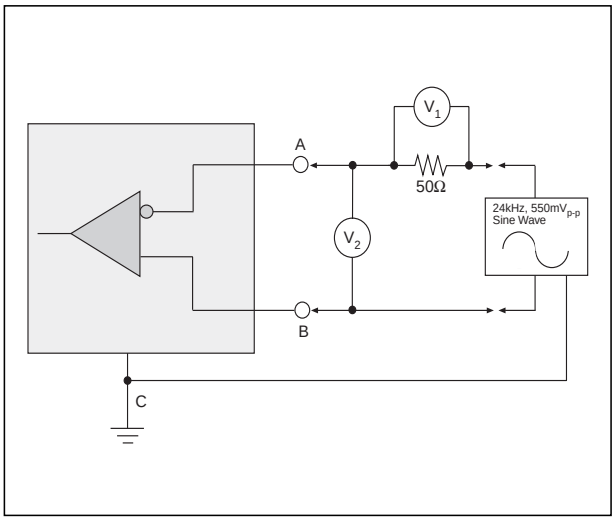


Figure 30. V.35 Receiver Input Source Impedance

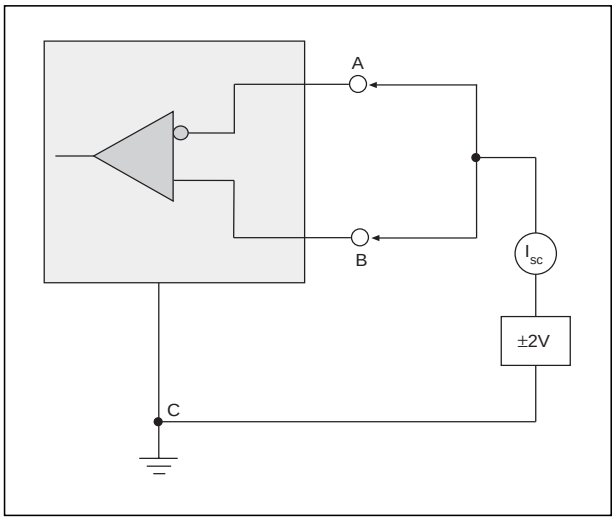


Figure 31. V.35 Receiver Input Short-Circuit Impedance

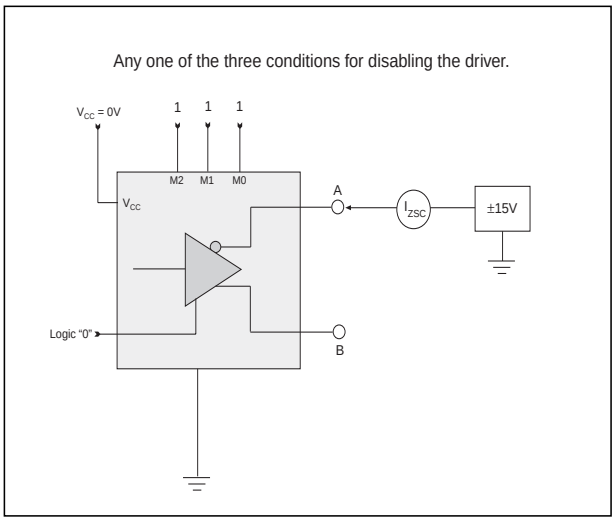


Figure 32. Driver Output Leakage Current Test

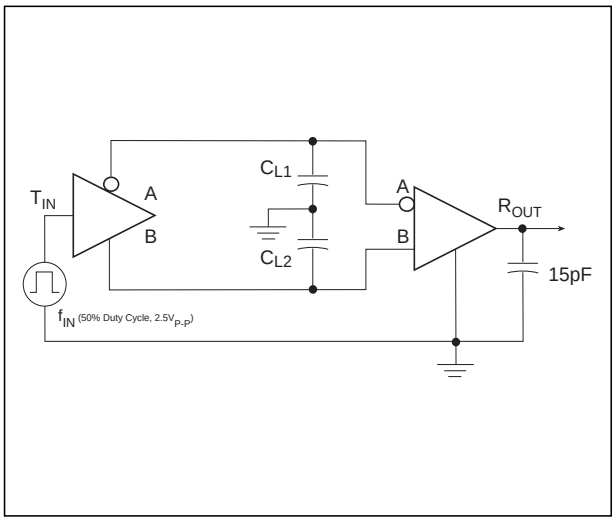


Figure 33. Driver/Receiver Timing Test Circuit

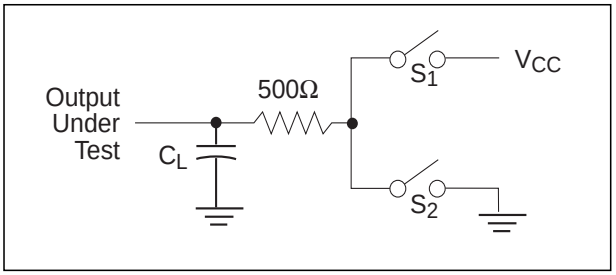


Figure 34. Driver Timing Test Load Circuit

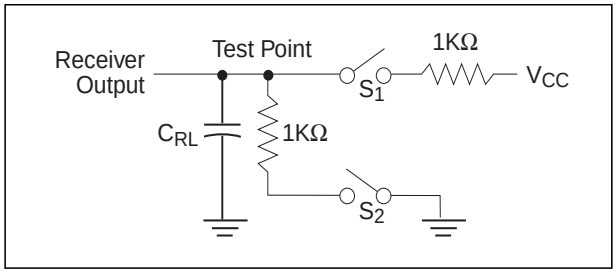


Figure 35. Receiver Timing Test Load Circuit

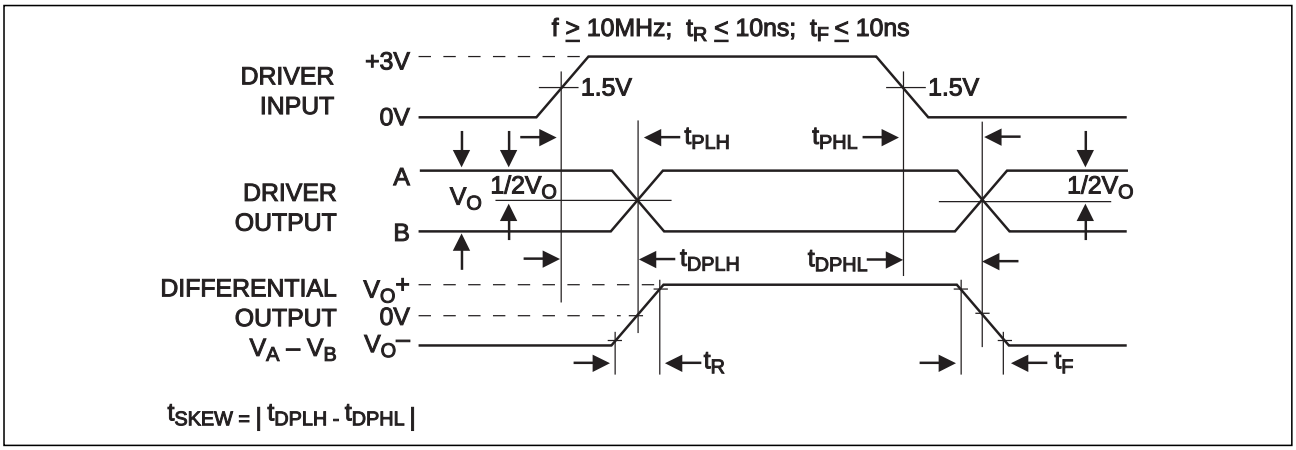


Figure 36. Driver Propagation Delays

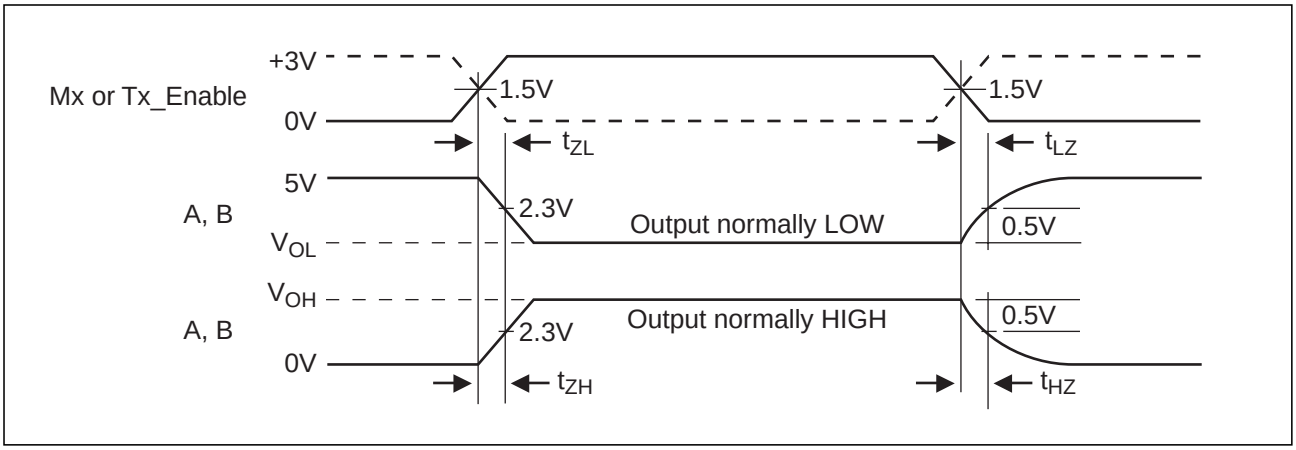


Figure 37. Driver Enable and Disable Times

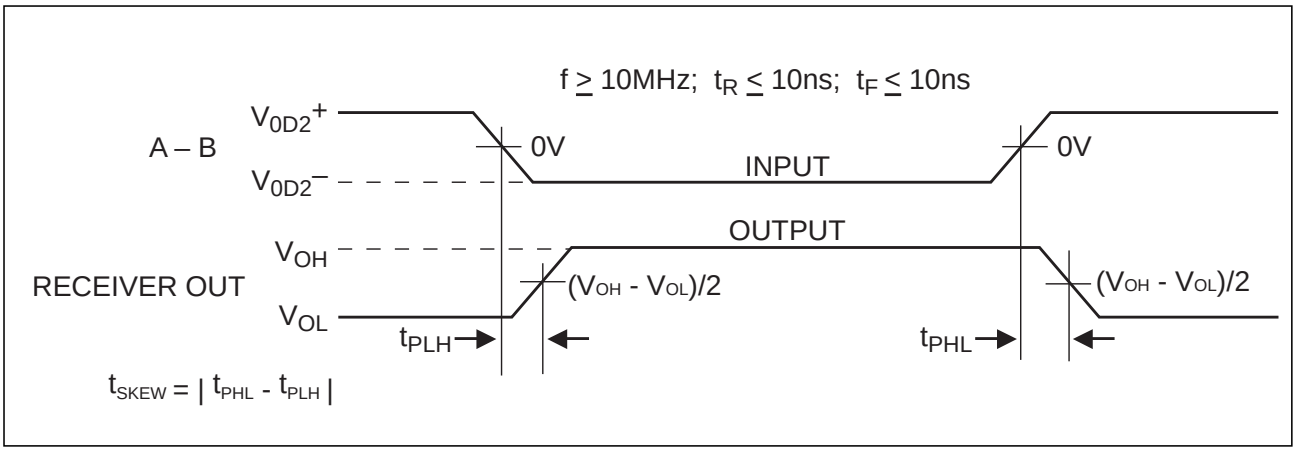


Figure 38. Receiver Propagation Delays

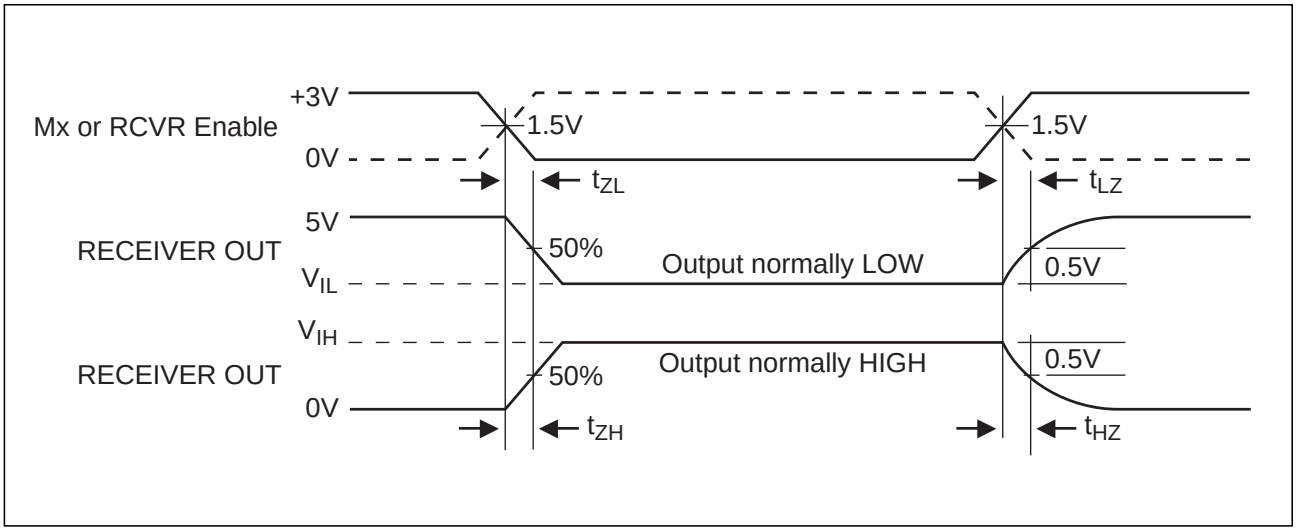


Figure 39. Receiver Enable and Disable Times

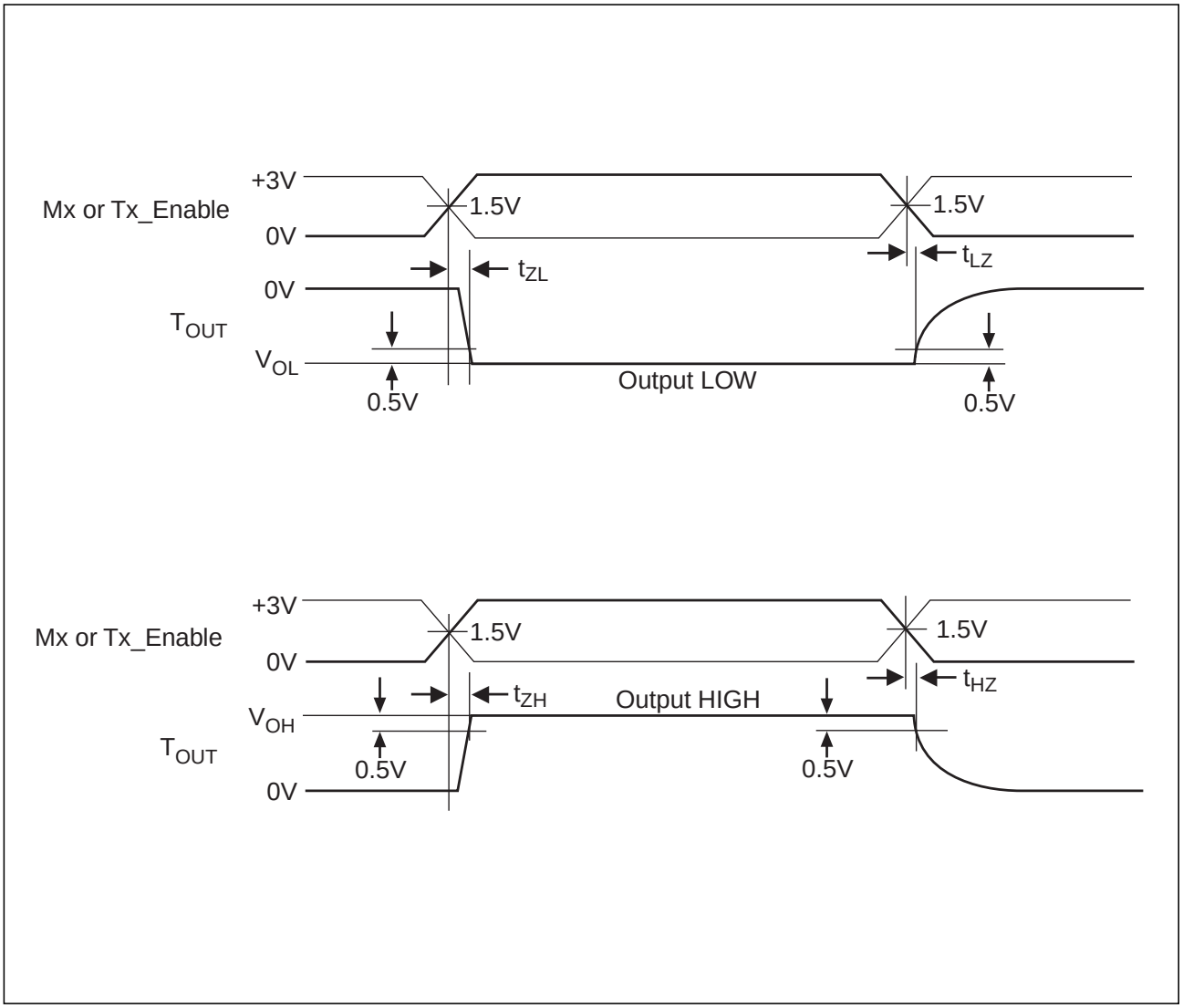


Figure 40. V.28 (RS-232) and V.10 (RS-423) Driver Enable and Disable Times

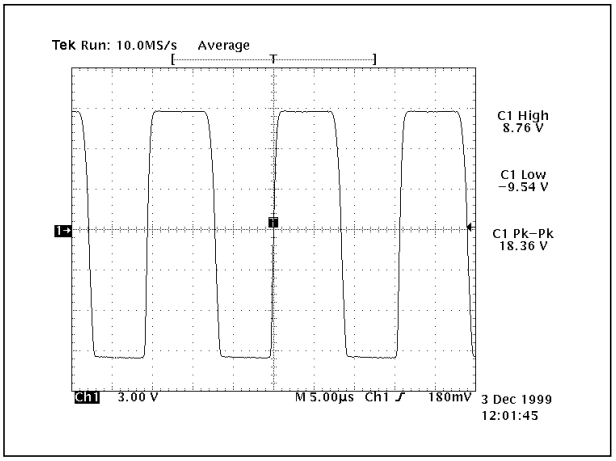


Figure 41. Typical V.28 Driver Output Waveform

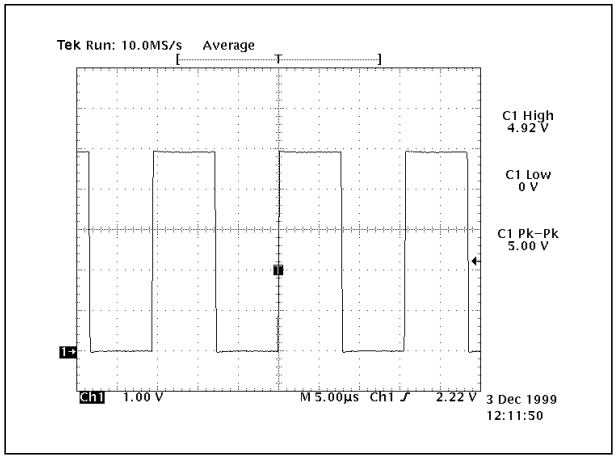


Figure 42. Typical V.10 Driver Output Waveform

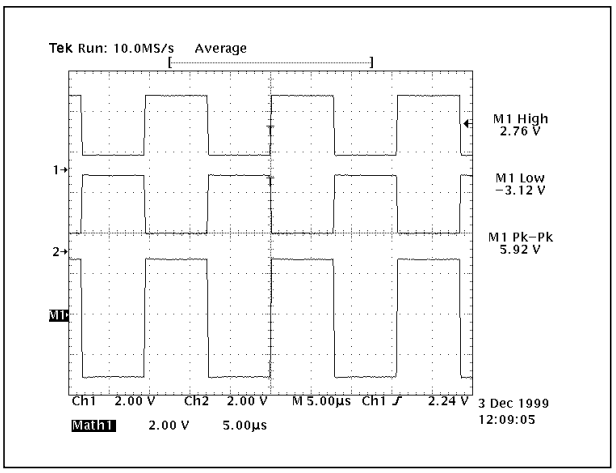


Figure 43. Typical V.11 Driver Output Waveforms

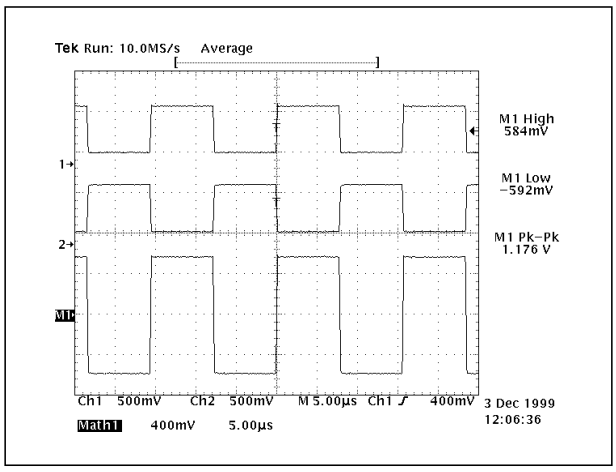
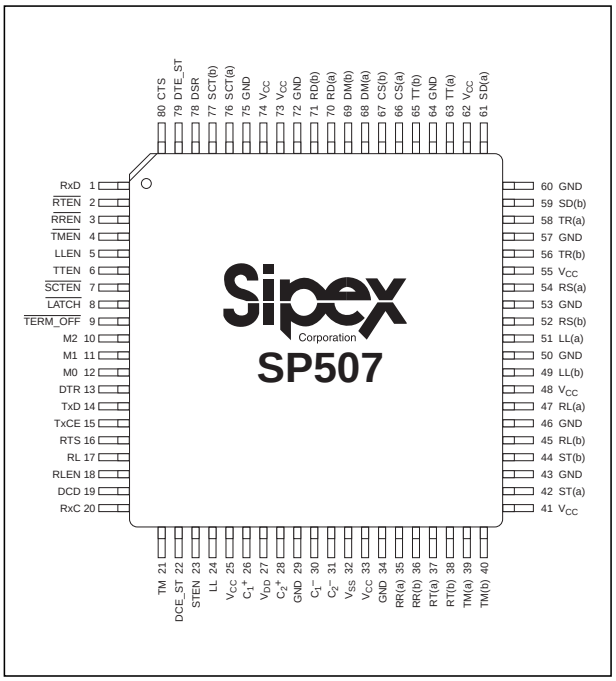


Figure 44. Typical V.35 Driver Output Waveforms

PINOUT



PIN ASSIGNMENTS

CLOCK AND DATA GROUP

Pin 1 — RxD — Receive Data; TTL output, sourced from RD(a) and RD(b) inputs.

Pin 14 — TxD — TTL input ; transmit data source for SD(a) and SD(b) outputs.

Pin 15 — TxCE — Transmit Clock; TTL input for TT driver outputs.

Pin 20 — RxC — Receive Clock; TTL output sourced from RT(a) and RT(b) inputs.

Pin 22 — DCE_ST — Send Timing; TTL input; source for ST(a) and ST(b) outputs.

Pin 37 — RT(a) — Receive Timing; analog input, inverted; source for RxC.

Pin 38 — RT(b) — Receive Timing; analog input, non-inverted; source for RxC.

Pin 42 — ST(a) — Send Timing; analog output, inverted; sourced from DCE_ST.

Pin 44 — ST(b) — Send Timing; analog output, non-inverted; sourced from DCE_ST.

Pin 59 — SD(b) — Analog Out — Send data, non-inverted; sourced from TxD.

Pin 61 — SD(a) — Analog Out — Send data, inverted; sourced from TxD.

Pin 63 — TT(a) — Analog Out — Terminal Timing, inverted; sourced from TxCE.

Pin 65 — TT(b) — Analog Out — Terminal Timing, non–inverted; sourced from TxCE.

Pin 70 — RD(a) — Receive Data, analog input; inverted; source for RxD.

Pin 71 — RD(b) — Receive Data; analog input; non-inverted; source for RxD.

Pin 76 — SCT(a) — Serial Clock Transmit; analog input, inverted; source for DCE_ST.

Pin 77 — SCT(b) — Serial Clock Transmit: analog input, non–inverted; source for DCE_ST.

Pin 79 — DTE_ST — Serial Clock Transmit; TTL output; sources from SCT(a) and SCT(b) inputs.

CONTROL LINE GROUP

Pin 13 — DTR — Data Terminal Ready; TTL input; source for TR(a) and TR(b) outputs.

Pin 16 — RTS — Ready To Send; TTL input; source for RS(a) and RS(b) outputs.

Pin 17 — RL — Remote Loopback; TTL input; source for RL(a) and RL(b) outputs.

Pin 19 — DCD— Data Carrier Detect; TTL output; sourced from RR(a) and RR(b) inputs.

Pin 21 — TM — Ring In; TTL output; sourced from TM(a) and TM(b) inputs.

Pin 24 — LL — Local Loopback; TTL input; source for LL(a) and LL(b) outputs.

Pin 35 — RR(a)— Receiver Ready; analog input, inverted; source for DCD.

Pin 36 — RR(b)— Receiver Ready; analog input, non-inverted; source for DCD.

Pin 39 — TM(a)— Incoming Call; analog input, inverted; source for TM.

Pin 40 — TM(b)— Incoming Call; analog input, non-inverted; source for TM.

Pin 45 — RL(b) — Remote Loopback; analog output, non-inverted; sourced from RL.

Pin 47 — RL(a) — Remote Loopback; analog output inverted; sourced from RL.

Pin 49— LL(b) — Local Loopback; analog output, non-inverted; sourced from LL.

Pin 51 — LL(a) — Local Loopback; analog output, inverted; sourced from LL.

Pin 52 — RS(b) — Ready To Send; analog output, non-inverted; sourced from RTS.

Pin 54 — RS(a) — Ready To Send; analog output, inverted; sourced from RTS.

Pin 56 — TR(b) — Terminal Ready; analog output, non-inverted; sourced from DTR.

Pin 58 — TR(a) — Terminal Ready; analog output, inverted; sourced from DTR.

Pin 66 — CS(a)— Clear To Send; analog input, inverted; source for CTS.

Pin 67 — CS(b)— Clear To Send; analog input, non-inverted; source for CTS.

Pin 68 — DM(a)— Data Mode; analog input, inverted; source for DSR.

Pin 69 — DM(b)— Data Mode; analog input, non-inverted; source for DSR

Pin 78 — DSR— Data Set Ready; TTL output; sourced from DM(a) and DM(b) inputs.

Pin 80 — CTS— Clear To Send; TTL output; sourced from CS(a) and CS(b) inputs.

CONTROL REGISTERS

Pin 2 — $\overline{\text{RTEN}}$ — Enables RxC receiver, active low; TTL input.

Pin 3 — $\overline{\text{RREN}}$ — Enables DCD receiver, active low; TTL input.

Pin 4 — TMEN — Enables TM receiver, active high; TTL input.

Pin 5 — $\overline{\text{LLEN}}$ — Enables LL driver, active low; TTL input.

Pin 6 — TTEN — Enables TxCE driver, active high; TTL input.

Pin 7 — $\overline{\text{SCTEN}}$ — Enables DTE_ST receiver; active low; TTL input.

Pin 8 — $\overline{\text{LATCH}}$ — Latch control for decoder bits (pins 10-12), active low. Logic high input will make decoder transparent.

Pin 9 — $\overline{\text{TERM\_OFF}}$ — Disables receiver termination networks for RxD, RxC, and DTE_ST; TTL input.

Pins 10,11, 12 — M2, M1, M0 — Transmitter and receiver decode register; configures transmitter and receiver modes; TTL inputs.

Pin 18 — RLEN — Enables RL driver; active high; TTL input.

Pin 23 — STEN — Enables DTE_ST driver; active high; TTL input.

POWER SUPPLIES

Pins 25, 33, 41, 48, 55, 62, 73, 74 — V_{CC} — +5V input.

Pins 29, 34, 43, 46, 50, 53, 57, 60, 64, 72, 75 — GND — Ground.

Pin 27 — V_{DD} +10V Charge Pump Capacitor — Connects from V_{DD} to V_{CC}. Suggested capacitor size is 22µF, 16V.

Pin 32 — V_{SS} –10V Charge Pump Capacitor — Connects from ground to V_{SS}. Suggested capacitor size is 22µF, 16V.

Pins 26 and 30 — C_1^+ and C_1^- — Charge Pump Capacitor — Connects from C_1^+ to C_1^-. Suggested capacitor size is 22µF, 16V.

Pins 28 and 31 — C_2^+ and C_2^- — Charge Pump Capacitor — Connects from C_2^+ to C_2^-. Suggested capacitor size is 22µF, 16V.

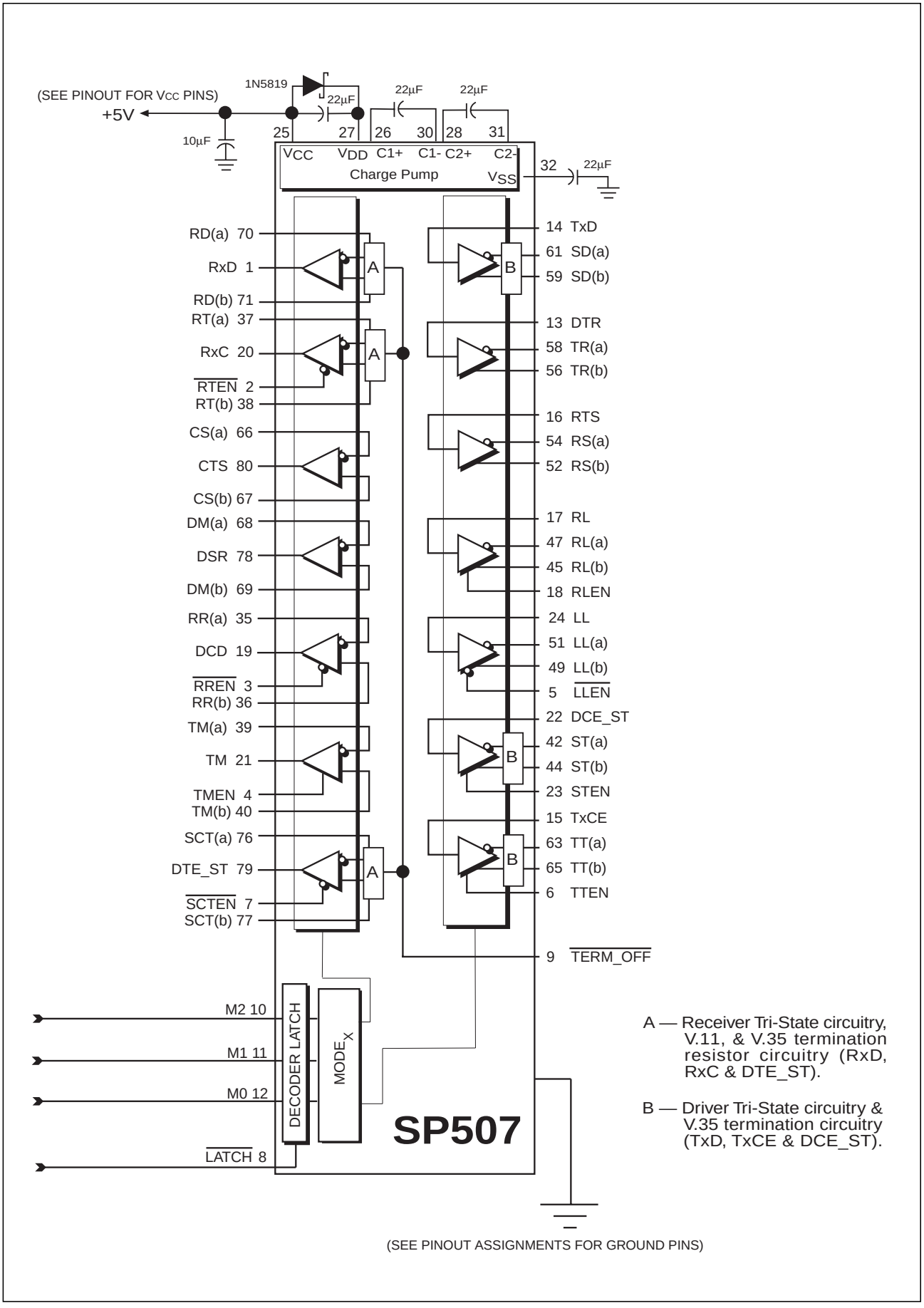


Figure 45. Typical Operating Circuit

SP507 Driver Mode Selection

Pin Label	Mode	V.11	EIA-530A	EIA-530	X.21	V.35	RS-449	RS-232
M2 - M0	111	000	001	010	011	100	101	110
SD(a)	3-state	V.11-	V.11-	V.11-	V.11-	V.35-	V.11-	V.28
SD(b)	3-state	V.11+	V.11+	V.11+	V.11+	V.35+	V.11+	3-state
TR(a)	3-state	V.11-	V.10	V.11-	V.11-	V.28	V.11-	V.28
TR(b)	3-state	V.11+	3-state	V.11+	V.11+	3-state	V.11+	3-state
RS(a)	3-state	V.11-	V.11-	V.11-	V.11-	V.28	V.11-	V.28
RS(b)	3-state	V.11+	V.11+	V.11+	V.11+	3-state	V.11+	3-state
RL(a)	3-state	V.11-	V.11-	V.11-	V.11-	V.28	V.11-	V.28
RL(b)	3-state	V.11+	V.11+	V.11+	V.11+	3-state	V.11+	3-state
LL(a)	3-state	V.10	V.10	V.10	V.10	V.28	V.10	V.28
LL(b)	3-state	3-state	3-state	3-state	3-state	3-state	3-state	3-state
ST(a)	3-state	V.11-	V.11-	V.11-	V.11-	V.35-	V.11-	V.28
ST(b)	3-state	V.11+	V.11+	V.11+	V.11+	V.35+	V.11+	3-state
TT(a)	3-state	V.11-	V.11-	V.11-	V.11-	V.35-	V.11-	V.28
TT(b)	3-state	V.11+	V.11+	V.11+	V.11+	V.35+	V.11+	3-state

Table 1. SP507 Driver Decoder Table

SP507 Receiver Mode Selection

Pin Label	Mode	V.11	EIA-530A	EIA-530	X.21	V.35	RS-449	RS-232
M2 - M0	111	000	001	010	011	100	101	110
RD(a)	>10kΩ to GND	V.11-	V.11-	V.11-	V.11-	V.35-	V.11-	V.28
RD(b)	>10kΩ to GND	V.11+	V.11+	V.11+	V.11+	V.35+	V.11+	>10kΩ to GND
RT(a)	>10kΩ to GND	V.11-	V.11-	V.11-	V.11-	V.35-	V.11-	V.28
RT(b)	>10kΩ to GND	V.11+	V.11+	V.11+	V.11+	V.35+	V.11+	>10kΩ to GND
CS(a)	>10kΩ to GND	V.11-	V.11-	V.11-	V.11-	V.28	V.11-	V.28
CS(b)	>10kΩ to GND	V.11+	V.11+	V.11+	V.11+	>10kΩ to GND	V.11+	>10kΩ to GND
DM(a)	>10kΩ to GND	V.11-	V.10	V.11-	V.11-	V.28	V.11-	V.28
DM(b)	>10kΩ to GND	V.11+	>10kΩ to GND	V.11+	V.11+	>10kΩ to GND	V.11+	>10kΩ to GND
RR(a)	>10kΩ to GND	V.11-	V.11-	V.11-	V.11-	V.28	V.11-	V.28
RR(b)	>10kΩ to GND	V.11+	V.11+	V.11+	V.11+	>10kΩ to GND	V.11+	>10kΩ to GND
TM(a)	>10kΩ to GND	V.10	V.10	V.10	V.10	V.28	V.10	V.28
TM(b)	>10kΩ to GND	>10kΩ to GND	>10kΩ to GND	>10kΩ to GND	>10kΩ to GND	>10kΩ to GND	>10kΩ to GND	>10kΩ to GND
SCT(a)	>10kΩ to GND	V.11-	V.11-	V.11-	V.11-	V.35-	V.11-	V.28
SCT(b)	>10kΩ to GND	V.11+	V.11+	V.11+	V.11+	V.35+	V.11+	>10kΩ to GND

Table 2. SP507 Receiver Decoder Table

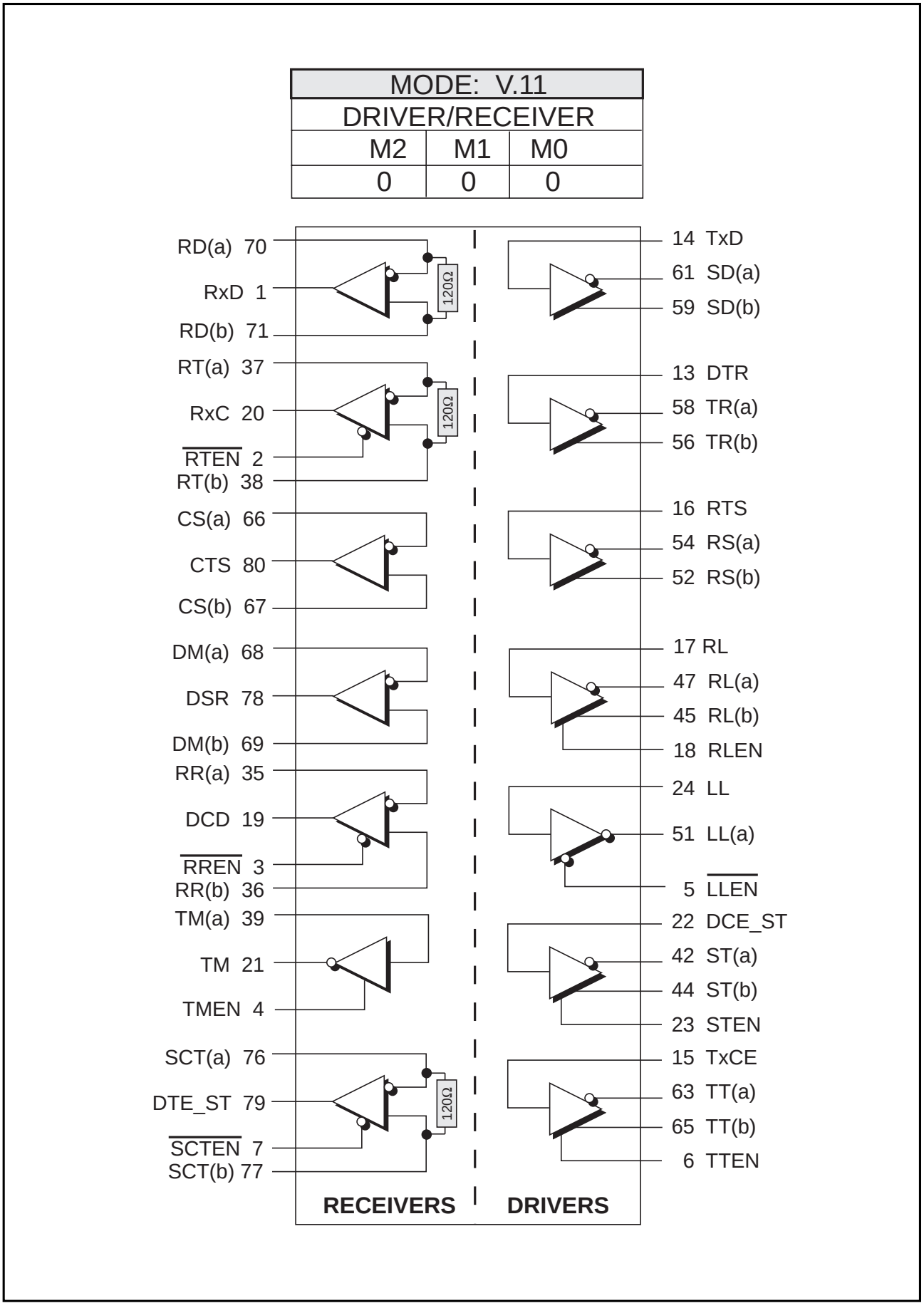


Figure 46. Mode Diagram – V.11

MODE: EIA-530A		
DRIVER/RECEIVER		
M2	M1	M0
0	0	1

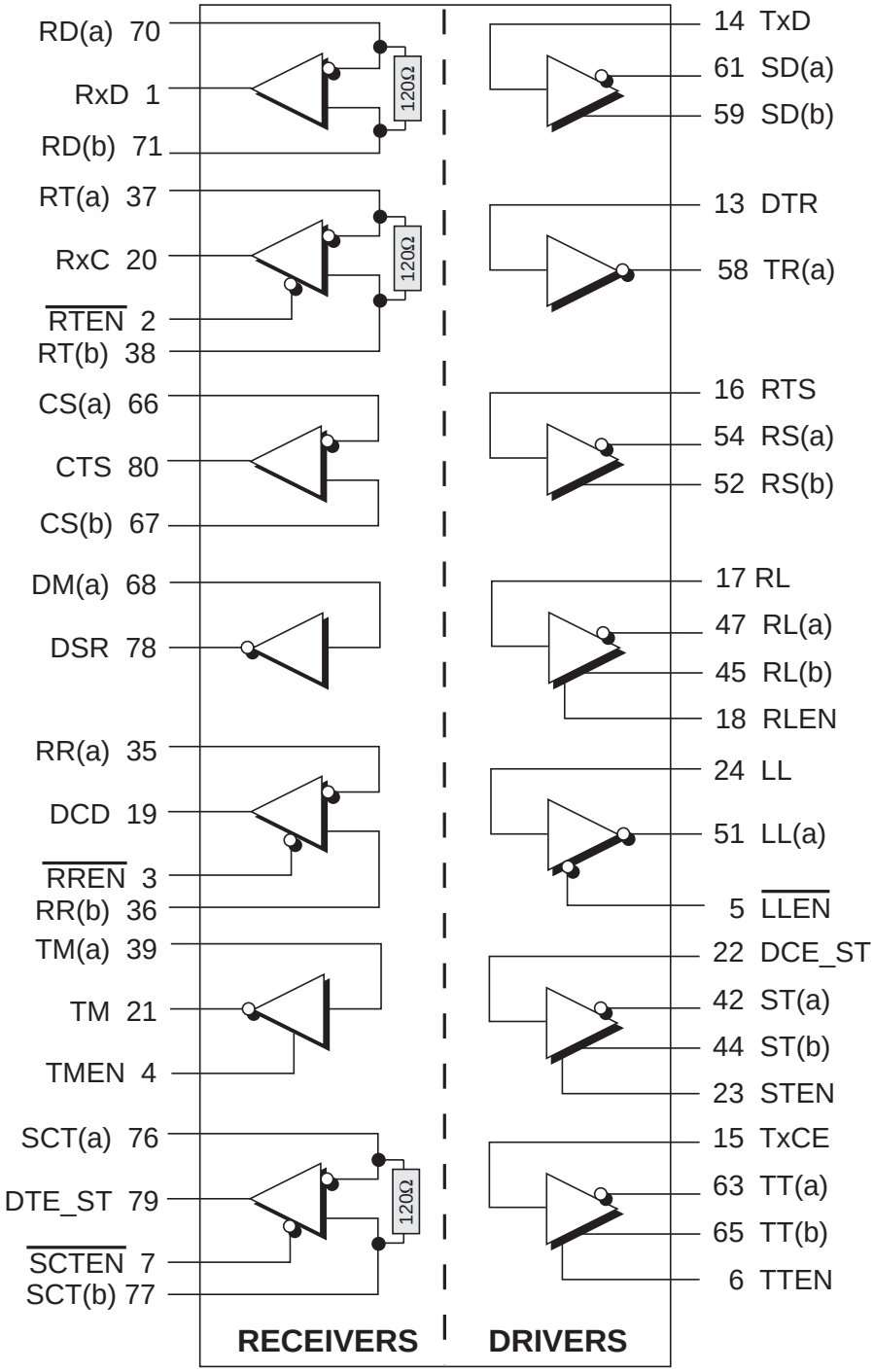


Figure 47. Mode Diagram – EIA-530A

MODE: EIA-530		
DRIVER/RECEIVER		
M2	M1	M0
0	1	0

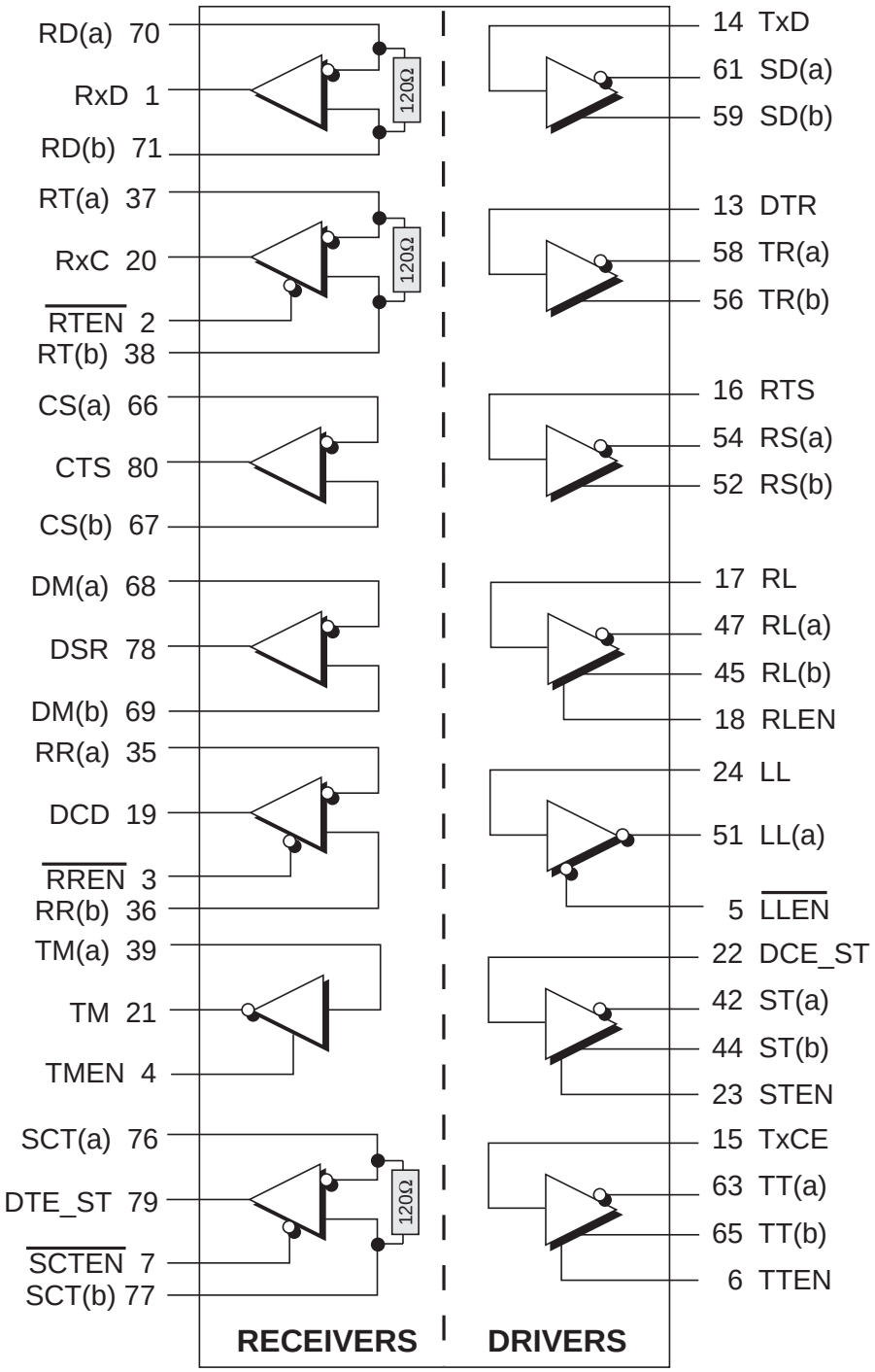


Figure 48. Mode Diagram – EIA-530

MODE: X.21		
DRIVER/RECEIVER		
M2	M1	M0
0	1	1

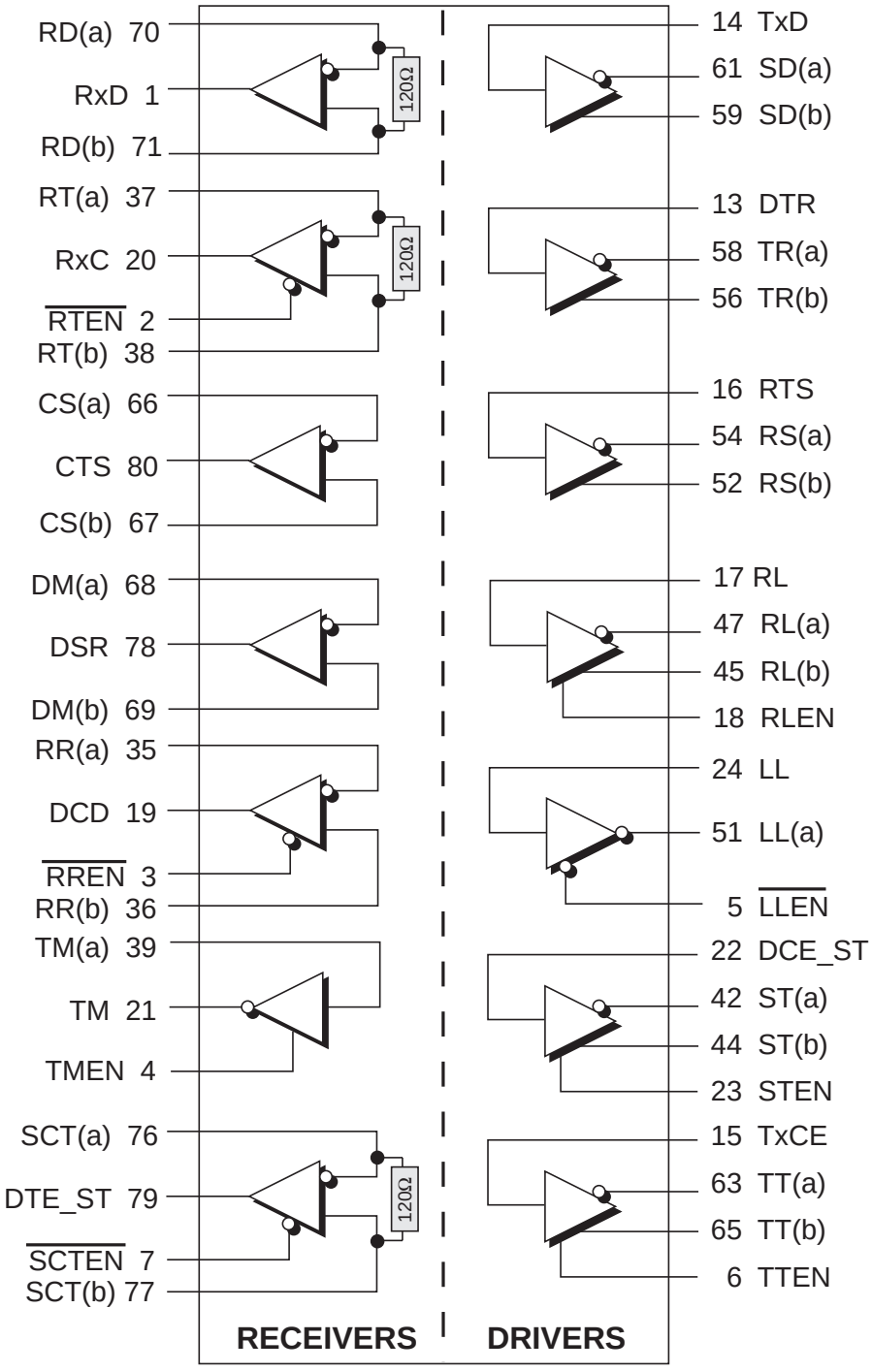


Figure 49. Mode Diagram – X.21

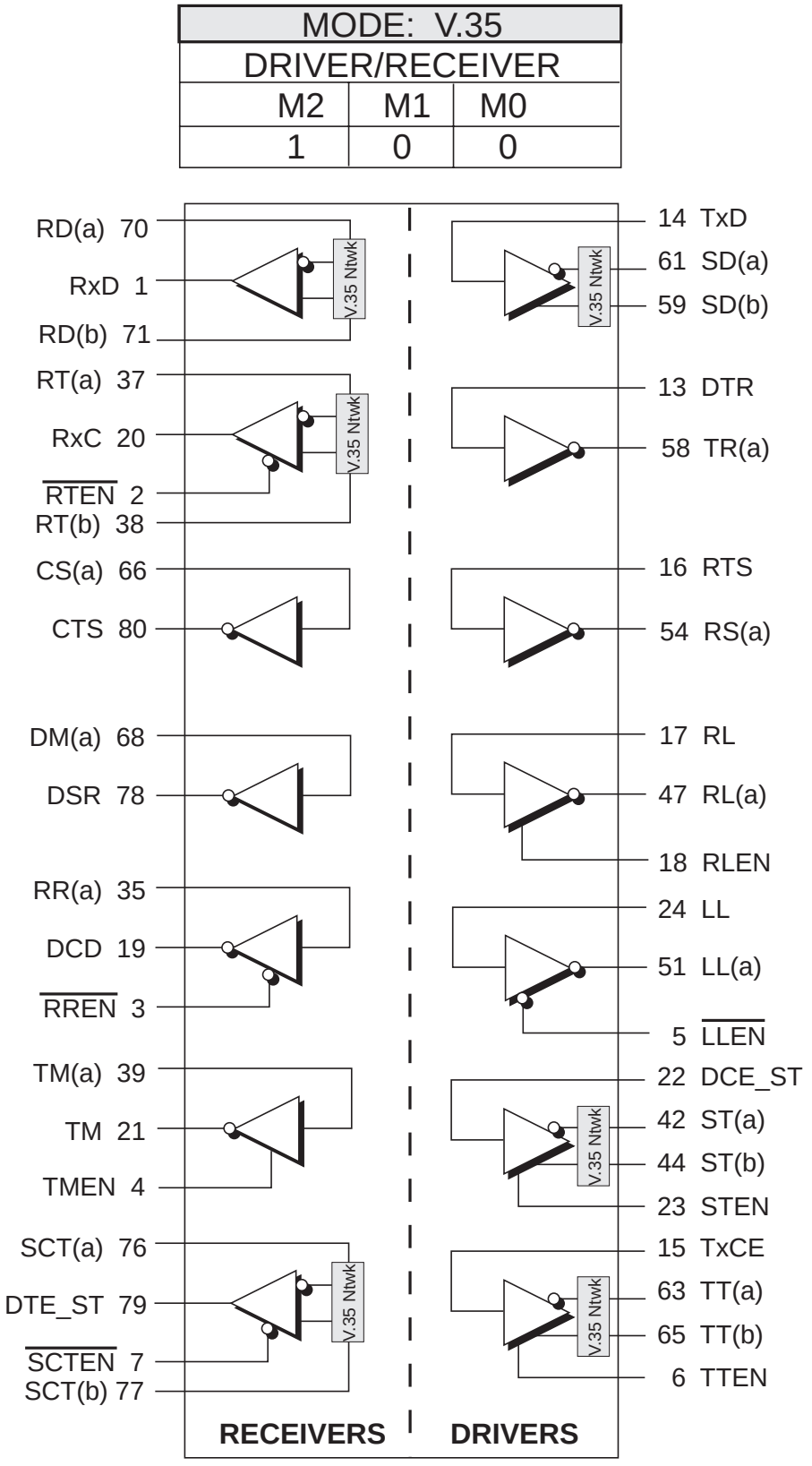


Figure 50. Mode Diagram – V.35

MODE: RS-449		
DRIVER/RECEIVER		
M2	M1	M0
1	0	1

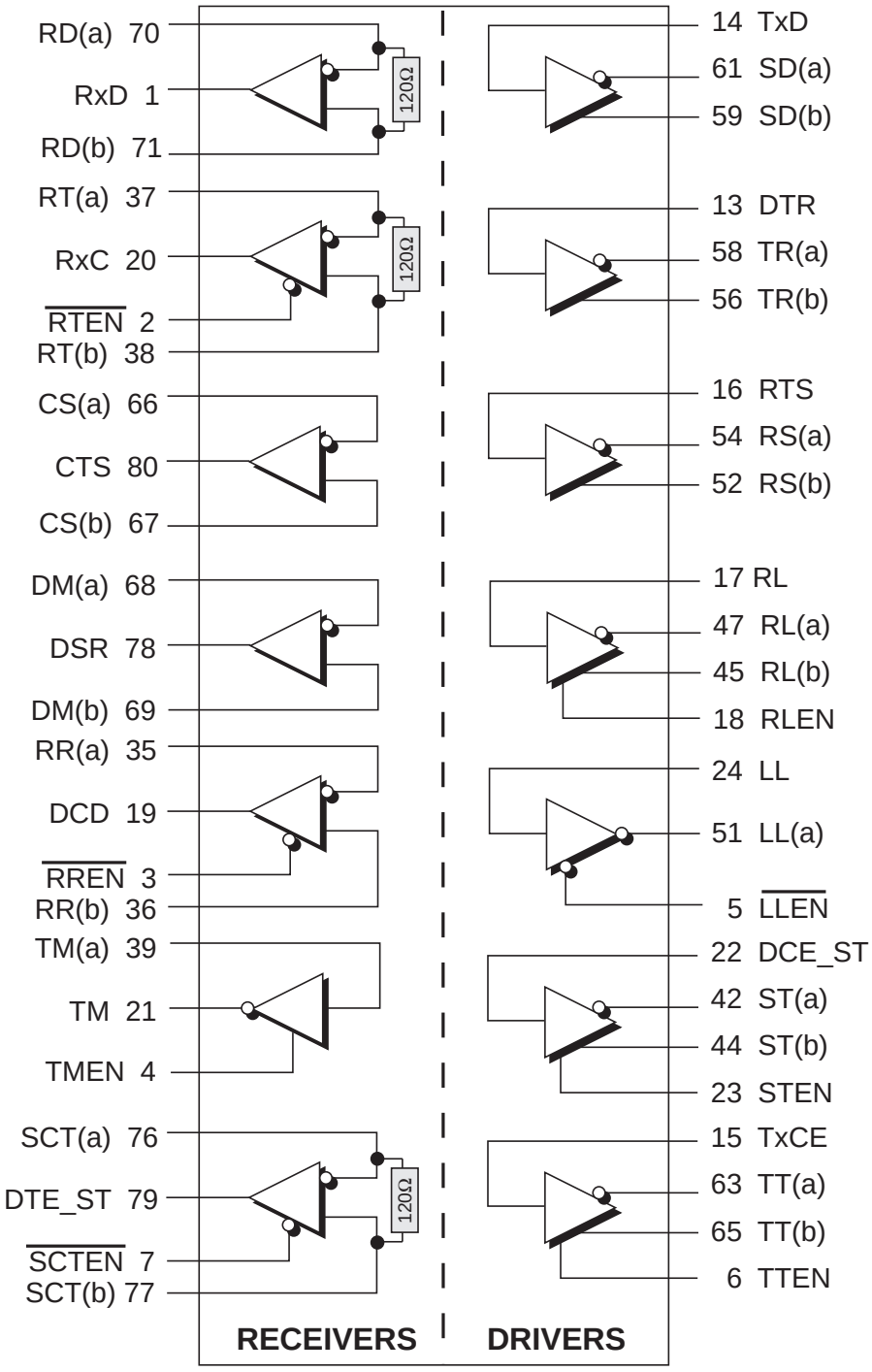


Figure 51. Mode Diagram – RS-449

MODE: RS-232 (V.28)		
DRIVER/RECEIVER		
M2	M1	M0
1	1	0

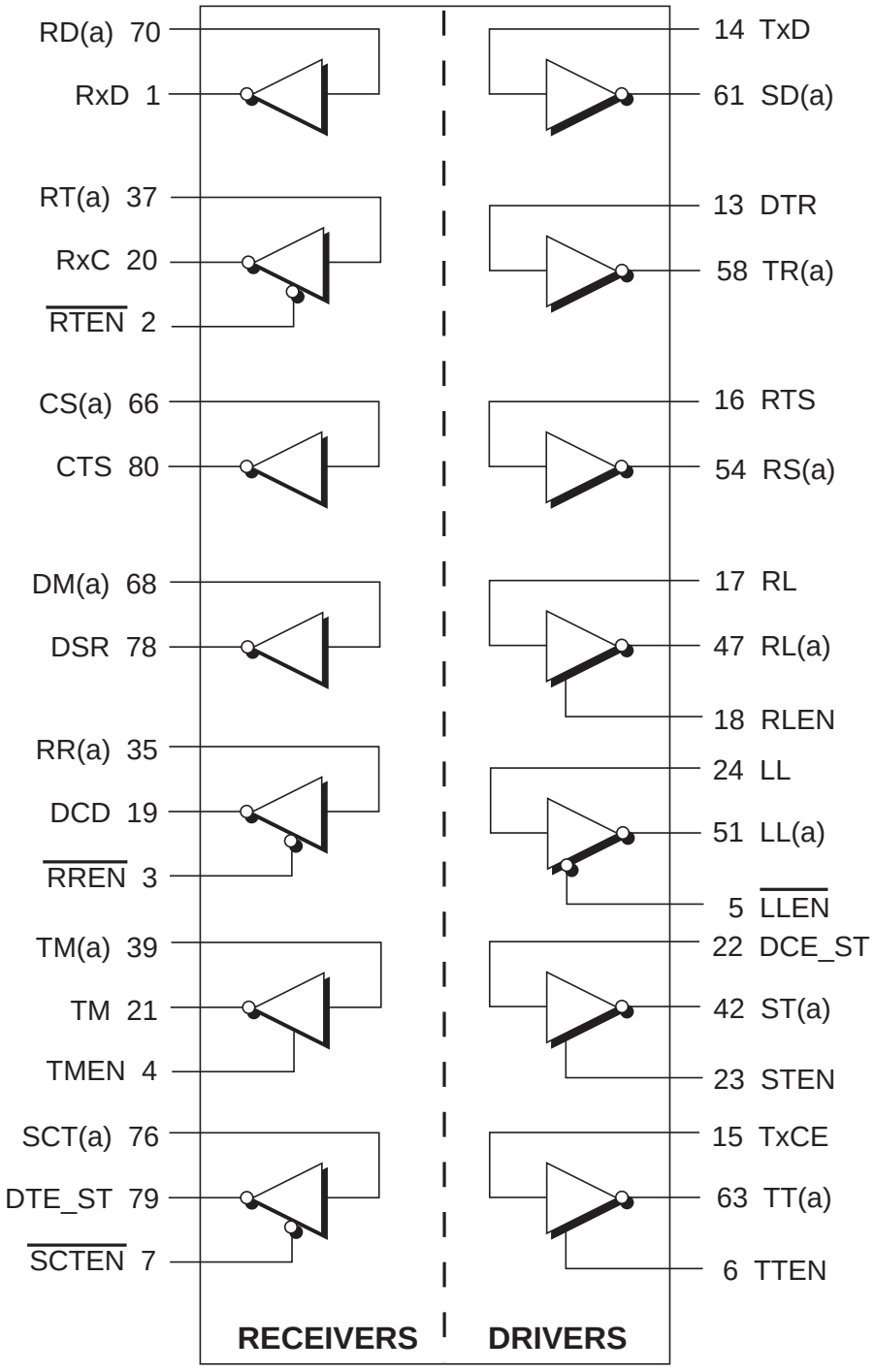
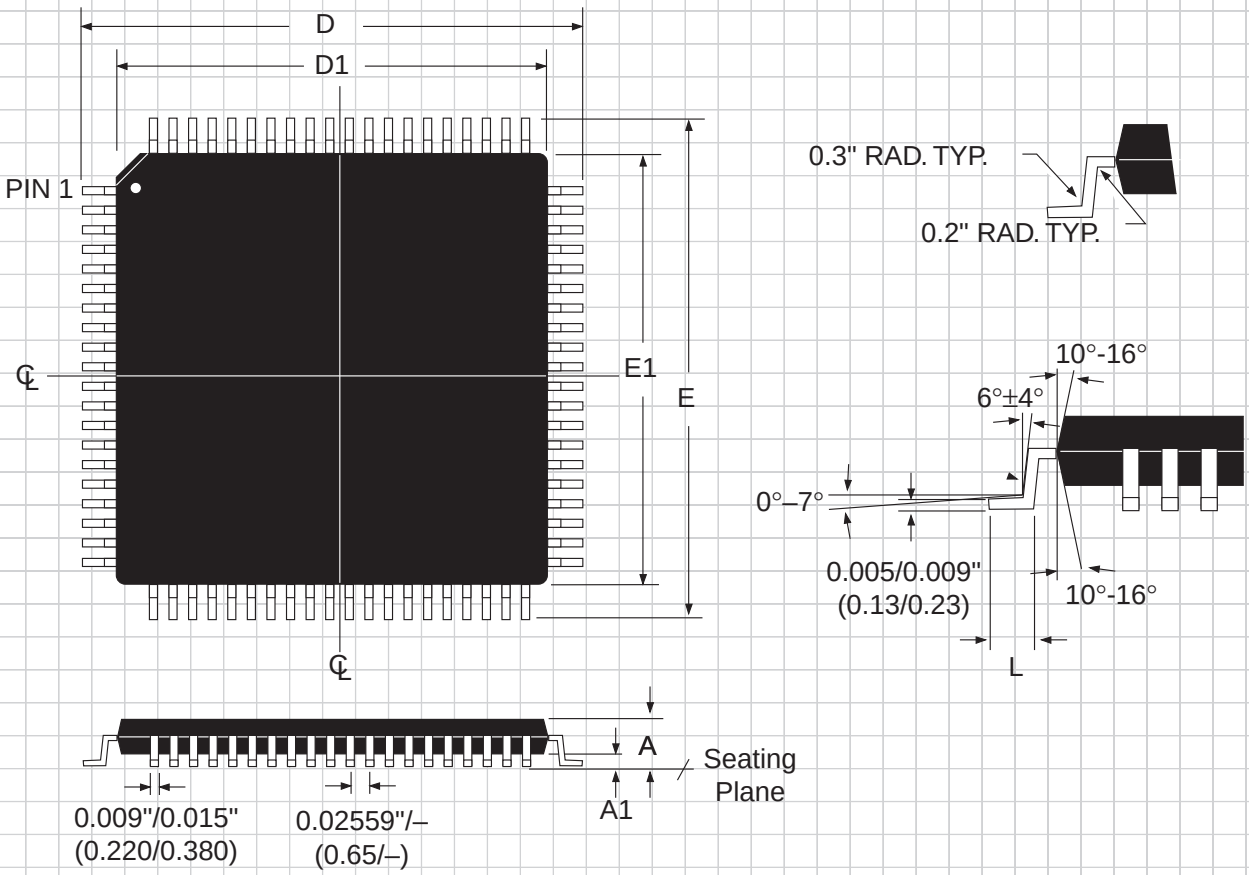


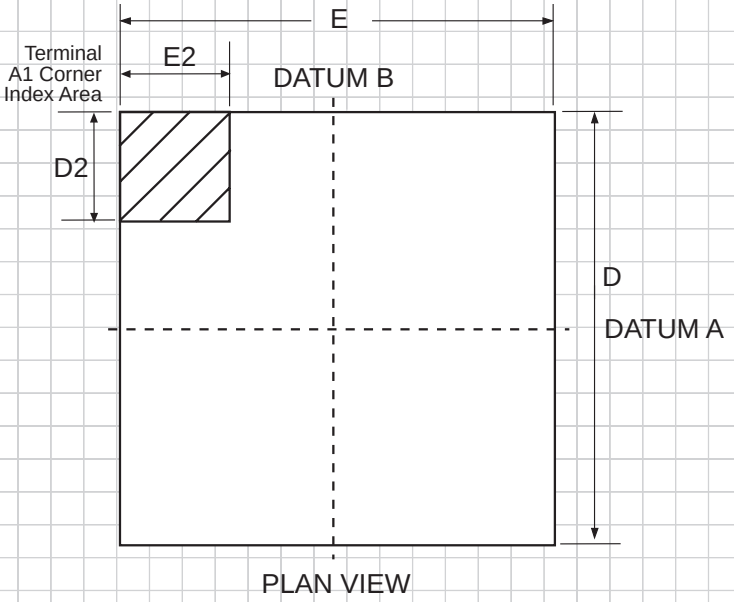
Figure 52. Mode Diagram – RS-232

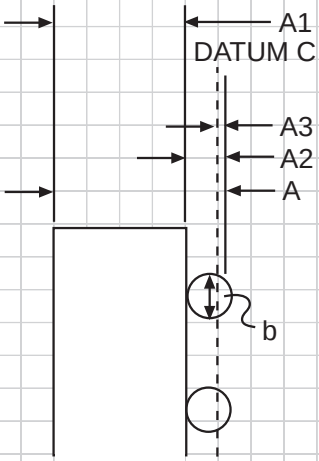
PACKAGE: QUAD FLATPACK
JEDEC "BE-2" OUTLINE

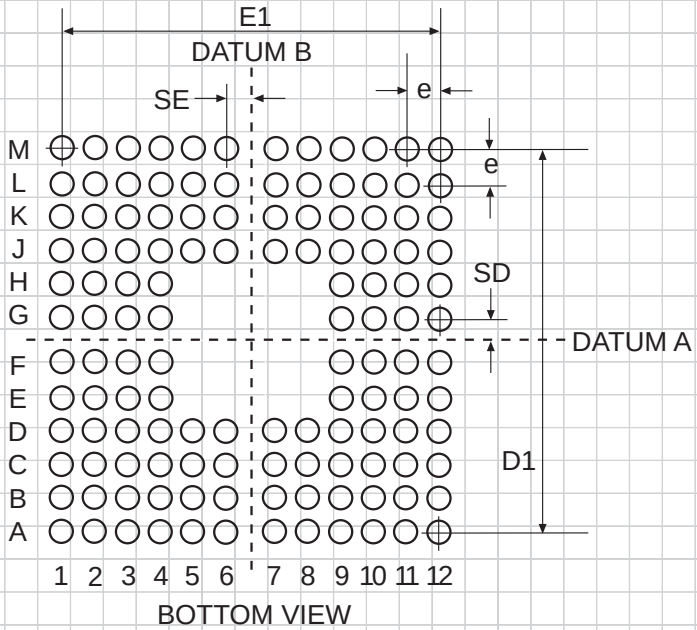


DIMENSIONS in Inches Minimum/Maximum (mm)	JEDEC BE-2 Outline 80–PIN
A	–/0.0925 (–/2.350)
A1	–/0.010 (–/0.250)
D	0.667/0.687 (16.950/17.450)
D1	0.547/0.555 (13.900/14.100)
E	0.667/0.687 (16.950/17.450)
E1	0.547/0.555 (13.900/14.100)
L	0.0255/0.0375 (0.650/0.950)

PACKAGE: BALL GRID ARRAY







DIMENSIONS in Inches Minimum/Maximum (mm)	BALL GRID ARRAY 80–PIN
D	0.429/0.437 (10.9/11.1)
D1	0.346 TYP (8.80 TYP)
D2 (D2=D/4)	0.107/0.109 (2.73/2.78)
E	0.429/0.437 (10.9/11.1)
E1	0.346 TYP (8.80 TYP)
E2	0.107/0.109 (2.73/2.78)
E2 (E2=E/4)	0.107/0.109 (2.73/2.78)
e	0.0315 TYP (0.800 TYP)
SE	0.0157 TYP (0.400 TYP)
SD	0.0157 TYP (0.400 TYP)
A	0.0669 MAX (1.70 MAX)
A1	0.0138/0/0177 (0.350/0.450)
A2	0.335 MIN (0.850 MIN)
A3	0.00472 MAX (0.120 MAX)
b	0.0177/0.0217 (0.450/0.550)

ORDERING INFORMATION

Model	Temperature Range	Package Types
SP507CF	0°C to +70°C	80–pin JEDEC (BE-2 Outline) QFP
SP507CB	0°C to +70°C	128-lead small scale ball grid array

Please consult the factory for pricing and availability on a Tape-On-Reel option.

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