

**Document Title**

256Kx16 bit Dynamic RAM with Fast Page Mode

**Revision History**

<u>Revision No</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0A	Initial Draft	August 11,2001	

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# 256K x 16 (4-MBIT) DYNAMIC RAM WITH FAST PAGE MODE

## FEATURES

- Fast access and cycle time
- TTL compatible inputs and outputs
- Refresh Interval: 512 cycles/8 ms
- Refresh Mode:  $\overline{\text{RAS}}$ -Only,  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  (CBR), Hidden
- Self Refresh Mode: 512 cycles/64 ms (S version only)
- JEDEC standard pinout
- Single power supply:
  - 5V  $\pm$  10% (IC41C16257)
  - 3.3V  $\pm$  10% (IC41LV16257)
- Byte Write and Byte Read operation via two  $\overline{\text{CAS}}$
- Available in 40-pin SOJ and TSOP-2

## DESCRIPTION

The *ICSI* IC41C16257 and the IC41LV16257 are 262,144 x 16-bit high-performance CMOS Dynamic Random Access Memory. Fast Page Mode allows 512 random accesses within a single row with access cycle time as short as 12 ns per 16-bit word. The Byte Write control, of upper and lower byte, makes these devices ideal for use in 16-, 32-bit wide data bus systems.

These features make the IC41C16257 and the IC41LV16257 ideally suited for high band-width graphics, digital signal processing, high-performance computing systems, and peripheral applications.

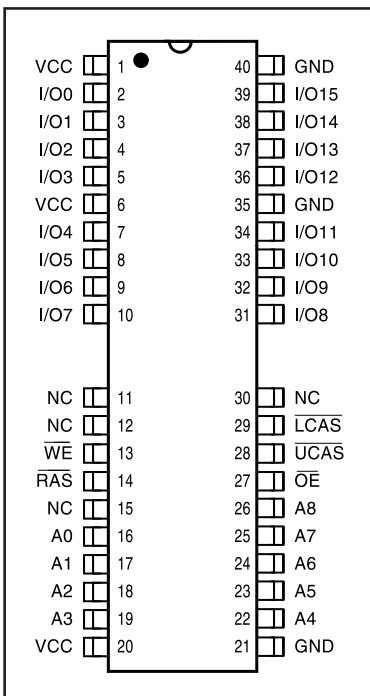
The IC41C16257 and the IC41LV16257 are packaged in a 40-pin, 400mil SOJ and TSOP-2.

## KEY TIMING PARAMETERS

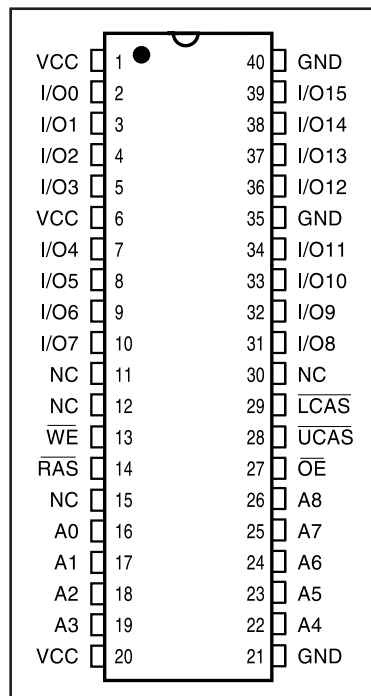
Parameter	-35	-50	-60	Unit
Max. $\overline{\text{RAS}}$ Access Time ( $t_{\text{RAC}}$ )	35	50	60	ns
Max. $\overline{\text{CAS}}$ Access Time ( $t_{\text{CAC}}$ )	10	14	15	ns
Max. Column Address Access Time ( $t_{\text{AA}}$ )	18	25	30	ns
Min. Fast Page Mode Cycle Time ( $t_{\text{PC}}$ )	12	20	25	ns
Min. Read/Write Cycle Time ( $t_{\text{RC}}$ )	60	90	110	ns

## PIN CONFIGURATIONS

### 40-Pin TSOP-2



### 40-Pin SOJ

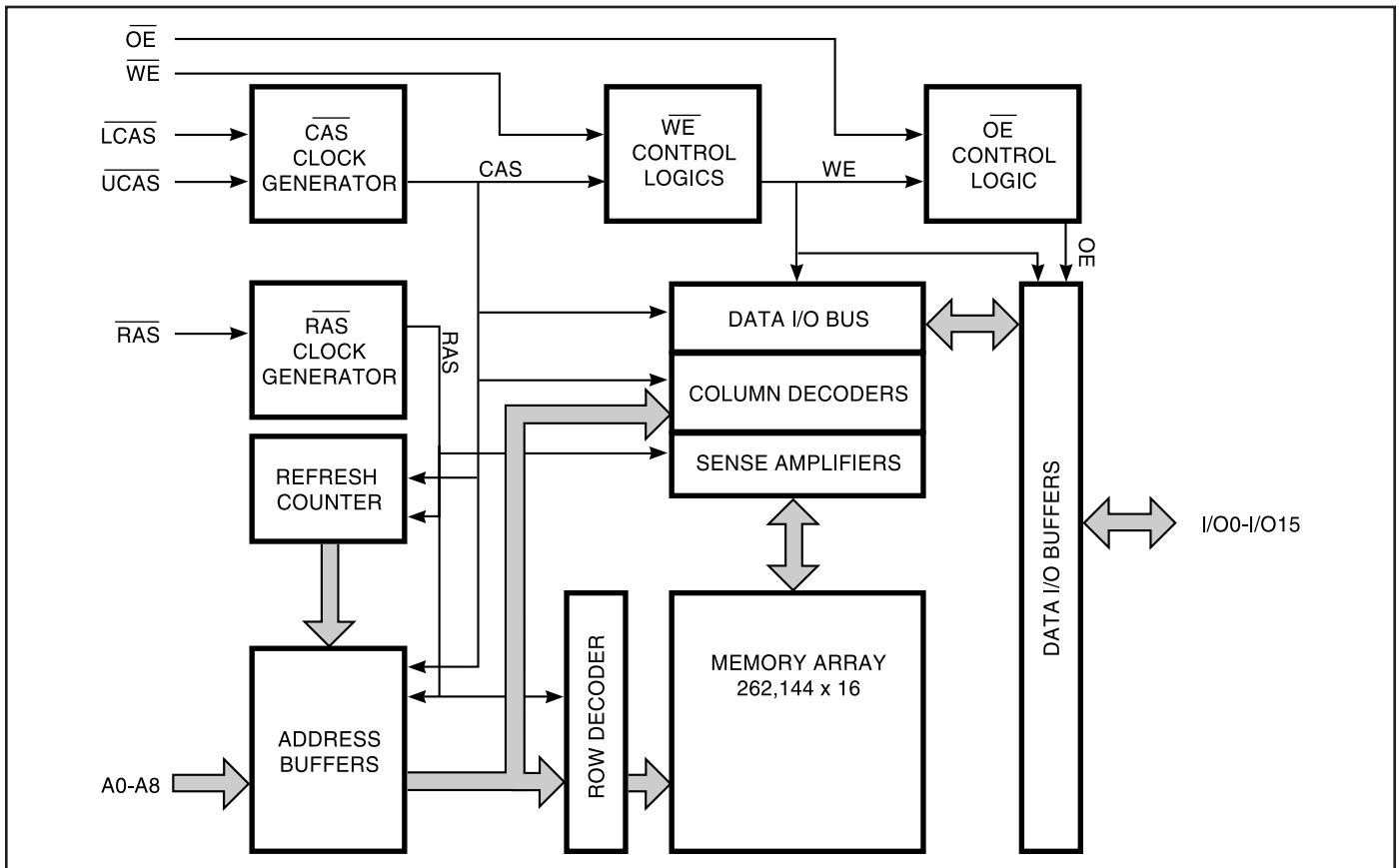


## PIN DESCRIPTIONS

A0-A8	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{UCAS}}$	Upper Column Address Strobe
$\overline{\text{LCAS}}$	Lower Column Address Strobe
Vcc	Power
GND	Ground
NC	No Connection

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### FUNCTIONAL BLOCK DIAGRAM



**TRUTH TABLE**

Function	$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Address $t_{\text{r}}/t_{\text{c}}$	I/O	
Standby	H	H	H	X	X	X	High-Z	
Read: Word	L	L	L	H	L	ROW/COL	DOUT	
Read: Lower Byte	L	L	H	H	L	ROW/COL	Lower Byte, DOUT Upper Byte, High-Z	
Read: Upper Byte	L	H	L	H	L	ROW/COL	Lower Byte, High-Z Upper Byte, DOUT	
Write: Word (Early Write)	L	L	L	L	X	ROW/COL	DIN	
Write: Lower Byte (Early Write)	L	L	H	L	X	ROW/COL	Lower Byte, DIN Upper Byte, High-Z	
Write: Upper Byte (Early Write)	L	H	L	L	X	ROW/COL	Lower Byte, High-Z Upper Byte, DIN	
Read-Write <sup>(1,2)</sup>	L	L	L	H→L	L→H	ROW/COL	DOUT, DIN	
Hidden Refresh <sup>2)</sup>	Read	L→H→L	L	L	H	L	ROW/COL	DOUT
	Write	L→H→L	L	L	L	X	ROW/COL	DOUT
RAS-Only Refresh	L	H	H	X	X	ROW/NA	High-Z	
CBR Refresh <sup>(3)</sup>	H→L	L	L	X	X	X	High-Z	

**Notes:**

1. These WRITE cycles may also be BYTE WRITE cycles (either  $\overline{\text{LCAS}}$  or  $\overline{\text{UCAS}}$  active).
2. These READ cycles may also be BYTE READ cycles (either  $\overline{\text{LCAS}}$  or  $\overline{\text{UCAS}}$  active).
3. At least one of the two CAS signals must be active ( $\overline{\text{LCAS}}$  or  $\overline{\text{UCAS}}$ ).

## FUNCTIONAL DESCRIPTION

The IC41C16257 and the IC41LV16257 are CMOS DRAMs optimized for high-speed bandwidth, low-power applications. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits. These are entered nine bits (A0-A8) at a time. The row address is latched by the Row Address Strobe ( $\overline{\text{RAS}}$ ). The column address is latched by the Column Address Strobe ( $\overline{\text{CAS}}$ ).  $\overline{\text{RAS}}$  is used to latch the first nine bits and  $\overline{\text{CAS}}$  is used to latch the latter nine bits.

The IC41C16257 and the IC41LV16257 have two  $\overline{\text{CAS}}$  controls,  $\overline{\text{LCAS}}$  and  $\overline{\text{UCAS}}$ . The  $\overline{\text{LCAS}}$  and  $\overline{\text{UCAS}}$  inputs internally generate a  $\overline{\text{CAS}}$  signal functioning in an identical manner to the single  $\overline{\text{CAS}}$  input on the other 256K x 16 DRAMs. The key difference is that each  $\overline{\text{CAS}}$  controls its corresponding I/O tristate logic (in conjunction with  $\overline{\text{OE}}$  and  $\overline{\text{WE}}$  and  $\overline{\text{RAS}}$ ).  $\overline{\text{LCAS}}$  controls I/O0 - I/O7 and  $\overline{\text{UCAS}}$  controls I/O8 - I/O15.

The IC41C16257/IC41LV16257  $\overline{\text{CAS}}$  function is determined by the first  $\overline{\text{CAS}}$  ( $\overline{\text{LCAS}}$  or  $\overline{\text{UCAS}}$ ) transitioning LOW and the last transitioning back HIGH. The two  $\overline{\text{CAS}}$  controls give the IC41C16257 both BYTE READ and BYTE WRITE cycle capabilities.

### Memory Cycle

A memory cycle is initiated by bringing  $\overline{\text{RAS}}$  LOW and it is terminated by returning both  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  HIGH. To ensure proper device operation and data integrity any memory cycle, once initiated, must not be ended or aborted before the minimum  $t_{\text{RAS}}$  time has expired. A new cycle must not be initiated until the minimum precharge time  $t_{\text{RP}}$ ,  $t_{\text{CP}}$  has elapsed.

### Read Cycle

A read cycle is initiated by the falling edge of  $\overline{\text{CAS}}$  or  $\overline{\text{OE}}$ , whichever occurs last, while holding  $\overline{\text{WE}}$  HIGH. The column address must be held for a minimum time specified by  $t_{\text{AR}}$ . Data Out becomes valid only when  $t_{\text{RAC}}$ ,  $t_{\text{AA}}$ ,  $t_{\text{CAC}}$  and  $t_{\text{OE}}$  are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters.

### Write Cycle

A write cycle is initiated by the falling edge of  $\overline{\text{CAS}}$  and  $\overline{\text{WE}}$ , whichever occurs last. The input data must be valid at or before the falling edge of  $\overline{\text{CAS}}$  or  $\overline{\text{WE}}$ , whichever occurs last.

### Refresh Cycle

To retain data, 512 refresh cycles are required in each 8 ms period. There are two ways to refresh the memory:

1. By clocking each of the 512 row addresses (A0 through A8) with  $\overline{\text{RAS}}$  at least once every 8 ms. Any read, write, read-modify-write or  $\overline{\text{RAS}}$ -only cycle refreshes the addressed row.
2. Using a  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle.  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh is activated by the falling edge of  $\overline{\text{RAS}}$ , while holding  $\overline{\text{CAS}}$  LOW. In  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle, an internal 9-bit counter provides the row addresses and the external address inputs are ignored.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  is a refresh-only mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle.

### Self Refresh Cycle<sup>(1)</sup>

The Self Refresh allows the user a dynamic refresh, data retention mode at the extended refresh period of 64 ms. i.e., 125  $\mu\text{s}$  per row when using distributed CBR refreshes. The feature also allows the user the choice of a fully static, low power data retention mode. The optional Self Refresh feature is initiated by performing a CBR Refresh cycle and holding  $\overline{\text{RAS}}$  LOW for the specified  $t_{\text{RAS}}$ .

The Self Refresh mode is terminated by driving  $\overline{\text{RAS}}$  HIGH for a minimum time of  $t_{\text{RPS}}$ . This delay allows for the completion of any internal refresh cycles that may be in process at the time of the  $\overline{\text{RAS}}$  LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting Self Refresh.

However, if the DRAM controller utilizes a  $\overline{\text{RAS}}$ -only or burst refresh sequence, all 512 rows must be refreshed within the average internal refresh rate, prior to the resumption of normal operation.

### Power-On

After application of the  $V_{\text{CC}}$  supply, an initial pause of 200  $\mu\text{s}$  is required followed by a minimum of eight initialization cycles (any combination of cycles containing a  $\overline{\text{RAS}}$  signal).

During power-on, it is recommended that  $\overline{\text{RAS}}$  track with  $V_{\text{CC}}$  or be held at a valid  $V_{\text{IH}}$  to avoid current surges.

Note:

1. Self Refresh is for Sversion only.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Parameters		Rating	Unit
V <sub>T</sub>	Voltage on Any Pin Relative to GND	5V	-1.0 to +7.0	V
		3.3V	-0.5 to +4.6	V
V <sub>CC</sub>	Supply Voltage	5V	-1.0 to +7.0	V
		3.3V	-0.5 to +4.6	V
I <sub>OUT</sub>	Output Current		50	mA
P <sub>D</sub>	Power Dissipation		1	W
T <sub>A</sub>	Operation Temperature	Com.	0 to +70	°C
		Ind.	-40 to +85	°C
T <sub>STG</sub>	Storage Temperature		-55 to +125	°C

### Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED OPERATING CONDITIONS (Voltages are referenced to GND)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	5V	4.5	5.0	5.5	V
		3.3V	3.0	3.3	3.6	V
V <sub>IH</sub>	Input High Voltage	5V	2.4	—	V <sub>CC</sub> + 1.0	V
		3.3V	2.0	—	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input Low Voltage	5V	-1.0	—	0.8	V
		3.3V	-0.3	—	0.8	V
T <sub>A</sub>	Ambient Temperature	Com.	0	—	70	°C
		Ind.	-40	—	85	°C

## CAPACITANCE<sup>(1,2)</sup>

Symbol	Parameter	Max.	Unit
C <sub>IN1</sub>	Input Capacitance: A0-A8	5	pF
C <sub>IN2</sub>	Input Capacitance: RAS, UCAS, LCAS, WE, OE	7	pF
C <sub>IO</sub>	Data Input/Output Capacitance: I/O0-I/O15	7	pF

### Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>CC</sub> = 5.0V + 10%, or V<sub>CC</sub> = 3.3V + 10%.

**ELECTRICAL CHARACTERISTICS<sup>(1)</sup>** (Recommended Operation Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition	Speed	Min.	Max.	Unit
I <sub>IL</sub>	Input Leakage Current	Any input $0V \leq V_{IN} \leq V_{CC}$ Other inputs not under test = $0V$		-10	10	$\mu A$
I <sub>IO</sub>	Output Leakage Current	Output is disabled (Hi-Z) $0V \leq V_{OUT} \leq V_{CC}$		-10	10	$\mu A$
V <sub>OH</sub>	Output High Voltage Level	I <sub>OH</sub> = -2.5 mA		2.4	—	V
V <sub>OL</sub>	Output Low Voltage Level	I <sub>OL</sub> = +2.1 mA		—	0.4	V
I <sub>CC1</sub>	Stand-by Current: TTL	$\overline{RAS}, \overline{LCAS}, \overline{UCAS} \geq V_{IH}$	Com. 5V Ind. 5V	—	2 3	mA mA
I <sub>CC1</sub>	Stand-by Current: TTL	$\overline{RAS}, \overline{LCAS}, \overline{UCAS} \geq V_{IH}$	Com. 3.3V Ind. 3.3V	—	1 2	mA mA
I <sub>CC2</sub>	Stand-by Current: CMOS	$\overline{RAS}, \overline{LCAS}, \overline{UCAS} \geq V_{CC} - 0.2V$	5V	—	1	mA
I <sub>CC2</sub>	Stand-by Current: CMOS	$\overline{RAS}, \overline{LCAS}, \overline{UCAS} \geq V_{CC} - 0.2V$	3.3V	—	0.5	mA
I <sub>CC3</sub>	Operating Current: Random Read/Write <sup>(2,3,4)</sup> Average Power Supply Current	$\overline{RAS}, \overline{LCAS}, \overline{UCAS}$ , Address Cycling, t <sub>RC</sub> = t <sub>RC</sub> (min.)	-35 -50 -60	—	230 180 170	mA
I <sub>CC4</sub>	Operating Current: Fast Page Mode <sup>(2,3,4)</sup> Average Power Supply Current	$\overline{RAS} = V_{IL}, \overline{LCAS}, \overline{UCAS}$ , Cycling t <sub>PC</sub> = t <sub>PC</sub> (min.)	-35 -50 -60	—	220 170 160	mA
I <sub>CC5</sub>	Refresh Current: $\overline{RAS}$ -Only <sup>(2,3)</sup> Average Power Supply Current	$\overline{RAS}$ Cycling, $\overline{LCAS}, \overline{UCAS} \geq V_{IH}$ t <sub>RC</sub> = t <sub>RC</sub> (min.)	-35 -50 -60	—	230 180 170	mA
I <sub>CC6</sub>	Refresh Current: CBR <sup>(2,3,5)</sup> Average Power Supply Current	$\overline{RAS}, \overline{LCAS}, \overline{UCAS}$ Cycling t <sub>RC</sub> = t <sub>RC</sub> (min.)	-35 -50 -60	—	230 180 170	mA
I <sub>CCS</sub>	Self Refresh current <sup>(6)</sup>	Self Refresh Mode	5V 3.3V	—	300 300	$\mu A$ $\mu A$

**Notes:**

1. An initial pause of 200  $\mu s$  is required after power-up followed by eight  $\overline{RAS}$  refresh cycles ( $\overline{RAS}$ -Only or CBR) before proper device operation is assured. The eight  $\overline{RAS}$  cycles wake-up should be repeated any time the t<sub>REF</sub> refresh requirement is exceeded.
2. Dependent on cycle rates.
3. Specified values are obtained with minimum cycle time and the output open.
4. Column-address is changed once each fast page cycle.
5. Enables on-chip refresh and address counters.
6. I<sub>CCS</sub> is for S version only.

**AC CHARACTERISTICS**<sup>(1,2,3,4,5,6)</sup>

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	-35		-50		-60		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Random READ or WRITE Cycle Time	60	—	90	—	110	—	ns
t <sub>RAC</sub>	Access Time from $\overline{\text{RAS}}^{(6,7)}$	—	35	—	50	—	60	ns
t <sub>CAC</sub>	Access Time from $\overline{\text{CAS}}^{(6,8,15)}$	—	10	—	14	—	15	ns
t <sub>AA</sub>	Access Time from Column-Address <sup>(6)</sup>	—	18	—	25	—	30	ns
t <sub>RAS</sub>	$\overline{\text{RAS}}$ Pulse Width	35	10K	50	10K	60	10K	ns
t <sub>RP</sub>	$\overline{\text{RAS}}$ Precharge Time	20	—	30	—	40	—	ns
t <sub>CAS</sub>	$\overline{\text{CAS}}$ Pulse Width <sup>(26)</sup>	6	10K	8	10K	10	10K	ns
t <sub>CP</sub>	$\overline{\text{CAS}}$ Precharge Time <sup>(9,25)</sup>	5	—	8	—	10	—	ns
t <sub>CSH</sub>	$\overline{\text{CAS}}$ Hold Time <sup>(21)</sup>	35	—	50	—	60	—	ns
t <sub>RCD</sub>	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time <sup>(10,20)</sup>	11	28	19	36	20	45	ns
t <sub>ASR</sub>	Row-Address Setup Time	0	—	0	—	0	—	ns
t <sub>RAH</sub>	Row-Address Hold Time	6	—	8	—	10	—	ns
t <sub>ASC</sub>	Column-Address Setup Time <sup>(20)</sup>	0	—	0	—	0	—	ns
t <sub>CAH</sub>	Column-Address Hold Time <sup>(20)</sup>	6	—	8	—	10	—	ns
t <sub>AR</sub>	Column-Address Hold Time (referenced to $\overline{\text{RAS}}$ )	30	—	40	—	40	—	ns
t <sub>RAD</sub>	$\overline{\text{RAS}}$ to Column-Address Delay Time <sup>(11)</sup>	12	20	14	25	15	30	ns
t <sub>RAL</sub>	Column-Address to $\overline{\text{RAS}}$ Lead Time	18	—	25	—	30	—	ns
t <sub>RPC</sub>	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	0	—	0	—	0	—	ns
t <sub>RSH</sub>	$\overline{\text{RAS}}$ Hold Time <sup>(27)</sup>	8	—	14	—	15	—	ns
t <sub>CLZ</sub>	$\overline{\text{CAS}}$ to Output in Low-Z <sup>(15,29)</sup>	3	—	3	—	3	—	ns
t <sub>CRP</sub>	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time <sup>(21)</sup>	5	—	5	—	5	—	ns
t <sub>OD</sub>	Output Disable Time <sup>(19,28,29)</sup>	3	15	3	15	3	15	ns
t <sub>OE</sub>	Output Enable Time <sup>(15,16)</sup>	—	10	—	15	—	15	ns
t <sub>OES</sub>	$\overline{\text{OE}}$ LOW to $\overline{\text{CAS}}$ HIGH Setup Time	5	—	5	—	5	—	ns
t <sub>RCS</sub>	Read Command Setup Time <sup>(17,20)</sup>	0	—	0	—	0	—	ns
t <sub>RRH</sub>	Read Command Hold Time (referenced to $\overline{\text{RAS}}$ ) <sup>(12)</sup>	0	—	0	—	0	—	ns
t <sub>RCH</sub>	Read Command Hold Time (referenced to $\overline{\text{CAS}}$ ) <sup>(12,17,21)</sup>	0	—	0	—	0	—	ns
t <sub>WCH</sub>	Write Command Hold Time <sup>(17,27)</sup>	5	—	8	—	10	—	ns
t <sub>WCR</sub>	Write Command Hold Time (referenced to $\overline{\text{RAS}}$ ) <sup>(17)</sup>	30	—	40	—	50	—	ns
t <sub>WP</sub>	Write Command Pulse Width <sup>(17)</sup>	5	—	8	—	10	—	ns
t <sub>RWL</sub>	Write Command to $\overline{\text{RAS}}$ Lead Time <sup>(17)</sup>	8	—	14	—	15	—	ns
t <sub>CWL</sub>	Write Command to $\overline{\text{CAS}}$ Lead Time <sup>(17,21)</sup>	8	—	14	—	15	—	ns
t <sub>WCS</sub>	Write Command Setup Time <sup>(14,17,20)</sup>	0	—	0	—	0	—	ns
t <sub>DHR</sub>	Data-in Hold Time (referenced to $\overline{\text{RAS}}$ )	30	—	40	—	45	—	ns

(Continued)



## AC CHARACTERISTICS<sup>(1,2,3,4,5,6)</sup>

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	-35		-50		-60		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
tACH	Column-Address Setup Time to $\overline{\text{CAS}}$ Precharge during WRITE Cycle	15	—	15	—	15	—	ns
toEH	$\overline{\text{OE}}$ Hold Time from $\overline{\text{WE}}$ during READ-MODIFY-WRITE cycle <sup>(18)</sup>	8	—	10	—	15	—	ns
tDS	Data-In Setup Time <sup>(15, 22)</sup>	0	—	0	—	0	—	ns
tDH	Data-In Hold Time <sup>(15, 22)</sup>	6	—	8	—	10	—	ns
trWC	READ-MODIFY-WRITE Cycle Time	80	—	125	—	140	—	ns
trWD	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time during READ-MODIFY-WRITE Cycle <sup>(14)</sup>	45	—	70	—	80	—	ns
tcWD	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time <sup>(14, 20)</sup>	25	—	34	—	36	—	ns
tAWD	Column-Address to $\overline{\text{WE}}$ Delay Time <sup>(14)</sup>	30	—	42	—	49	—	ns
tPC	Fast Page Mode READ or WRITE Cycle Time <sup>(24)</sup>	12	—	20	—	25	—	ns
trASP	Fast Page Mode $\overline{\text{RAS}}$ Pulse Width	35	100K	50	100K	60	100K	ns
tCPA	Access Time from $\overline{\text{CAS}}$ Precharge <sup>(15)</sup>	—	21	—	27	—	34	ns
tPRWC	Fast Page Mode READ-WRITE Cycle Time <sup>(24)</sup>	40	—	47	—	56	—	ns
toFF	Output Buffer Turn-Off Delay from $\overline{\text{CAS}}$ or $\overline{\text{RAS}}$ <sup>(13,15,19, 29)</sup>	3	15	3	15	3	15	ns
tCLCH	Last $\overline{\text{CAS}}$ going LOW to First $\overline{\text{CAS}}$ returning HIGH <sup>(23)</sup>	10	—	10	—	10	—	ns
tCSR	$\overline{\text{CAS}}$ Setup Time (CBR REFRESH) <sup>(30, 20)</sup>	8	—	10	—	10	—	ns
tCHR	$\overline{\text{CAS}}$ Hold Time (CBR REFRESH) <sup>(30, 21)</sup>	8	—	10	—	10	—	ns
tORD	$\overline{\text{OE}}$ Setup Time prior to $\overline{\text{RAS}}$ during HIDDEN REFRESH Cycle	0	—	0	—	0	—	ns
tREF	Refresh Period (512 Cycles)	—	8	—	8	—	8	ms
tT	Transition Time (Rise or Fall) <sup>(2, 3)</sup>	1	50	1	50	1	50	ns

## AC TEST CONDITIONS

Output load: Two TTL Loads and 50 pF ( $V_{CC} = 5.0V \pm 10\%$ )  
 One TTL Load and 50 pF ( $V_{CC} = 3.3V \pm 10\%$ )

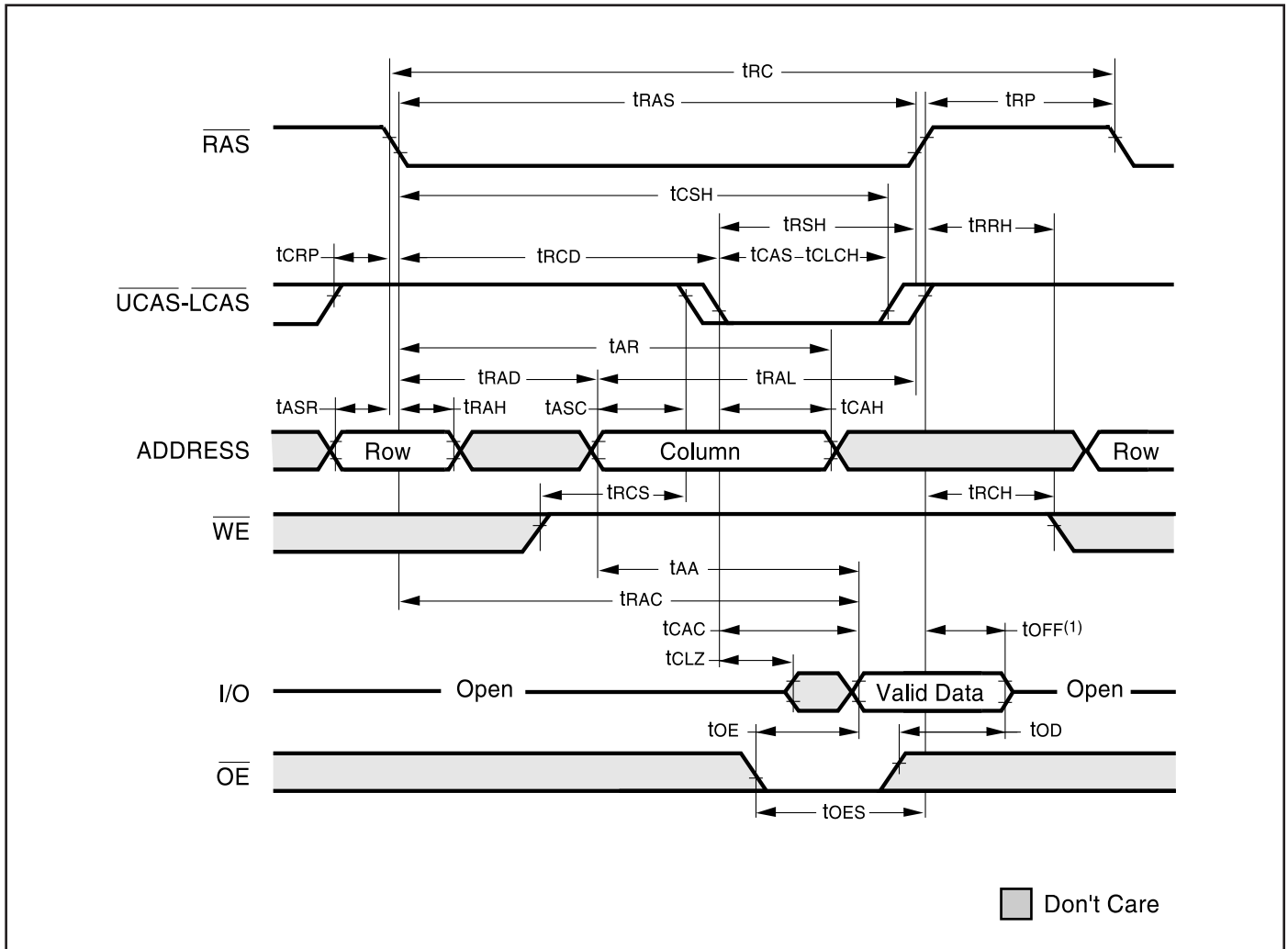
Input timing reference levels:  $V_{IH} = 2.4V$ ,  $V_{IL} = 0.8V$  ( $V_{CC} = 5.0V \pm 10\%$ );  
 $V_{IH} = 2.0V$ ,  $V_{IL} = 0.8V$  ( $V_{CC} = 3.3V \pm 10\%$ )

Output timing reference levels:  $V_{OH} = 2.0V$ ,  $V_{OL} = 0.8V$  ( $V_{CC} = 5V \pm 10\%$ ,  $3.3V \pm 10\%$ )

**Notes:**

1. An initial pause of 200  $\mu$ s is required after power-up followed by eight  $\overline{\text{RAS}}$  refresh cycle ( $\overline{\text{RAS}}$ -Only or CBR) before proper device operation is assured. The eight RAS cycles wake-up should be repeated any time the  $t_{\text{REF}}$  refresh requirement is exceeded.
2.  $V_{\text{IH}}$  (MIN) and  $V_{\text{IL}}$  (MAX) are reference levels for measuring timing of input signals. Transition times, are measured between  $V_{\text{IH}}$  and  $V_{\text{IL}}$  (or between  $V_{\text{IL}}$  and  $V_{\text{IH}}$ ) and assume to be 1 ns for all inputs.
3. In addition to meeting the transition rate specification, all input signals must transit between  $V_{\text{IH}}$  and  $V_{\text{IL}}$  (or between  $V_{\text{IL}}$  and  $V_{\text{IH}}$ ) in a monotonic manner.
4. If  $\overline{\text{CAS}}$  and  $\text{RAS} = V_{\text{IH}}$ , data output is High-Z.
5. If  $\overline{\text{CAS}} = V_{\text{IL}}$ , data output may contain data from the last valid READ cycle.
6. Measured with a load equivalent to one TTL gate and 50 pF.
7. Assumes that  $t_{\text{RCD}} \leq t_{\text{RCD}} (\text{MAX})$ . If  $t_{\text{RCD}}$  is greater than the maximum recommended value shown in this table,  $t_{\text{RAC}}$  will increase by the amount that  $t_{\text{RCD}}$  exceeds the value shown.
8. Assumes that  $t_{\text{RCD}} \geq t_{\text{RCD}} (\text{MAX})$ .
9. If  $\overline{\text{CAS}}$  is LOW at the falling edge of  $\overline{\text{RAS}}$ , data out will be maintained from the previous cycle. To initiate a new cycle and clear the data output buffer,  $\overline{\text{CAS}}$  and  $\overline{\text{RAS}}$  must be pulsed for  $t_{\text{CP}}$ .
10. Operation with the  $t_{\text{RCD}} (\text{MAX})$  limit ensures that  $t_{\text{RAC}} (\text{MAX})$  can be met.  $t_{\text{RCD}} (\text{MAX})$  is specified as a reference point only; if  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}} (\text{MAX})$  limit, access time is controlled exclusively by  $t_{\text{CAC}}$ .
11. Operation within the  $t_{\text{RAD}} (\text{MAX})$  limit ensures that  $t_{\text{RCD}} (\text{MAX})$  can be met.  $t_{\text{RAD}} (\text{MAX})$  is specified as a reference point only; if  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}} (\text{MAX})$  limit, access time is controlled exclusively by  $t_{\text{AA}}$ .
12. Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a READ cycle.
13.  $t_{\text{OFF}} (\text{MAX})$  defines the time at which the output achieves the open circuit condition; it is not a reference to  $V_{\text{OH}}$  or  $V_{\text{OL}}$ .
14.  $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{AWD}}$  and  $t_{\text{CWD}}$  are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycle only. If  $t_{\text{WCS}} \geq t_{\text{WCS}} (\text{MIN})$ , the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If  $t_{\text{RWD}} \geq t_{\text{RWD}} (\text{MIN})$ ,  $t_{\text{AWD}} \geq t_{\text{AWD}} (\text{MIN})$  and  $t_{\text{CWD}} \geq t_{\text{CWD}} (\text{MIN})$ , the cycle is a READ-WRITE cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until  $\overline{\text{CAS}}$  and  $\overline{\text{RAS}}$  or  $\overline{\text{OE}}$  go back to  $V_{\text{IH}}$ ) is indeterminate.  $\overline{\text{OE}}$  held HIGH and  $\overline{\text{WE}}$  taken LOW after  $\overline{\text{CAS}}$  goes LOW result in a LATE WRITE ( $\overline{\text{OE}}$ -controlled) cycle.
15. Output parameter (I/O) is referenced to corresponding  $\overline{\text{CAS}}$  input, I/O0-I/O7 by  $\overline{\text{LCAS}}$  and I/O8-I/O15 by  $\overline{\text{UCAS}}$ .
16. During a READ cycle, if  $\overline{\text{OE}}$  is LOW then taken HIGH before  $\overline{\text{CAS}}$  goes HIGH, I/O goes open. If  $\overline{\text{OE}}$  is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE is not possible.
17. Write command is defined as  $\overline{\text{WE}}$  going low.
18. LATE WRITE and READ-MODIFY-WRITE cycles must have both  $t_{\text{OD}}$  and  $t_{\text{OEH}}$  met ( $\overline{\text{OE}}$  HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The I/Os will provide the previously written data if  $\overline{\text{CAS}}$  remains LOW and  $\overline{\text{OE}}$  is taken back to LOW after  $t_{\text{OEH}}$  is met.
19. The I/Os are in open during READ cycles once  $t_{\text{OD}}$  or  $t_{\text{OFF}}$  occur.
20. The first  $\chi\overline{\text{CAS}}$  edge to transition LOW.
21. The last  $\chi\overline{\text{CAS}}$  edge to transition HIGH.
22. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in EARLY WRITE cycles and  $\overline{\text{WE}}$  leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. Last falling  $\chi\overline{\text{CAS}}$  edge to first rising  $\chi\overline{\text{CAS}}$  edge.
24. Last rising  $\chi\overline{\text{CAS}}$  edge to next cycle's last rising  $\chi\overline{\text{CAS}}$  edge.
25. Last rising  $\chi\overline{\text{CAS}}$  edge to first falling  $\chi\overline{\text{CAS}}$  edge.
26. Each  $\chi\overline{\text{CAS}}$  must meet minimum pulse width.
27. Last  $\chi\overline{\text{CAS}}$  to go LOW.
28. I/Os controlled, regardless  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$ .
29. The 3 ns minimum is a parameter guaranteed by design.
30. Enables on-chip refresh and address counters.

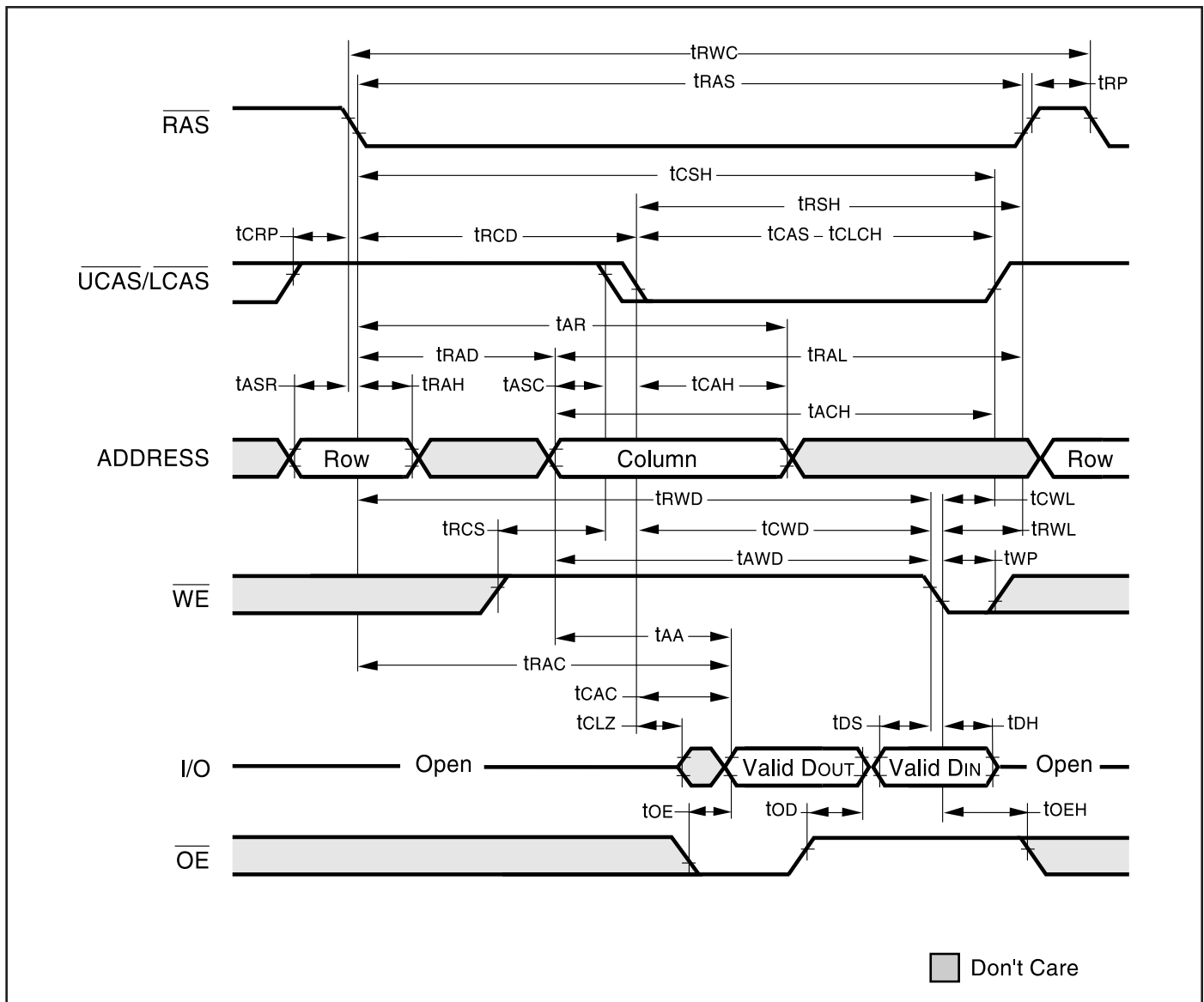
READ CYCLE



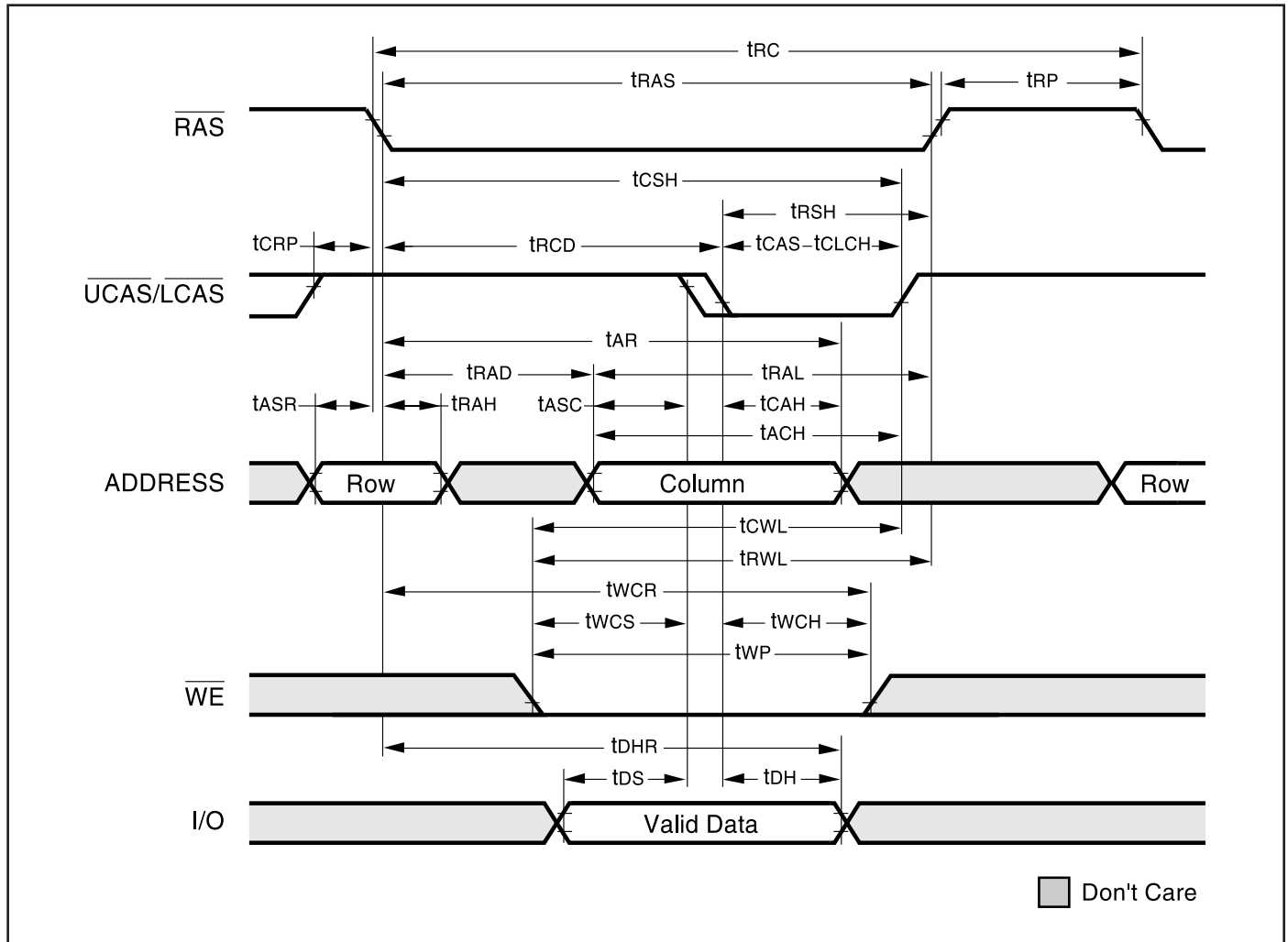
**Note:**

1.  $t_{\text{OFF}}$  is referenced from rising edge of  $\overline{\text{RAS}}$  or  $\overline{\text{CAS}}$ , whichever occurs last.

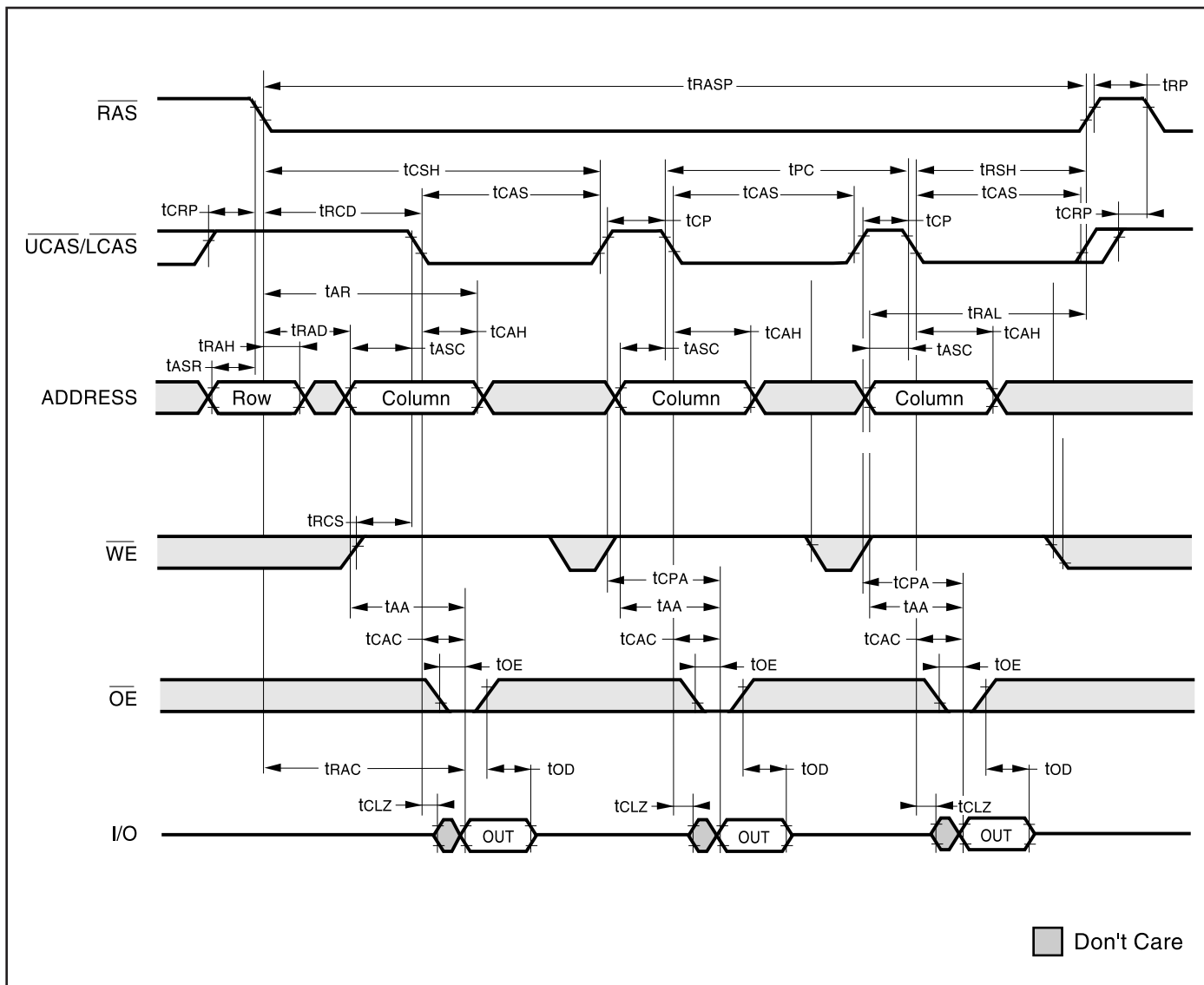
**READ WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE Cycles)**



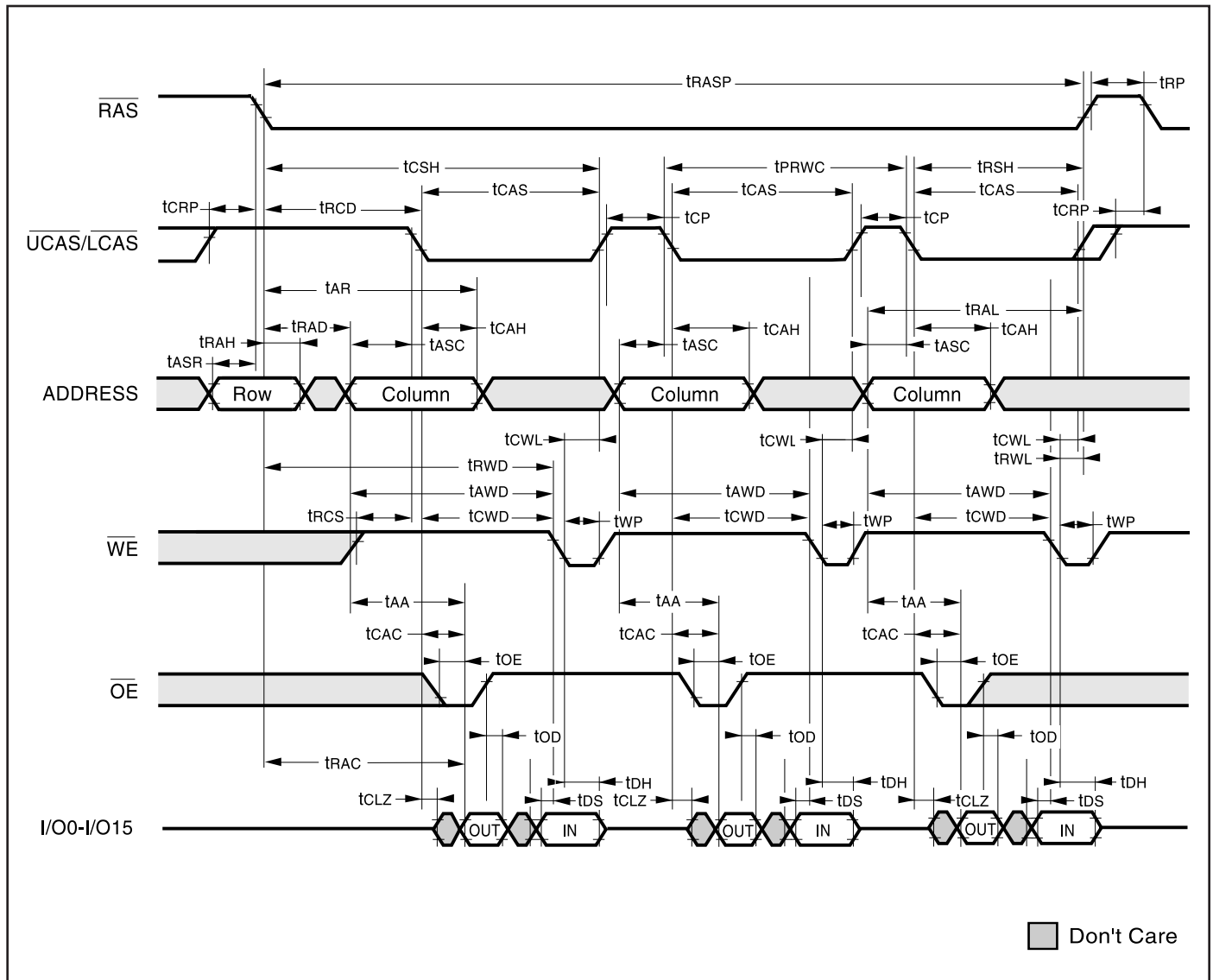
EARLY WRITE CYCLE ( $\overline{OE}$  = DON'T CARE)



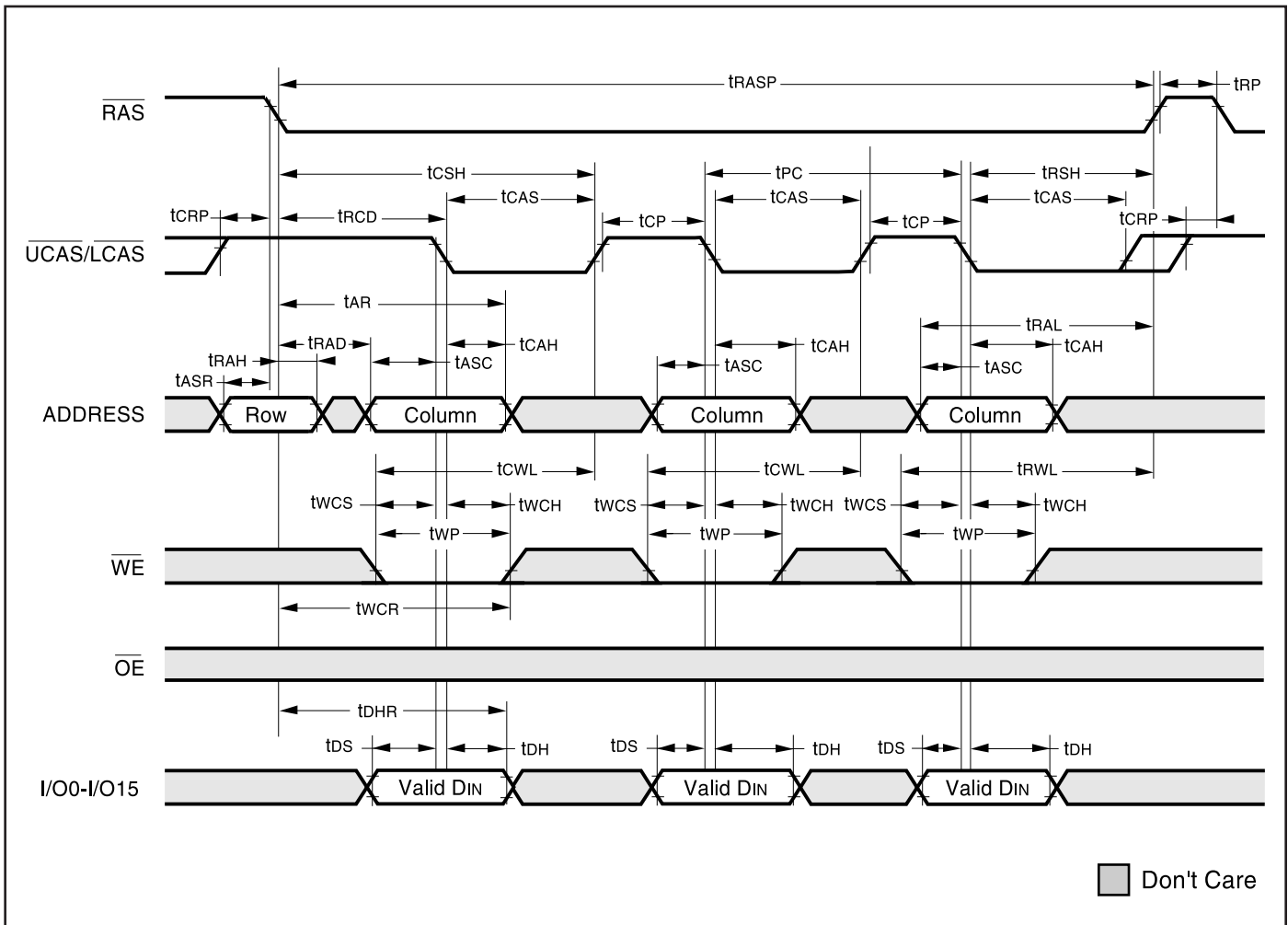
FAST PAGE MODE READ CYCLE



**FAST PAGE MODE READ WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE Cycles)**

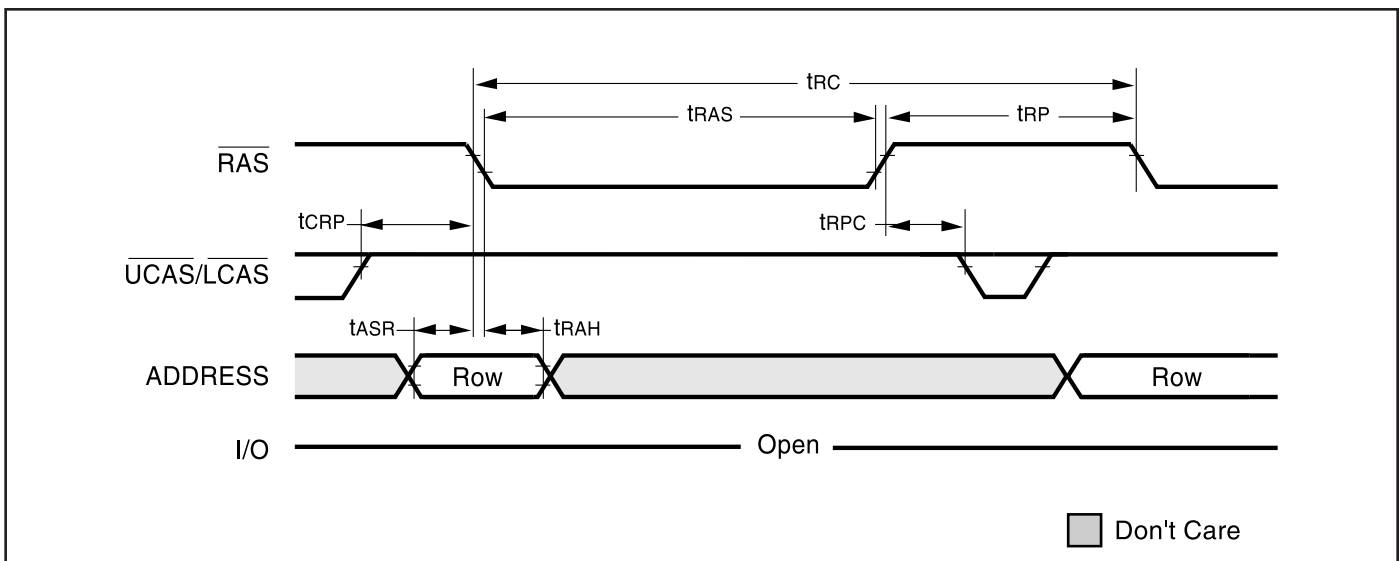


**FAST PAGE MODE EARLY WRITE CYCLE**



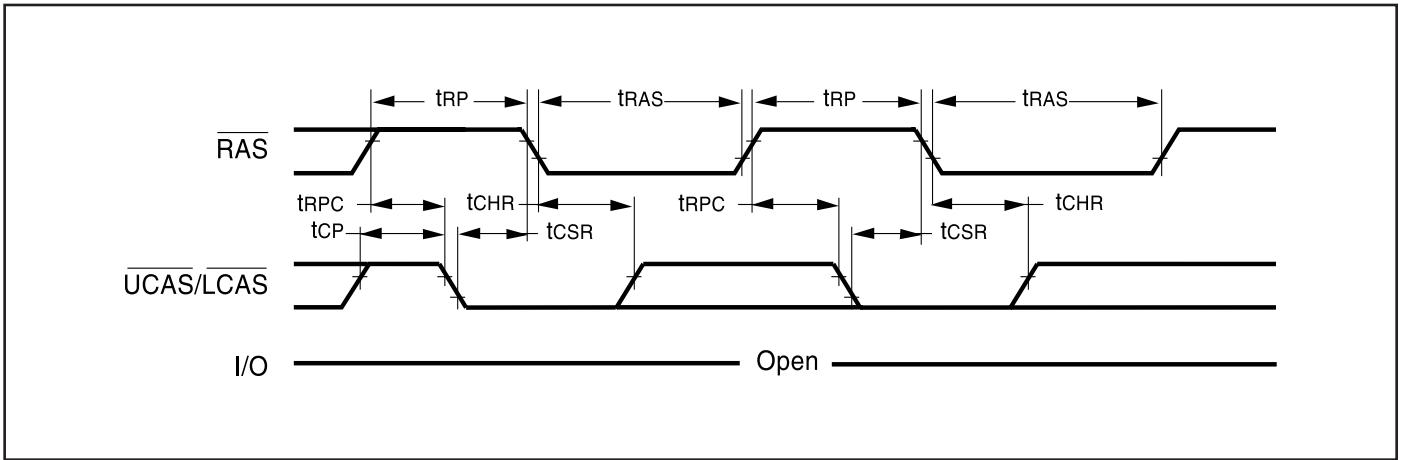
**AC WAVEFORMS**

**RAS-ONLY REFRESH CYCLE ( $\overline{OE}$ ,  $\overline{WE}$  = DON'T CARE)**

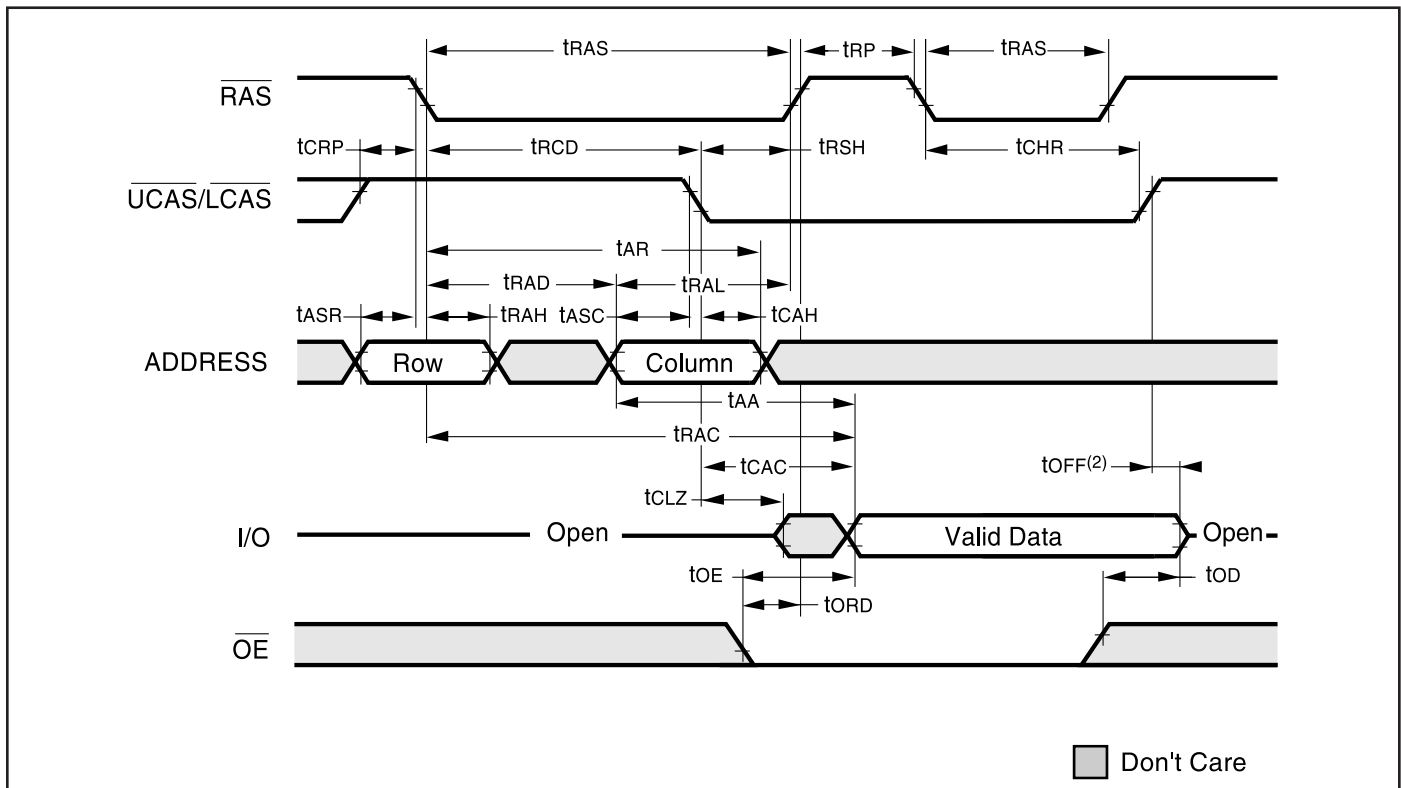




**CBR REFRESH CYCLE** (Addresses;  $\overline{WE}$ ,  $\overline{OE}$  = DON'T CARE)



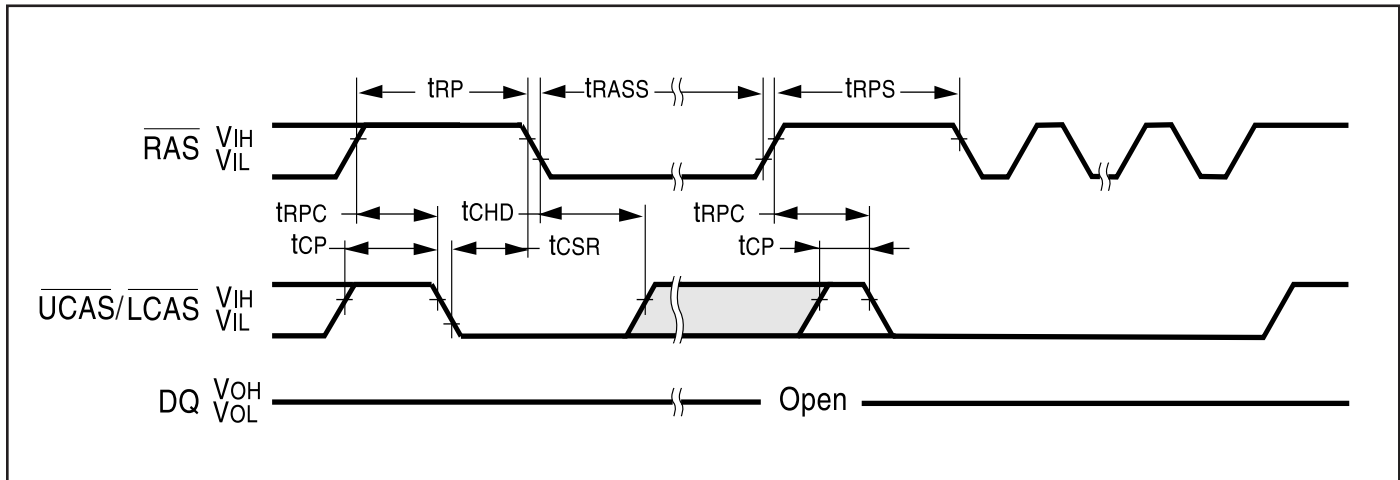
**HIDDEN REFRESH CYCLE<sup>(1)</sup>** ( $\overline{WE}$  = HIGH;  $\overline{OE}$  = LOW)



**Notes:**

1. A Hidden Refresh may also be performed after a Write Cycle. In this case,  $\overline{WE}$  = LOW and  $\overline{OE}$  = HIGH.
2.  $t_{OFF}$  is referenced from rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ , whichever occurs last.

**SELF REFRESH CYCLE** (Addresses :  $\overline{WE}$  and  $\overline{OE}$  = DON'T CARE)



**TIMING PARAMETERS**

Symbol	-35		-50		-60		Units
	Min.	Max.	Min.	Max.	Min.	Max.	
tCHD	8	—	10	—	10	—	ns
tCP	5	—	9	—	9	—	ns
tCSR	8	—	10	—	10	—	ns
tRASS	100	—	100	—	100	—	μs
tRP	20	—	30	—	40	—	ns
tRPS	64	—	84	—	104	—	ns
tRPC	5	—	5	—	5	—	ns

**ORDERING INFORMATION**

**IC41C16257**

**Commercial Range: 0°C to 70°C**

Speed (ns)	Order Part No.	Package
35	IC41C16257-35K	400mil SOJ
	IC41C16257-35T	400mil TSOP-2
50	IC41C16257-50K	400mil SOJ
	IC41C16257-50T	400mil TSOP-2
60	IC41C16257-60K	400mil SOJ
	IC41C16257-60T	400mil TSOP-2

**Industrial Range: -40°C to 85°C**

Speed (ns)	Order Part No.	Package
35	IC41C16257-35KI	400mil SOJ
	IC41C16257-35TI	400mil TSOP-2
50	IC41C16257-50KI	400mil SOJ
	IC41C16257-50TI	400mil TSOP-2
60	IC41C16257-60KI	400mil SOJ
	IC41C16257-60TI	400mil TSOP-2

**ORDERING INFORMATION**

**IC41LV16257**

**Commercial Range: 0°C to 70°C**

Speed (ns)	Order Part No.	Package
35	IC41LV16257-35K	400mil SOJ
	IC41LV16257-35T	400mil TSOP-2
50	IC41LV16257-50K	400mil SOJ
	IC41LV16257-50T	400mil TSOP-2
60	IS41LV16257-60K	400mil SOJ
	IC41LV16257-60T	400mil TSOP-2

**Industrial Range: -40°C to 85°C**

Speed (ns)	Order Part No.	Package
35	IC41LV16257-35KI	400mil SOJ
	IC41LV16257-35TI	400mil TSOP-2
50	IC41LV16257-50KI	400mil SOJ
	IC41LV16257-50TI	400mil TSOP-2
60	IC41LV16257-60KI	400mil SOJ
	IC41LV16257-60TI	400mil TSOP-2

**ORDERING INFORMATION**

**IC41C16257S**

**Commercial Range: 0°C to 70°C**

Speed(ns)	OrderPartNo.	Package
35	IC41C16257S-35K	400mil SOJ
	IC41C16257S-35T	400mil TSOP-2
50	IC41C16257S-50K	400mil SOJ
	IC41C16257S-50T	400mil TSOP-2
60	IC41C16257S-60K	400mil SOJ
	IC41C16257S-60T	400mil TSOP-2

**Industrial Range: -40°C to 85°C**

Speed(ns)	Order PartNo.	Package
35	IC41C16257S-35KI	400mil SOJ
	IC41C16257S-35TI	400mil TSOP-2
50	IC41C16257S-50KI	400mil SOJ
	IC41C16257S-50TI	400mil TSOP-2
60	IC41C16257S-60KI	400mil SOJ
	IC41C16257S-60TI	400mil TSOP-2

**ORDERING INFORMATION**

**IC41LV16257S**

**Commercial Range: 0°C to 70°C**

Speed(ns)	OrderPartNo.	Package
35	IC41LV16257S-35K	400mil SOJ
	IC41LV16257S-35T	400mil TSOP-2
50	IC41LV16257S-50K	400mil SOJ
	IC41LV16257S-50T	400mil TSOP-2
60	IS41LV16257S-60K	400mil SOJ
	IC41LV16257S-60T	400mil TSOP-2

**Industrial Range: -40°C to 85°C**

Speed(ns)	OrderPartNo.	Package
35	IC41LV16257S-35KI	400mil SOJ
	IC41LV16257S-35TI	400mil TSOP-2
50	IC41LV16257S-50KI	400mil SOJ
	IC41LV16257S-50TI	400mil TSOP-2
60	IC41LV16257S-60KI	400mil SOJ
	IC41LV16257S-60TI	400mil TSOP-2



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