OVERVIEW

The SM5021 series are crystal oscillator module ICs fabricated in NPC's Molybdenum-gate CMOS, that incorporate high-frequency, low current consumption oscillator and output buffer circuits. Highly accurate thin-film feedback resistors and high-frequency capacitors are built-in, eliminating the need for external components to make a stable 3rd overtone oscillator.

FEATURES

- 3rd overtone oscillation
- Oscillator capacitors C_G, C_D built-in
- Inverter amplifier feedback resistor built-in (A×, B× series)
- TTL input level
- Output drive capability
  - 4mA (V_{DD} = 2.7V)
  - 8mA (V_{DD} = 4.5V)
- Output three-state function
- Operating supply voltage range
  - 2.7 to 5.5V (A×, K× series)
  - 4.5 to 5.5V (B×, L× series)
- Oscillator frequency output
- 6-pin SOT (SM5021××H)
- Chip form (CF5021××)

SERIES CONFIGURATION

Version[*1]	Operating supply voltage range [V]		Recommended operating frequency range[*2] [MHz]		Built-in capacitance [pF]		gm ratio	Rf [kΩ]	Output frequency	Output level	Standby output state
	Chip	SOT	3V operation	5V operation	C_G	C_D					
SM5021AAH	4.5 to 5.5	4.5 to 5.5	×	22 to 30	8	15	1	6.0	fo	CMOS	High impedance
SM5021ABH	2.7 to 5.5	2.7 to 5.5	22 to 30	30 to 43			1	3.3			
SM5021ACH			30 to 40	43 to 55			2	3.9			
SM5021ADH			40 to 50	55 to 70			3	2.7			
SM5021AEH	2.7 to 3.6	×	50 to 70	×		12	4	2.7			
SM5021BAH	4.5 to 5.5	4.5 to 5.5	×	22 to 30	8	15	1	6.0	fo	TTL	High impedance
SM5021BBH				30 to 43			1	3.3			
SM5021BCH				43 to 55			2	3.9			
SM5021BDH				55 to 70			3	2.7			
SM5021KDH	2.7 to 5.5	2.7 to 5.5	22 to 50[*3]	22 to 70[*3]	8	15	3	–	fo	CMOS	High impedance
SM5021KEH	2.7 to 3.6	2.7 to 3.6	50 to 70[*3]	×		12	4				
SM5021LDH	4.5 to 5.5	4.5 to 5.5	×	22 to 70[*3]	8	15	3	–	fo	TTL	High impedance

*1. Chip form devices have designation CF5021××.

*2. The recommended operating frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillator frequency band is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

*3. The 3rd overtone frequency range using an external resistor to set the cutoff frequency.

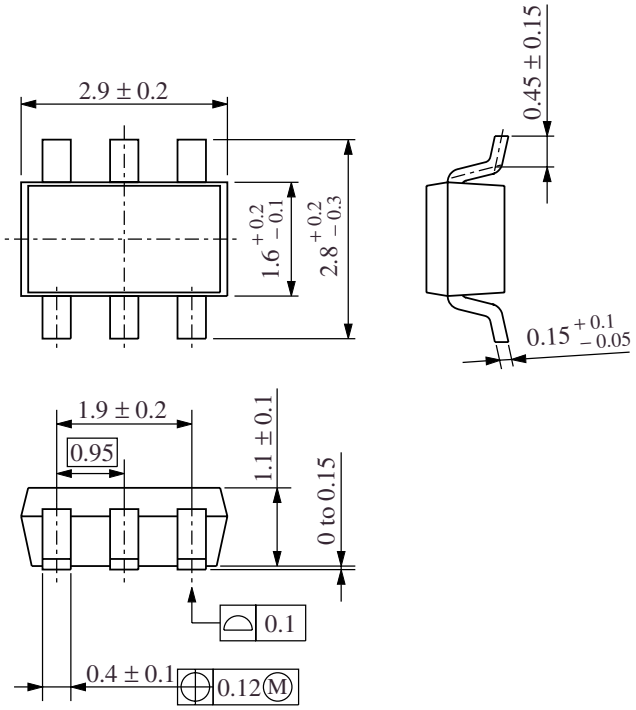
ORDERING INFORMATION

Device	Package
SM5021××H	SOT23-6
CF5021××–2	Chip form

PACKAGE DIMENSIONS

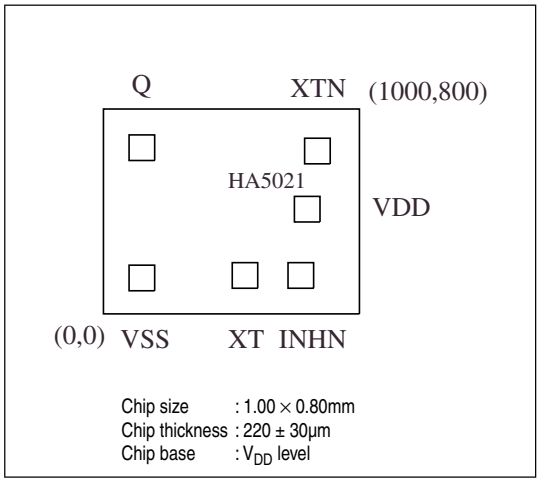
(Unit: mm)

• 6-pin SOT



PAD LAYOUT

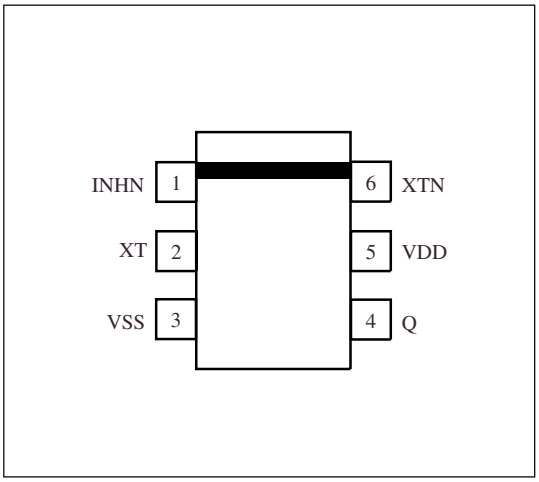
(Unit: µm)



Chip size : 1.00 × 0.80mm
Chip thickness : 220 ± 30µm
Chip base : V_{DD} level

PINOUT

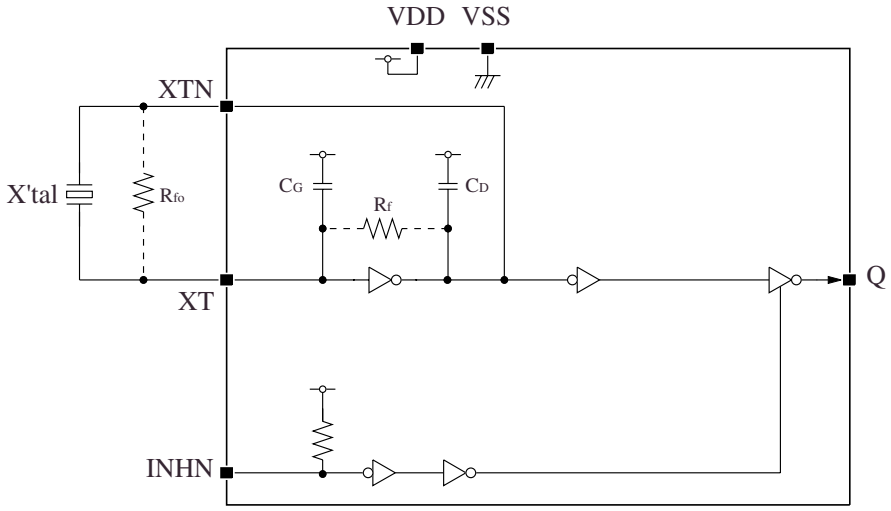
(Top view)



PIN DESCRIPTION and PAD DIMENSIONS

Number	Name	I/O	Description		Pad dimensions [µm]	
					X	Y
1	INHN	I	Output state control input. High impedance when LOW. Pull-up resistor built in		771	150
2	XT	I	Amplifier input.	Crystal oscillator connection pins. Crystal oscillator is connected between XT and XTN	553	150
3	VSS	–	Ground		150	140
4	Q	O	Output. Output frequency (f_O)		150	649
5	VDD	–	Supply voltage		796	409
6	XTN	O	Amplifier output.	Crystal oscillator connection pins. Crystal oscillator is connected between XT and XTN	836	636

BLOCK DIAGRAM



SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		– 0.5 to + 7.0	V
Input voltage range	V_{IN}		– 0.5 to V_{DD} + 0.5	V
Output voltage range	V_{OUT}		– 0.5 to V_{DD} + 0.5	V
Operating temperature range	T_{opr}		– 40 to + 85	°C
Storage temperature range	T_{stg}	Chip form	– 65 to + 150	°C
		SOT23-6	– 55 to + 125	
Output current	I_{OUT}		13	mA
Power dissipation	P_D	SOT23-6	250	mW

Recommended Operating Conditions

V_{SS} = 0V, f ≤ 70MHz, C_L ≤ 15pF

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage	V_{DD}		2.7	–	5.5	V
Input voltage	V_{IN}		V_{SS}	–	V_{DD}	V
Operating temperature	T_{OPR}		– 20	–	+ 80	°C

Note: Recommended operating conditions will change in accordance with operating frequency, load capacitance, or power dissipation.

Electrical Characteristics

3V operation: AA, AB, AC, AD, AE, KD, KE series

V_{DD} = 2.7 to 3.6V, V_{SS} = 0V, Ta = – 20 to + 80°C unless otherwise noted.

Parameter	Symbol	Condition		Rating min	Rating typ	Rating max	Unit
HIGH-level output voltage	V_{OH}	Q: Measurement cct 1, V_{DD} = 2.7V, I_{OH} = 4mA	SM5021×AH, CF5021×A SM5021×BH, CF5021×B SM5021×CH, CF5021×C SM5021×DH, CF5021×D	2.1	2.4	–	V
		Q: Measurement cct 1, V_{DD} = 2.7V, I_{OH} = 8mA	SM5021×EH, CF5021×E				
LOW-level output voltage	V_{OL}	Q: Measurement cct 2, V_{DD} = 2.7V, I_{OL} = 4mA	SM5021×AH, CF5021×A SM5021×BH, CF5021×B SM5021×CH, CF5021×C SM5021×DH, CF5021×D	–	0.3	0.4	V
		Q: Measurement cct 2, V_{DD} = 2.7V, I_{OL} = 8mA	SM5021×EH, CF5021×E				
HIGH-level input voltage	V_{IH}	INHN		2.0	–	–	V
LOW-level input voltage	V_{IL}	INHN		–	–	0.5	V
Output leakage current	I_Z	Q: Measurement cct 2, V_{DD} = 3.3V, INHN = LOW, V_{OH} = V_{DD}		–	–	10	µA
		Q: Measurement cct 2, V_{DD} = 3.3V, INHN = LOW, V_{OL} = V_{SS}		–	–	10	
Current consumption	I_{DD}	70MHz crystal oscillator, measurement cct 3, load cct 1, INHN = open, C_L = 15pF	SM5021A×H, CF5021A× SM5021K×H, CF5021K×	–	13	25	mA
INHN pull-up resistance	R_{UP}	Measurement cct 4		25	100	250	kΩ
Feedback resistance (A× series only)	R_f	Measurement cct 5	SM5021×AH, CF5021×A	5.1	6.0	6.9	kΩ
			SM5021×BH, CF5021×B	2.8	3.3	3.8	
			SM5021×CH, CF5021×C	3.3	3.9	4.5	
			SM5021×DH, CF5021×D SM5021×EH, CF5021×E	2.3	2.7	3.1	
Built-in capacitance	C_G	Design value. A monitor pattern on a wafer is tested.		7.44	8	8.56	pF
	C_D	Design value. A monitor pattern on a wafer is tested.	SM5021×AH, CF5021×A SM5021×BH, CF5021×B SM5021×CH, CF5021×C SM5021×DH, CF5021×D	13.95	15	16.05	pF
			SM5021×EH, CF5021×E	11.16	12	12.84	

5V operation: AA, AB, AC, AD, BA, BB, BC, BD, KD, LD series

V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, Ta = – 20 to + 80°C unless otherwise noted.

Parameter	Symbol	Condition		Rating min	Rating typ	Rating max	Unit
HIGH-level output voltage	V_{OH}	Q: Measurement cct 1, V_{DD} = 4.5V, I_{OH} = 8mA		3.9	4.2	–	V
LOW-level output voltage	V_{OL}	Q: Measurement cct 2, V_{DD} = 4.5V, I_{OL} = 8mA		–	0.3	0.4	V
HIGH-level input voltage	V_{IH}	INHN		2.0	–	–	V
LOW-level input voltage	V_{IL}	INHN		–	–	0.8	V
Output leakage current	I_Z	Q: Measurement cct 2, V_{DD} = 5.5V, INHN = LOW, V_{OH} = V_{DD}		–	–	10	µA
		Q: Measurement cct 2, V_{DD} = 5.5V, INHN = LOW, V_{OL} = V_{SS}		–	–	10	
Current consumption	I_{DD}	70MHz crystal oscillator, measurement cct 3, load cct 1, INHN = open, C_L = 15pF	SM5021AAH, CF5021AA SM5021ABH, CF5021AB SM5021ACH, CF5021AC SM5021ADH, CF5021AD SM5021KDH, CF5021KD	–	18	35	mA
		70MHz crystal oscillator, measurement cct 3, load cct 2, INHN = open, C_L = 15pF	SM5021B×H, CF5021B× SM5021L×H, CF5021L×	–	18	35	
INHN pull-up resistance	R_{UP}	Measurement cct 4		25	100	250	kΩ
Feedback resistance (A×, B× series only)	R_f	Measurement cct 5	SM5021×AH, CF5021×A	5.1	6.0	6.9	kΩ
			SM5021×BH, CF5021×B	2.8	3.3	3.8	
			SM5021×CH, CF5021×C	3.3	3.9	4.5	
			SM5021×DH, CF5021×D	2.3	2.7	3.1	
Built-in capacitance	C_G	Design value. A monitor pattern on a wafer is tested.	SM5021×AH, CF5021×A SM5021×BH, CF5021×B SM5021×CH, CF5021×C SM5021×DH, CF5021×D	7.44	8	8.56	pF
	C_D			13.95	15	16.05	pF

Switching Characteristics

CMOS Output Version

3V operation: AA, AB, AC, AD, AE, KD, KE series

V_{DD} = 2.7 to 3.6V, V_{SS} = 0V, Ta = – 20 to + 80°C unless otherwise noted.

Parameter	Symbol	Condition		Rating min	Rating typ	Rating max	Unit
Output rise time	t_{r1}	Measurement cct 6, load cct 1, $0.1V_{DD}$ to $0.9V_{DD}$, C_L = 15pF	SM5021AAH, CF5021AA SM5021ABH, CF5021AB SM5021ACH, CF5021AC SM5021ADH, CF5021AD SM5021KDH, CF5021KD	–	5	10	ns
			SM5021AEH, CF5021AE SM5021KEH, CF5021KE	–	3.5	7	
		Measurement cct 6, load cct 1, $0.2V_{DD}$ to $0.8V_{DD}$, C_L = 15pF	SM5021AAH, CF5021AA SM5021ABH, CF5021AB SM5021ACH, CF5021AC SM5021ADH, CF5021AD SM5021KDH, CF5021KD	–	3.5	7	
Output fall time	t_{f1}	Measurement cct 6, load cct 1, $0.9V_{DD}$ to $0.1V_{DD}$, C_L = 15pF	SM5021AAH, CF5021AA SM5021ABH, CF5021AB SM5021ACH, CF5021AC SM5021ADH, CF5021AD SM5021KDH, CF5021KD	–	5	10	ns
			SM5021AEH, CF5021AE SM5021KEH, CF5021KE	–	3.5	7	
		Measurement cct 6, load cct 1, $0.8V_{DD}$ to $0.2V_{DD}$, C_L = 15pF	SM5021AAH, CF5021AA SM5021ABH, CF5021AB SM5021ACH, CF5021AC SM5021ADH, CF5021AD SM5021KDH, CF5021KD	–	3.5	7	
Output duty cycle*1	Duty	Measurement cct 6, load cct 1, V_{DD} = 3V, Ta = 25°C, C_L = 15pF, f ≤ 70MHz		45	–	55	%
Output disable delay time	t_{PLZ}	Measurement cct 6, load cct 1, V_{DD} = 3V, Ta = 25°C, C_L = 15pF		–	–	100	ns
Output enable delay time	t_{PZL}			–	–	100	ns

*1. The duty cycle characteristic is checked the sample chips of each production lot.

5V operation: AA, AB, AC, AD, KD series

V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, Ta = – 20 to + 80°C unless otherwise noted.

Parameter	Symbol	Condition	Rating min	Rating typ	Rating max	Unit
Output rise time	t_{r1}	Measurement cct 6, load cct 1, $0.1V_{DD}$ to $0.9V_{DD}$, C_L = 15pF	–	3.5	7	ns
Output fall time	t_{f1}	Measurement cct 6, load cct 1, $0.9V_{DD}$ to $0.1V_{DD}$, C_L = 15pF	–	3.5	7	ns
Output duty cycle*1	Duty	Measurement cct 6, load cct 1, V_{DD} = 5V, Ta = 25°C, C_L = 15pF, f ≤ 70MHz	45	–	55	%
Output disable delay time	t_{PLZ}	Measurement cct 6, load cct 1, V_{DD} = 5V, Ta = 25°C, C_L = 15pF	–	–	100	ns
Output enable delay time	t_{PZL}		–	–	100	ns

*1. The duty cycle characteristic is checked the sample chips of each production lot.

TTL Output Version

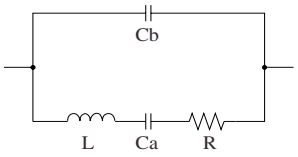
5V operation: BA, BB, BC, BD, LD series

V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, Ta = – 20 to + 80°C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Output rise time	t_{r2}	Measurement cct 6, load cct 2, 0.4V to 2.4V, C_L = 15pF	–	2.5	7	ns
Output fall time	t_{f2}	Measurement cct 6, load cct 2, 2.4V to 0.4V, C_L = 15pF	–	2.5	7	ns
Output duty cycle*1	Duty	Measurement cct 6, load cct 2, V_{DD} = 5V, Ta = 25°C, C_L = 15pF, f ≤ 70MHz	45	–	55	%
Output disable delay time	t_{PLZ}	Measurement cct 6, load cct 2, V_{DD} = 5V, Ta = 25°C, C_L = 15pF	–	–	100	ns
Output enable delay time	t_{PZL}		–	–	100	ns

*1. The duty cycle characteristic is checked the sample chips of each production lot.

Current consumption and Output waveform with NPC's standard crystal



f [MHz]	R [Ω]	L [mH]	Ca [fF]	Cb [pF]
30	18.62	16.24	1.733	5.337
40	20.53	11.34	1.396	3.989
50	22.17	7.40	1.370	4.105
60	22.20	5.05	1.388	4.226
70	25.42	4.18	1.254	5.170

FUNCTIONAL DESCRIPTION

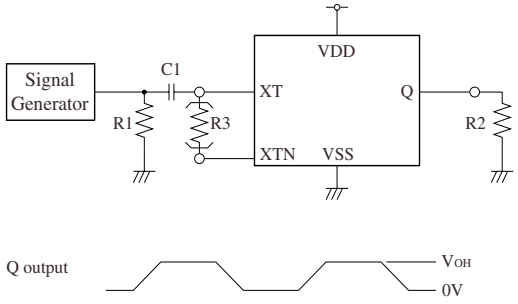
Standby Function

When INHN goes LOW, the oscillator output on Q goes high impedance.

INHN	Q	Oscillator
HIGH (or open)	f_O	Normal operation
LOW	High impedance	Normal operation

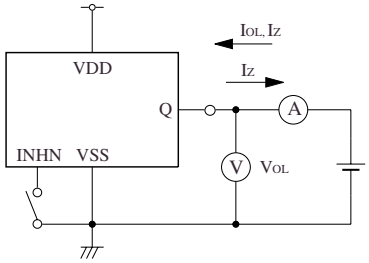
MEASUREMENT CIRCUITS

Measurement cct 1

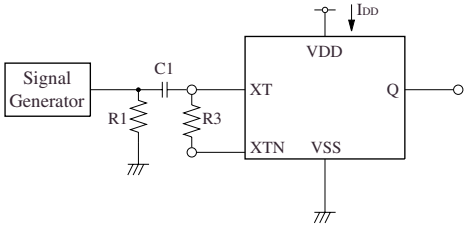


2.0Vp-p, 10MHz sine wave input signal (3V operation)
3.5Vp-p, 10MHz sine wave input signal (5V operation)
C1: 0.001µF
R1: 50Ω
R2: 525Ω (3V operation/ ×A, ×B, ×C, ×D series)
263Ω (3V operation/ ×E series)
490Ω (5V operation)
R3: 100kΩ (K×, L× series)

Measurement cct 2

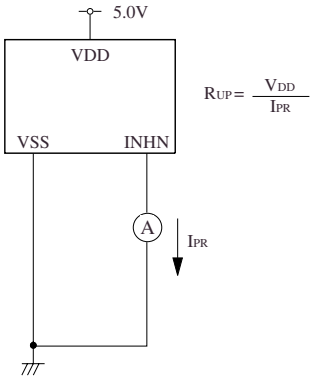


Measurement cct 3

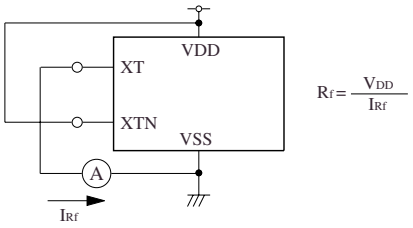


2.0Vp-p, 70MHz sine wave input signal (3V operation)
3.5Vp-p, 70MHz sine wave input signal (5V operation)
C1: 0.001µF
R1: 50Ω
R3: 100kΩ (K×, L× series)

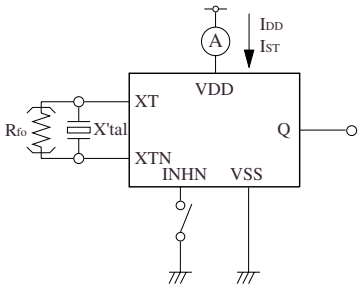
Measurement cct 4



Measurement cct 5

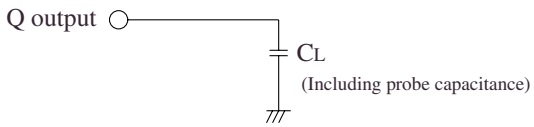


Measurement cct 6



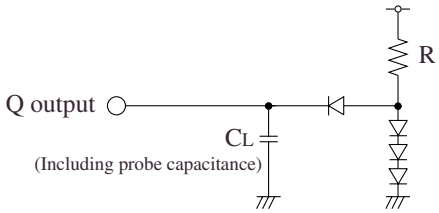
R_{fo}: 2.7kΩ (K×, L× series)

Load cct 1



C_L = 15pF: t_{r1}, t_{f1}

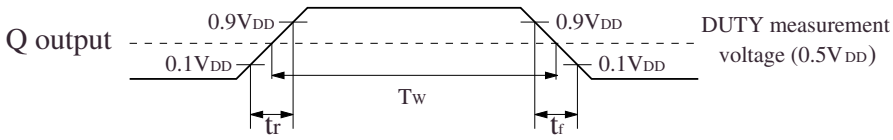
Load cct 2



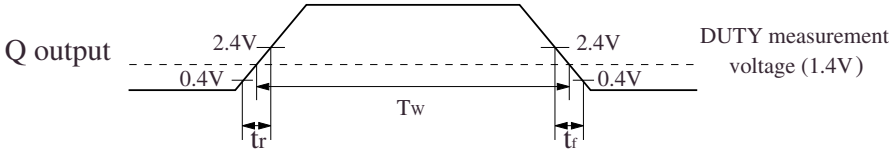
C_L = 15pF: t_{r2} , t_{f2}
R = 800Ω

Switching Time Measurement Waveform

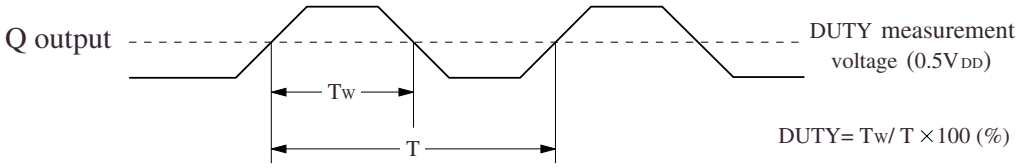
Output duty level (CMOS)



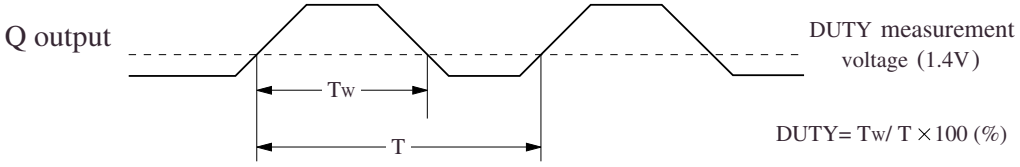
Output duty level (TTL)



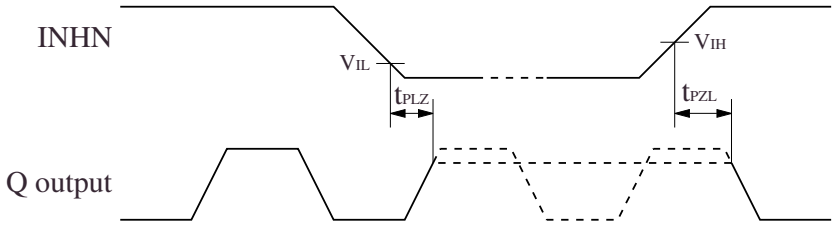
Output duty cycle (CMOS)



Output duty cycle (TTL)



Output Enable/Disable Delay



INHN input waveform $t_r = t_f \leq 10ns$

Please pay your attention to the following points at time of using the products shown in this document.

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