SYSTEM RESET IC

GENERAL DESCRIPTION NUMBER AND ADDRESS OF ADDRESS OF

NJM2103 is supply voltage supervisory IC to detect the abnormal conditions, such as shut down of all supply voltages at once, or sudden voltage down and then generate the reset signal. It supervises both 5V supply voltage and the voltage optionally set up.

FEATURES

- Precise Detection of Supply Voltage Down
- Possible Detection of Optional Voltage Down
- Possible Detection of Optional Over-loading
- Low Operating Current
- Reference Voltage can be taken out.
- Low Reset Validated Voltage
- Voltage Detection with Hystersis Feature
- Package Outline
- Bipolar Technology

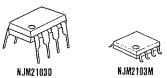
(V*=0.8V Typ.) DIP8, DMP8, SIP8

 $(V_{SA}=4.2V\pm2.5\%)$

 $(V_{SB}=1.22V \pm 1.5\%)$

 $(I_{CC} \le 560 \, \mu A @V_{SB} = 5V)$

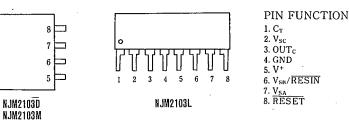
PACKAGE OUTLINE



NJM2103L

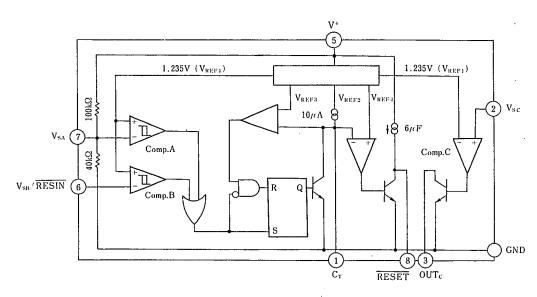
PIN CONFIGURATION

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BLOCK DIAGRAM

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ABSOLUTE MAXIMUM RATINGS

ABSOLUTE MAXIMUM RAT	(Ta=25℃)		
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V*	20	V
Power Dissipation	PD	(DIP8) 500	mW
		(DM8) 300	mW
		(SIP8) 800	mW
Input Voltage A	Vsa	V ⁺ +0.3(<20)	v
Input Voltage B	Vsb	20	v
Input Voltage C	Vsc	20	v
Operating Temperature Range	Topr	-40~+85	Ĉ
Storage Temperature Range	Tstg	-40~+125	Ĉ

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

 $(V^+=5.0V, V_{SB}=0V, V_{SC}=0V, Ta=25^{\circ}C)$. _____

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PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current (1)	Icci	V _{SB} =5V	_	380	560	μA
Operating Current (2)	I _{CC2}			460	700	μA
V _{SA} Detecting Voltage (1)	VSAL	V^+ fall time $V_{SB} = V^+$	4.10	4.20	4.30	ν
V _{SA} Detecting Voltage (2)	VSAH	V^+ rise time $V_{SB}=V^+$	4.20	4.30	4.40	ν
V _{SA} Hysterisis Width	VHRSA		50	100	150	mV
V _{SB} Detecting Voltage	V _{SBL}	V _{SB} fall time	1.202	1.220	1.238	v
V _{SB} Detecting Supply Voltage Fluctuation	ΔV_{SBL}	V*=3.5~18V	_	3	10	mV
V _{SB} Hysterisis Width	VHRSB		14	28	42	mV
V _{SB} Input Current (1)	Пнв	$V_{SB}=5V$		0	250	nA
V _{SB} Input Current (2)	1 _{ILB}			20	250	nA
High Level RESET Output Voltage	VOHR	$I_{RESET} = -5\mu A$, $V_{SB} = 5V$	4.5	4.9	—	μV
RESET Output Saturating Voltage(1)	Volri	I _{RESET} =2mA		0.20	0.40	v
RESET Output Saturating Voltage(2)	VOLR2	I _{RESET} =10mA		0.30	0.50	V _
RESET Output Sink Current	IRESET	$V_{OLR} = 1.0V$	20	80	-	mΑ
C _T Charge Current	Іст	$V_{SB}=5V, VCT=0.5V$	6.0	9.5	13.0	μA
V _{SC} Input Current (1)	LINC	$V_{SC}=5V$	-	0	500	nA
V _{SC} Input Current (2)	lilc		-	50	500	nA
V _{SC} Detecting Voltage	V _{SC}		1.215	1.235	1.255	v
V _{SC} Detecting Supply Voltage Fluctuation	ΔV_{SC}	V+=3.5~13.5V	-	3	10	mV
OUT _C Output Leak Current	Іонс	$V_{OHC} = 13.5V$	-	0	L 1	μA
OUT _C Output Saturation Voltage	VOLC	$I_{OUT} = 4mA, V_{SC} = 5V$	-	0.10	0.40	V
OUT _C Output Sink Current RESET Guarantee Minimum Supply Voltage	I _{outc} V*l	$V_{OLC}=1.0V, V_{SC}=5V$ $V_{OLR}=0.4V, I_{RESET}=200\mu A$	6	20 0.8	1.2	mA V
	1		1	1	1	1

AC CHARACTERISTICS

(V⁺=5.0V V_{SB}=5.0V, V_{SC}=0V, CT=0.01 μ F, Ta=25°C)

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
V _{SA} Input Pulse Width	teiv			3.0	_	μs
V _{SB} Input Pulse Width	tein		-	1.5		μs
RESET Output Pulse Width	tpo	V _{SB} =V ⁺	-	1.5	-	ms
RESET Rise Time	tr	$V_{SB} = V^+$, $R_L = 2.2 k\Omega$, $C_1 = 100 pF$		1.0		μs
RESET Fall Time	tr	$V_{SB} = V^+, R_L = 2.2 k\Omega, C_L = 100 pF$	-	0.1		μs
Output Delay Time	tpD	V _{SB} fall time	-	2	-	μs
Output, Delay Time	t PHL	V_{SC} rise time, $R_L = 2.2k\Omega$, $C_L = 100pF$		0.5		μs
Output Delay Time	t _{PLH}	V_{SC} fall time, $R_L = 2.2k\Omega$, $C_L = 100 pF$	-	1.0		μs

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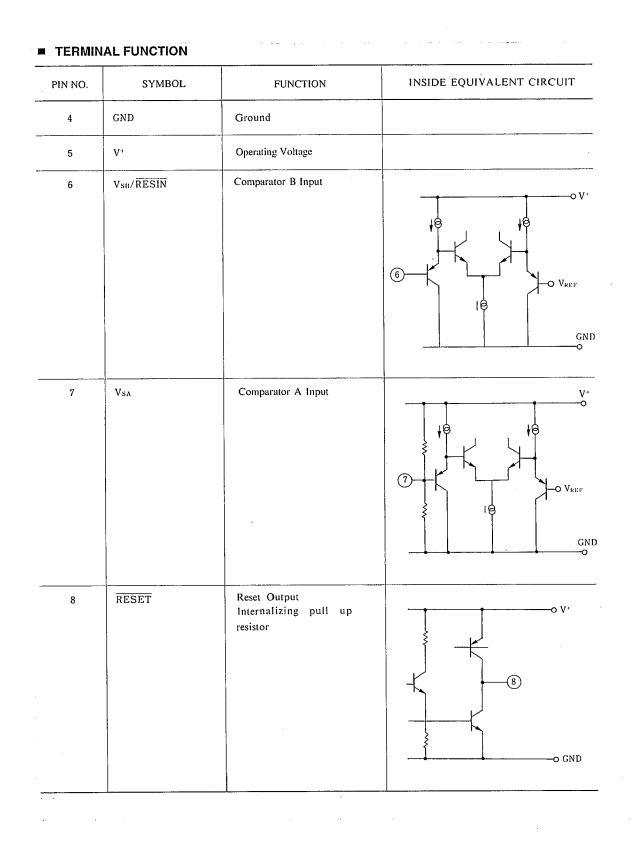
TERMINAL FUNCTION

PIN NO.	SYMBOL	FUNCTION	INSIDE EQUIVALENT CIRCUIT
1	Ст	Pin Connection to Capacitor, Set the reset holding time,	
2	Vsc .	Comparator Input	
3	OUTc	Open Collector Output of Comparator C.	

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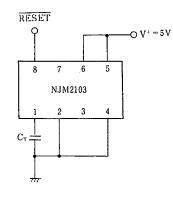
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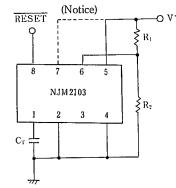
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APPLICATION CIRCUIT

1) 5V Supply Voltage Monitor



2) Monitoring of Optional Supply Voltage ($V^+ \leq 13.5V$)

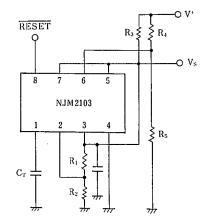


Detecting Voltage \Rightarrow (1+ $\frac{R_1}{R_2}$)×V_{SB}

(Notice)

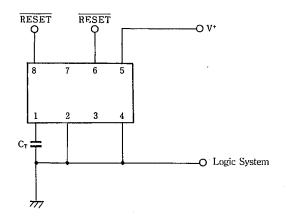
If it were that V⁺ indicates under 4.50V, Connect 7 pin to V⁺

3) Monitoring of Optional Supply Voltage (V⁺>13.5V)



 $\begin{array}{l} \text{Detecting Voltage} \doteq (1 + \frac{R_J}{R_5}) \times V_{SB} \\ \text{Constant Voltage Output } V_S \approx (1 + \frac{R_J}{R_2}) \times V_{SC} \\ \hline \hline RESET \text{ Output} = \{ \begin{matrix} V_S & (\text{High Level}) \\ OV & (\text{Low Level}) \end{matrix} \end{array}$

4) Compulsry Reset

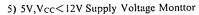


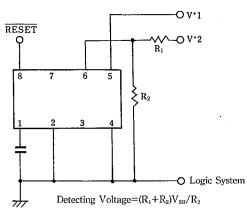
Input Reset signal TTL level to Vss-terminal

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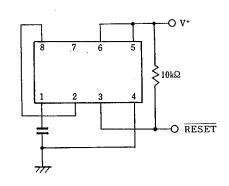
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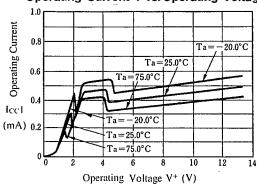
6) Non-Inverting Reset



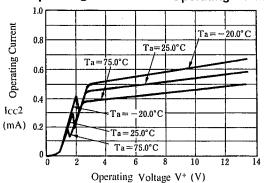
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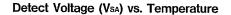
TYPICAL CHARACTERISTICS

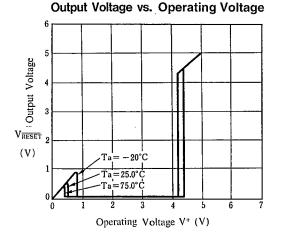


Operating Current 1 vs. Operating Voltage

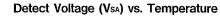


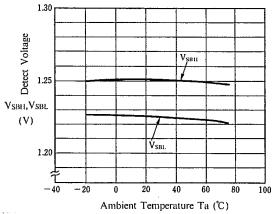
Operating Current 2 vs. Operating Voltage

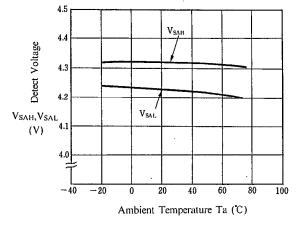


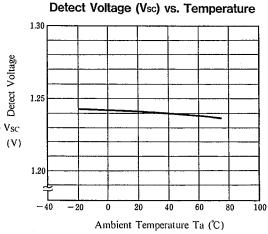


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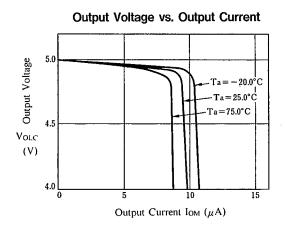
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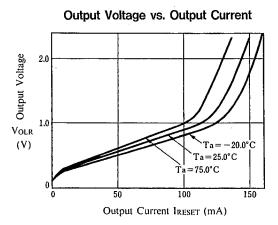
Detect Veltage (V.) up Terresentur

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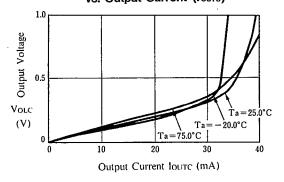
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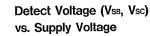
TYPICAL CHARACTERISTICS

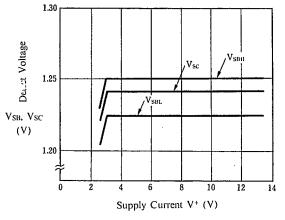


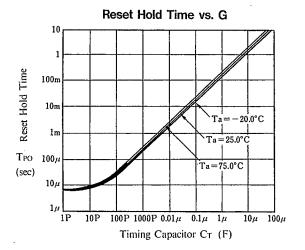


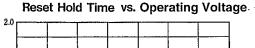
Output Voltage (OUTc) vs. Output Current (lourc)

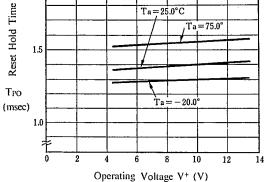












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