Features

- Precision supply-voltage monitor
  - 4.63V (PT7A7511, 7521, 7531)
  - 4.38V (PT7A7512, 7522, 7532)
  - 3.08V (PT7A7513, 7523, 7533)
  - 2.93V (PT7A7514, 7524, 7534)
  - 2.63V (PT7A7515, 7525, 7535)

- 200ms reset pulse width
- Debounced TTL/CMOS-compatible manual-reset input
- Independent watchdog timer 1.6sec time-out (not available for PT7A7531 - 7535)
- Reset output signal:
  - Active-low only (PT7A7511 - 7515)
  - Active-high only (PT7A7521 - 7525)
  - Active-high and active-low (PT7A7531 - 7535)
- Voltage monitor for power-fail or low battery warning
- Guaranteed $\overline{\text{RESET}}$/RESET valid at V_{CC} = 1.2V

Discription

The PT7A751X/752X/753X family microprocessor (µP) supervisory circuits are targeted to improve reliability and accuracy of power-supply circuitry in µP's systems. These devices reduce the complexity and number of components required to monitor power-supply and battery functions.

The main functions are:

1. Asserting reset output during power-up, power-down and brownout conditions for µP system;
2. Detecting power failure or low-battery conditions with a 1.25V threshold detector;
3. Watchdog functions (not for PT7A753x).

Applications

- Power-supply circuitry in µP systems

Ordering Information

Part No.	Package	Part No.	Package	Part No.	Package
PT7A7511P	PDIP-8	PT7A7511W	SOIC-8	PT7A7511DE	Die Form
PT7A7521P	PDIP-8	PT7A7521W	SOIC-8	PT7A7521DE	Die Form
PT7A7531P	PDIP-8	PT7A7531W	SOIC-8	PT7A7531DE	Die Form
PT7A7512P	PDIP-8	PT7A7512W	SOIC-8	PT7A7512DE	Die Form
PT7A7522P	PDIP-8	PT7A7522W	SOIC-8	PT7A7522DE	Die Form
PT7A7532P	PDIP-8	PT7A7532W	SOIC-8	PT7A7532DE	Die Form
PT7A7513P	PDIP-8	PT7A7513W	SOIC-8	PT7A7513DE	Die Form
PT7A7523P	PDIP-8	PT7A7523W	SOIC-8	PT7A7523DE	Die Form
PT7A7533P	PDIP-8	PT7A7533W	SOIC-8	PT7A7533DE	Die Form
PT7A7514P	PDIP-8	PT7A7514W	SOIC-8	PT7A7514DE	Die Form
PT7A7524P	PDIP-8	PT7A7524W	SOIC-8	PT7A7524DE	Die Form
PT7A7534P	PDIP-8	PT7A7534W	SOIC-8	PT7A7534DE	Die Form
PT7A7515P	PDIP-8	PT7A7515W	SOIC-8	PT7A7515DE	Die Form
PT7A7525P	PDIP-8	PT7A7525W	SOIC-8	PT7A7525DE	Die Form
PT7A7535P	PDIP-8	PT7A7535W	SOIC-8	PT7A7535DE	Die Form

Note: Lead free package is available by add E after each part no. For example: PT7A7511PE for PDIP-8 lead free.

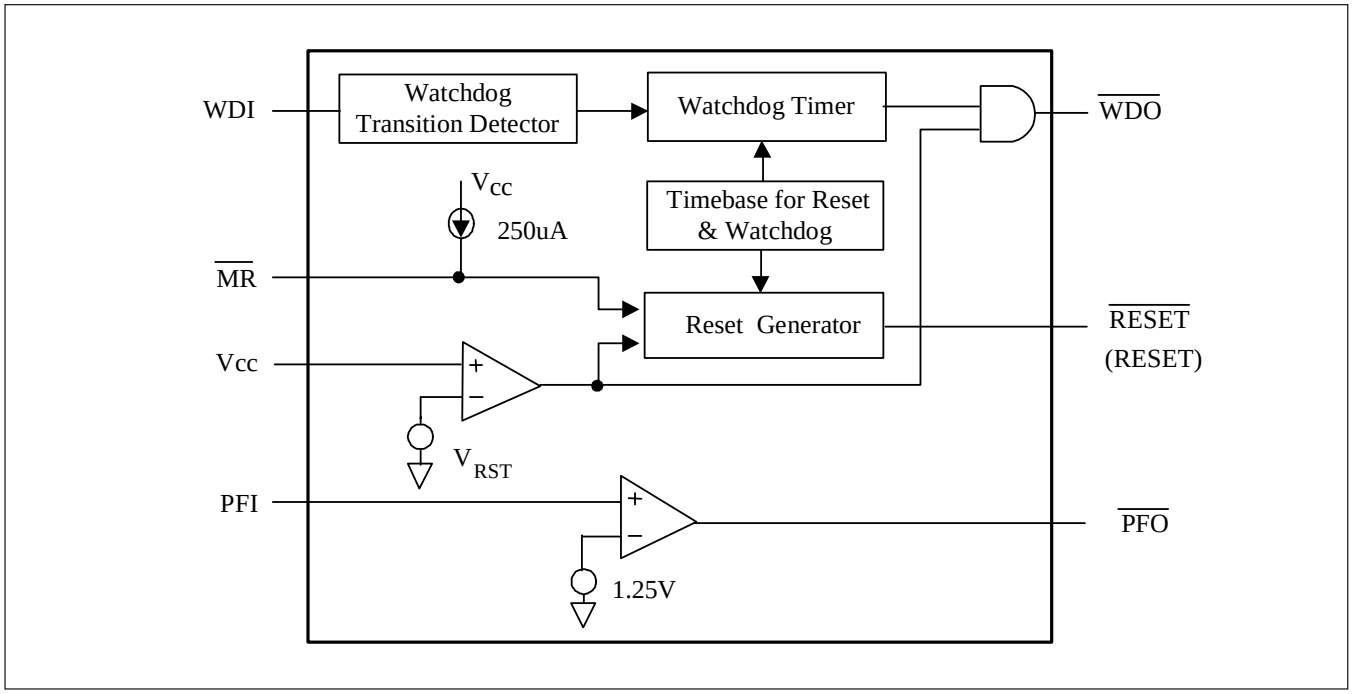
Function Comparison

Function Table of PT7A75xx Family

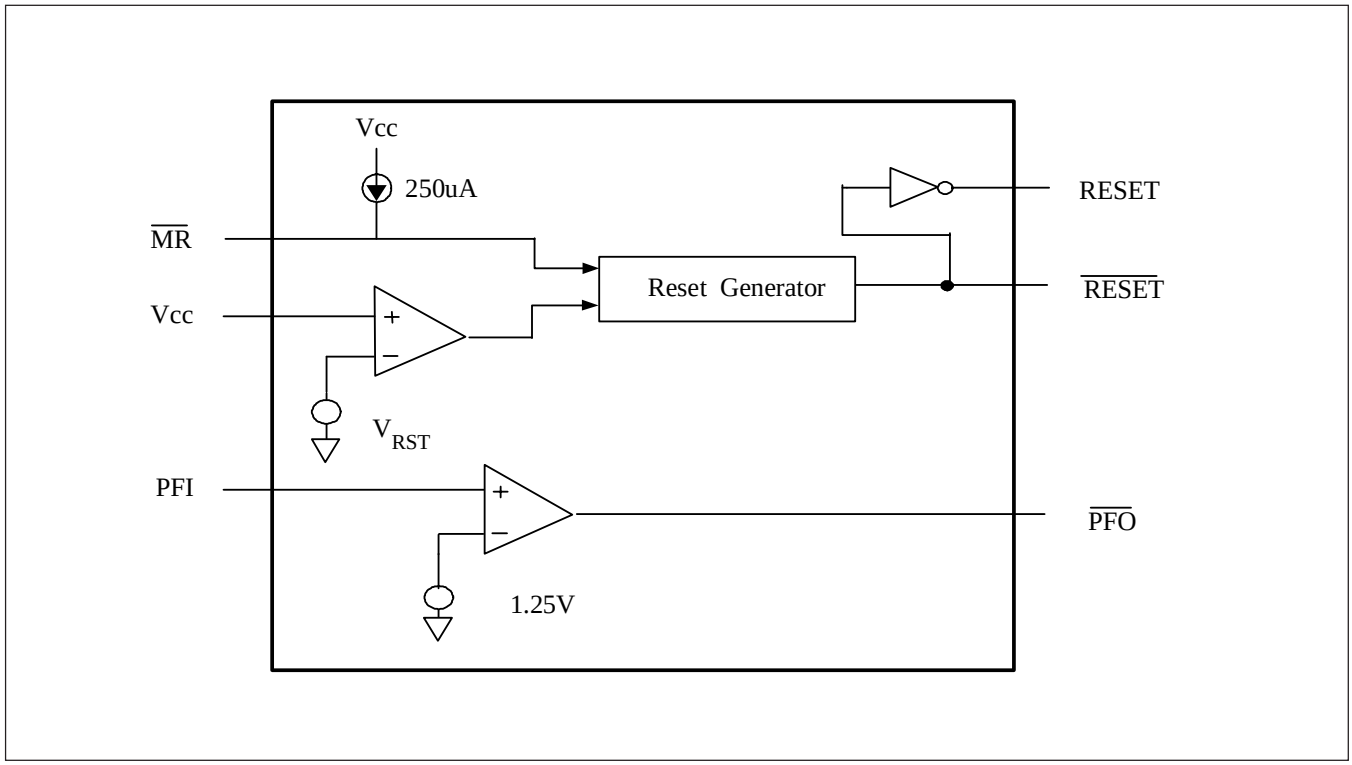
Part No.	Reset Threshold	Reset Active Low or High	Nom. Reset Time (ms), t_{RS}	Nom. Watch dog Time (sec), t_{WD}	Power Fail Comp.	Manual Reset Input
PT7A7511	4.63V	LOW	200	1.6	1.25V detector	Yes
PT7A7521	4.63V	HIGH	200	1.6	1.25V detector	Yes
PT7A7531	4.63V	LOW, HIGH	200	unavailable	1.25V detector	Yes
PT7A7512	4.38V	LOW	200	1.6	1.25V detector	Yes
PT7A7522	4.38V	HIGH	200	1.6	1.25V detector	Yes
PT7A7532	4.38V	LOW, HIGH	200	unavailable	1.25V detector	Yes
PT7A7513	3.08V	LOW	200	1.6	1.25V detector	Yes
PT7A7523	3.08V	HIGH	200	1.6	1.25V detector	Yes
PT7A7533	3.08V	LOW, HIGH	200	unavailable	1.25V detector	Yes
PT7A7514	2.93V	LOW	200	1.6	1.25V detector	Yes
PT7A7524	2.93V	HIGH	200	1.6	1.25V detector	Yes
PT7A7534	2.93V	LOW, HIGH	200	unavailable	1.25V detector	Yes
PT7A7515	2.63V	LOW	200	1.6	1.25V detector	Yes
PT7A7525	2.63V	HIGH	200	1.6	1.25V detector	Yes
PT7A7535	2.63V	LOW, HIGH	200	unavailable	1.25V detector	Yes

Block Diagram

Block Diagram of PT7A7511-7515/7521-7525



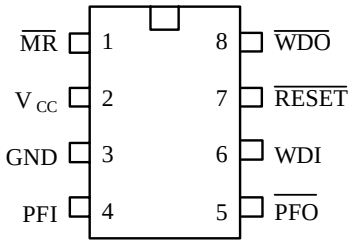
Block Diagram of PT7A7531-7535



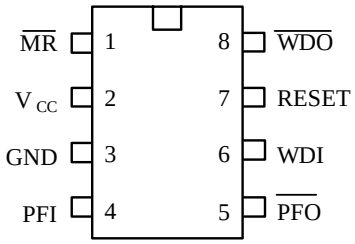
Pin Information

Pin Configuration

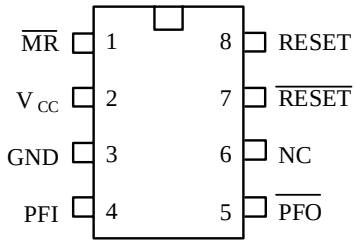
PT7A7511P-7515P
PT7A7511W-7515W
8-Pin PDIP/8-Pin SOIC



PT7A7521P-7525P
PT7A7521W-7525W
8-Pin PDIP/8-Pin SOIC



PT7A7531P-7535P
PT7A7531W-7535W
8-Pin PDIP/8-Pin SOIC



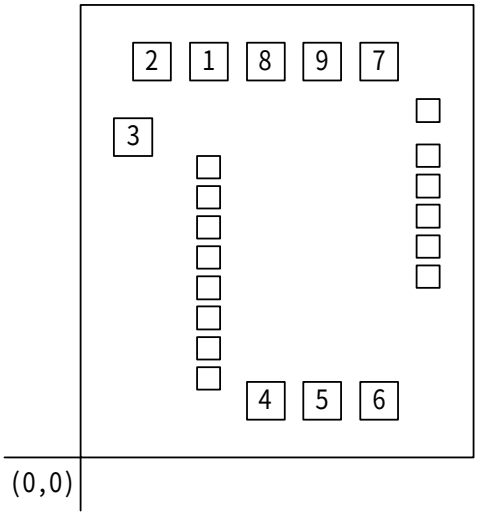
Top View

Pin Description

Pin Name	Type	Description
$\overline{MR}$	I	**Manual-Reset:** triggers a reset pulse when pulled below 0.8V, active low. It has an internal 250µA pull-up current and be driven from a TTL or CMOS logic line as well as shorted to ground with a switch.
Vcc	Power	**Power Supply**
GND	Ground	**Ground Reference** for all signals
PFI	I	**Power-Fail Voltage Monitor Input**: When PFI is less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to GND or Vcc when not used.
$\overline{PFO}$	O	**Power-Fail Output:** it gets low and sinks current when PFI is less than 1.25V; otherwise $\overline{PFO}$ stays high.
WDI	I	**Watchdog Input**: If WDI remains high or low for 1.6sec, the internal watchdog timer runs out and $\overline{WDO}$ goes low. Floating WDI or connecting WDI to a high-impedance three-state buffer disables the watchdog feature. The internal watchdog timer clears whenever reset is asserted. WDI is three-stated, or WDI sees a rising or falling edge.
NC		No Connect
$\overline{RESET}$	O	**Reset Output pulses:** low for 200ms when triggered, and stays low whenever Vcc is below the reset threshold. It remains low for 200ms after Vcc rises above the reset threshold or $\overline{MR}$ goes from low to high. A watchdog timeout will not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to $\overline{MR}$.
$\overline{WDO}$	O	**Watchdog Output**: pulls low when the internal watchdog timer finishes its 1.6sec count and does not go high again until the watchdog is cleared. $\overline{WDO}$ also goes low during low-line conditions. Whenever Vcc is below the reset threshold, $\overline{WDO}$ stays low; however, unlike $\overline{RESET}$, $\overline{WDO}$ does not have minimum pulse width. As soon as Vcc rises above the reset threshold, $\overline{WDO}$ goes high with no delay.
RESET	O	**The inverse of $\overline{RESET}$**: active high. Whenever $\overline{RESET}$ is high, RESET is low.

Pad Identification

PT7A7511, PT7A7513, PT7A7514, PT7A7515,

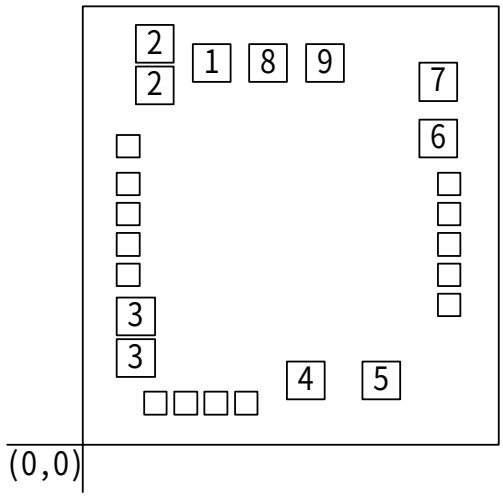


No.	Symbol	Location (X,Y)
1	$\overline{MR}$	(229.25, 815.60)
2	Vcc	(130.25, 815.60)
3	GND	(88.00, 626.80)
4	PFI	(383.75, 151.05)
5	$\overline{PFO}$	(482.95, 151.05)
6	WDI	(581.95, 151.05)
7	$\overline{RESET}$	(526.65, 815.60)
8	$\overline{WDO}$	(328.45, 815.60)
9	NC	(427.45, 815.60)

Note:

1)Wafer Size: 6 inch
2)Wafer Thickness: 675um
3)Chip Size: 810um*1060um (include scribe line width 100um*100um)
4)PAD Location: Refer above diagram and table. PAD size75um*75um
5)PAD discription refer to Pin discription

PT7A7512

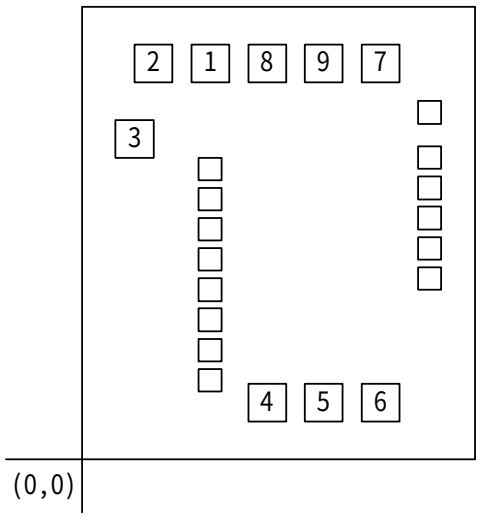


No.	Symbol	Location (X,Y)
1	$\overline{MR}$	(323.20, 973.00)
2	Vcc	(158.00, 1047.10) (158.00, 947.00)
3	GND	(123.60, 313.4) (123.60, 213.4)
4	PFI	(577.50, 149.90)
5	$\overline{PFO}$	(733.50, 149.9)
6	WDI	(893.80, 785.90)
7	$\overline{RESET}$	(893.80, 941.90)
8	$\overline{WDO}$	(479.20, 973.00)
9	NC	(605.20, 973.00)

Note:

1)Wafer Size: 6 inch
2)Wafer Thickness: 350um
3)Chip Size: 1190um*1210um (include scribe line width 150um*90um)
4)PAD Location: Refer above diagram and table. PAD size85um*85um
5)PAD discription refer to Pin discription

PT7A7521, PT7A7523, PT7A7524, PT7A7525

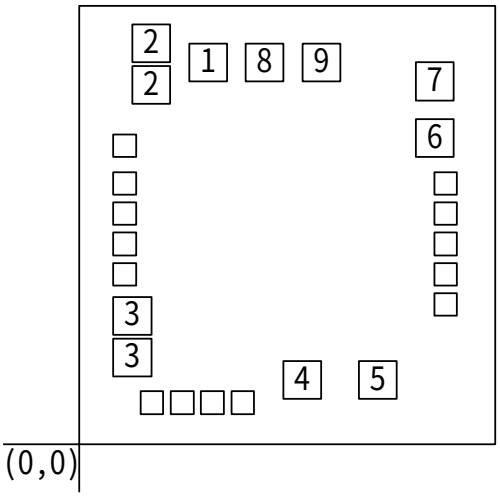


No.	Symbol	Location (X,Y)
1	$\overline{MR}$	(229.25, 815.60)
2	Vcc	(130.25, 815.60)
3	GND	(88.00, 626.80)
4	PFI	(383.75, 151.05)
5	$\overline{PFO}$	(482.95, 151.05)
6	WDI	(581.95, 151.05)
7	RESET	(526.65, 815.60)
8	$\overline{WDO}$	(328.45, 815.60)
9	NC	(427.45, 815.60)

Note:

1)Wafer Size: 6 inch
2)Wafer Thickness: 675um
3)Chip Size: 810um*1060um (include scribe line width 100um*100um)
4)PAD Location: Refer above diagram and table. PAD size75um*75um
5)PAD discription refer to Pin discription

PT7A7522

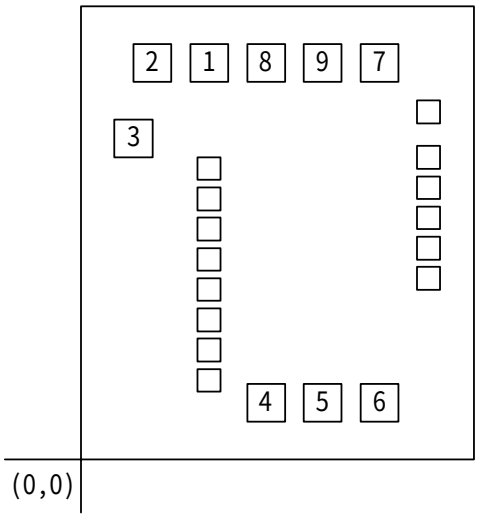


No.	Symbol	Location (X,Y)
1	$\overline{MR}$	(323.20, 973.00)
2	Vcc	(158.00, 1047.10) (158.00, 947.00)
3	GND	(123.60, 313.4) (123.60, 213.4)
4	PFI	(577.50, 149.90)
5	$\overline{PFO}$	(733.50, 149.9)
6	WDI	(893.80, 785.90)
7	RESET	(893.80, 941.90)
8	$\overline{WDO}$	(479.20, 973.00)
9	NC	(605.20, 973.00)

Note:

1)Wafer Size: 6 inch
2)Wafer Thickness: 350um
3)Chip Size: 1190um*1210um (include scribe line width 150um*90um)
4)PAD Location: Refer above diagram and table. PAD size85um*85um
5)PAD discription refer to Pin discription

PT7A7531, PT7A7534

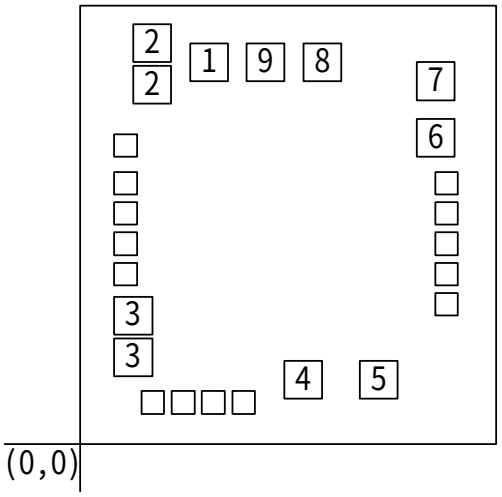


No.	Symbol	Location (X,Y)
1	$\overline{MR}$	(229.25, 815.60)
2	Vcc	(130.25, 815.60)
3	GND	(88.00, 626.80)
4	PFI	(383.75, 151.05)
5	$\overline{PFO}$	(482.95, 151.05)
6	NC	(581.95, 151.05)
7	$\overline{RESET}$	(526.65, 815.60)
8	RESET	(328.45, 815.60)
9	NC	(427.45, 815.60)

Note:

1)Wafer Size: 6 inch
2)Wafer Thickness: 675um
3)Chip Size: 810um*1060um (include scribe line width 100um*100um)
4)PAD Location: Refer above diagram and table. PAD size75um*75um
5)PAD discription refer to Pin discription

PT7A7532, PT7A7533, PT7A7535



No.	Symbol	Location (X,Y)
1	$\overline{MR}$	(323.20, 973.00)
2	Vcc	(158.00, 1047.10) (158.00, 947.00)
3	GND	(123.60, 313.4) (123.60, 213.4)
4	PFI	(577.50, 149.90)
5	$\overline{PFO}$	(733.50, 149.9)
6	NC	(893.80, 785.90)
7	$\overline{RESET}$	(893.80, 941.90)
8	RESET	(479.20, 973.00)
9	NC	(605.20, 973.00)

Note:

1)Wafer Size: 6 inch
2)Wafer Thickness: 350um
3)Chip Size: 1190um*1210um (include scribe line width 150um*90um)
4)PAD Location: Refer above diagram and table. PAD size85um*85um
5)PAD discription refer to Pin discription

Functional Description

The PT75xx family can assert reset output during power-up, power-down and brownout conditions for µP system, detect power failure or low-battery conditions with a 1.25V threshold detector and have watchdog functions. Refer to Function Table of PT7A75xx Family for their individual features. The typical application see Figure 4.

Reset Output

The supervisory circuits can assert reset for a microprocessor during power-up, power-down and brownout to prevent code execution errors.

On power-up, once V_{CC} reaches about 1.2V, $\overline{RESET}$ is a guaranteed logic low of 0.4V or less. As V_{CC} rises, $\overline{RESET}$ stays low. When V_{CC} rises above the reset threshold, an internal timer releases $\overline{RESET}$ after about 200ms. $\overline{RESET}$ pulses low whenever V_{CC} drops below the reset threshold (brownout condition). If brownout occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 140ms.

On power-down, once V_{CC} falls below the reset threshold, $\overline{RESET}$ stays low and is guaranteed to be 0.4V or less until Vcc drops below 1V.

The PT7A752x and PT7A753x active-high RESET output is simply the complement of the $\overline{RESET}$ output, and is guaranteed to be valid with V_{CC} down to 1.2V. Some µPs, such as Intel's 80C51, require an active-high reset pulse.

Watchdog Timer

The watchdog circuit monitors the µP activity. If the µP does not toggle the watchdog input (WDI) within 1.6sec and WDI is not in high impedance, $\overline{WDO}$ goes low. As long as $\overline{RESET}$ is asserted or the WDI input is in high impedance, the watchdog timer will stay cleared and will not count. As soon as reset is released and WDI is driven high or low, the timer will start counting. Pulses as short as 50ns can be detected.

Typically, $\overline{WDO}$ will be connected to the non-maskable interrupt input (NMI) of a µP. When V_{CC} drops below the reset threshold, $\overline{WDO}$ will go low whether or not the watchdog timer has timed out yet. Normally this would trigger an NMI interrupt, but $\overline{RESET}$ goes low simultaneously, and thus overrides the NMI interrupt. If WDI is left unconnected, $\overline{WDO}$ can be used as a low-line output. Since floating WDI disables the internal timer, $\overline{WDO}$ goes low only when V_{CC} falls below the reset threshold, thus functioning as a low-line output.

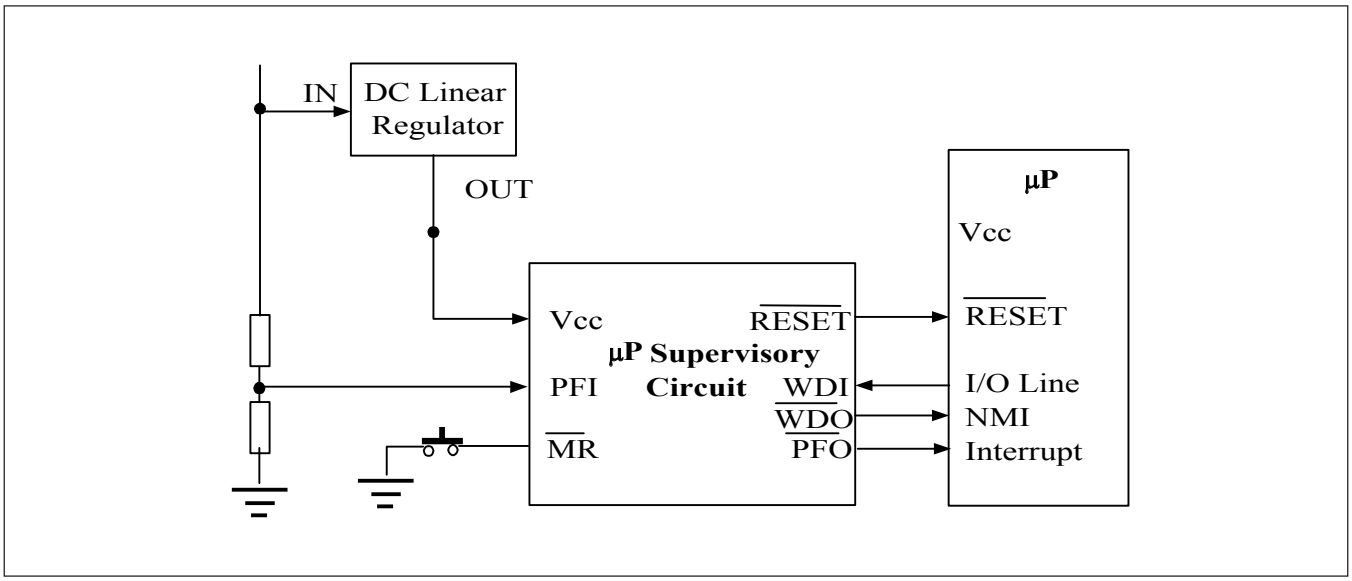
Manual Reset

The manual-reset input ($\overline{MR}$) allows reset to be triggered by a push-button switch. The switch is effectively debounced by the 140ms minimum reset pulse width. $\overline{MR}$ is TTL/CMOS logic compatible, so it can be driven by any logic reset output.

Power-Fail Comparator

The power-fail comparator will send out a Low signal once detects a voltage lowered than 1.25V. It can be used for various purposes because its output and non-inverting input are not internally connected. The inverting input is internally connected to a 1.25V reference.

Typical Application Circuit



Detailed Specifications

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Ambient Temperature with Power Applied ..... -40°C to +85°C
Supply Voltage to Ground Potential (Vcc to GND) ..... -0.3V to +7.0V
DC Input Voltage (All inputs except Vcc and GND) ..... -0.3V to V_{CC}+0.3V
DC Output Current (All outputs) 20mA
Power Dissipation 500mW
(Depend on package)

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Condition

DC Electrical Characteristics

Sym	Description	Test Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage for 75x1, 75x2		4.5	5.0	5.5	V
	Supply Voltage for 75x3, 75x4		3.0	3.3	5.5	V
	Supply Voltage for 75x5,		2.7	3.0	5.5	V
V_{IH1}	$\overline{MR}$ Input High Voltage	V_{CC} > 4.0V	2.0	2.4		V
		V_{CC} ≤ 4.0V	0.7V_{CC}			V
V_{IH2}	WDI Input High Voltage		0.7V_{CC}			V
V_{IL1}	$\overline{MR}$ Input Low Voltage	V_{CC} > 4.0V			0.8	V
		V_{CC} ≤ 4.0V			0.2V_{CC}	V
V_{IL2}	WDI Input Low Voltage				0.3V_{CC}	V
T_A	Operating Temperature		-40		85	°C

DC Electrical Characteristics

DC Electrical Characteristics

Sym	Description	Test Conditions	Min	Typ	Max	Unit
I_{CC}	Operational Power Supply Current	T7A75x1/75x2 V_{CC} = 5V PT7A75x3/75x4 V_{CC} = 3.3V PT7A75x5 V_{CC} = 3.0V Left WDI un-connected (No output load)		30	200	µA
V_{RST}	Reset Threshold Voltage *	T_A=25°C	V_{RN}-1.5%	V_{RN}	V_{RN}+1.5%	V
		PT7A75x1	4.560	4.630	4.699	
		PT7A75x2	4.314	4.380	4.446	
		PT7A75x3	3.034	3.080	3.126	
		PT7A75x4	2.886	2.930	2.974	
		PT7A75x5	2.590	2.630	2.669	
V_{RTH}	Reset Threshold Hysteresis *	V_{CC} varies between V_{RN} - 5%		70		mV
V_{OH}	Output HIGH Voltage	Vcc > 4.5V Isource=800µA	V_{CC}-1.5			V
		Vcc > 2.7V Isource=500µA	0.8V_{CC}			
		Vcc >1.8V Isource=150µA	0.8V_{CC}			
V_{OL}	Output LOW Voltage	Vcc > 4.5V Isink=3.2mA			0.4	V
		Vcc > 2.7V Isink=1.2mA			0.3	
		Vcc > 1.2V Isink=100µA			0.3	
V_{PFT}	PFI Input Threshold	V_{PFI} varies from1.0V to 1.5V (T_A = 25°C)	1.23	1.25	1.27	V
		V_{PFI} varies from1.0V to 1.5V	1.20	1.25	1.30	V
I_{PFI}	PFI Input Current	PFI connected to V_{CC}			2.00	µA
		PFI connected to GND	-2.00			
I_{WDI}	Average WDI Input Current**	WDI connected to V_{CC}		30	100	µA
		WDI connected to GND	-100	-30		
I_{MR}	$\overline{MR}$ Input Current	$\overline{MR}$ = 0, V_{CC}= 5V	-600	-250	-100	µA

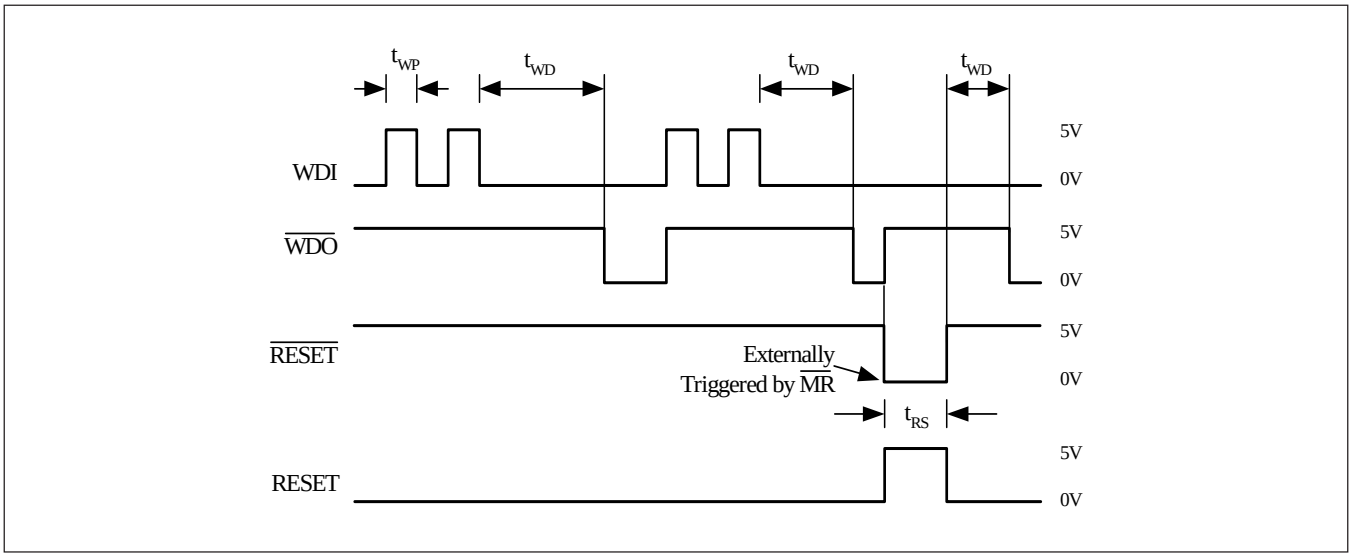
* Valid for both $\overline{RESET}$ and RESET. V_{RST} is voltage threshold when Vcc falls from high to low. V_{RN} is nominal reset threshold voltage.
** WDI is internally serviced within the watchdog period if WDI is left unconnected.

AC Electrical Characteristics

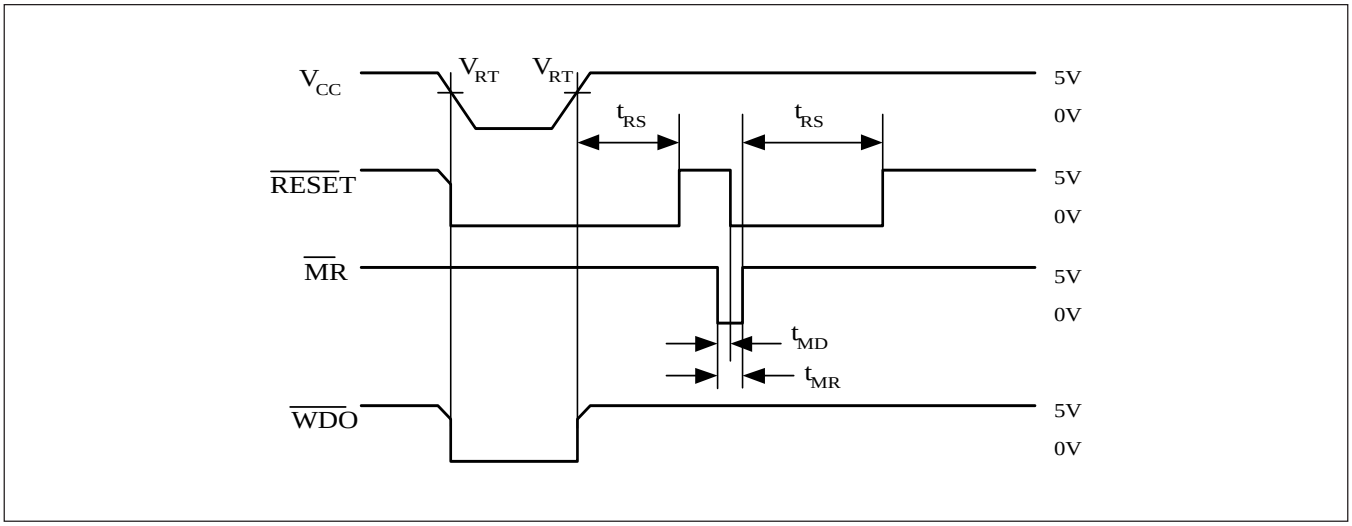
AC Electrical Characteristics

Sym	Description	Test Conditions	Min	Typ	Max	Units
t_{RS}	Reset Pulse Width	$\overline{MR}$ from low to High	140	200	280	ms
t_{WD}	Watchdog Timeout Period	WDI and $\overline{MR}$ tied to V_{CC}, $V_{CC} > V_{RN} + 5\%$	1.0	1.6	2.25	s
t_{MR}	$\overline{MR}$ Pulse Width		150			ns
t_{MD}	$\overline{MR}$ to RESET Delay	V_{CC} = 5.0V			250	ns
t_{WP}	WDI Pulse Width		50			ns

Watchdog Timing Diagram

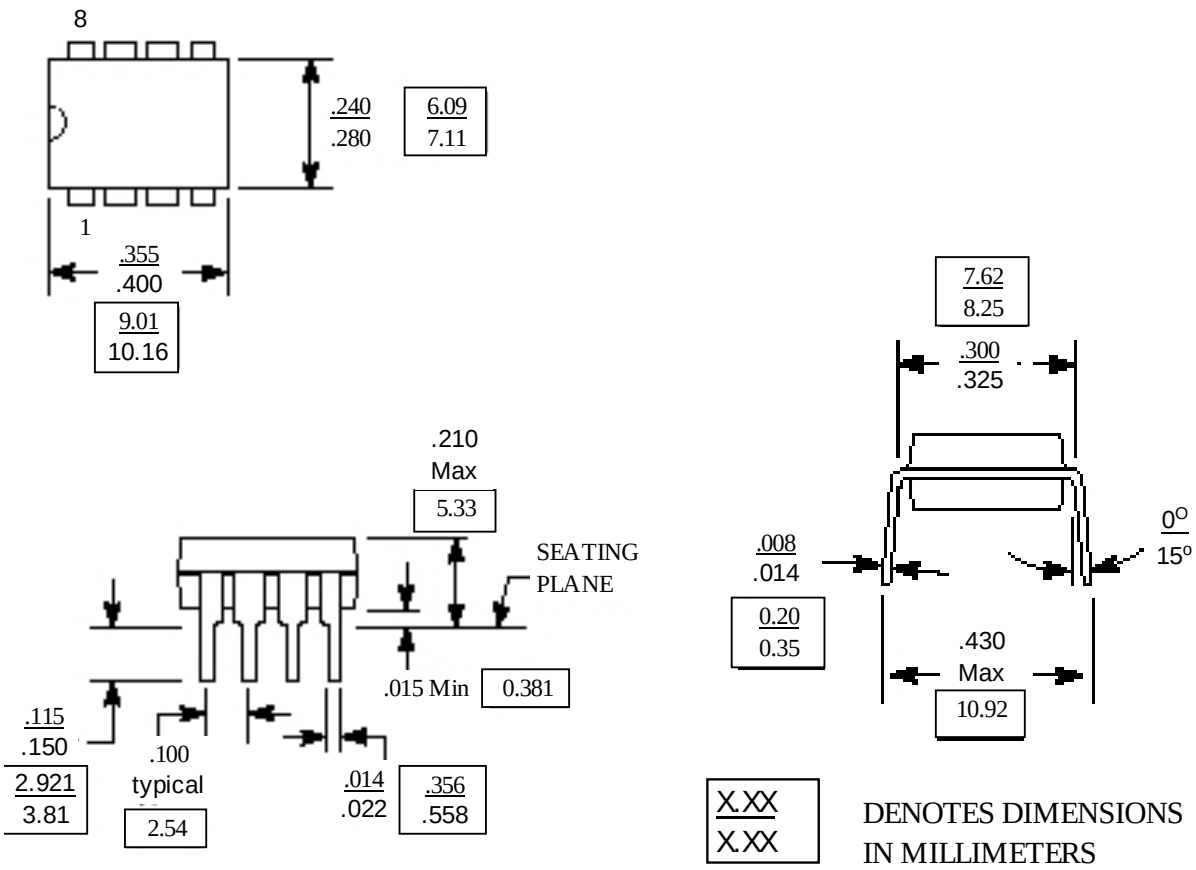


Watchdog Timing Diagram



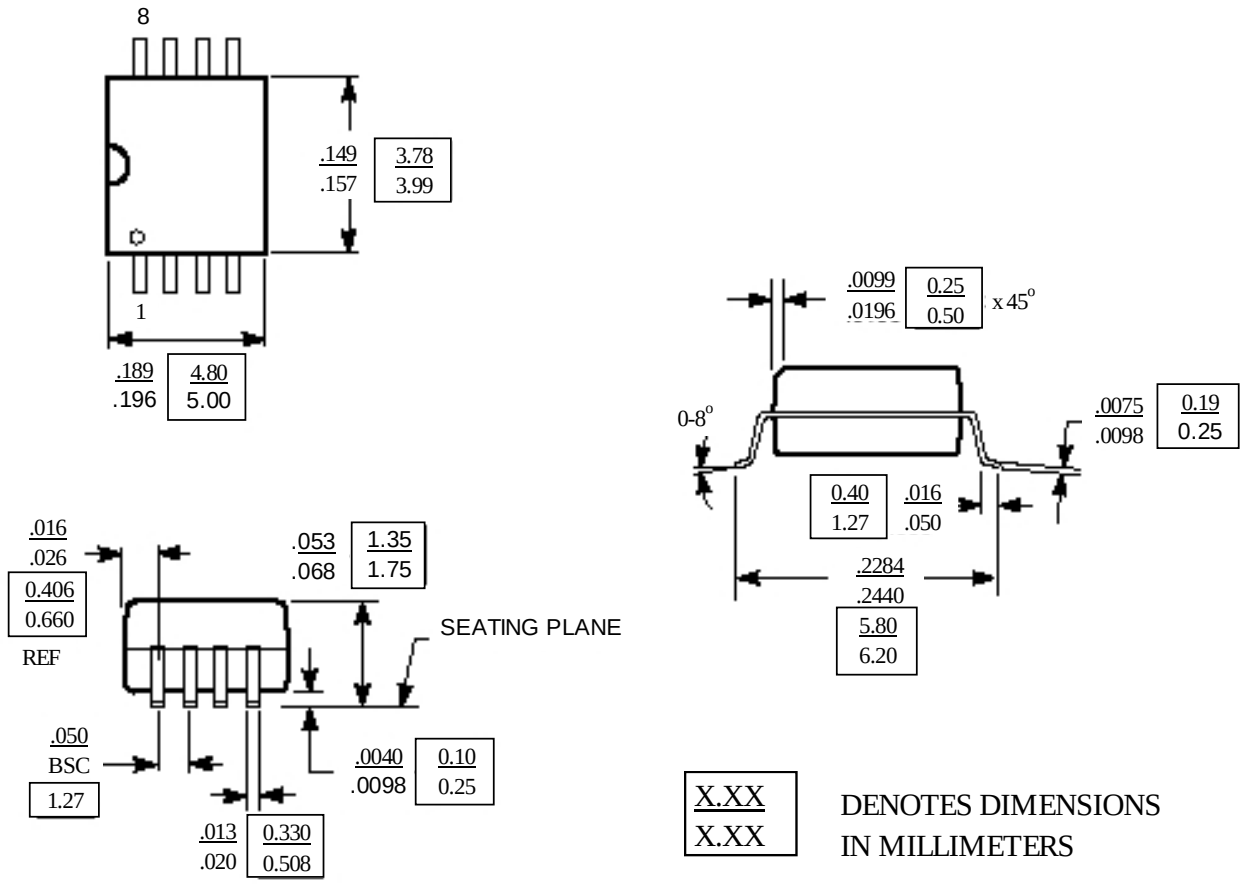
Mechanical Information

P/PE (8-Pin PDIP)



Note:
1) Controlling dimensions in inches.
2) Ref: JEDEC MS-001 BA

W/WE (8-Pin SOIC)



Note:
1) Controlling dimensions in millimeters.
2) Ref: JEDEC MS-012 AA

Notes

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