NIPPON PRECISION CIRCUITS INC.

SM5876AM

3rd-order ΣΔ, 2-channel D/A Converter

OVERVIEW

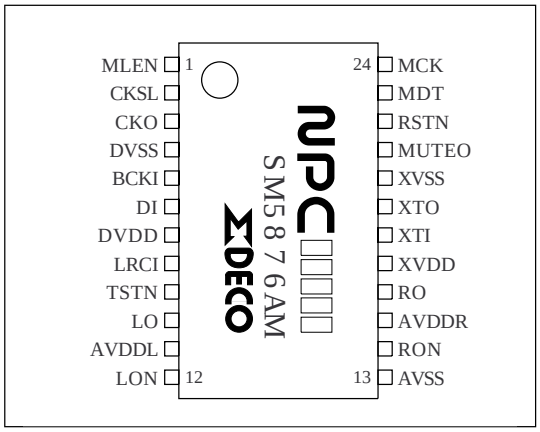
The SM5876AM is a 3rd-order ΣΔ, 2-channel D/A converter LSI for CD-ROM digital audio reproduction equipment. It incorporates an 8-times oversampling digital filter, deemphasis filter, attenuator, and soft mute circuits built-in., using NPC's Molybdenum-gate CMOS technology.

The SM5876AM operates from a 2.7 to 5.5 V supply, and is available in 24-pin SSOPs.

FEATURES

- System clock
  - 768fs (33.8688MHz)
  - 384fs (16.9344MHz)
- Crystal oscillator circuit built-in
- Infinity-zero detector circuit built-in
- MSB first, rear-packed serial data input format (≤ 64fs bit clock)
- 8-times oversampling digital filter
  - 32 dB stopband attenuation
  - ±0.05 dB passband ripple
  - –0.34 dB passband correction for 70 kHz LPF
- 3-line microcontroller interface for output mode and attenuator control settings
- 16 output modes
- Deemphasis filter operation
  - 36 dB stopband attenuation
  - –0.09 to +0.23 dB deviation
  - –0.34 dB passband correction for 70 kHz LPF
- Attenuator
  - 8-bit attenuator (linear 256 steps)
  - Independent left/right-channel set function
  - Soft mute function (approx. 1024/fs mute time)
- ΣΔ 2-channel D/A converter
  - 3rd-order noise shaper
  - 32fs oversampling
- 44.1 kHz sampling frequency
- 2.7 to 5.5 V operating supply voltage range (4.5 to 5.5 V operating supply voltage range with 768fs system clock)
- 24-pin SSOP
- Molybdenum-gate CMOS process

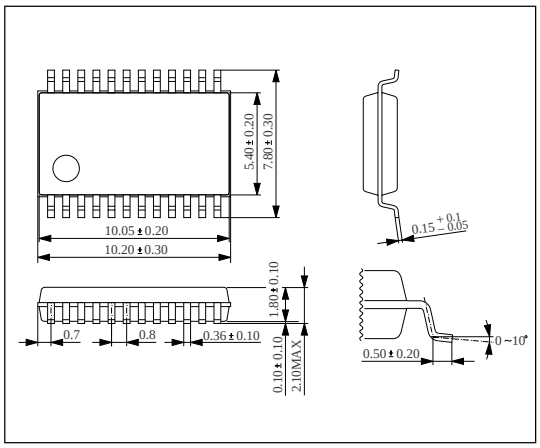
PINOUT



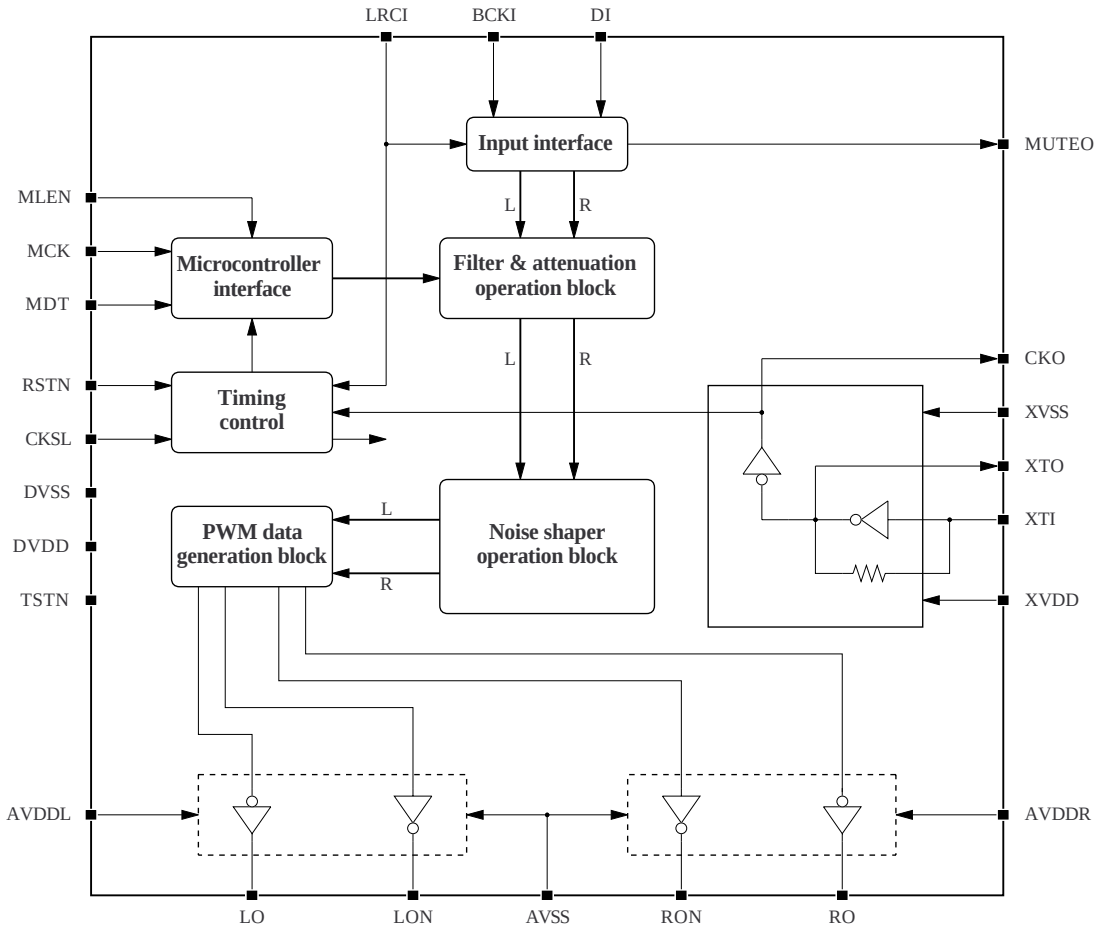
PACKAGE DIMENSIONS

Unit: mm

24-pin SSOP



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Description
1	MLEN	Ip	Microcontroller control latch clock input
2	CKSL	Ip	768fs/384fs clock select. 768fs when HIGH, and 384fs when LOW.
3	CKO	O	Oscillator clock buffer output
4	DVSS		Digital ground pin
5	BCKI	Ip	Data bit clock input pin
6	DI	Ip	Serial data input pin
7	DVDD		Digital supply pin
8	LRCI	Ip	Sample data rate (fs) clock input pin. Left channel when HIGH, and right channel when LOW.
9	TSTN	Ip	Test input pin
10	LO	O	Left-channel analog output (+)
11	AVDDL		Left-channel analog supply pin
12	LON	O	Left-channel analog output (–)
13	AVSS		Analog ground pin
14	RON	O	Right-channel analog output (–)

Number	Name	I/O	Description
15	AVDDR		Right-channel analog supply pin
16	RO	O	Right-channel analog output (+)
17	XVDD		Crystal oscillator supply pin
18	XTI	I	Crystal oscillator or external clock input pin
19	XTO	O	Crystal oscillator output pin
20	XVSS		Crystal oscillator ground pin
21	MUTEO	O	Infinity-zero detector output (analog mute control)
22	RSTN	Ip	Reset pin. Reset when LOW.
23	MDT	Ip	Microcontroller control data input pin
24	MCK	Ip	Microcontroller control clock input pin

I: INPUT O: OUTPUT Ip: Input with pull-up Registor

SPECIFICATIONS

Absolute Maximum Ratings

$DV_{SS} = AV_{SS} = XV_{SS} = 0$ V, $AV_{DD} = AV_{DDL} = AV_{DDR}$

Parameter	Symbol	Rating	Unit
Supply voltage range	DV_{DD}, AV_{DD}, XV_{DD}	–0.3 to 7.0	V
Input voltage range[1]	V_{IN1}	DV_{SS} – 0.3 to DV_{DD} + 0.3	V
XTI input voltage range	V_{IN}	XV_{SS} – 0.3 to XV_{DD} + 0.3	V
Storage temperature range	T_{stg}	–40 to 125	°C
Power dissipation	P_D	250	mW
Soldering temperature	T_{sld}	255	°C
Soldering time	t_{sld}	10	s

1. Pins MLEN, CKSL, BCKI, DI, LRCI, TSTN, MCK, MDT.
Also applicable during supply switching.

Recommended Operating Conditions

5 V operation: $DV_{SS} = AV_{SS} = XV_{SS} = 0$ V, $AV_{DD} = AV_{DDL} = AV_{DDR}$

Parameter	Symbol	Rating	Unit
Supply voltage range	DV_{DD}, AV_{DD}, XV_{DD}	4.5 to 5.5	V
Supply voltage variation	$DV_{DD} – XV_{DD}$, $DV_{DD} – AV_{DD}$, $XV_{DD} – AV_{DD}$, $DV_{SS} – XV_{SS}$, $DV_{SS} – AV_{SS}$, $XV_{SS} – AV_{SS}$	±0.1	V
Operating temperature range	T_{opr}	–40 to 85	°C

3 V operation: $DV_{SS} = AV_{SS} = XV_{SS} = 0$ V, $AV_{DD} = AV_{DDL} = AV_{DDR}$, CKSL = LOW (384fs)

Parameter	Symbol	Rating	Unit
Supply voltage range	DV_{DD}, AV_{DD}, XV_{DD}	2.7 to 4.5	V
Supply voltage variation	$DV_{DD} - XV_{DD}$, $DV_{DD} - AV_{DD}$, $XV_{DD} - AV_{DD}$, $DV_{SS} - XV_{SS}$, $DV_{SS} - AV_{SS}$, $XV_{SS} - AV_{SS}$	±0.1	V
Operating temperature range	T_{opr}	–20 to 70	°C

DC Electrical Characteristics

5 V operation: $DV_{SS} = AV_{SS} = XV_{SS} = 0$ V, $DV_{DD} = AV_{DD} = XV_{DD} = 4.5$ to 5.5 V, $AV_{DD} = AV_{DDL} = AV_{DDR}$, $T_a = -40$ to 85 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
DVDD digital supply current[1]	I_{DDD}		–	15	25	mA
XVDD system clock supply current[1]	I_{DDX}		–	6	10	mA
AVDD analog supply current[1]	I_{DDA}	Total current	–	1	2	mA
XTI HIGH-level input voltage	V_{IH1}	Clock input	$0.7XV_{DD}$	–	–	V
XTI LOW-level input voltage	V_{IL1}	Clock input	–	–	$0.3XV_{DD}$	V
XTI AC-coupled input voltage	V_{INAC}		$0.3XV_{DD}$	–	–	V_{p-p}
HIGH-level input voltage[2]	V_{IH2}		2.4	–	–	V
LOW-level input voltage[2]	V_{IL2}		–	–	0.5	V
HIGH-level output voltage[3]	V_{OHA}	$I_{OH} = -1$ mA	$AV_{DD} - 0.4$	–	–	V
LOW-level output voltage[3]	V_{OLA}	$I_{OL} = 1$ mA	–	–	0.4	V
CKO HIGH-level output voltage	V_{OHC}	$I_{OH} = -1$ mA	$DV_{DD} - 0.4$	–	–	V
CKO LOW-level output voltage	V_{OLC}	$I_{OL} = 1$ mA	–	–	0.4	V
XTI HIGH-level input current	I_{IH1}	$V_{IN} = XV_{DD}$	–	12	25	µA
XTI LOW-level input current	I_{IL1}	$V_{IN} = 0$ V	–	12	25	µA
LOW-level input current[2]	I_{IL2}	$V_{IN} = 0$ V	–	12	25	µA
Input leakage current[2]	I_{LH}	$V_{IN} = DV_{DD}$	–	–	1.0	µA

1. $DV_{DD} = AV_{DD} = XV_{DD} = 5$ V, CKSL = HIGH (768fs), XTI clock input frequency $f_{XTI} = 33.8688$ MHz, no output load, NPC-standard input data pattern.
2. Pins MLEN, CKSL, BCKI, DI, LRCI, TSTN, MCK, MDT.
3. Pins LO, LON, RO, RON,MUTEO.

3 V operation: $DV_{SS} = AV_{SS} = XV_{SS} = 0$ V, $DV_{DD} = AV_{DD} = XV_{DD} = 2.7$ to 4.5 V, $AV_{DD} = AV_{DDL} = AV_{DDR}$, $T_a = -20$ to 70 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
DVDD digital supply current[1]	I_{DDD}		–	6	9	mA
XVDD system clock supply current[1]	I_{DDX}		–	1.5	3	mA
AVDD analog supply current[1]	I_{DDA}	Total current	–	0.5	1	mA
XTI HIGH-level input voltage	V_{IH1}	Clock input	$0.7XV_{DD}$	–	–	V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
XTI LOW-level input voltage	V_{IL1}	Clock input	–	–	$0.3XV_{DD}$	V
XTI AC-coupled input voltage	V_{INAC}		$0.3XV_{DD}$	–	–	V_{p-p}
HIGH-level input voltage[2]	V_{IH2}		2.4	–	–	V
LOW-level input voltage[2]	V_{IL2}		–	–	0.5	V
HIGH-level output voltage[3]	V_{OHA}	I_{OH} = –0.5 mA	AV_{DD} – 0.4	–	–	V
LOW-level output voltage[3]	V_{OLA}	I_{OL} = 0.5 mA	–	–	0.4	V
CKO HIGH-level output voltage	V_{OHC}	I_{OH} = –0.5 mA	DV_{DD} – 0.4	–	–	V
CKO LOW-level output voltage	V_{OLC}	I_{OL} = 0.5 mA	–	–	0.4	V
XTI HIGH-level input current	I_{IH1}	$V_{IN} = XV_{DD}$	–	4	15	µA
XTI LOW-level input current	I_{IL1}	V_{IN} = 0 V	–	4	15	µA
LOW-level input current[2]	I_{IL2}	V_{IN} = 0 V	–	4	15	µA
Input leakage current[2]	I_{LH}	$V_{IN} = DV_{DD}$	–	–	1.0	µA

1. $DV_{DD} = AV_{DD} = XV_{DD}$ = 3 V, CKSL = LOW (384fs), XTI clock input frequency f_{XTI} = 16.9344 MHz, no output load, NPC-standard input data pattern.
2. Pins MLEN, CKSL, BCKI, DI, LRCI, TSTN, MCK, MDT.
3. Pins LO, LON, RO, RON,MUTEO.

AC Electrical Characteristics

5 V operation: $DV_{SS} = AV_{SS} = XV_{SS}$ = 0 V, $DV_{DD} = AV_{DD} = XV_{DD}$ = 4.5 to 5.5 V, $AV_{DD} = AV_{DDL} = AV_{DDR}$, T_a = –40 to 85 °C

3 V operation: $DV_{SS} = AV_{SS} = XV_{SS}$ = 0 V, $DV_{DD} = AV_{DD} = XV_{DD}$ = 2.7 to 4.5 V, $AV_{DD} = AV_{DDL} = AV_{DDR}$, T_a = –20 to 70 °C, CKSL = LOW (384fs system clock)

System clock (XTI)

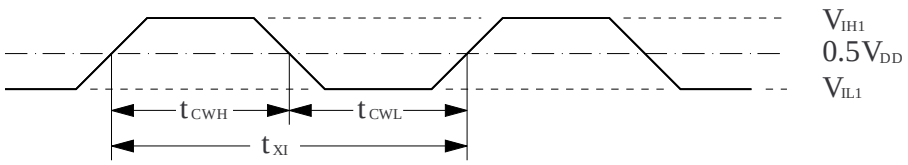
Crystal Oscillator

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Oscillator frequency	f_{OSC}	768fs	8.0	33.8688	35.6	MHz
		384fs	4.0	16.9344	17.8	MHz

External clock input

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
HIGH-level clock pulsewidth	t_{CWH}	768fs	13.0	14.75	62.5	ns
		384fs	26.0	29.5	125	ns
LOW-level clock pulsewidth	t_{CWL}	768fs	13.0	14.75	62.5	ns
		384fs	26.0	29.5	125	ns
Clock pulse cycle	t_{XI}	768fs	28.0	29.5	125	ns
		384fs	56.0	59.0	250	ns

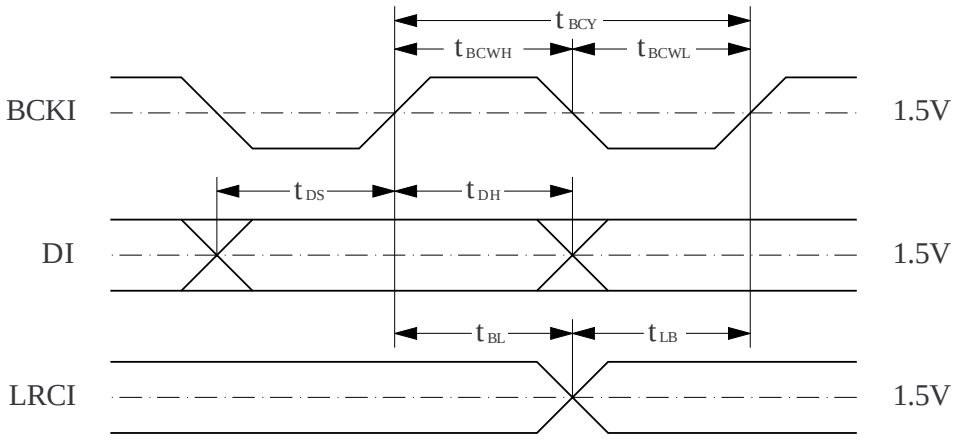
XTI input clock



Serial input (BCKI, DI, LRCI)

Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKI HIGH-level pulsewidth	t_{BCWH}	50	–	–	ns
BCKI LOW-level pulsewidth	t_{BCWL}	50	–	–	ns
BCKI pulse cycle	t_{BCY}	1/(64fs)	–	–	ns
DI setup time	t_{DS}	50	–	–	ns
DI hold time	t_{DH}	50	–	–	ns
Last BCKI rising edge to LRCI edge	t_{BL}	50	–	–	ns
LRCI edge to first BCKI rising edge	t_{LB}	50	–	–	ns

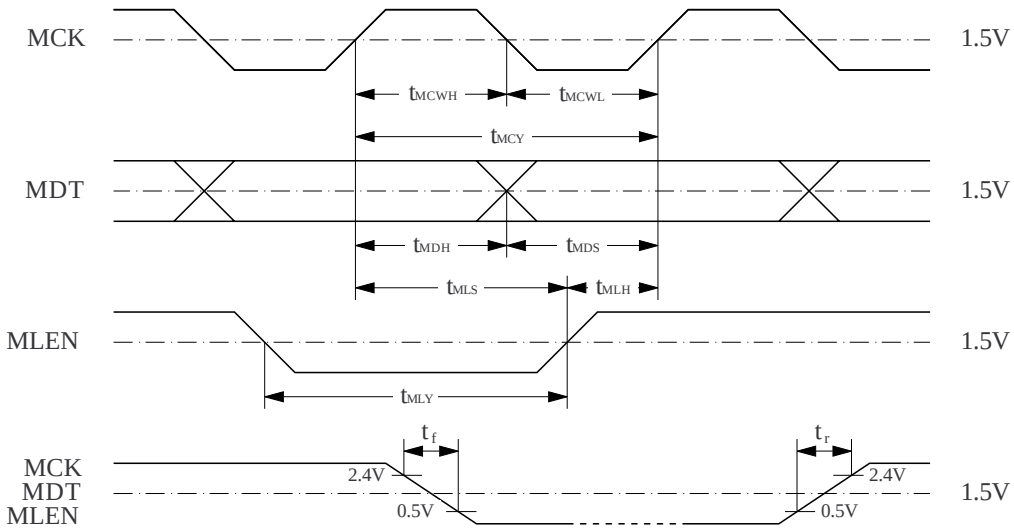
Serial input timing



Control input (MCK, MDT, MLEN)

Parameter	Symbol	Rating			Unit
		min	typ	max	
MCK HIGH-level pulsewidth	t_{MCWH}	140	–	–	ns
MCK LOW-level pulsewidth	t_{MCWL}	140	–	–	ns
MCK pulse cycle	t_{MCY}	280	–	–	ns
MDT setup time	t_{MDS}	100	–	–	ns
MDT hold time	t_{MDH}	100	–	–	ns
MLEN setup time	t_{MLS}	1/(192fs) + 20	–	–	ns
MLEN hold time	t_{MLH}	1/(192fs) + 20	–	–	ns
MLEN level pulsewidth	T_{MLH}	1/(192fs) + 20	–	–	ns
Rise time	t_r	–	–	50	ns
Fall time	t_f	–	–	50	ns

Control input timing



Reset Input (RSTN)

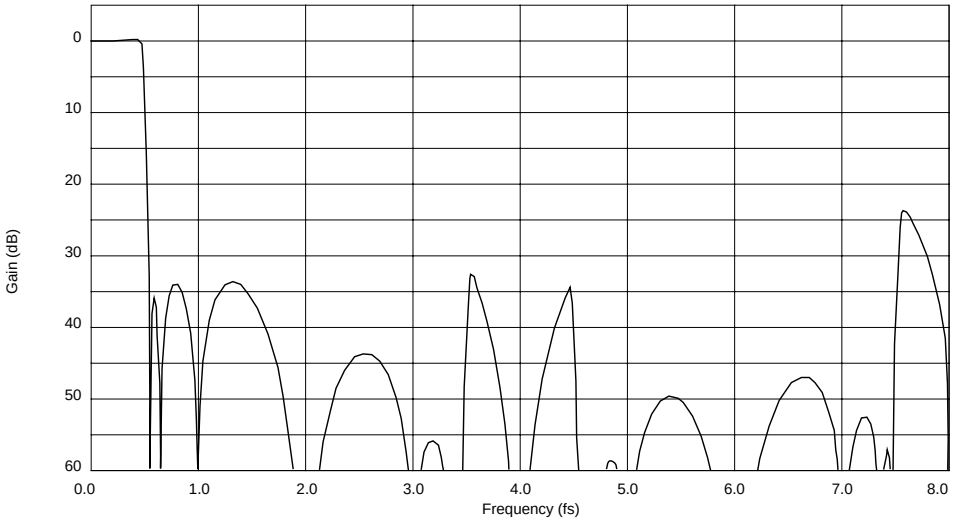
Parameter	Symbol	Rating			Unit
		min	typ	max	
RSTN LOW-level pulsewidth after supply rising edge	t_{RSTN}	50	–	–	ns

Theoretical Filter Characteristics

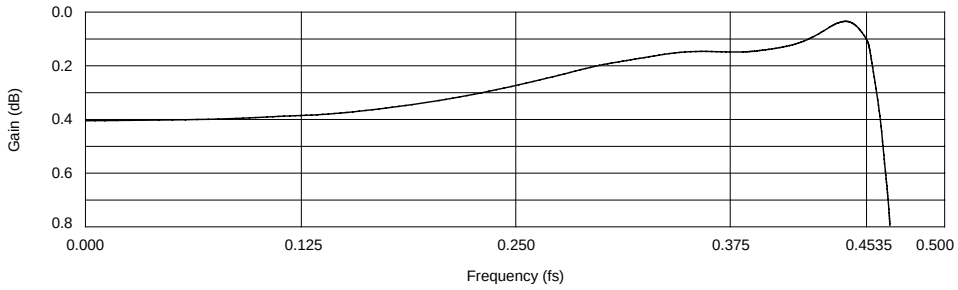
Deemphasis OFF overall characteristics

Parameter	Frequency band		Attenuation (dB)		
	f	@ fs = 44.1 kHz	min	typ	max
Passband ripple	0 to 0.4535fs	0 to 20.0 kHz	–0.05	–	+0.05
Stopband attenuation	0.5465fs to 7.4535fs	24.1 to 328.7 kHz	32	–	–
Built-in analog LPF compensation	0.4535fs	20.0 kHz	–	–0.34	–

Overall frequency characteristic (deemphasis OFF)



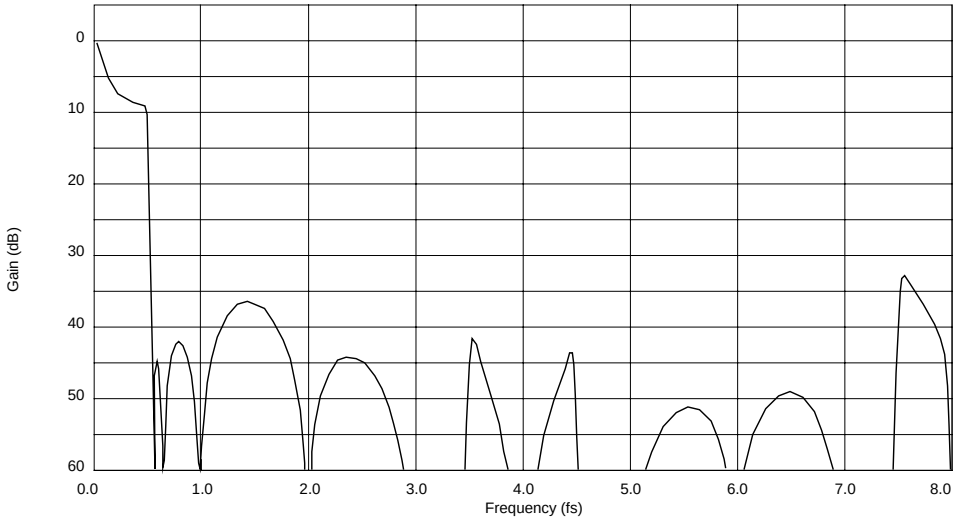
Passband characteristic (deemphasis OFF)



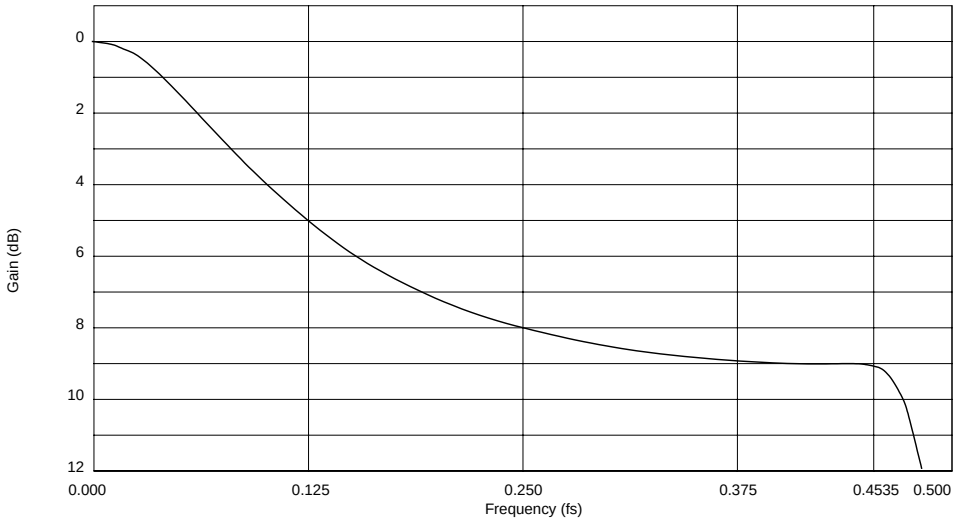
Deemphasis ON overall characteristics

Parameter	Frequency band		Attenuation (dB)		
	f	@ fs = 44.1 kHz	min	typ	max
Deviation from ideal deemphasis filter characteristics	0 to 0.4535fs	0 to 20.0 kHz	–0.09	–	+0.23
Stopband attenuation	0.5465fs to 7.4535fs	24.1 to 328.7 kHz	36	–	–
Built-in analog LPF compensation	0.4535fs	20.0 kHz	–	–0.34	–

Overall frequency characteristic (deemphasis ON)



Passband characteristic (deemphasis ON)



AC Analog Characteristics

5 V operation: $DV_{SS} = AV_{SS} = XV_{SS} = 0$ V, $DV_{DD} = AV_{DD} = XV_{DD} = 5$ V, $AV_{DD} = AV_{DDL} = AV_{DDR}$, CKSL = 0 V, deemphasis OFF, crystal oscillator frequency $f_{OSC} = 16.9344$ MHz, $T_a = 25$ °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Total harmonic distortion	THD + N	1 kHz, 0 dB	–	0.005	0.01	%
LSI output level[1]	V_{out1}	1 kHz, 0 dB	–	1.53	–	V_{rms}
Evaluation board output level	V_{out2}	1 kHz, 0 dB	1.8	2.0	2.2	V_{rms}
Dynamic range	D.R	1 kHz, –60 dB	88	92	–	dB
Signal-to-noise ratio[2]	S/N	1 kHz, 0/–∞ dB	88	92	–	dB
Channel separation	Ch. Sep	1 kHz, –∞/0 dB	84	86	–	dB

1. The LSI output level = $0.3058AV_{DD}$ Vrms.
2. Signal-to-noise is measured following a device reset, with DATA = 0 (DI = LOW). Under these conditions, the signal-to-noise ratio includes noise-shaper noise.

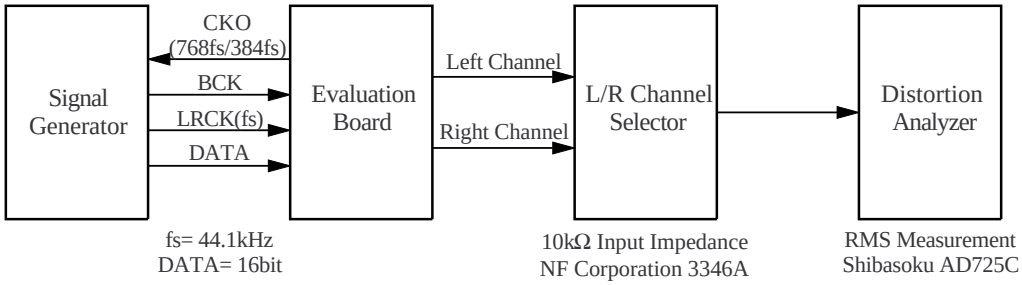
3 V operation: $DV_{SS} = AV_{SS} = XV_{SS} = 0$ V, $DV_{DD} = AV_{DD} = XV_{DD} = 3$ V, $AV_{DD} = AV_{DDL} = AV_{DDR}$, CKSL = 0 V, deemphasis OFF, crystal oscillator frequency $f_{OSC} = 16.9344$ MHz, $T_a = 25$ °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Total harmonic distortion	THD + N	1 kHz, 0 dB	–	0.007	–	%
LSI output level[1]	V_{out1}	1 kHz, 0 dB	–	0.92	–	V_{rms}
Evaluation board output level	V_{out2}	1 kHz, 0 dB	–	1.2	–	V_{rms}
Dynamic range	D.R	1 kHz, –60 dB	–	90	–	dB
Signal-to-noise ratio[2]	S/N	1 kHz, 0/–∞ dB	–	90	–	dB
Channel separation	Ch. Sep	1 kHz, –∞/0 dB	–	82	–	dB

1. The LSI output level = $0.3058AV_{DD}$ Vrms.
2. Signal-to-noise is measured following a device reset, with DATA = 0 (DI = LOW). Under these conditions, the signal-to-noise ratio includes noise-shaper noise.

AC Measurement Circuit and Conditions

Measurement circuit block diagram

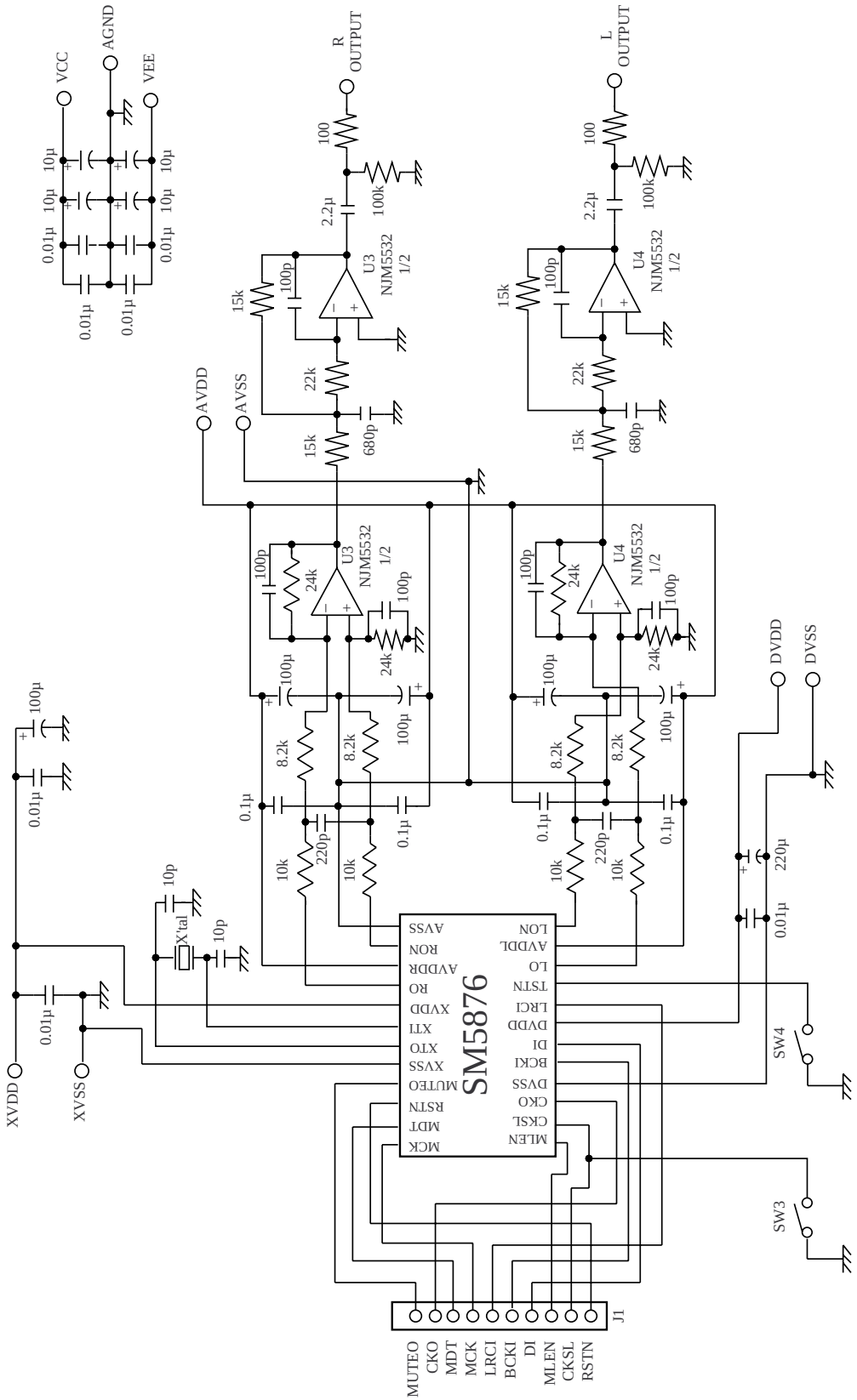


Measurement conditions

Parameter[1]	Symbol	3346A left/right-channel selector switch	AD725C distortion analyzer with built-in filter
Total harmonic distortion	THD + N	THRU	20 kHz lowpass filter ON 400 Hz highpass filter OFF
Output level	V_{out}		
Dynamic range	DR	D-RANGE	
Signal-to-noise ratio	S/N	THRU	20 kHz lowpass filter ON 400 Hz highpass filter OFF JIS A filter ON
Channel separation	Ch. Sep	THRU	20 kHz lowpass filter ON 400 Hz highpass filter OFF

1. Pins LO and RO should have an output load of 10 kΩ (min).

Measurement circuit



FUNCTIONAL DESCRIPTION

System Clock/Speed Switching (XTI, XTO, CKO, CKSL)

The system clock on XTI can be set to run at one of two speeds, 384fs (normal speed) or 768fs (double-speed), where fs is the input frequency on LRCI. The speed for CD playback is set by the input level on CKSL, as shown in table 1.

Table 1. System clock select

Parameter	Symbol	CKSL	
		HIGH	LOW
XTI input clock frequency	f_{XI} (= $1/t_{XI}$)	768fs	384fs
CD playback XTI frequency	f_{XI}	33.8688 MHz at fs = 44.1 kHz	16.9344 MHz at fs = 44.1 kHz
CKO output clock frequency	f_{CO}	768fs	384fs
Internal system clock period	T_{SYS}	$2t_{XI}$	t_{XI}

Note that the input clock accuracy and signal-to-noise ratio greatly influence the AC analog characteristics. Accordingly, care should be taken to ensure that the clock is free from jitter.

The system clock can be controlled by a crystal oscillator comprising a crystal connected between XTI and XTO and the built-in CMOS inverter. Alternatively, an external system clock can be input on XTI. As the internal CMOS inverter has a feedback resistor, the external clock can be AC coupled to XTI. The system clock is output on CKO.

System Reset (RSTN)

The device should be reset in the following cases.

- At power ON
- When LRCI and/or the system clock XTI stop, or other abnormalities occur.
- When switching the XTI clock 768fs ⇔ 384fs.

The device is reset by applying a LOW-level pulse on RSTN. At system reset, the internal arithmetic operation and output timing counter are synchronized on the next LRCI rising edge, as shown in figure 1.

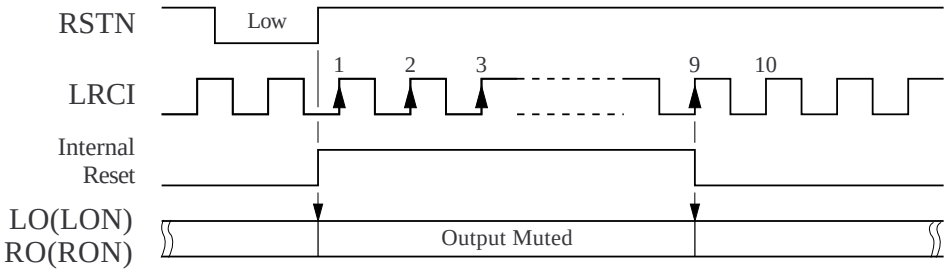


Figure 1. System reset timing

Output mute

At power-ON reset (when RSTN goes LOW), the outputs LO (LON) and RO (RON) enter the output mute state. Mute is released on the 9th LRCI rising edge after RSTN goes HIGH. During this cycle, the timing reset can cause output noise to be generated.

Infinity-Zero Detector (analog mute control) Output (MUTEO)

The SM5876AM outputs an infinity-zero detection output signal under the following circumstances.

1. When an infinity-zero occurs on both the left and right channels.
2. When an infinity-zero occurs in the input data for the channel set by the output mode setting.
3. When the output mode setting is muting for both the left and right channels.
4. When the attenuation counter for both the left and right channels is 0 (−∞).

Also from immediately after a reset input on RSTN until the initialization cycle finishes and the first data cycle occurs.

In cases 1 and 2, from when an infinity-zero is detected a period of $2^{14} \times (1/fs) \approx 0.37$ seconds takes place before MUTEO goes HIGH.

In cases 3 and 4, from when the attenuation counter value is 0 a period of $2^{14} \times (1/fs) \approx 0.37$ seconds takes place before MUTEO goes HIGH.

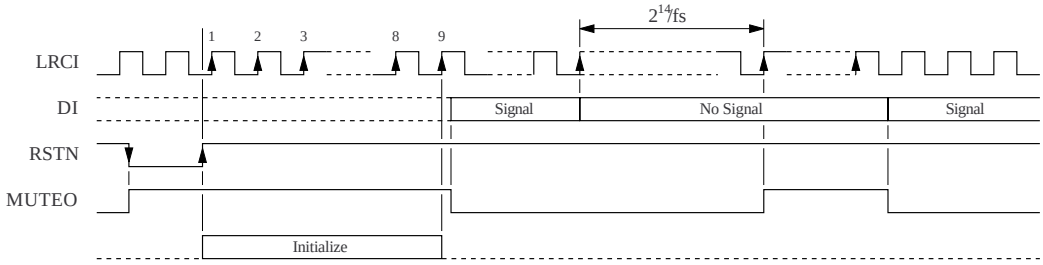


Figure 2. MUTEO output timing

Audio Data Input (DI, BCKI, LRCI)

The digital audio data is input on DI in MSB-first, 2s-complement, 16-bit serial format.

Serial data bits are read into the SIPO register (serial-to-parallel converter register) on the rising edge of the bit clock BCKI.

The arithmetic operation and output timing are independent of the input timing. Accordingly, after a reset, as long as the clock frequency ratio between LRCI and the system clock XTI is maintained, phase differences between LRCI, BCKI and the system clock XTI do not affect the functional operation. Also, any jitter present on the data input clock does not appear as output pulse jitter.

The bit clock frequency on BCKI should be between 32fs and 64fs.

Operating Modes (MLEN, MDT, MCK)

The microcontroller data is used to control the following parameters.

Digital attenuator

Digital attenuation is controlled by attenuation data input on MDT.

The attenuation operation is determined by a mathematical operation of the internal 8-bit up/down counter's output data on the signal data. The 8-bit up/down counter, when attenuation data is input on MDT, can control the left and right channels either independently or together (independent when the MDT attenuation control flag is LOW, and together when HIGH).

The left-channel counter contents DATTL and the right-channel counter contents DATTR control the left-channel gain and right-channel gain, respectively, using the following equations.

$$\text{Left-channel gain} = 20 \times \log\left(\frac{\text{DATTL}}{255}\right)[\text{dB}]$$

$$\text{Right-channel gain} = 20 \times \log\left(\frac{\text{DATTR}}{255}\right)[\text{dB}]$$

After system reset initialization, independent left/right-channel attenuation mode with the maximum gain of 0 dB is the default.

Deemphasis filter (MDT DEM flag)

The built-in digital deemphasis filter is designed to operate at 44.1 kHz. Deemphasis is ON when the DEM flag is HIGH, and OFF when the DEM flag is LOW. After reset, deemphasis OFF is the default.

Output mode setting (MDT 4-bit data)

The left-channel and right-channel outputs can be set to any one of 16 different modes, as shown in table 2.

Table 2. Output mode control

PL0	PL1	PL2	PL3	Left-channel output	Right-channel output	Notes
0	0	0	0	Mute	Mute	Mute
0	0	0	1	Mute	R	
0	0	1	0	Mute	L	
0	0	1	1	Mute	(L + R)/2	
0	1	0	0	R	Mute	
0	1	0	1	R	R	
0	1	1	0	R	L	Reverse
0	1	1	1	R	(L + R)/2	
1	0	0	0	L	Mute	
1	0	0	1	L	R	Stereo
1	0	1	0	L	L	
1	0	1	1	L	(L + R)/2	
1	1	0	0	(L + R)/2	Mute	
1	1	0	1	(L + R)/2	R	
1	1	1	0	(L + R)/2	L	
1	1	1	1	(L + R)/2	(L + R)/2	

"Stereo" is the default after system reset.
"Mute" refers to soft muting.

Soft mute (output mode setting)

The channel output muting set by the output mode control 4-bit data is soft mute mode.

The attenuation counter output decrements by 1 step at a time, reducing the gain. The signal is completely muted after a time of (1024/fs), which corresponds to approximately 23.2 ms when fs = 44.1 kHz.

Conversely, when soft mute is released using the output mode control, the attenuation counter output increments by 1 step at a time, increasing the gain. The time taken to return to 0 dB from full muting is also (1024/fs).

When an attenuation value is set, the output gain decreases from the value set by the attenuation data until the gain is −∞. Similarly for mute release, the output gain increases from the current value until the gain is 0 dB.

Soft mute operation is shown in figure 3. Upon system reset initialization, mute is released, which corresponds to the maximum gain of 0 dB.

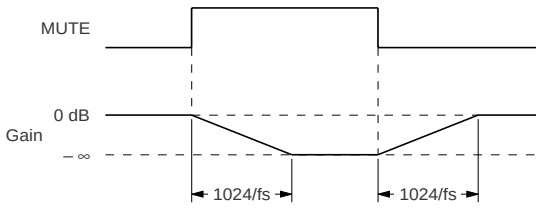


Figure 3. Soft mute operation example

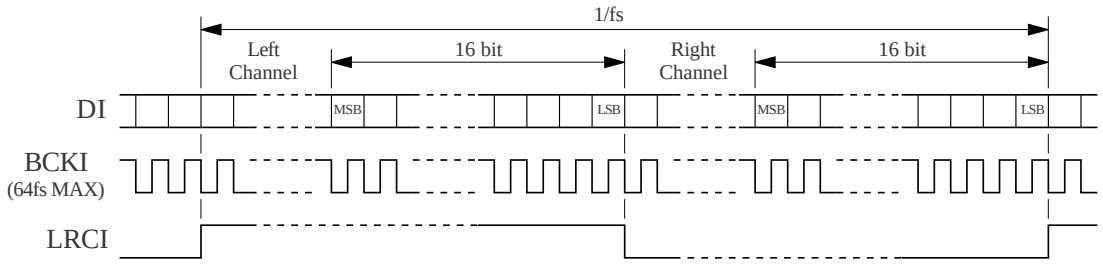
Attenuator control (ATC flag)

The attenuator control (ATC) flag is input on MDT. When the ATC flag is HIGH, the left-channel and right-channel attenuator data is common. In this mode, the left-channel data is used for both channels.

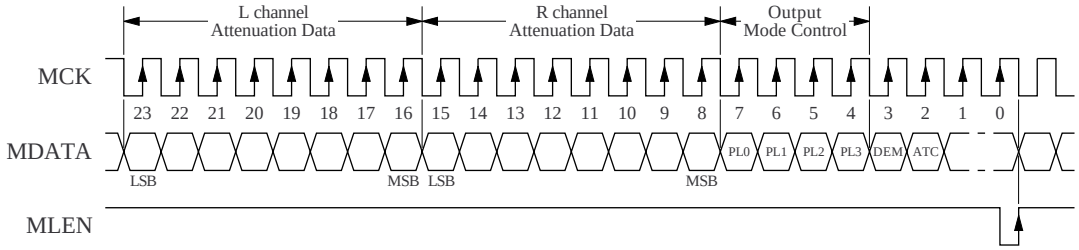
TIMING DIAGRAMS

Input Timing

(DI, BCKI, LRCI)



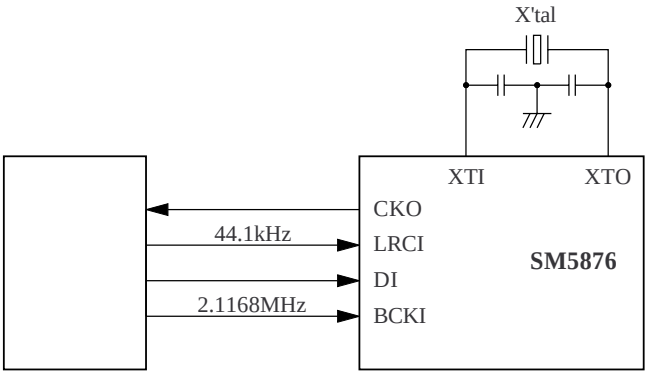
(MDT, MCK, MLEN)



Data is recognized on the rising edge of MLEN.

TYPICAL APPLICATIONS

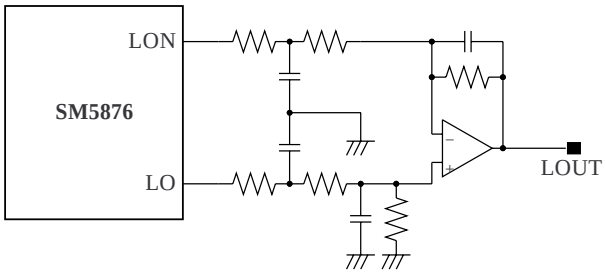
Input Interface Circuit



Note that the output analog characteristics and other specifications are not guaranteed for a particular format or application circuit.

Output Analog Processing Circuit

(Left channel only is shown.)



NPC
NIPPON PRECISION CIRCUITS INC.

NIPPON PRECISION CIRCUITS INC.

4-3, 2-chome Fukuzumi
Koutou-ku, Tokyo 135-8430, Japan
Telephone: 03-3642-6661
Facsimile: 03-3642-6698

NC9504BE 1996.06