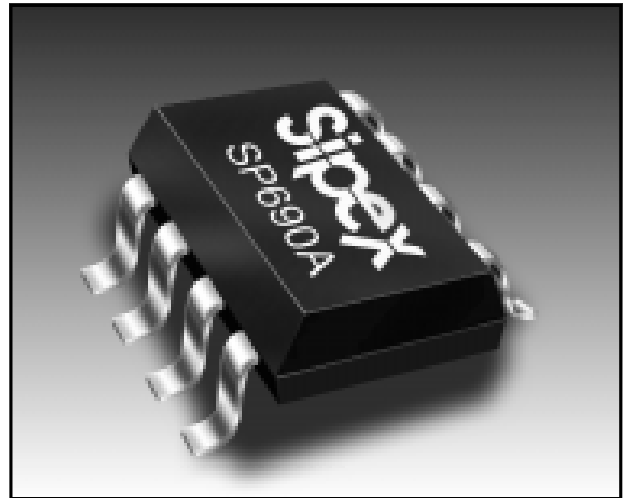




# SP690A/692A/802L/ 802M/805L/805M

## Low Power Microprocessor Supervisory with Battery Switch-Over

- Precision Voltage Monitor:
  - SP690A/SP802L/SP805L at 4.65V
  - SP692A/SP802M/SP805M at 4.40V
- Reset Time Delay - 200ms
- Watchdog Timer - 1.6 sec timeout
- Minimum component count
- 60µA Maximum Operating Supply Current
- 0.6µA Maximum Battery Backup Current
- 0.1µA Maximum Battery Standby Current
- Power Switching
  - 250mA Output in  $V_{CC}$  Mode (0.6Ω)
  - 25mA Output in Battery Mode (5Ω)
- Voltage Monitor for Power Fail or Low Battery Warning
- Available in 8 pin SO and DIP packages
- RESET asserted down to  $V_{CC} = 1V$
- Pin Compatible Upgrades to  
MAX690A/692A/802L/802M/805L



### DESCRIPTION

The **SP690A/692A/802L/802M/805L/805M** are a family of microprocessor ( $\mu P$ ) supervisory circuits that integrate a myriad of components involved in discrete solutions to monitor power-supply and battery-control functions in  $\mu P$  and digital systems. The series will significantly improve system reliability and operational efficiency when compared to discrete solutions. The features of the **SP690A/692A/802L/802M/805L/805M** include a watchdog timer, a  $\mu P$  reset and backup-battery switchover, and power-failure warning, a complete  $\mu P$  monitoring and watchdog solution. The series is ideal for applications in automotive systems, computers, controllers, and intelligent instruments. All designs where it is critical to monitor the power supply to the  $\mu P$  and it's related digital components will find the series to be an ideal solution.

PART NUMBER	RESET Threshold	RESET Accuracy	RESET Active	PFI Accuracy
SP690A	4.65 V	125mV	LOW	4%
SP692A	4.40 V	125mV	LOW	4%
SP802L	4.65 V	75mV	LOW	2%
SP802M	4.40 V	75mV	LOW	2%
SP805L	4.65 V	125mV	HIGH	4%
SP805M	4.40 V	125mV	HIGH	4%

## ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

$V_{CC}$ .....-0.3V to 6.0V

$V_{BATT}$ .....-0.3V to 6.0V

All Other Inputs (NOTE 1).....-0.3V to ( $V_{CC}$  to 0.3V)

Input Current:

$V_{CC}$ .....250mA

$V_{BATT}$ .....50mA

GND.....20mA

Output Current:

$V_{OUT}$ .....Short-Circuit Protected for up to 10sec

All Other Inputs.....20mA

Rate of Rise,  $V_{CC}$ ,  $V_{BATT}$ .....100V/ $\mu$ s

Continuous Power Dissipation.....500mW

Storage Temperature.....-65°C to +160°C

Lead Temperature(soldering, 10sec).....+300°C

ESD Rating.....4KV



**CAUTION:**  
ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

## SPECIFICATIONS

$V_{CC}$  = 4.75v to 5.50V for SP690A/SP802L/SP805L,  $V_{CC}$  = 4.50V to 5.50V for SP692A/SP802M/SP805M,  $V_{BATT}$  = 2.80V,  $T_A$  =  $T_{MIN}$  to  $T_{MAX}$ , typical specified at 25°C, unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Operating Voltage Range, $V_{CC}$ or $V_{BATT}$ , Note 2	0		5.5	Volts	
Supply Current, $I_{SUPPLY}$		35	60	$\mu$ A	excluding $I_{OUT}$
$I_{SUPPLY}$ in Battery Backup Mode, $V_{CC} = 0V$ , $V_{BATT} = 2.8V$		0.001	0.6	$\mu$ A	
$V_{BATT}$ Standby Current, NOTE 3	-0.1		0.02	$\mu$ A	$V_{CC} > V_{BATT} + 0.2V$
$V_{OUT}$ Output	$V_{CC} - 0.1$	$V_{CC} - 0.03$ $V_{CC} - 0.15$		Volts	$I_{OUT} = 50mA$ $I_{OUT} = 250mA$
$V_{OUT}$ in Battery-Backup Mode $V_{CC} < V_{BATT} - 0.2V$	$V_{BATT} - 0.15$	$V_{BATT} - 0.04$ $V_{BATT} - 0.20$		Volts	$I_{OUT} = 5mA$ $I_{OUT} = 25mA$
Battery Switch Threshold, $V_{CC}$ to $V_{BATT}$		20 -20		mV	Power-up Power-down
Battery Switchover Hysteresis		40		mV	Peak to Peak
Reset Threshold	4.50 4.25 4.55 4.30	4.65 4.40	4.75 4.50 4.70 4.45	Volts	SP690A, SP802L, SP805L SP692A, SP802M, SP805M SP802L, $T_A = +25^\circ C$ , $V_{CC}$ falling SP802M, $T_A = +25^\circ C$ , $V_{CC}$ falling

## SPECIFICATIONS (continued)

$V_{CC}$  = 4.75V to 5.50V for SP690A/SP802L/SP805L,  $V_{CC}$  = 4.50V to 5.50V for SP692A/SP802M/SP805M,  $V_{BATT}$  = 2.80V,  $T_A$  =  $T_{MIN}$  to  $T_{MAX}$ , typical specified at 25°C, unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Reset Threshold Hysteresis		40		mV	Peak to Peak
Reset Pulse Width, $t_{RS}$	140	200	280	ms	
RESET Output Voltage, NOTE 5	$V_{CC} - 1.5$	0.1 0.004	0.4 0.3	Volts	$I_{SOURCE} = 800\mu A$ $I_{SINK} = 3.2mA$ $I_{SINK} = 50\mu A, V_{CC} = 1.0$
RESET Output Voltage, NOTE 6	0.8 $V_{CC} - 1.5$	0.1	0.4	Volts	$I_{SOURCE} = 4\mu A, V_{CC} = 1.0V,$ $I_{SOURCE} = 800\mu A$ $I_{SINK} = 3.2mA$
Watchdog Timeout, $t_{WD}$	1.00	1.60	2.25	sec	
WDI Pulse Width, $t_{WP}$	50			ns	$V_{IL} = 0.4V, V_{IH} = (0.8)(V_{CC})$
WDI Input Threshold, $V_{CC} = 5V$ , NOTE 4	3.5		0.8	Volts	Logic low Logic high
WDI Input Current	-150	50 -50	150	$\mu A$	WDI = $V_{CC}$ WDI = 0V
PFI Input Threshold	1.200 1.225	1.250 1.250	1.300 1.275	Volts	SP690A/692A, SP805L/M SP802L/M
PFI Input Current	-25	0.01	25	nA	
PFO Output Voltage	$V_{CC} - 1.5$	0.1	0.4	Volts	$I_{SOURCE} = 800\mu A$ $I_{SINK} = 3.2mA$

**NOTE 1:** The input voltage limits on PFI (pin 4) and WDI (pin 6) may be exceeded if the current into these pins is limited to less than 10 mA.

**NOTE 2:** Either  $V_{CC}$  or  $V_{BATT}$  can go to 0V if the other is greater than 2.0V.

**NOTE 3:** "-" equals the battery-charging current, "+" equals the battery-discharging current.

**NOTE 4:** WDI is guaranteed to be in an intermediate, non-logic level state if WDI is floating and  $V_{CC}$  is in the operating voltage range. WDI is internally biased to 35% of  $V_{CC}$  with an input impedance of 50K $\Omega$ .

**NOTE 5:** SP690A, SP692A, SP802L, and SP802M only.

**NOTE 6:** SP805L and SP805M only.

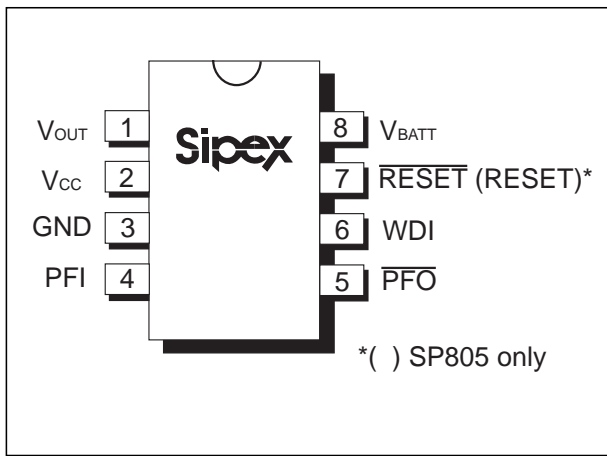


Figure 10. Pinout

## PIN ASSIGNMENTS

Pin 1 —  $V_{OUT}$  — Output Supply Voltage.  $V_{OUT}$  connects to  $V_{CC}$  when  $V_{CC}$  is greater than  $V_{BATT}$  and  $V_{CC}$  is above the reset threshold. When  $V_{CC}$  falls below  $V_{BATT}$  and  $V_{CC}$  is below the reset threshold,  $V_{OUT}$  connects to  $V_{BATT}$ . Connect a  $0.1\mu\text{F}$  capacitor from  $V_{OUT}$  to GND.

Pin 2 —  $V_{CC}$  — +5V Supply Input

Pin 3 — GND — Ground reference for all signals

Pin 4 — PFI — Power-Fail Input. This is the noninverting input to the power-fail comparator. When PFI is less than 1.25V, PFO goes low. Connect PFI to GND or  $V_{OUT}$  when not used.

Pin 5 —  $\overline{\text{PFO}}$  — Power-Fail Output.

Pin 6 — WDI — Watchdog Input. WDI is a three level input. If WDI remains high or low for 1.6sec, the internal watchdog timer triggers a reset. If WDI is left floating or connected to a high-impedance tri-state buffer, the watchdog feature is disabled. The internal watchdog timer clears whenever reset is asserted.

Pin 7 for **SP690A/692A/802 only** —  $\overline{\text{RESET}}$  (Active Low)–Reset Output.  $\overline{\text{RESET}}$  Output goes low whenever  $V_{CC}$  falls below the reset threshold or whenever WDI remains high or low longer than 1.6 seconds.  $\overline{\text{RESET}}$  remains low for 200ms after  $V_{CC}$  crosses the reset threshold voltage on power-up or after being triggered by WDI.

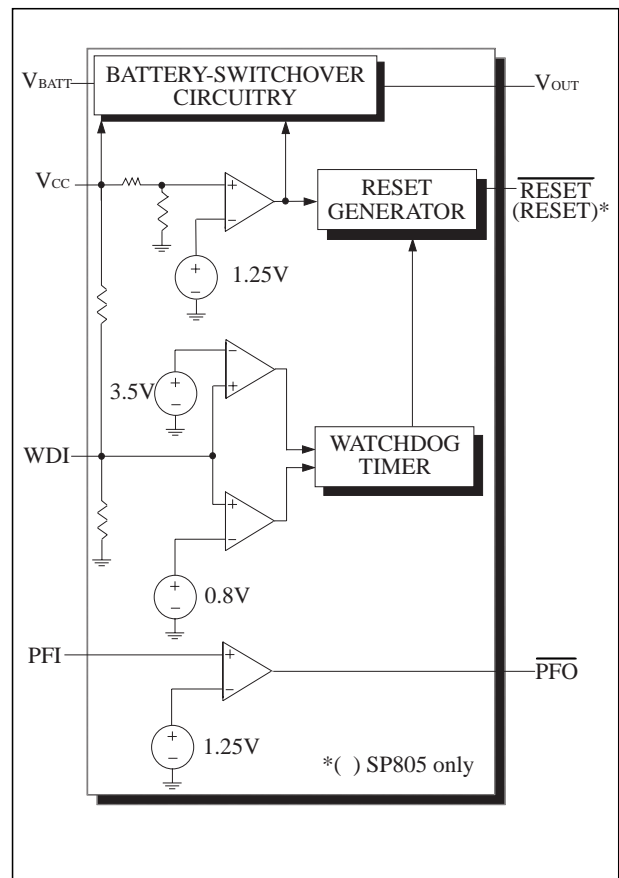
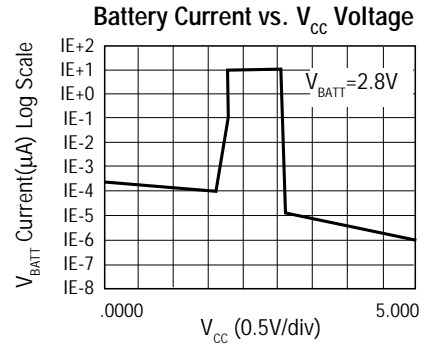
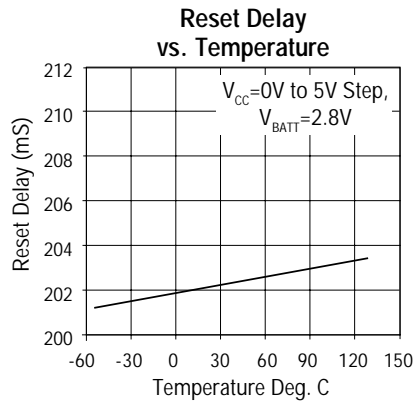
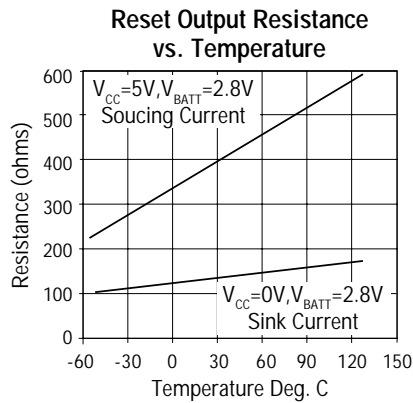
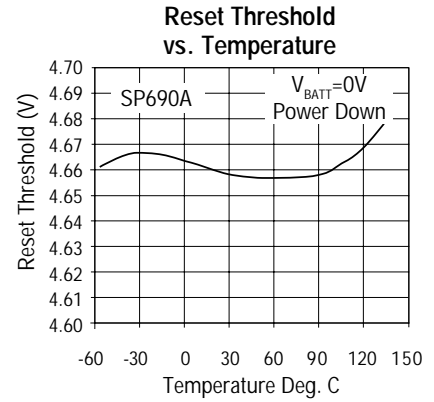
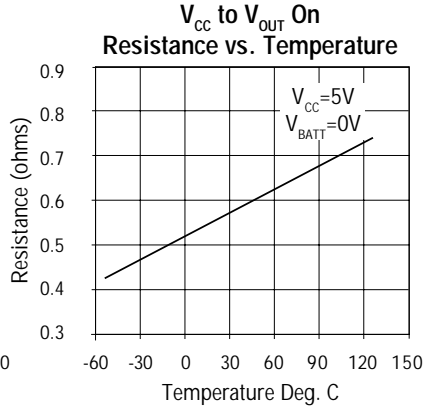
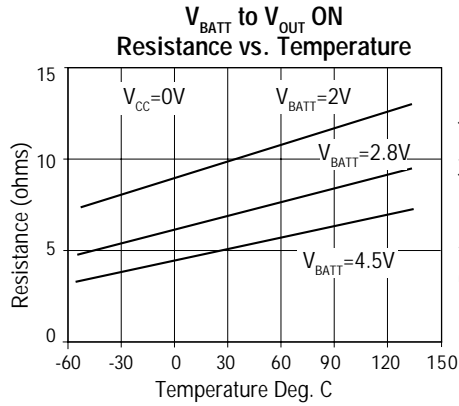
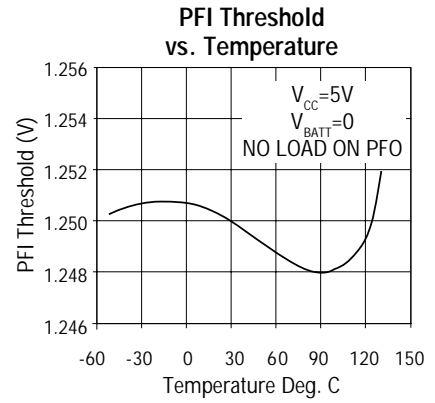
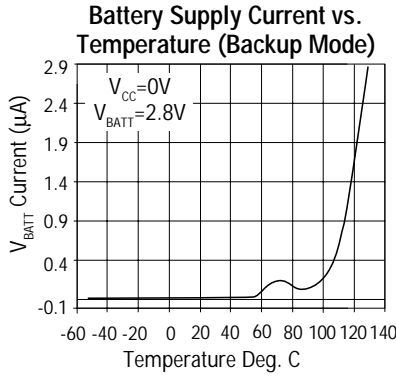
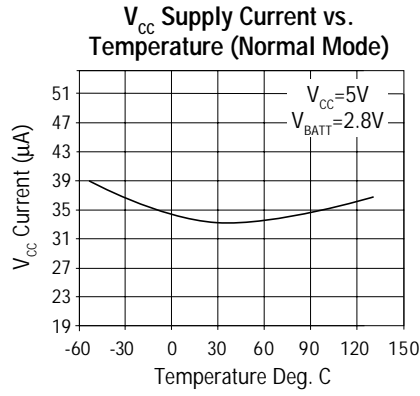


Figure 11. Internal Block Diagram

Pin 7 for **SP805 only** — RESET (Active High)–Reset Output is the inverse of  $\overline{\text{RESET}}$ ; when RESET is asserted, the RESET output voltage =  $V_{CC}$  or  $V_{BATT}$ , whichever is higher.

Pin 8 —  $V_{BATT}$  — Backup-Battery Input. When  $V_{CC}$  falls below the reset threshold,  $V_{BATT}$  will be switched to  $V_{OUT}$  if  $V_{BATT}$  is 20mV greater than  $V_{CC}$ . When  $V_{CC}$  rises 20mV above  $V_{BATT}$ ,  $V_{OUT}$  will be reconnected to  $V_{CC}$ . The 40mV hysteresis prevents repeated switching if  $V_{CC}$  falls slowly.

# TYPICAL CHARACTERISTICS (25°C, unless otherwise noted)



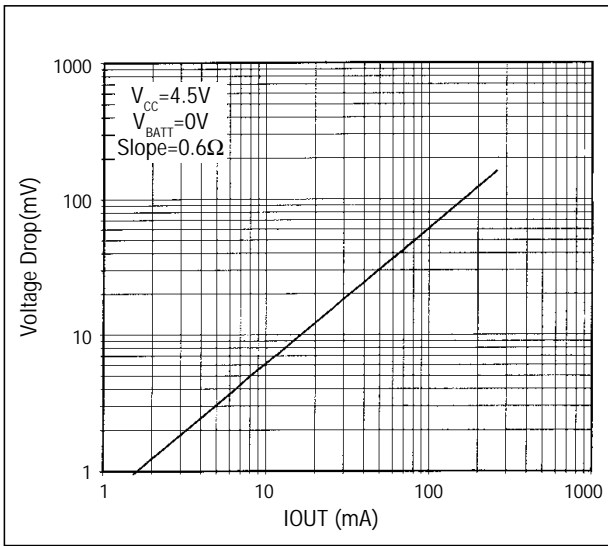


Figure 1.  $V_{CC}$  to  $V_{OUT}$  Vs. Output Current

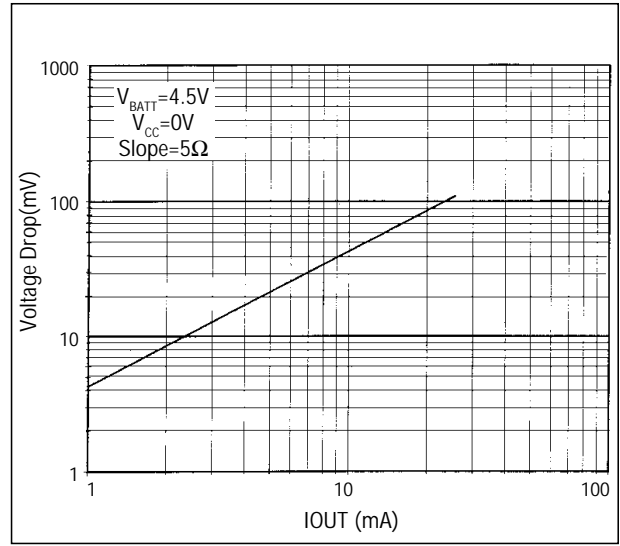


Figure 2.  $V_{BATT}$  to  $V_{OUT}$  Vs. Output Current

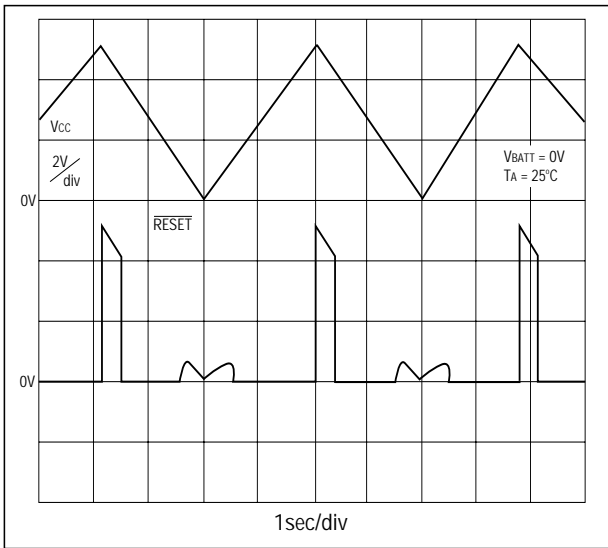


Figure 3A. SP690A  $\overline{RESET}$  Output Voltage vs. Supply Voltage

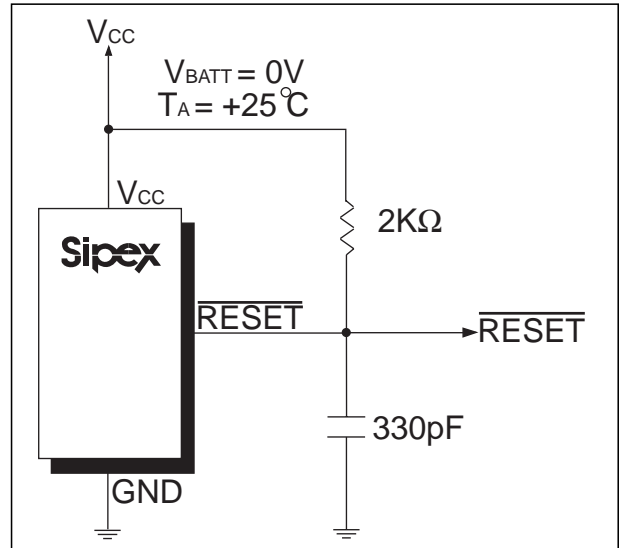


Figure 3B. Circuit for the SP690A/802L  $\overline{RESET}$  Output Voltage vs. Supply Voltage

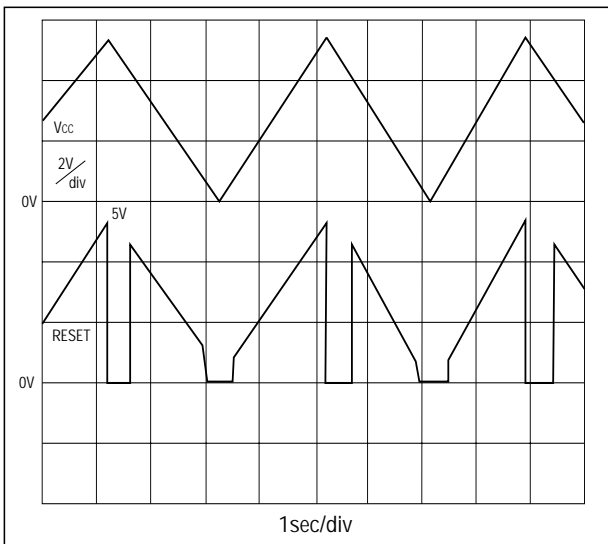


Figure 4A. SP805L  $\overline{RESET}$  Output Voltage vs. Supply Voltage

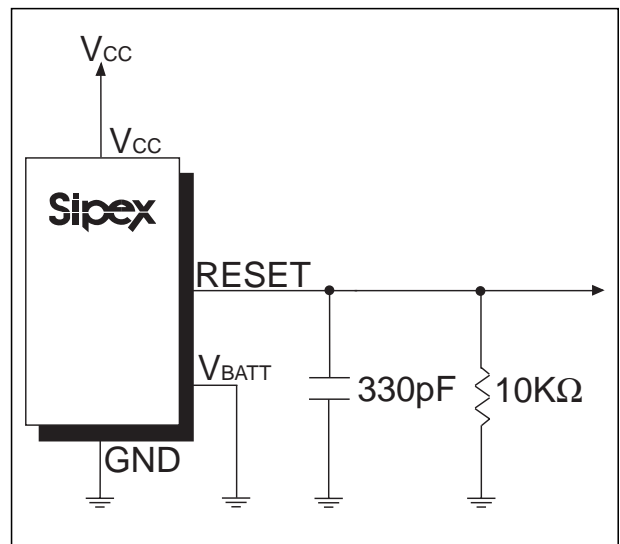


Figure 4B. Circuit for the SP805  $\overline{RESET}$  Output Voltage vs. Supply Voltage

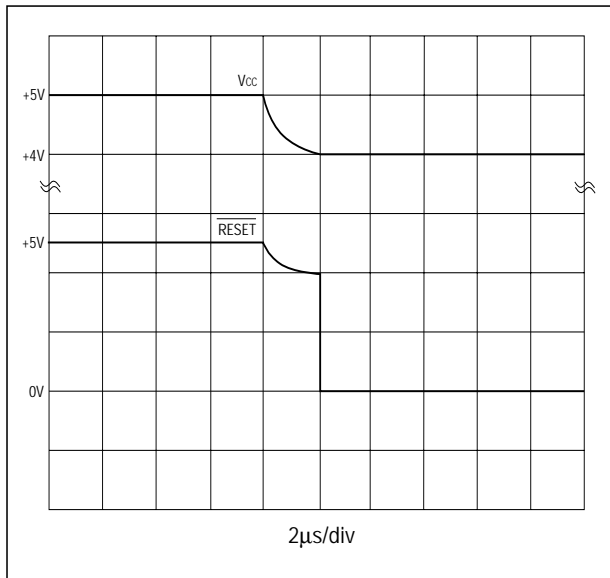


Figure 5A. SP690A  $\overline{\text{RESET}}$  Response Time

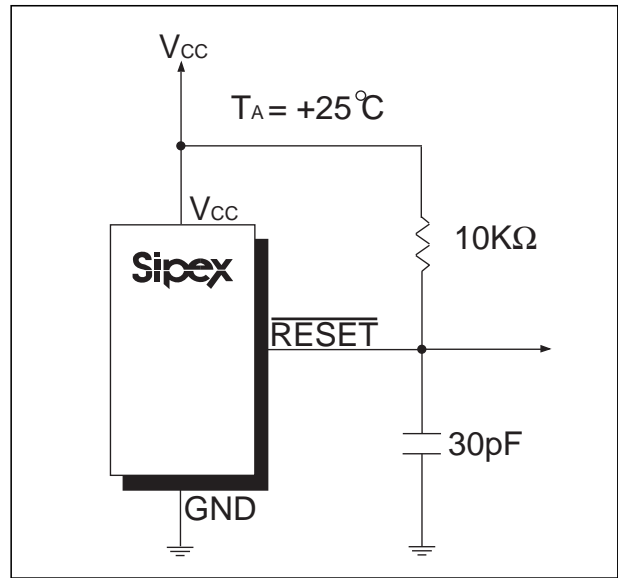


Figure 5B. Circuit for the SP690A/802L  $\overline{\text{RESET}}$  Response Time

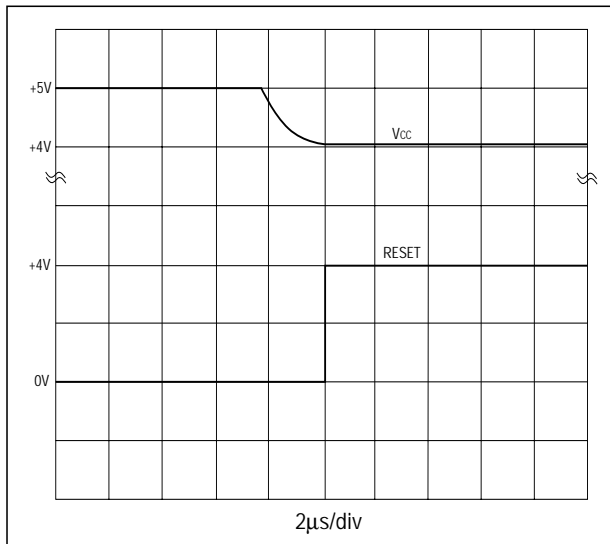


Figure 6A. SP805L RESET Response Time

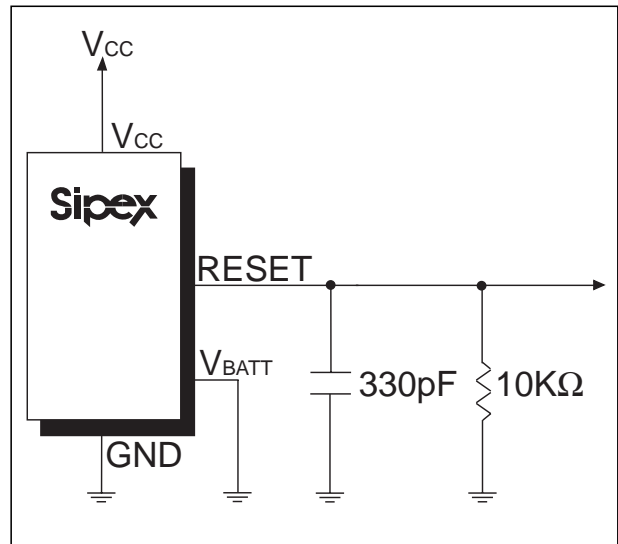


Figure 6B. Circuit for the SP805L RESET Response Time

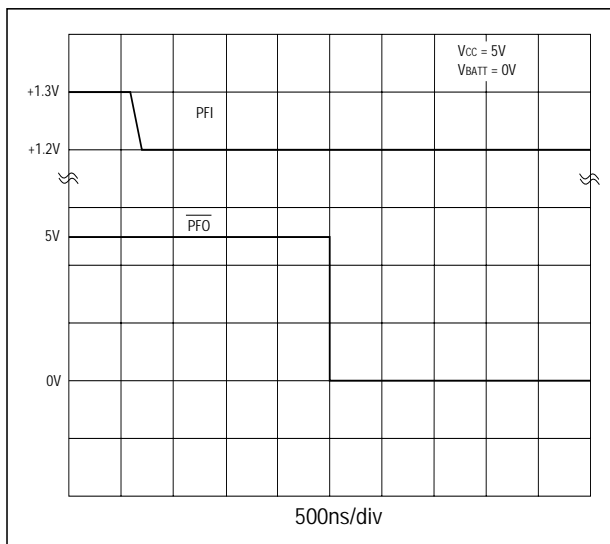


Figure 7A. Power-Fail Comparator Response Time (FALL)

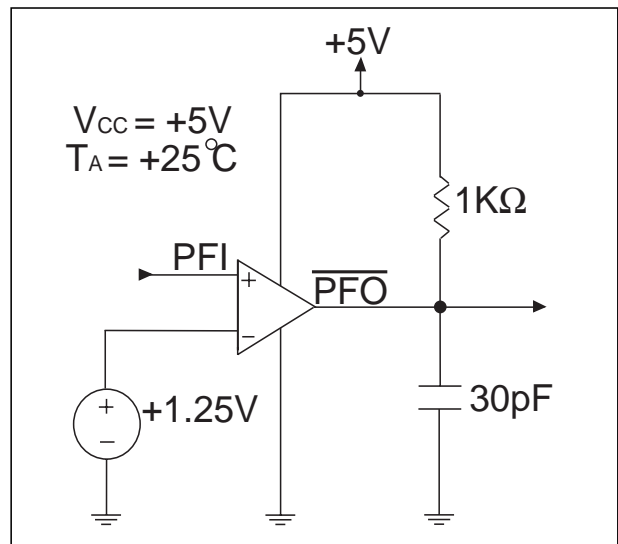


Figure 7B. Circuit for the Power-Fail Comparator Response Time (FALL)

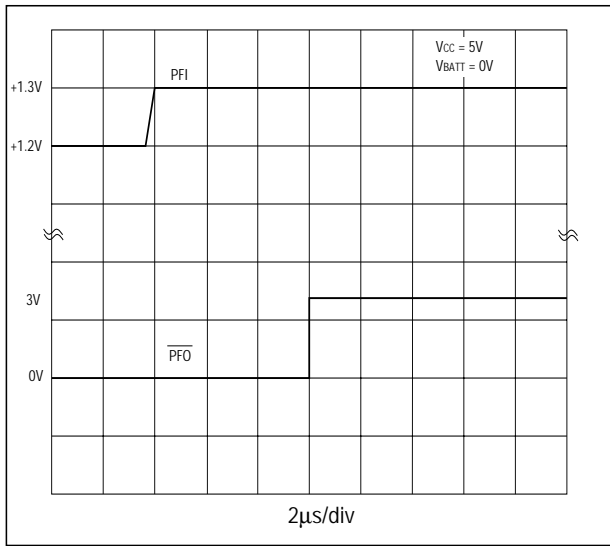


Figure 8A. Power-Fail Comparator Response Time (RISE)

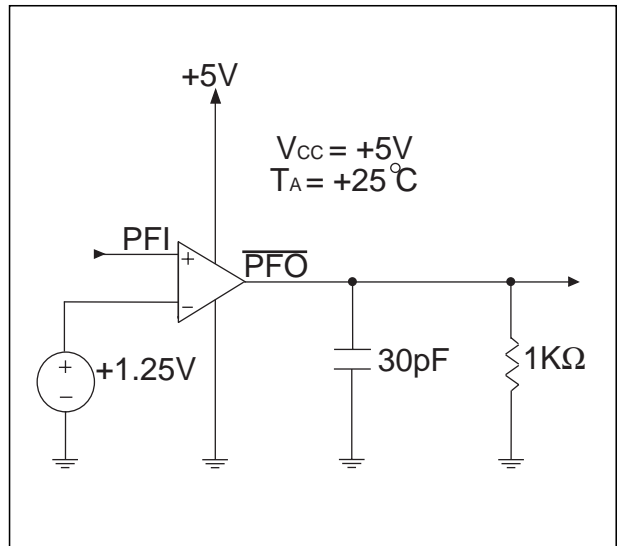


Figure 8B. Circuit for the Power-Fail Comparator Response Time (RISE)

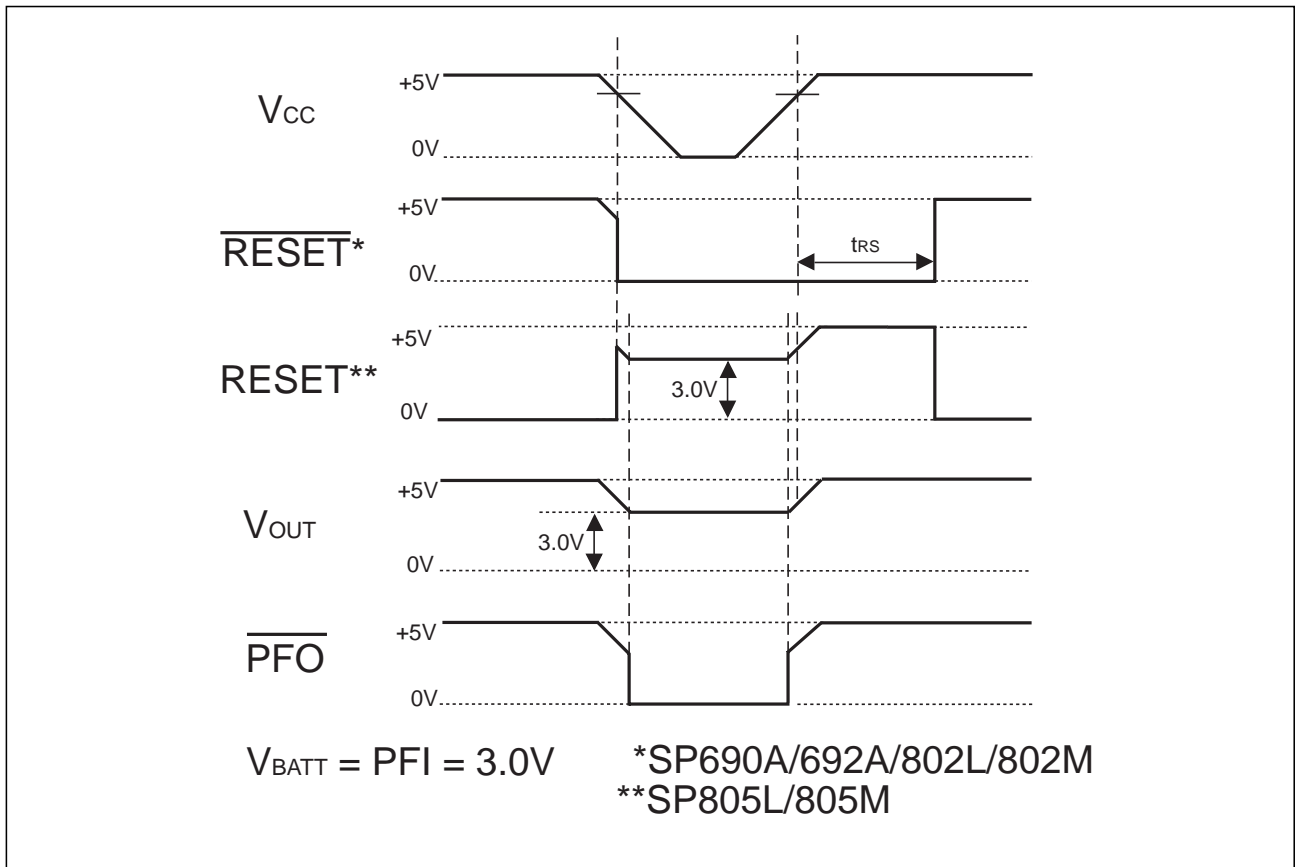


Figure 9. Timing Diagram



## FEATURES

The **SP690A/692A/802L/802M/805L/805M** provide four key functions:

1. A battery backup switching for CMOS RAM, CMOS microprocessors, or other logic.
2. A reset output during power-up, power-down and brownout conditions.
3. A reset pulse if the optional watchdog timer has not been toggled within a specified time.
4. A 1.25V threshold detector for power-fail warning, low battery detection, or to monitor a power supply other than +5V.

The parts differ in their reset-voltage threshold levels and reset outputs. The **SP690A/802L/805L** generate a reset when the supply voltage drops below 4.65V. The **SP692A/802M/805M** generate a reset below 4.40V.

The **SP690A/692A/802L/802M/805L/805M** are ideally suited for applications in automotive systems, intelligent instruments, and battery-powered computers and controllers. All designs into an environment where it is critical to monitor the power supply to the  $\mu\text{P}$  and it's related digital components will find the **SSP690A/692A/802L/802M/805L/805M** ideal.

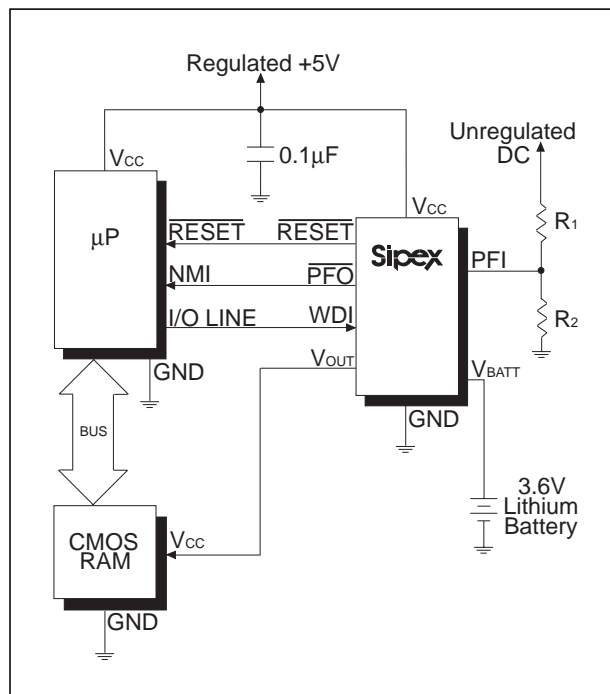


Figure 12. Typical Operating Circuit

## THEORY OF OPERATION

The **SP690A/692A/802L/802M/805L/805M** microprocessor ( $\mu\text{P}$ ) supervisory circuits monitor the power supplied to digital circuits such as microprocessors, microcontrollers, or memory. The series is an ideal solution for portable, battery-powered equipment that requires power supply monitoring. Implementing this series will reduce the number of components and overall complexity. The watchdog functions of this product family will continuously oversee the operational status of a system. The operational features and benefits of the **SP690A/692A/802L/802M/805L/805M** are described in more detail below.

### Reset Output

The microprocessor's ( $\mu\text{P}$ 's) reset input starts the  $\mu\text{P}$  in a known state. When the  $\mu\text{P}$  is in an unknown state, it should be held in reset. The **SP690A/SP692A/SP802** assert reset during power-up and prevent code execution errors during power-down or brownout conditions.

On power-up, once  $V_{CC}$  reaches 1V,  $\overline{\text{RESET}}$  is guaranteed to be a logic low. As  $V_{CC}$  rises,  $\overline{\text{RESET}}$  remains low. When  $V_{CC}$  exceeds the reset threshold,  $\overline{\text{RESET}}$  will remain low for 200ms, Figure 9. If a brownout condition occurs and  $V_{CC}$  dips below the reset threshold,  $\overline{\text{RESET}}$  is triggered. Each time  $\overline{\text{RESET}}$  is triggered, it stays low for the reset pulse width interval. If a brownout condition interrupts a previously initiated reset pulse, the reset pulse continues for another 200ms. On power-down, once  $V_{CC}$  goes below the threshold,  $\overline{\text{RESET}}$  is guaranteed to be logic low until  $V_{CC}$  drops below 1V.

$\overline{\text{RESET}}$  is also triggered by a watchdog timeout. If WDI remains either high or low for a period that exceeds the watchdog timeout period (1.6 sec),  $\overline{\text{RESET}}$  pulses low for 200mS. As long as  $\overline{\text{RESET}}$  is asserted, the watchdog timer remains clear. When  $\overline{\text{RESET}}$  comes high, the watchdog resumes timing and must be serviced within 1.6sec. If WDI is tied high or low, a  $\overline{\text{RESET}}$  pulse is triggered every 1.8sec ( $t_{WD}$  plus  $t_{RS}$ ).

The **SP805L/M** active-high RESET output is the inverse of the **SP690A/SP692A/SP802** RESET output, and is valid with  $V_{CC}$  down to 1V. Some  $\mu P$ 's, such as Intel's 80C51, require an active-high reset pulse.

### Watchdog Input

The watchdog circuit monitors the  $\mu P$ 's activity. If the  $\mu P$  does not toggle the watchdog input (WDI) within 1.6sec, a reset pulse is triggered. The internal 1.6sec timer is cleared by either a reset pulse or by floating the WDI input. As long as RESET is asserted or the WDI input is floating, the timer remains cleared and does not count. As soon as RESET is released and WDI is driven high or low, the timer starts counting. It can detect pulses as short as 50ns.

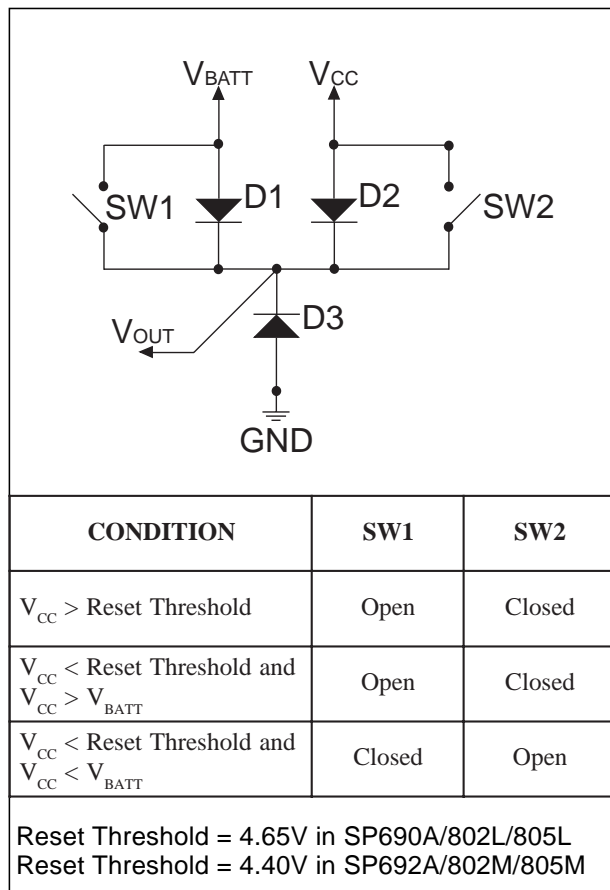


Figure 13. BACKUP-BATTERY Switchover Block Diagram

### Power-Fail Comparator

The Power-Fail Comparator can be used as an under-voltage detector to signal the failing of a power supply (it is completely separate from the rest of the circuitry and does not need to be dedicated to this function). The PFI input is compared to an internal 1.25V reference. If PFI is less than 1.25V,  $\overline{PFO}$  goes low. The external voltage divider drives PFI to sense the unregulated DC input to the +5V regulator. The voltage-divider ratio can be chosen such that the voltage at PFI falls below 1.25V just before the +5V regulator drops out.  $\overline{PFO}$  then triggers an interrupt which signals the  $\mu P$  to prepare for power-down.

When  $V_{BATT}$  connects to  $V_{OUT}$ , the power-fail comparator is turned off and  $\overline{PFO}$  is forced low to conserve backup-battery power.

### Backup-Battery Switchover

In the event of a brownout or power failure, it may be necessary to preserve the contents of RAM. With a backup battery installed at  $V_{BATT}$ , the RAM is assured to have power if  $V_{CC}$  fails. As long as  $V_{CC}$  exceeds the reset threshold,  $V_{OUT}$  connects to  $V_{CC}$  through a 0.6 $\Omega$  PMOS power switch. Once  $V_{CC}$  falls below the reset threshold,  $V_{CC}$  or  $V_{BATT}$ , whichever is higher, switches to  $V_{OUT}$ .  $V_{BATT}$  connects to  $V_{OUT}$  through a 5 $\Omega$  switch only when  $V_{CC}$  is below the reset threshold and  $V_{BATT}$  is greater than  $V_{CC}$ .

When  $V_{CC}$  exceeds the reset threshold, it is connected to  $V_{OUT}$ , regardless of the voltage applied to  $V_{BATT}$  Figure 13. During this time, the diode (D1) between  $V_{BATT}$  and  $V_{OUT}$  will conduct current from  $V_{BATT}$  to  $V_{OUT}$  if  $V_{BATT}$  is more than .6V above  $V_{OUT}$ .

When  $V_{BATT}$  connects to  $V_{OUT}$ , backup mode is activated and the internal circuitry will be powered from the battery Figure 14. When  $V_{CC}$  is just below  $V_{BATT}$ , in the backup mode the current drawn from  $V_{BATT}$  will be typically 30 $\mu A$ . When  $V_{CC}$  drops to more than 1V below  $V_{BATT}$ , the internal switchover comparator shuts off and the supply current falls to less than 0.6 $\mu A$ .

SIGNAL	STATUS
V <sub>CC</sub>	Disconnected from V <sub>OUT</sub>
V <sub>OUT</sub>	Connected to V <sub>BATT</sub> through an internal 8Ω PMOS switch
V <sub>BATT</sub>	Connected to V <sub>OUT</sub> . Current drawn from the battery is less than 0.6μA, as long as V <sub>CC</sub> < V <sub>BATT</sub> - 1V.
PFI	Power-fail comparator is disabled.
PFO	Logic low
RESET	Logic low
RESET	Logic high (SP805 only)
WDI	Watchdog timer is disabled

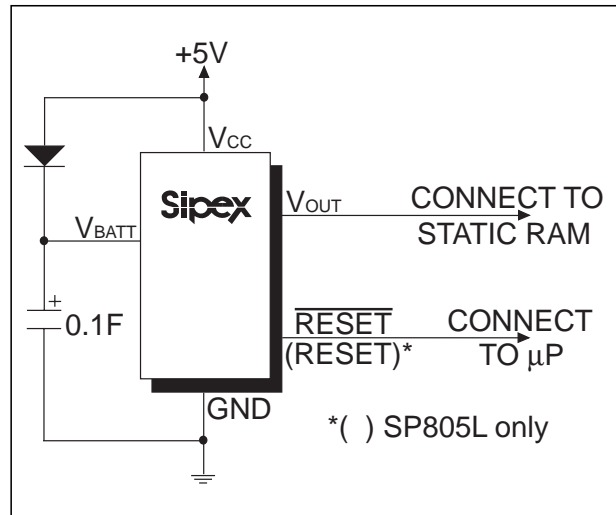
**Figure 14. Input and Output Status in Battery-Backup Mode.**  
To enter the Battery-Backup mode, V<sub>CC</sub> must be less than the Reset threshold and less than V<sub>BATT</sub>

### Using a High Capacity Capacitor as a Backup Power Source

V<sub>BATT</sub> has the same operating voltage range as V<sub>CC</sub>, and the battery-switchover threshold voltages are typically +20mV centered at V<sub>BATT</sub>, allowing use of a capacitor and a simple charging circuit as a backup source (see Figure 16).

PART NUMBER	MAXIMUM BACKUP-BATTERY VOLTAGE [V]
SP690A SP802L SP805L	4.80
SP692A SP802M SP805M	4.55

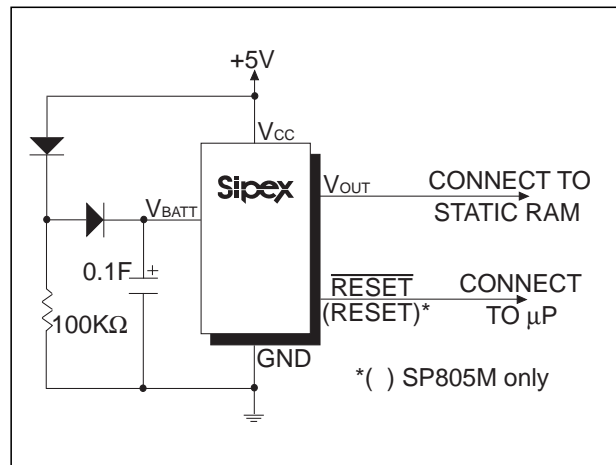
**Figure 15. Allowable BACKUP-BATTERY Voltages**



**Figure 16. Backup Power Source Using High Capacity Capacitor with SP690A/802L/805L and a +5V ±5% Supply**

If V<sub>CC</sub> is above the reset threshold and V<sub>BATT</sub> is 0.5V above V<sub>CC</sub>, current flows to V<sub>OUT</sub> and V<sub>CC</sub> from V<sub>BATT</sub> until the voltage at V<sub>BATT</sub> is less than 0.5V above V<sub>CC</sub>.

Leakage current through the capacitor charging diode and the SP690A/SP802L/SP805L internal power diode eventually discharges the capacitor to V<sub>CC</sub>. Also, if V<sub>CC</sub> and V<sub>BATT</sub> start from 0.5V above the reset threshold and power is lost at V<sub>CC</sub>, the capacitor on V<sub>BATT</sub> discharges through V<sub>CC</sub> until V<sub>BATT</sub> reaches the reset threshold; the SP690A/SP802L/SP805L then switches to battery-backup mode.



**Figure 17. Backup Power Source Using High Capacity Capacitor with SP692A/802M/805M and a +5V ±10% Supply**

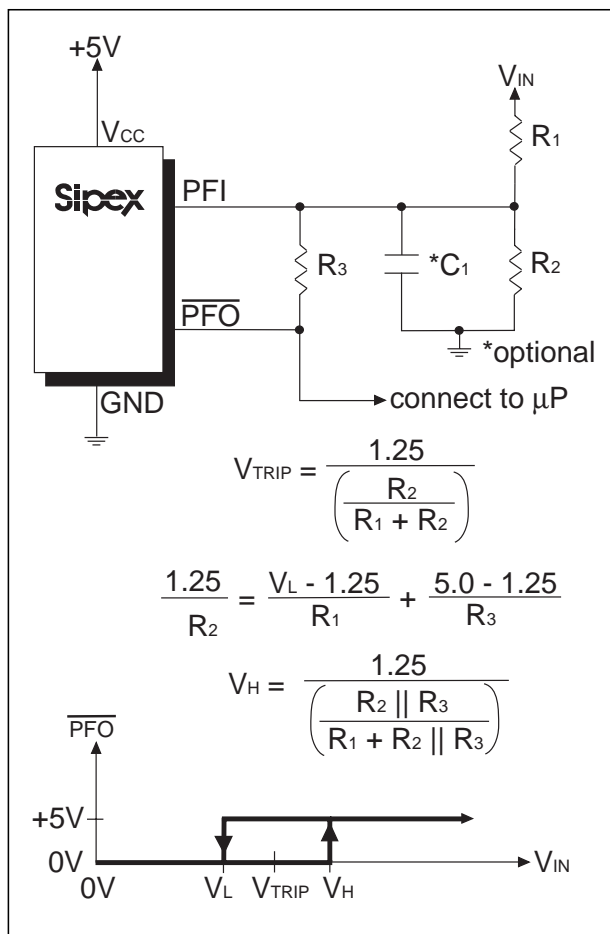


Figure 18. Adding Hysteresis to the POWER-FAIL Comparator

### Allowable Backup Power-Source Batteries

Lithium batteries work very well as backup batteries due to very low self-discharge rate and high energy density. Single lithium batteries with open-circuit voltages of 3.0V to 3.6V are ideal. Any battery with an open-circuit voltage less than the minimum reset threshold plus 0.3V can be connected directly to the  $V_{BATT}$  input of this series with no additional circuitry; see FIGURE 12. However, batteries with open-circuit voltages that are greater than this value cannot be used for backup, as current is sourced into  $V_{OUT}$  through the diode (*D1* in Figure 13) when  $V_{CC}$  is close to the reset threshold.

### Operation Without a Backup Power Source

If a backup power source is not used, ground  $V_{BATT}$  and connect  $V_{OUT}$  to  $V_{CC}$ . Since there is no need to switch over to any backup power source,  $V_{OUT}$  does not need to be switched. A direct connection to  $V_{CC}$  eliminates any voltage drops across the switch which may push  $V_{OUT}$  below  $V_{CC}$ .

### Replacing the Backup Battery

The backup battery can be removed while  $V_{CC}$  remains valid, without danger of triggering RESET/RESET. As long as  $V_{CC}$  stays above the reset threshold, battery-backup mode cannot be entered.

### Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of PFO when  $V_{IN}$  is close to its trip point. Figure 18 shows how to add hysteresis to the power-fail comparator. Select the ratio of  $R_1$  and  $R_2$  such that PFI sees 1.25V when  $V_{IN}$  falls to its trip point ( $V_{TRIP}$ ).  $R_3$  adds the hysteresis. It will typically be an order of magnitude greater (about 10 times) than  $R_1$  or  $R_2$ . The current through  $R_1$  and  $R_2$  should be at least 1 $\mu$ A to ensure that the 25nA (max) PFI input current does not shift the trip point.  $R_3$  should be larger than 10K $\Omega$  so it does not load down the PFO pin. Capacitor C1 adds additional noise rejection.

### Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply rail using the circuit of Figure 19. When the negative rail is valid,  $\overline{PFO}$  is low. When the negative supply voltage drops,  $\overline{PFO}$  goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the  $V_{CC}$  voltage, and the resistors,  $R_1$  and  $R_2$ .

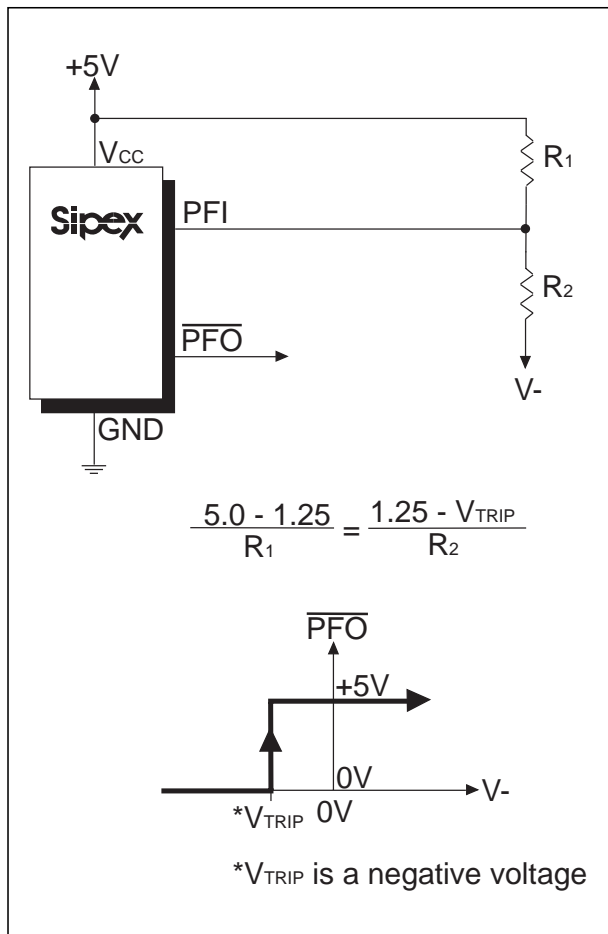


Figure 19. Monitoring a Negative Voltage

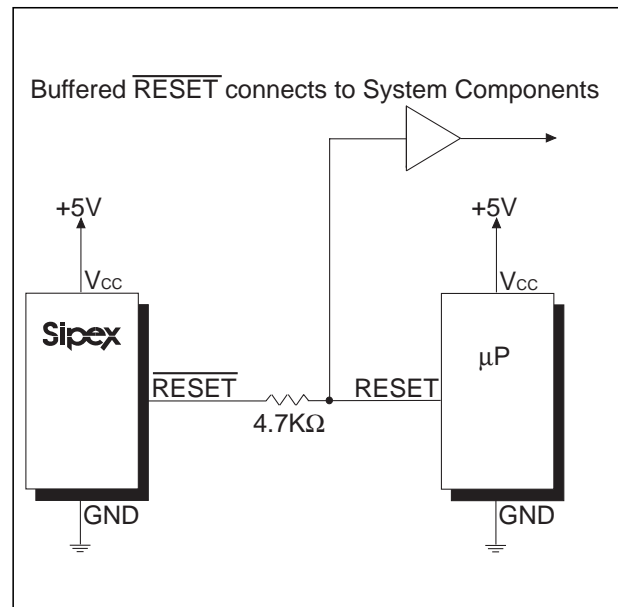
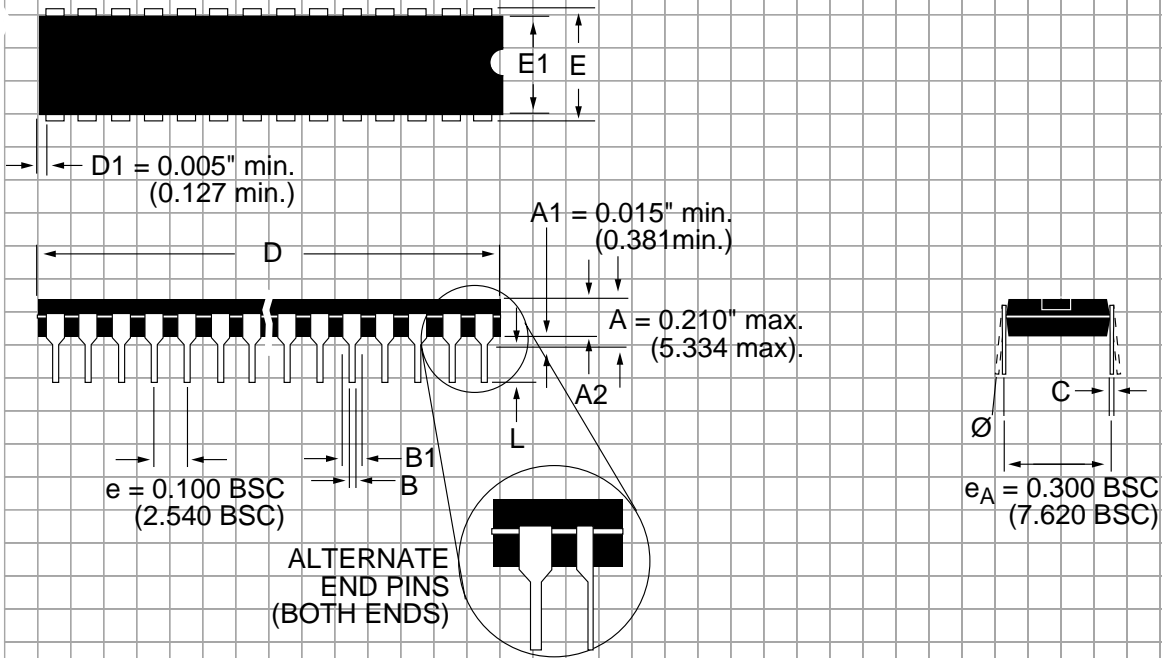


Figure 20. Interfacing to Microprocessors with Bidirectional  $\overline{\text{RESET}}$  I/O

## Interfacing to Microprocessors with Bidirectional Reset Pins

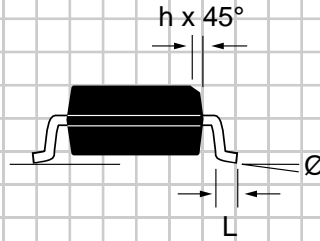
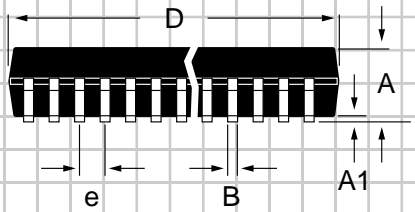
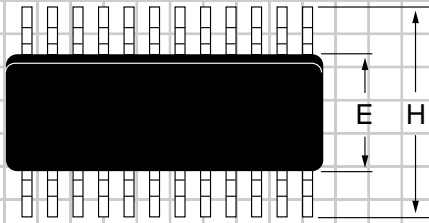
Microprocessors with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with this series'  $\overline{\text{RESET}}$  output. If, for example, the  $\overline{\text{RESET}}$  output is driven high and the  $\mu\text{P}$  wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7K $\Omega$  resistor between the  $\overline{\text{RESET}}$  output and the  $\mu\text{P}$  reset I/O, as in Figure 20. Buffer the  $\overline{\text{RESET}}$  output to other system components.

# PACKAGE: PLASTIC DUAL-IN-LINE (NARROW)



DIMENSIONS (Inches) Minimum/Maximum (mm)	8-PIN	14-PIN	16-PIN	18-PIN	20-PIN	22-PIN
A2	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)
B	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)
B1	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)
C	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)
D	0.355/0.400 (9.017/10.160)	0.735/0.775 (18.669/19.685)	0.780/0.800 (19.812/20.320)	0.880/0.920 (22.352/23.368)	0.980/1.060 (24.892/26.924)	1.145/1.155 (29.083/29.337)
E	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)
E1	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)
L	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)
Ø	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)

**PACKAGE: PLASTIC  
SMALL OUTLINE (SOIC)  
(NARROW)**



DIMENSIONS (Inches) Minimum/Maximum (mm)	8-PIN	14-PIN	16-PIN			
A	0.053/0.069 (1.346/1.748)	0.053/0.069 (1.346/1.748)	0.053/0.069 (1.346/1.748)			
A1	0.004/0.010 (0.102/0.249)	0.004/0.010 (0.102/0.249)	0.004/0.010 (0.102/0.249)			
B	0.014/0.019 (0.35/0.49)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)			
D	0.189/0.197 (4.80/5.00)	0.337/0.344 (8.552/8.748)	0.386/0.394 (9.802/10.000)			
E	0.150/0.157 (3.802/3.988)	0.150/0.157 (3.802/3.988)	0.150/0.157 (3.802/3.988)			
e	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)			
H	0.228/0.244 (5.801/6.198)	0.228/0.244 (5.801/6.198)	0.228/0.244 (5.801/6.198)			
h	0.010/0.020 (0.254/0.498)	0.010/0.020 (0.254/0.498)	0.010/0.020 (0.254/0.498)			
L	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)			
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)			

## ORDERING INFORMATION

Model	Temperature Range	Package Types
SP690ACN.....	0°C to +70°C.....	8-Pin NSOIC
SP690ACP.....	0°C to +70°C.....	8-Pin PDIP
SP690AEN.....	-40°C to +85°C.....	8-Pin NSOIC
SP690AEP.....	-40°C to +85°C.....	8-Pin PDIP
SP692ACN.....	0°C to +70°C.....	8-Pin NSOIC
SP692ACP.....	0°C to +70°C.....	8-Pin PDIP
SP692AEN.....	-40°C to +85°C.....	8-Pin NSOIC
SP692AEP.....	-40°C to +85°C.....	8-Pin PDIP
SP802LCN.....	0°C to +70°C.....	8-Pin NSOIC
SP802LCP.....	0°C to +70°C.....	8-Pin PDIP
SP802LEN.....	-40°C to +85°C.....	8-Pin NSOIC
SP802LEP.....	-40°C to +85°C.....	8-Pin PDIP
SP802MCN.....	0°C to +70°C.....	8-Pin NSOIC
SP802MCP.....	0°C to +70°C.....	8-Pin PDIP
SP802MEN.....	-40°C to +85°C.....	8-Pin NSOIC
SP802MEP.....	-40°C to +85°C.....	8-Pin PDIP
SP805LCN.....	0°C to +70°C.....	8-Pin NSOIC
SP805LCP.....	0°C to +70°C.....	8-Pin PDIP
SP805LEN.....	-40°C to +85°C.....	8-Pin NSOIC
SP805LEP.....	-40°C to +85°C.....	8-Pin PDIP
SP805MCN.....	0°C to +70°C.....	8-Pin NSOIC
SP805MCP.....	0°C to +70°C.....	8-Pin PDIP
SP805MEN.....	-40°C to +85°C.....	8-Pin NSOIC
SP805MEP.....	-40°C to +85°C.....	8-Pin PDIP

Please consult the factory for pricing and availability on a Tape-On-Reel option.



SIGNAL PROCESSING EXCELLENCE

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